Gaining Insight into Parallel Program Performance Using HPCToolkit

John Mellor-Crummey

Department of Computer Science

Rice University



Challenges for Application Developers

- Rapidly evolving platforms and applications
 - architecture
 - rapidly changing microprocessor designs
 - rise of accelerated computing
 - increasing scale of parallel systems
 - applications
 - transition from MPI everywhere to threaded implementations
 - augment computational capabilities
- Application developer needs
 - adapt to changes in emerging architectures
 - improve scalability within and across nodes
 - assess weaknesses in algorithms and their implementations

Performance tools can play an important role as a guide

Performance Analysis Challenges

- Complex node architectures are hard to use efficiently
 - multi-level parallelism: multiple cores, ILP, SIMD, accelerators
 - multi-level memory hierarchy
 - result: gap between typical and peak performance is huge
- Complex applications present challenges
 - measurement and analysis
 - understanding behaviors and tuning performance
- Multifaceted performance concerns
 - computation
 - data movement
 - communication
 - **I/O**
- Supercomputers compound the complexity
 - unique hardware & microkernel-based operating systems

What Users Want

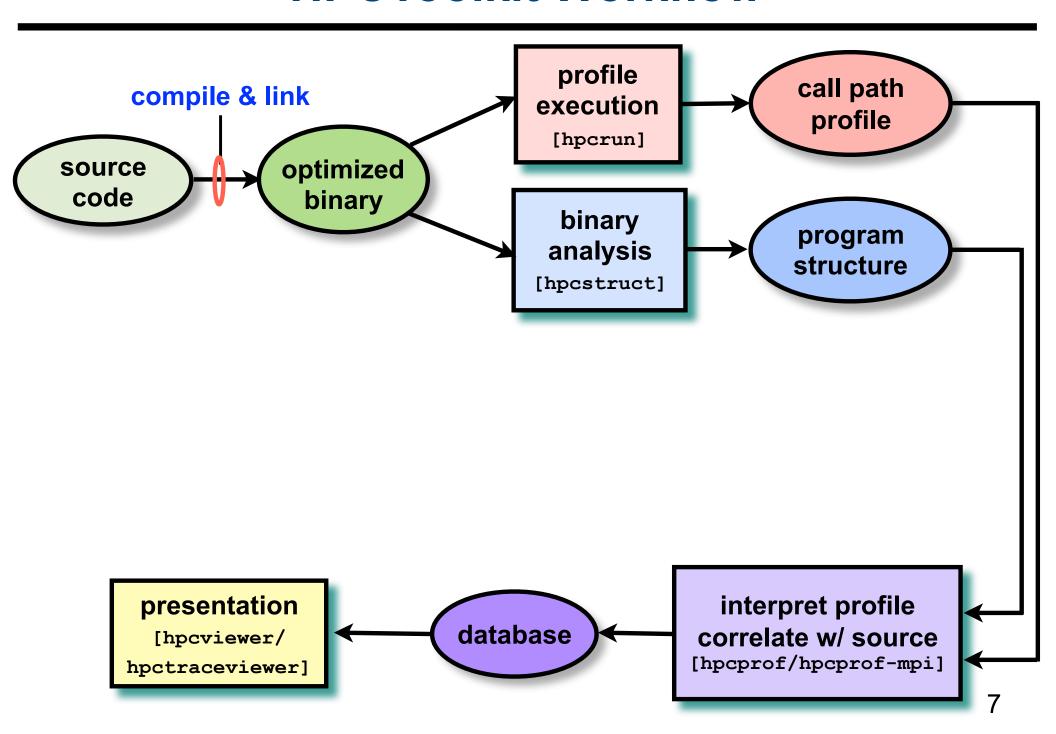
- Multi-platform, programming model independent tools
- Accurate measurement of complex parallel codes
 - large, multi-lingual programs
 - (heterogeneous) parallelism within and across nodes
 - optimized code: loop optimization, templates, inlining
 - binary-only libraries, sometimes partially stripped
 - complex execution environments
 - dynamic binaries on clusters; static binaries on supercomputers
 - batch jobs
- Effective performance analysis
 - insightful analysis that pinpoints and explains problems
 - correlate measurements with code for actionable results
 - support analysis at the desired level intuitive enough for application scientists and engineers detailed enough for library developers and compiler writers
- Scalable to full systems

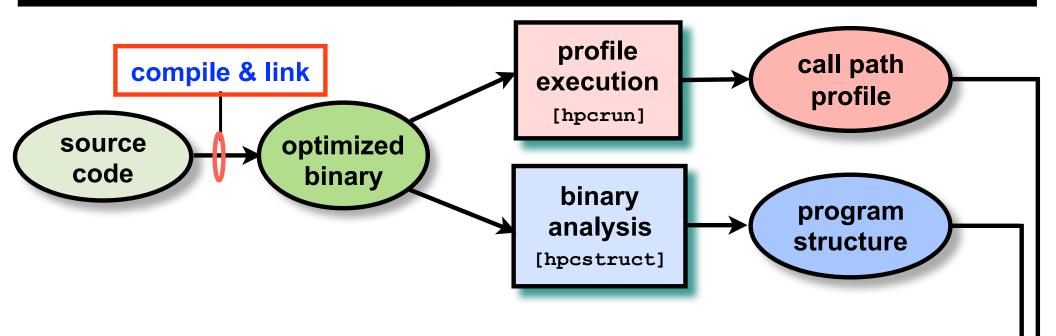
Rice University's HPCToolkit

- Employs binary-level measurement and analysis
 - observe fully optimized, dynamically linked executions
 - support multi-lingual codes with external binary-only libraries
- Uses sampling-based measurement (avoid instrumentation)
 - controllable overhead
 - minimize systematic error and avoid blind spots
 - enable data collection for large-scale parallelism
- Collects and correlates multiple derived performance metrics
 - diagnosis typically requires more than one species of metric
- Associates metrics with both static and dynamic context
 - loop nests, procedures, inlined code, calling context
- Supports top-down performance analysis
 - natural approach that minimizes burden on developers

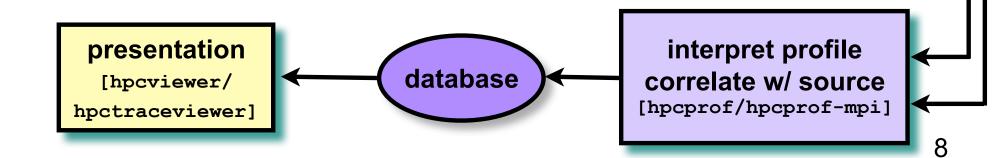
Outline

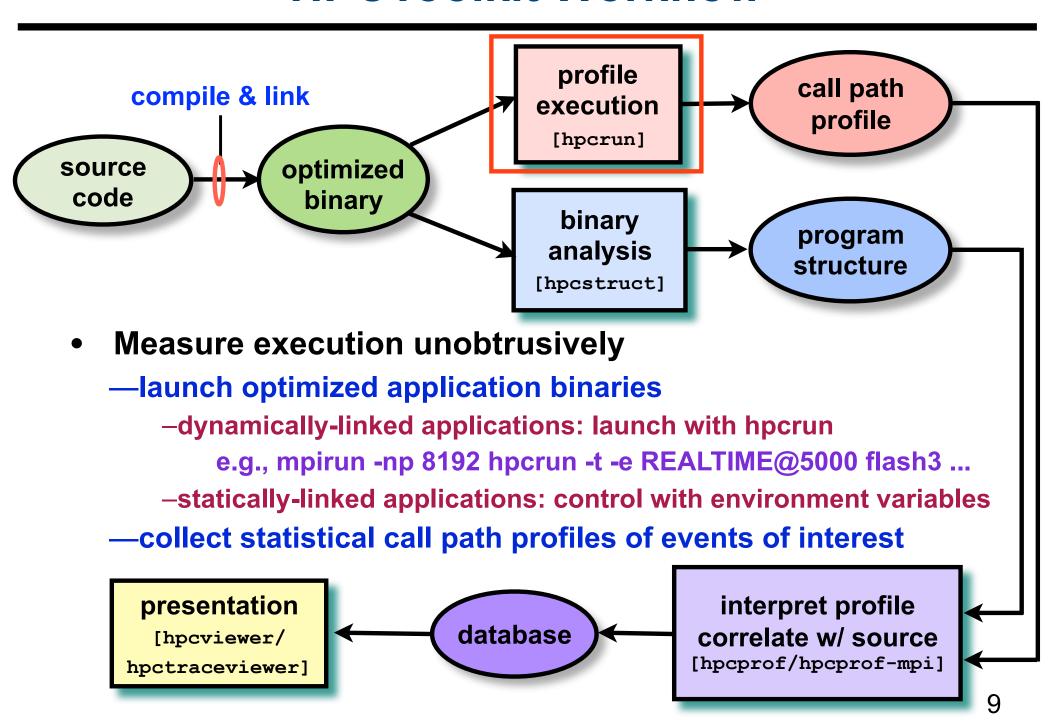
- Overview of Rice's HPCToolkit
- Pinpointing scalability bottlenecks
 - scalability bottlenecks on large-scale parallel systems
 - scaling on multicore processors
- Understanding temporal behavior
- Assessing process variability
- Understanding threading and memory hierarchy
 - blame shifting
 - attributing memory hierarchy costs to data
- Today and the future





- For dynamically-linked executables on stock Linux
 - compile and link as you usually do
- For statically-linked executables (e.g., for Blue Gene, Cray)
 - add monitoring by using hpclink as prefix to your link line

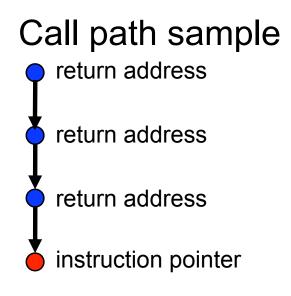


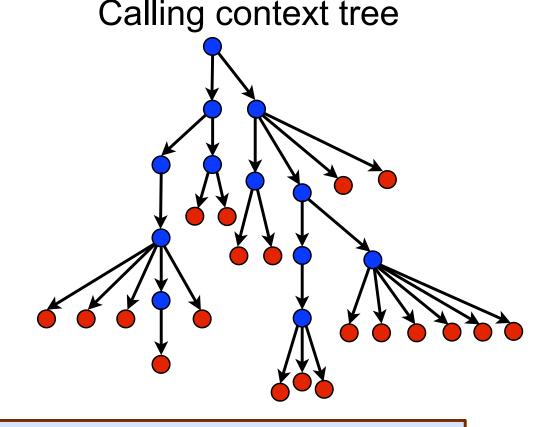


Call Path Profiling

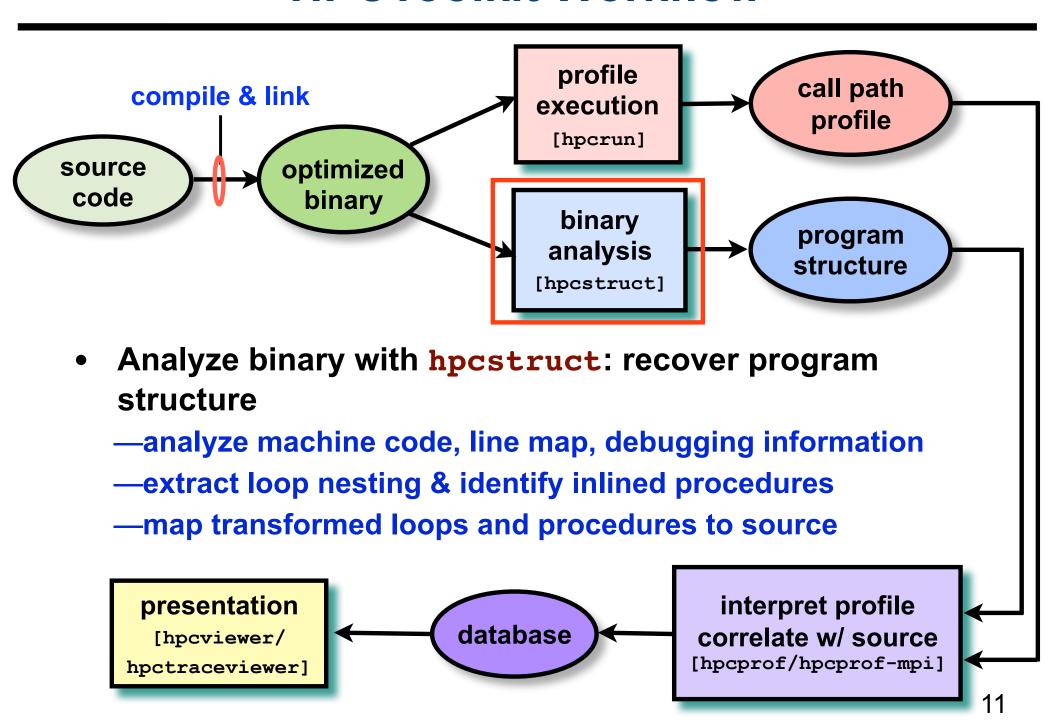
Measure and attribute costs in context

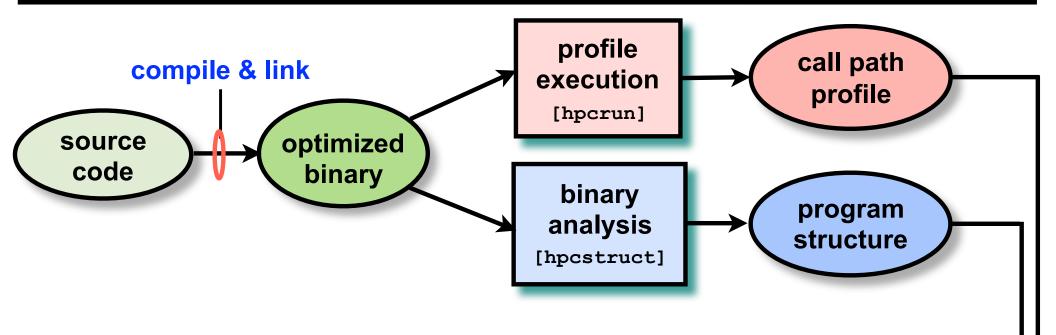
sample timer or hardware counter overflows gather calling context using stack unwinding



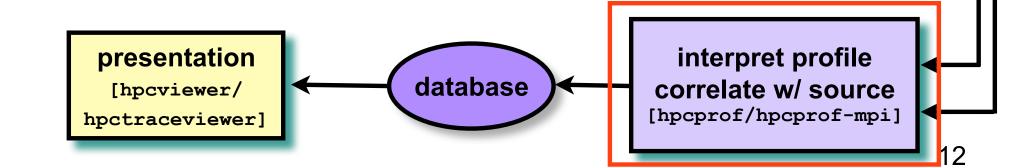


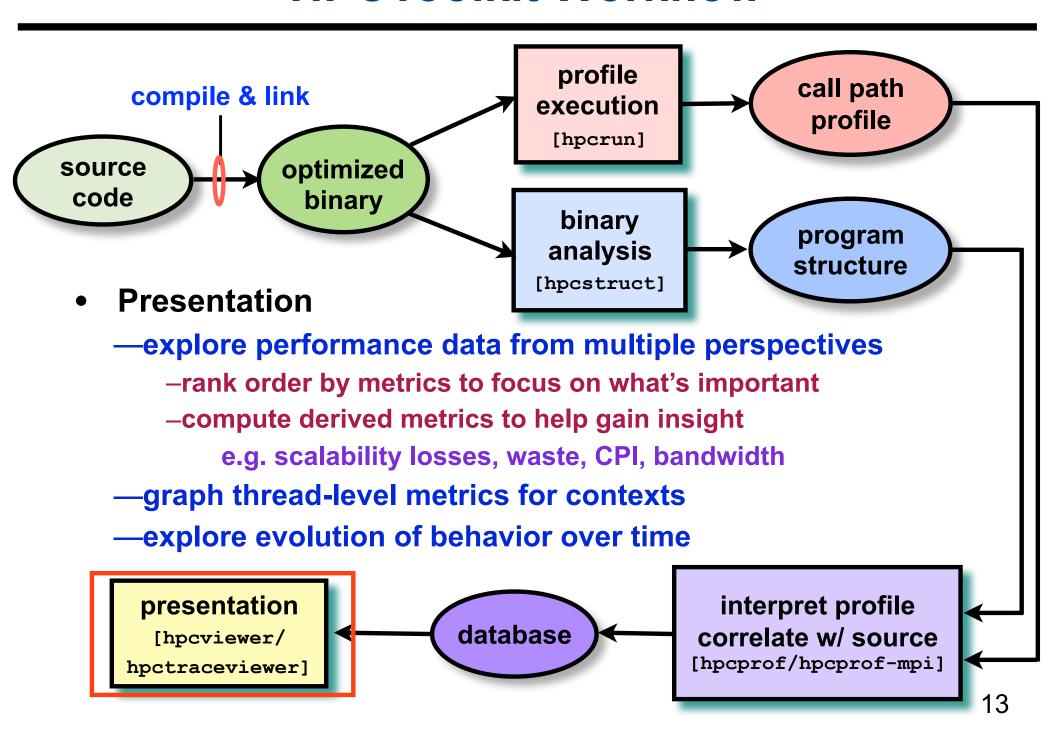
Overhead proportional to sampling frequency...
...not call frequency



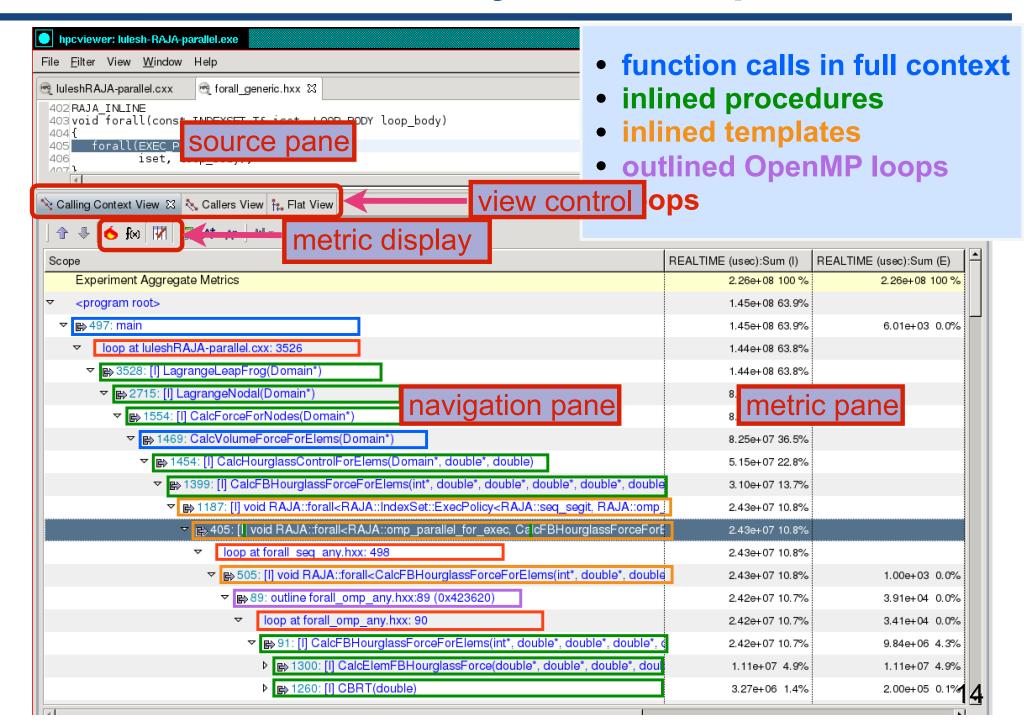


- Combine multiple profiles
 - —multiple threads; multiple processes; multiple executions
- Correlate metrics to static & dynamic program structure





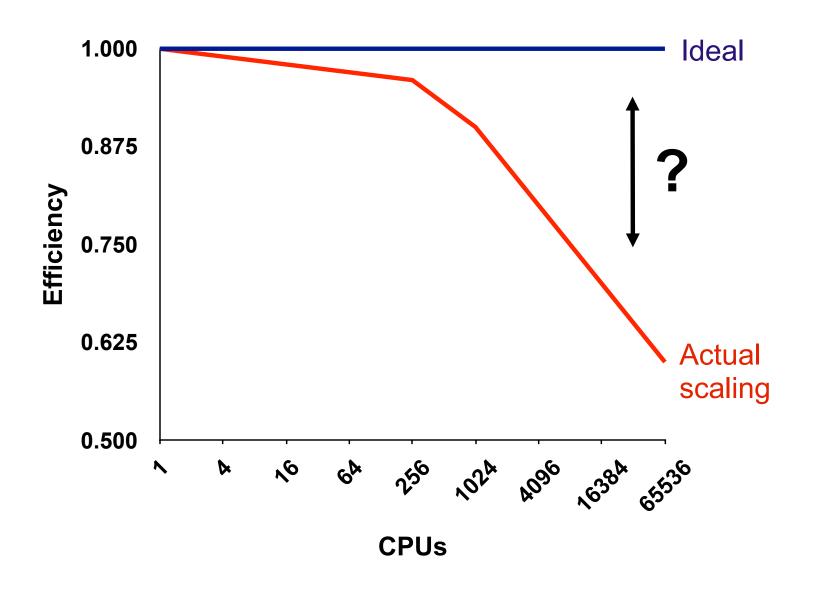
Code-centric Analysis with hpcviewer



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The Problem of Scaling



Note: higher is better

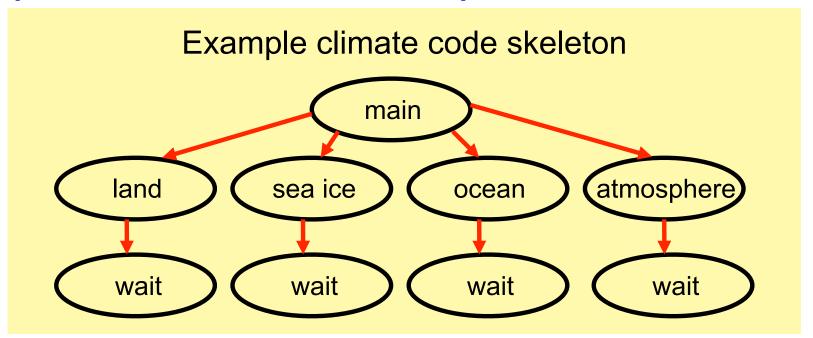
Wanted: Scalability Analysis

- Isolate scalability bottlenecks
- Guide user to problems
- Quantify the magnitude of each problem

Challenges for Pinpointing Scalability Bottlenecks

Parallel applications

- modern software uses layers of libraries
- performance is often context dependent



Monitoring

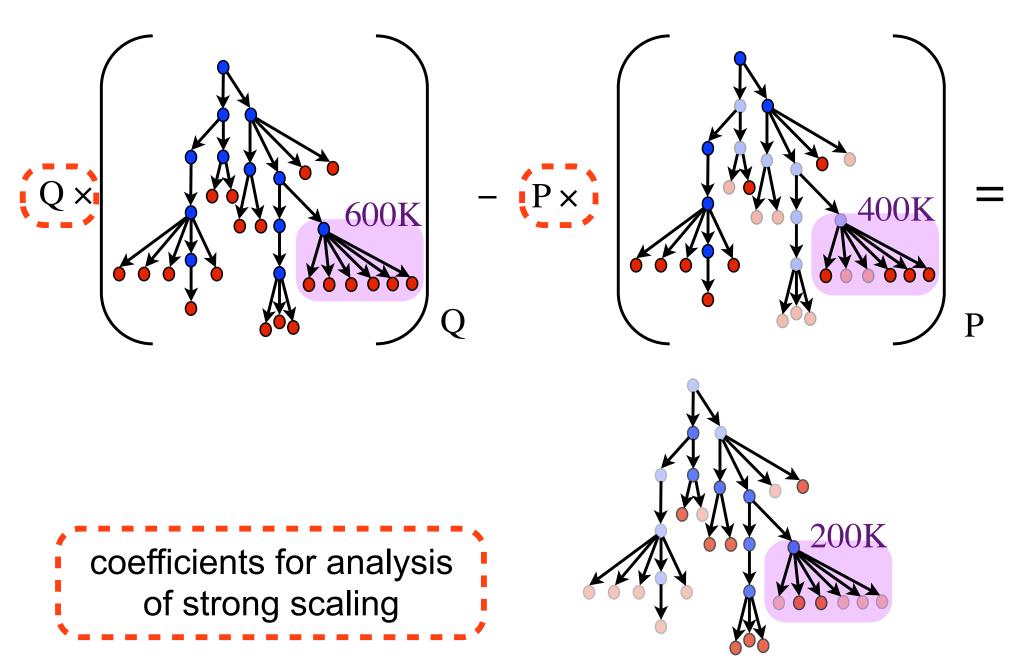
- bottleneck nature: computation, data movement, synchronization?
- 2 pragmatic constraints
 - acceptable data volume
 - low perturbation for use in production runs

Performance Analysis with Expectations

- You have performance expectations for your parallel code
 - strong scaling: linear speedup
 - weak scaling: constant execution time

- Put your expectations to work
 - measure performance under different conditions
 - e.g. different levels of parallelism and/or different problem size
 - express your expectations as an equation
 - compute the deviation from expectations for each calling context
 - for both inclusive and exclusive costs
 - correlate the metrics with the source code
 - explore the annotated call tree interactively

Pinpointing and Quantifying Scalability Bottlenecks



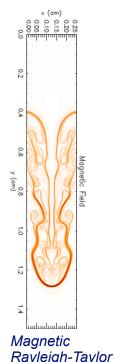
Scalability Analysis Demo: FLASH3

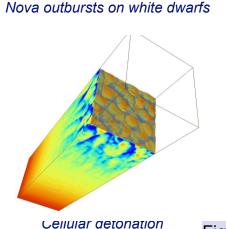
Code: Simulation: **Platform: Experiment:** Scaling type:

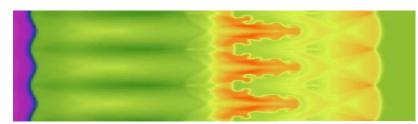
University of Chicago FLASH3 white dwarf detonation Blue Gene/P 8192 vs. 256 cores weak

Orzag/Tang MHD

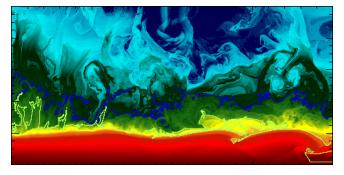
vortex

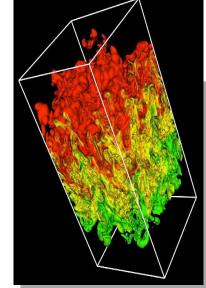






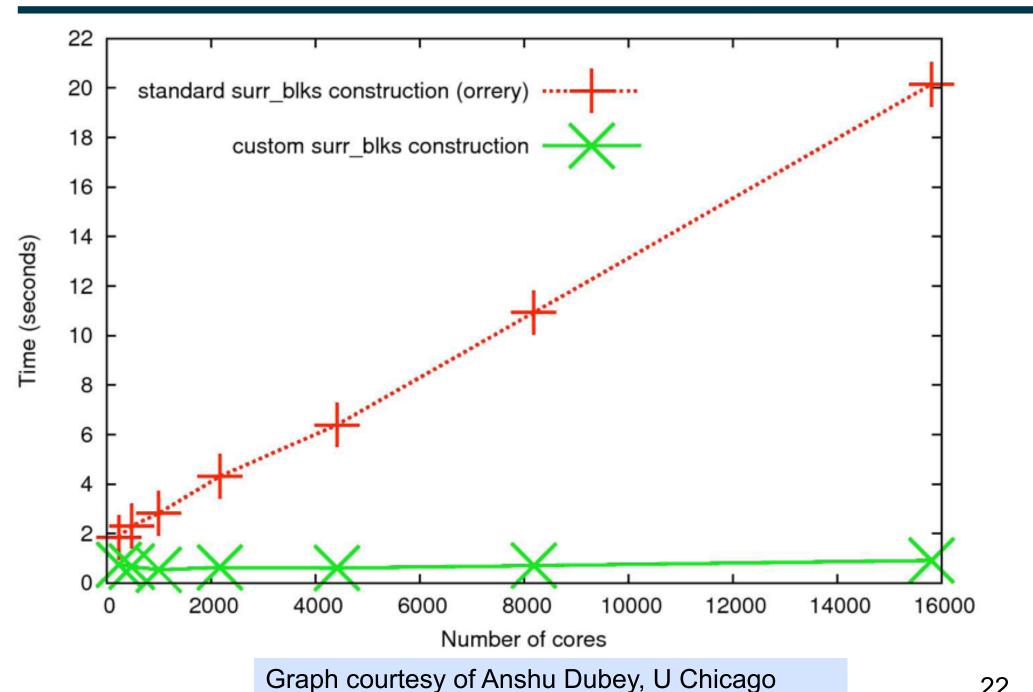
Laser-driven shock instabilities



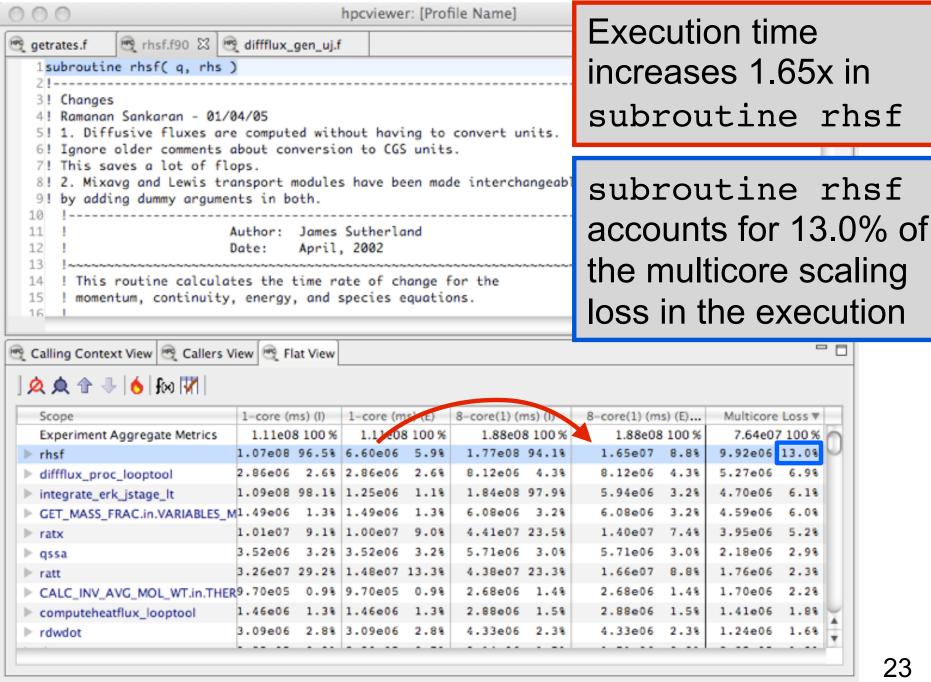


Rayleigh-Taylor instability

Improved Flash Scaling of AMR Setup



S3D: Multicore Losses at the Procedure Level



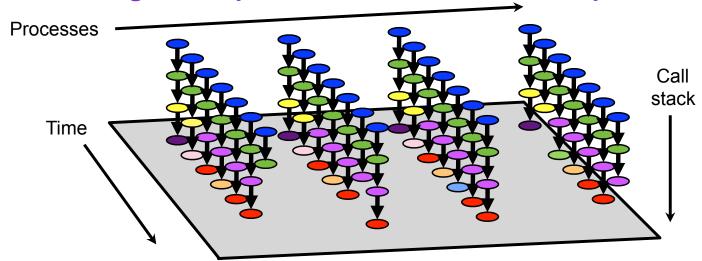
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Understanding Temporal Behavior

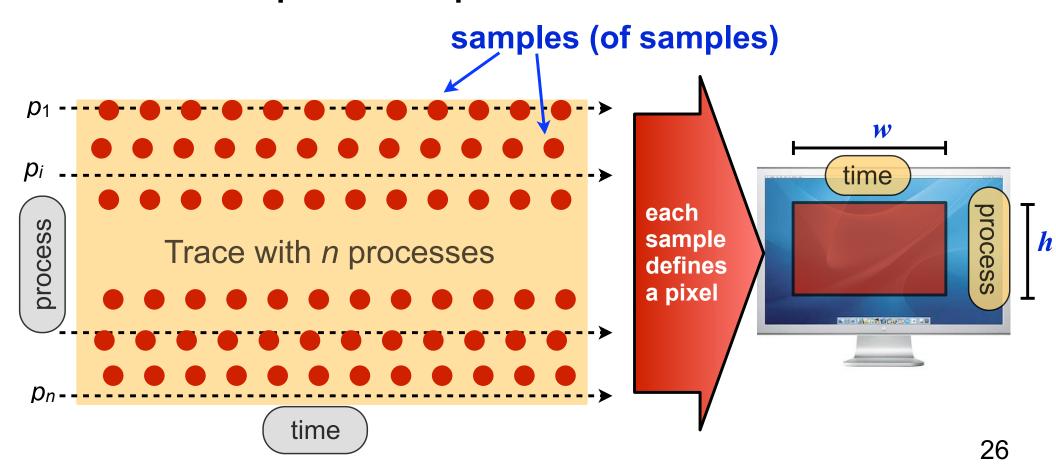
- Profiling compresses out the temporal dimension
 - —temporal patterns, e.g. serialization, are invisible in profiles
- What can we do? Trace call path samples
 - -sketch:
 - N times per second, take a call path sample of each thread
 - organize the samples for each thread along a time line
 - view how the execution evolves left to right
 - what do we view?

assign each procedure a color; view a depth slice of an execution



Presenting Large Traces on Small Displays

- How to render an arbitrary portion of an arbitrarily large trace?
 - we have a display window of dimensions h × w
 - typically many more processes (or threads) than h
 - typically many more samples (trace records) than w
- Solution: sample the samples!

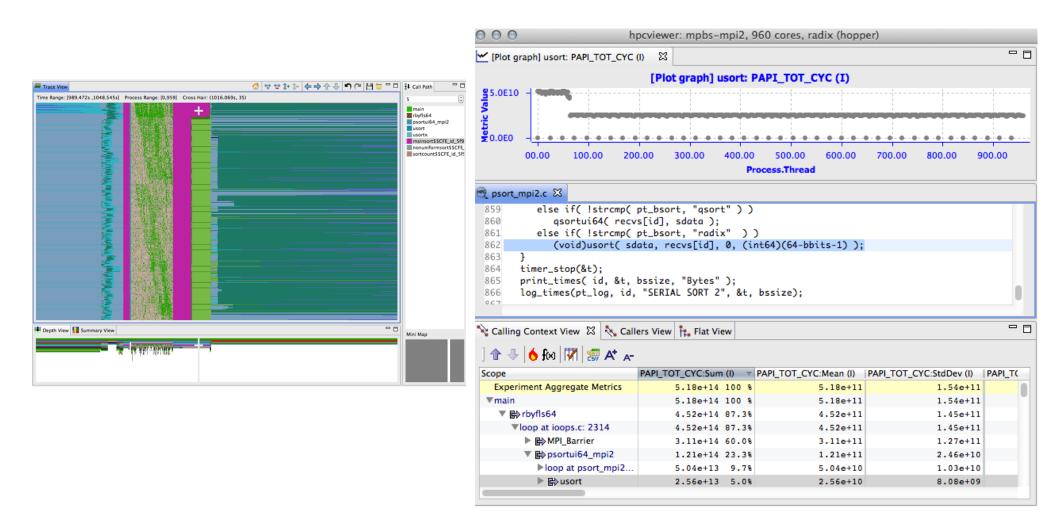


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MPBS @ 960 cores, radix sort

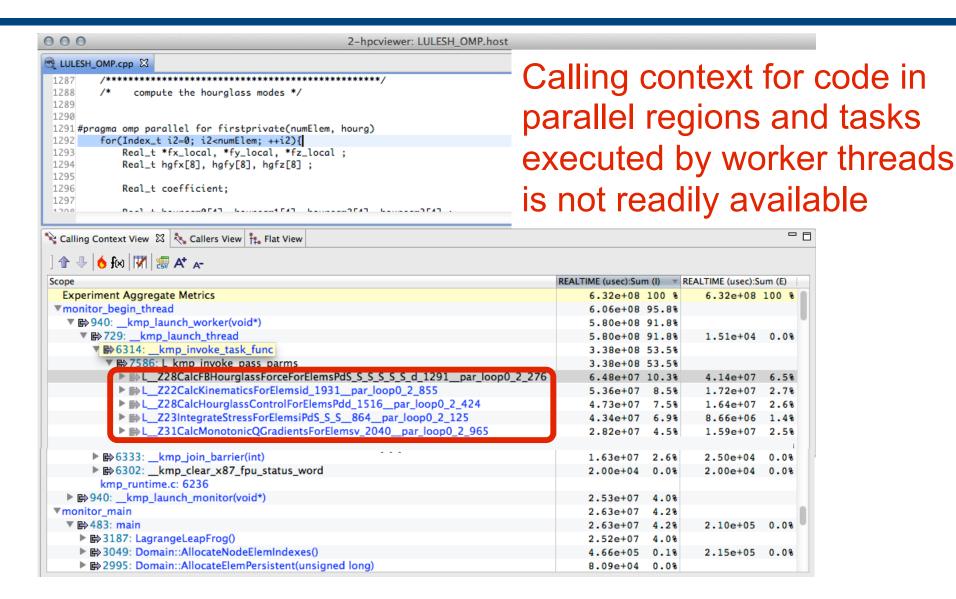
Two views of load imbalance since not on a 2^k cores



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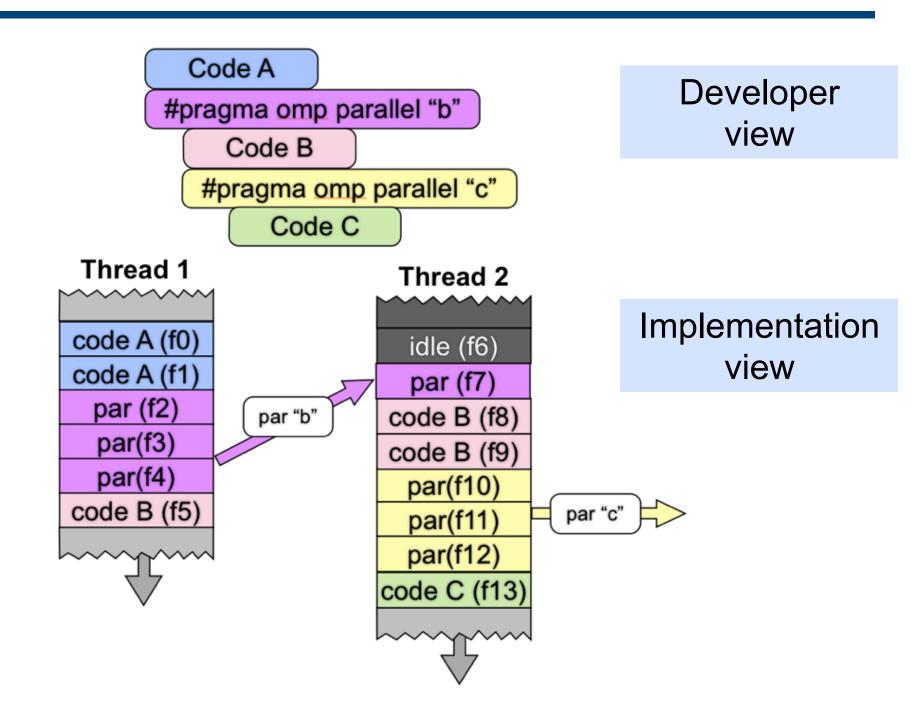
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OpenMP: Gap between Source and Implementation



Tools must bridge this gap to explain program performance

OpenMP Application-level Context is Distributed



OMPT Design Objectives

- Enable tools to gather information and associate costs with application source and runtime system
 - —construct low-overhead tools based on asynchronous sampling
 - —identify application stack frames vs. runtime frames
 - —associate a thread's activity at any point with a descriptive state
 - parallel work, idle, lock wait, ...
- Negligible overhead if OMPT interface is not in use
 - —features that may increase overhead are optional
- Define support for trace-based performance tools
- Don't impose an unreasonable development burden
 - —runtime implementers
 - —tool developers

Principal OMPT Features

State tracking

— have runtime track keep track of thread states

work (serial, parallel)	task wait
idle	mutual exclusion
barrier	overhead

- async signal safe query
 - if in a waiting state, handle identifies what is being awaited
- Call stack interpretation
 - provide hooks that enable tools to reconstruct applicationlevel call stacks from implementation-level information
- Event notification
 - provide callbacks for predefined events
 - few mandatory notifications
 - optional events for blame shifting, tracing

OMPT Mandatory Events

Essential support for any performance tool

- Threads
- Parallel regions

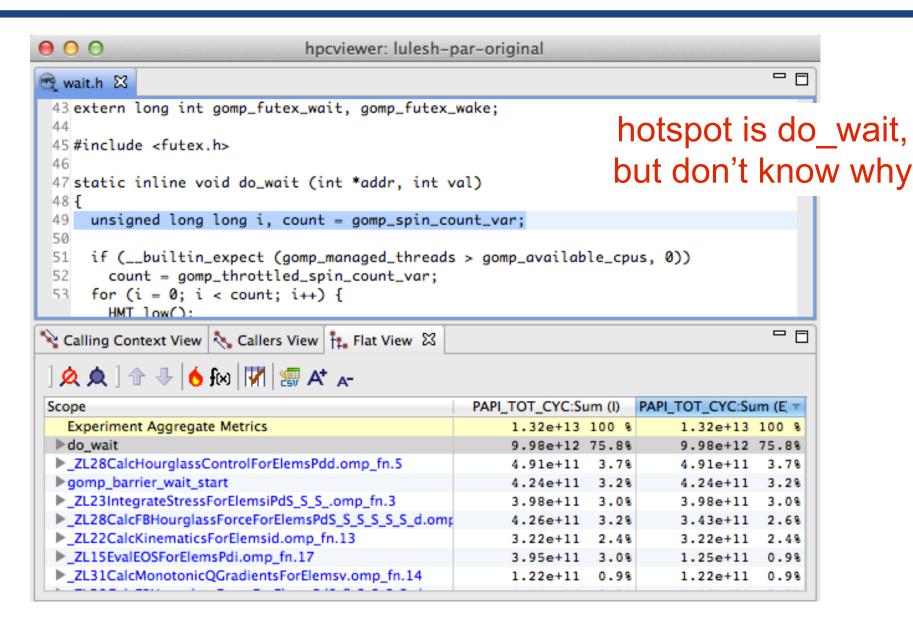
create/exit event pairs

- Tasks
- Runtime shutdown

singleton events

- User-level control API
 - e.g., support tool start/stop

OpenMP: Meaningless Hotspots



Identifying Causes of Bottlenecks

- Problem: in many circumstances sampling measures symptoms of performance losses rather than causes
 - worker threads waiting for work
 - threads waiting for a lock
 - process waiting for peers to arrive at a barrier
 - idle GPU waiting for work
- Approach: shift blame for losses from victims to perpetrators
 - blame code executing while other threads are idle
 - blame code executed by lock holder when thread(s) are waiting
 - blame processes that arrive late to collectives
 - shift blame between CPU and GPU for hybrid code

Blame Shifting from Symptoms to Causes

Approach

shift blame for idleness to code executing while other threads are idle

Implementation of undirected blame shifting

- callback at thread transitions idle ↔ working
- maintain two global counters
 - thread created (or dedicated HW resources that are reserved)
 - number of threads that are working
 - idleness is the difference between the two counters
- at a sample event
 - if the thread is actively working
 attribute a sample of work to the present context
 attribute partial blame for idleness to the present context
 - else, ignore the sample event

Blame-shifting for Analyzing Thread Performance

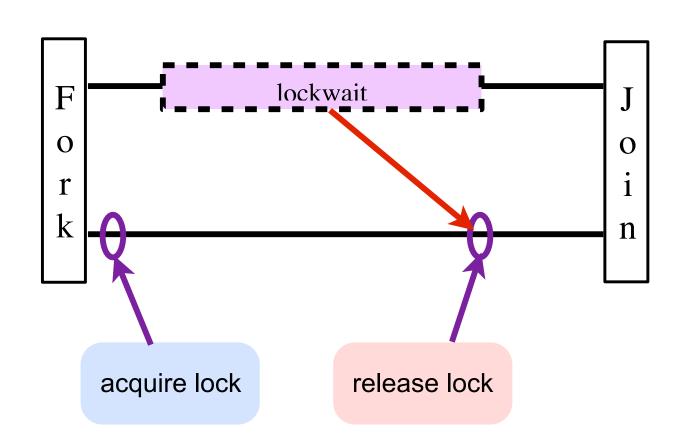
	Problem	Approach
Undirected Blame Shifting ¹	A thread is idle waiting for work	Apportion blame among working threads for not shedding enough parallelism to keep all threads busy
Directed Blame Shifting ²	A thread is idle waiting for a mutex	Blame the thread holding the mutex for idleness of threads waiting for the mutex

¹Tallent & Mellor-Crummey: PPoPP 2009

²Tallent, Mellor-Crummey, Porterfield: PPoPP 2010

Directed Blame Shifting

- Example:
 - threads waiting at a lock are the symptom
 - the cause is the lock holder
- Approach: blame lock waiting on lock holder



accumulate samples in a global hash table indexed by the lock address lock holder accepts these samples when it releases the lock

OMPT Events for Blame-shifting

Support designed for sampling-based performance tools

- Idle
- Wait
 - barrier
 - taskwait
 - taskgroup wait

Release

- lock
- nest lock
- critical
- atomic
- ordered section

begin/end event pairs

singleton events

Example: Directed Blame Shifting for Locks

hpcviewer: locktest-2.host

File View Window Help

1 #include <omp.h>

2 #include "fib.h"

omp lock t l; omp init lock(&l);

#pragma omp parallel

#pragma omp master

3 void a() { int i:

8 9

10

Blame a lock holder for delaying waiting threads

 Charge all samples that threads receive while awaiting a lock to the lock itself

 When releasing a lock, accept blame at all of the lock the

waiting

occurs

here

(cause) 11 omp set lock(&l); 12 fib(40); 13 omp unset lock(&l) 15 #pragma omp for $for(i = 0: i < 100: i++) {$ omp set lock(&l); fib(10); 19 omp unset lock(&l); 20 21 } 22 } 23 void f() { g(); } 24 int main() { f(); return 0; } 🔖 Calling Context View 🛭 🛝 Callers View 🏗 Flat View -- A S M M M → --MUTEX BLAME:Sum (I) Scope MUTEX WAIT:Sum (I) **Experiment Aggregate Metrics** 8.11e+07 100 % monitor main 8.11e+07 100 % ▼ № 483: main 8.11e+07 100 % ¬

□ 29: f 8.11e+07 100 % ¬ В 25: q 8.11e+07 100 % ¬ В 7: L g 7 par region0 2 90 8.11e+07 100 % ▷

□ 17: kmpc set lock 8.11e+07 100 % (symptom) D ₽ 12: fib ▶ 20: __kmpc_barrier locktest-2.c: 13

almost all blame

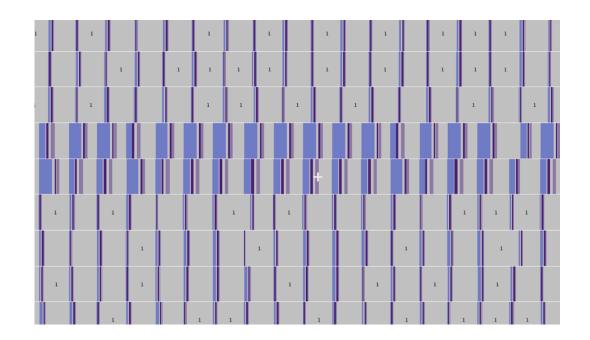
for the waiting is

7.93e+07 100 %

attributed here

GPU Successes with HPCToolkit

- LAMMPS: identified hardware problem with Keeneland system
 - improperly seated GPUs were observed to have lower data copy bandwidth

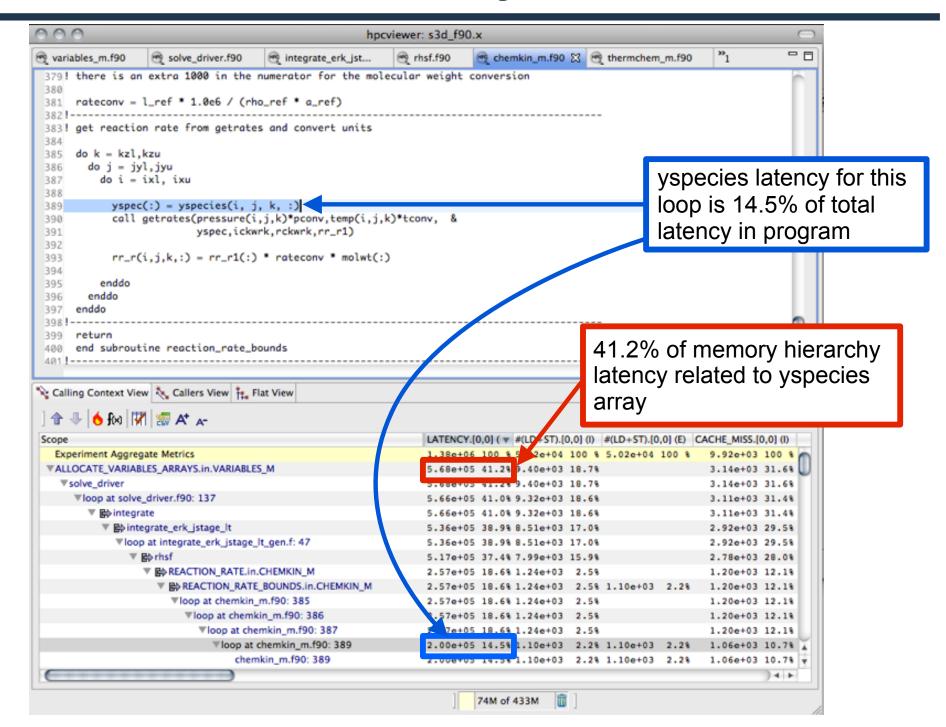


 LLNL's LULESH: identified that dynamic memory allocation using cudaMalloc and cudaFree accounted for 90% of the idleness of the GPU

Data Centric Analysis

- Goal: associate memory hierarchy access costs with data
- Approach
 - intercept allocations to associate with their data ranges
 - measure latency
 - "instruction-based sampling" (AMD Opteron)
 - "marked instructions" (IBM Power)
 - "load latency facility" (Intel x86_64)
 - present quantitative results using hpcviewer

Data Centric Analysis of S3D



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- Summary

Summary

- Sampling provides low overhead measurement
- Call path profiling + binary analysis + blame shifting = insight
 - scalability bottlenecks
 - where insufficient parallelism lurks
 - sources of lock contention
 - load imbalance
 - temporal dynamics
 - bottlenecks in hybrid code
 - problematic data structures
 - hardware counters for detailed diagnosis
- Other capabilities
 - attribute memory leaks back to their full calling context

Challenges Ahead

- Measure and analyze accelerated computations
- Measure and diagnose performance with billions of threads
- Understand how an application should best exploit complex, exposed memory hierarchies
- Help users optimize extreme-scale applications to reduce power consumption and improve energy efficiency
 - dynamic voltage and frequency scaling
- Evaluate behavior of adaptive runtime systems