Problem 1（25pts, 5pts for the last question, 4pts for the others）

1. Pipelined: 350ps
    Non-Pipelined: 1250ps
2. Pipelined: 1750ps
    Non-Pipelined: 1250ps
3. Split ID, the new clock cycle time is 300 ps.
4. Utilization= lw% + sw% = 35%
5. Utilization = alu% + beq% = 65%
6.

	CLOCK CYCLE TIME	EXECUTION TIME
SINGLE-CYCLE	1250ps	1250ps
MULTI-CYCLE	350ps	1400ps
PIPELINED	350ps	350ps

Clock cycle time -   single : multi : pipelined = 3.57 : 1 :1
Execution Time – single : multi: pipelined = 3.57: 4 : 1

Problem 2 (25pts, 5pts per question)

1. Hazards: or r1, r2, r3
                    or r2, r1, r4
                    or r1, r1, r2
    nop: or r1, r2, r3
            nop
            nop
            or r2, r1, r4
            nop
            nop
            or r1, r1, r2
2. **No hazards, no need to add nop instructions.**
3. without: 250ps * 11 = 2750ps
    with full: 300ps * 7 = 2100ps
    speedup: (2750ps – 2100ps) / 2750ps = 24%
4. or r1, r2, r3
    or r2, r1, r4
    nop
    nop
    or r1, r1, r2
5. **time = (5 + 4)*290ps = 2610ps**
    speedup = 2750ps/2610ps = 105% (approximately)

Problem 3(25pts, 5pts for the first question, 4pts for the others).

1. SW R16,12(R6)   IF ID EX MEM WB

   LW R16,8(R6)   IF ED EX MEM WB

   BEQ R5,R4,Lbl   IF ID EX MEM WB

   ADD R5,R1,R4   ** ** IF ID EX MEM WB

   SLT R5,R15,R4   IF ID EX MEM WB

   Therefore, we need 11 cycles, the execution time is 11 * 200 = 2200ps. Notice that nops are still an instruction. This means that they must still be fetched. This means that we cannot fix this problem by using them.

2. Unmodified: 5+4=9 cycles

   Modified: 5+3=8 cycles

   The speedup is:9/8 = 1.125

   If the branch outcome is determined in the EX phase, the stalling lasts 2 cycles.

   If the branch outcome is determined in the ID phase, the stalling lasts 1 cycle.

   So, the first case takes 5 + 4 + 2 = 11cycles, The second case takes 5 + 4 + 1 = 10 cycles, So, the speedup is 11/10 = 1.1.

3. The "EX+MEM" phase takes 210 ps, which is the new clock cycle time (since it becomes the slowest phase). This means that the execution time with this modification is 8 * 210 = 1680ps

   So, the speedup becomes 1800/1680 = 1.07

4. With this modification, the latency of EX phase becomes 140 ps, while the latency of ID phase becomes 180 ps. So, the clock cycle time remains 200 ps. This means that the speedup remains 1.1.

5. The new EX latency is 130 ps. However, the clock cycle time remains 200 ps.

   On the other hand, the stalling lasts one additional cycle. So, the execution lasts 5+4+3=12 cycles. This means that the speedup is 11/12 = 0.92.

Problem 4(25pts, 5pts per question).

1. ADD R5,R0,R0

   Again:

   BEQ R5,R6,End

   ADD R10,R5,R1

   LW R11,0(R10)

   LW R10,1(R10)

   SUB R10,R11,R10

   ADD R11,R5,R2

   SW R10,0(R11)

   ADDI R5,R5,2

   BEQ R0,R0,Again

   End:

2.

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
ADD R5,R0,R0	IF	ID	EX	ME	WB																			
nop	*	*	*	*	*																			
BEQ R5,R6,End		IF	ID	EX	ME	WB																		
nop		*	*	*	*	*																		
ADD R10,R5,R1			IF	ID	EX	ME	WB																	
nop			*	*	*	*	*																	
LW R11,0(R10)				IF	ID	EX	ME	WB																
nop				*	*	*	*	*																
LW R10,1(R10)					IF	ID	EX	ME	WB															
nop					*	*	*	*	*															
nop					*	*	*	*	*	*														
nop						*	*	*	*	*														
SUB R10,R11,R10							IF	ID	EX	ME	WB													
nop							*	*	*	*	*													
ADD R11,R5,R2								IF	ID	EX	ME	WB												
nop								*	*	*	*	*												
SW R10,0(R11)									IF	ID	EX	ME	WB											
ADDI R5,R5,2									IF	ID	EX	ME	WB											
BEQ R0,R0,Again										IF	ID	EX	ME	WB										
nop										*	*	*	*	*	*									
BEQ R5,R6,End											IF	ID	EX	ME	WB									
nop											*	*	*	*	*									
ADD R10,R5,R1												IF	ID	EX	ME	WB								
nop												*	*	*	*	*								
LW R11,0(R10)													IF	ID	EX	ME	WB							
nop													*	*	*	*	*							
LW R10,1(R10)														IF	ID	EX	ME	WB						
nop														*	*	*	*	*						
nop														*	*	*	*	*	*					
nop															*	*	*	*	*					
SUB R10,R11,R10																IF	ID	EX	ME	WB				
nop																*	*	*	*	*				
ADD R11,R5,R2																	IF	ID	EX	ME	WB			
nop																	*	*	*	*	*			
SW R10,0(R11)																		IF	ID	EX	ME	WB		
ADDI R5,R5,2																		IF	ID	EX	ME	WB		
BEQ R0,R0,Again																			IF	ID	EX	ME	WB	
nop																			*	*	*	*	*	*
BEQ R5,R6,End																				IF	ID	EX	ME	WB
nop																				*	*	*	*	*

3. ADD R5,R0,R0
   Again:
   ADD R10,R5,R1
   BEQ R5,R6,End
   LW R11,0(R10)
   LW R10,1(R10)
   ADD R11,R5,R2
   SUB R10,R11,R10
   ADDI R5,R5,2
   SW R10,0(R11)
   BEQ R0,R0,Again
   End:

4.

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
ADD R5,R0,R0	IF	ID	EX	ME	WB																
nop	*	*	*	*	*																
ADD R10,R5,R1		IF	ID	EX	ME	WB															
nop		*	*	*	*	*															
BEQ R5,R6,End			IF	ID	EX	ME	WB														
LW R11,0(R10)			IF	ID	EX	ME	WB														
LW R10,1(R10)				IF	ID	EX	ME	WB													
ADD R11,R5,R2				IF	ID	EX	ME	WB													
nop				*	*	*	*	*													
nop				*	*	*	*	*													
SUB R10,R11,R10						IF	ID	EX	ME	WB											
nop						*	*	*	*	*											
ADDI R5,R5,2							IF	ID	EX	ME	WB										
SW R10,0(R11)							IF	ID	EX	ME	WB										
BEQ R0,R0,Again								IF	ID	EX	ME	WB									
nop								*	*	*	*	*									
ADD R10,R5,R1									IF	ID	EX	ME	WB								
nop									*	*	*	*	*								
BEQ R5,R6,End										IF	ID	EX	ME	WB							
LW R11,0(R10)										IF	ID	EX	ME	WB							
LW R10,1(R10)											IF	ID	EX	ME	WB						
ADD R11,R5,R2											IF	ID	EX	ME	WB						
nop											*	*	*	*	*						
nop											*	*	*	*	*						
SUB R10,R11,R10													IF	ID	EX	ME	WB				
nop													*	*	*	*	*				
ADDI R5,R5,2														IF	ID	EX	ME	WB			
SW R10,0(R11)														IF	ID	EX	ME	WB			
BEQ R0,R0,Again															IF	ID	EX	ME	WB		
nop															*	*	*	*	*		
ADD R10,R5,R1																IF	ID	EX	ME	WB	
nop																*	*	*	*	*	
BEQ R5,R6,End																	IF	ID	EX	ME	WB
nop																	*	*	*	*	*

5.
Assume that the loop repeats twice:
1-issue: 20+4+2 = 26cycles
2-issue: 21cycles
Speed up:26/21 = 1.24