Answers for CS202 Computer Organization HW#4

Problem 1 (30 points)

1 (5 points)

Offset: 5 bits, thus the block size is 2^5 = 32 bytes = 8 words

2 (5 points)

Index: 5 bits, thus number of entries = $2^5 = 32$

3 (5 points)

Consider one block:

The cache has valid bit, dirty bit and reference bit.

$(32 * 8 + 22 + 3)/(32 * 8) = 1.098$

4 (5 points)

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	4	7	5	0	0	4	0	5	4
Tag	0	0	0	0	0	0	1	0	0	3	0	2
Hit/Miss	M	H	H	M	M	M	M	M	H	M	H	M
Replace	N	N	N	N	N	N	Y	Y	N	Y	N	Y

Index=number of block in cache
=[block address/block size] mod (number of entries)

Tag = [block address/block size] /(number of entries)

4 blocks are replaced

5 (5 points)

Hit ratio = 4/12=0.33

6 (5 points)

<index	tag	data>
$<00000_2$	$00000000000000000000011_2$	Mem[3072]>
$<00100_2$	$00000000000000000000010_2$	Mem[2176]>
$<00101_2$	$00000000000000000000000_2$	Mem[160]>
$<00111_2$	$00000000000000000000000_2$	Mem[224]>

或者:

<index	tag	data>
< 0	3	Mem[3072]-Mem[3103]>
< 4	2	Mem[2176]-Mem[2207]>
< 5	0	Mem[160]-Mem[191]>
< 7	0	Mem[224] -Mem[255]>

Index、Tag 用十进制或者二进制均可，data 段用 Mem[起始地址]或者 Mem[起始地址]到 Mem[终止地址]一整段表示均可。

评分标准：计算题公式正确（2 分），代入计算得到正确结果（3分）。 1.6 每行错误扣1分

Problem 2 (30 points)

1 (5 points)

4 set and offset:1

Index: 2-1

Tag: 31-3

2 (5 points)

Address	Index	Tag	Hit/Miss	Contents
3	1	0	M	{} {3} {} {}
180	2	22	M	{} {3} {180} {}
43	1	5	M	{} {3,43} {180} {}
2	1	0	H	{} {3,43} {180} {}
191	3	23	M	{} {3,43} {180} {191}
88	0	11	M	{88} {3,43} {180} {191}
190	3	23	H	{88} {3,43} {180} {191}
14	3	1	M	{88} {3,43} {180} {191, 14}
181	2	22	H	{88} {3,43} {180} {191, 14}

3 (5 points)

Since this cache is fully associative and has one-word blocks, the word address is equivalent to the tag. The only possible way for there to be a hit is a repeated reference to the same word, which doesn't occur for this sequence.

Index: no bits to represent index

Tag: 31-0

4 (5 points)

Tag	Hit/Miss	Contents
3	M	3
180	M	3, 180
43	M	3, 180, 43
2	M	3, 180, 43, 2
191	M	3, 180, 43, 2, 191
88	M	3, 180, 43, 2, 191, 88
190	M	3, 180, 43, 2, 191, 88, 190
14	M	3, 180, 43, 2, 191, 88, 190, 14
181	M	180, 43, 2, 191, 88, 190, 14, 181

5 (10 points)

Main memory access=200cycle

- Only first level cache:

CPI=1.5+200*0.07=15.5

- A second level direct-mapped cache:

CPI=1.5+12*0.07+200*0.035=9.34

- A second level eight-way set cache:

  CPI=1.5+28*0.07+200*0.015=6.46

评分标准：2.1-2.4每题5分，如果把word address当成了byte address但计算正确扣一半的分（-10分）。 2.5单个结果错误扣3分

Problem 3 (15 points)

1 (5 points)

Assume that number of parity bit = p, and number of data bits = d. So there are p + d bit word:
$2^p >= p + d + 1$

and we get p ≥ 8, we need 8 bits parity bit for single error correcting.

Considering double error detecting, we need another parity bit for checking all bits. Therefore, the minimum number of parity bits required to protect a 128-bit word using the SEC/DED code is 8+1=9.

评分标准：回答出8 bits parity bit for single error correcting（2 分），回答出正确的9 bits结果（3分）

2 (10 points)

0x375 = 0011 0111 0101

Bit position		1	2	3	4	5	6	7	8	9	10	11	12
Encoded date bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity bit coverate	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

Position 1 checks bits 1, 3, 5, 7 ,9, 11
Position 2 checks bits 2, 3, 6, 7 ,10, 11
Position 4 checks bits 4, 5, 6, 7 ,12
Position 8 checks bits 8, 9, 10, 11, 12

$$\text{Parity bits } 1 = \text{XOR}(0,1,0,1,0,0) = 0$$
$$\text{Parity bits } 2 = \text{XOR}(0,1,1,1,1,0) = 0$$
$$\text{Parity bits } 4 = \text{XOR}(1,0,1,1,1) = 0$$
$$\text{Parity bits } 8 = \text{XOR}(1,0,1,0,1) = 1$$

C = 1000, it is a single error in bit 8. Corrected value =0011 0110 0101 = 0x365

评分标准：回答出有error（2 分），纠正出正确结果（8分）

Problem 4 (25 points)

1 (5 points)

Bits 31-12 is virtual memory address.

Bits 11-0 is offset.

2 (15 points)

Address	Virtual Page	TLB H/M
4669	1	TLB miss,PT miss, PF
2227	0	TLB miss, PT hit
13916	3	TLB hit
34587	8	TLB miss,PT miss, PF
12608	3	TLB hit

Final TLB

Valid	Tag	Physical Page Number
1	0	5
1	8	14
1	3	6
1	1	13

FInal page table

Valid	Physical Page or in Disk
1	5
1	13
0	Disk
1	6
1	9
1	11
0	Disk
1	4
1	14
0	Disk
1	3
1	12

3 (5 points)

There are two sets, so index takes 1 bit.

Address	Virtual Page	Index	Tag	TLB H/M
4669	1	1	0	TLB miss,PT miss, PF
2227	0	0	0	TLB miss,PT hit
13916	3	1	1	TLB miss,PT hit
34587	8	0	4	TLB miss,PT miss, PF
12608	3	1	1	TLB hit

Final TLB

Valid	Tag	Physical page number	Index
1	4	14	0
1	0	5	0
1	0	13	1
1	1	6	1

All memory references must be cross referenced against the page table and the TLB allows this to be performed without accessing off-chip memory (in the common case). If there were no TLB, memory access time would increase significantly.

评分标准：4.2中过程，Final TLB，Final page table各5分，TLB中本身存在的数据各种替换顺序结果均正确。4.3 Final TLB正确4分，回答TLB优势合理1分