ELEC 3441 Hw_3 Part C:

Open-ended Survey Report

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1960s: IBM System/360 - Model 75

`A discontinued high end/high performance system`

- **Year of Relase**: April 22, 1965
- **Manufacturing technology**: primarily included discrete transistor-based components.
- **Clock frequency**: Fixed, 1 MHz (1μsec, Model 30) / 16.67 MHz （60 nsec, Model 91), no data found for Model 75.
- **Overall architecture**: Single-processor architecture designed for large enterprises and scientific computing.
- **Cache design**: None. The 360/75 was the top end of the classic 360 machines. The 360/85 was a prototype for the 370/165, which was a very similar machine. It was the first IBM machine to use a cache memory ("storage buffer") in static RAM.
- **Number of operations per cycle**: Executes a single scalar operation per cycle.
- **Other information**:
  The Model 75 implements the complete `System/360 universal instruction set` architecture, including floating-point, decimal, and character operations as standard features.
  Another feature was the independent storage sections provided `two-way (H75)` or `four-way (I75, J75)`. The implementation of `four-way interleaving` significantly improved the efficiency of sequential access, allowing for faster data retrieval and enhanced overall system performance. Even with only two-way interleaving, "an effective sequential access rate of 400 nanoseconds per double word (eight bytes) is possible".

1990s: IBM POWER1

`A multi-chip CPU developed and fabricated by IBM`

- **Year of Relase**: 1990
- **Manufacturing technology**: 0.72 μm for POWER2(1993), data of POWER1 not found.
- **Clock frequency**: Fixed, 25-41.6 MHz
- **Overall architecture**: Single-processor
- **Cache design**: 8 KB
- **Number of operations per cycle**: single scalar
- **Other information**:
  The POWER1 is the first microprocessor that used register renaming and out-of-order execution.

2020s: Apple M1

`Leap of ARM in general-purpose high-performance scenarios`

- **Year of Relase**: 2020
- **Manufacturing technology**: 5nm
- **Clock frequency**: Variable, Max 3.2GHz
- **Overall architecture**: Multi-core
- **Cache design**:
    - L1: 192+128 KB per performance core, 128+64 KB per efficient core
    - L2: 12MB per performance core, 4MB per efficient core
    - L3: 8MB
- **Number of operations per cycle**: Superscalar
- **Other information**:
  The energy efficiency of the M1 increases battery life of M1-based MacBooks by 50% compared to previous Intel-based MacBooks.
  The M1 contains dedicated neural network hardware in a 16-core Neural Engine, capable of executing 11 trillion operations per second. Other components include an image signal processor, a PCI Express storage controller, a USB4 controller that includes Thunderbolt 3 support, and a Secure Enclave.

Comparision

The three processors are very different.

The `System/360 series` was the first computer series to adopt a unified instruction set architecture. This meant that different models of System/360 could run the same software, providing a paradigm of compatibility that later computer designs followed. This concept has been widely applied in subsequent computer architectures, including the current x86 and ARM architectures. Although the `System/360 – Model 75` itself did not have a cache design, it introduced the concept of caching to IBM's later computers. Subsequent models like the `System/360` series started utilizing caches to improve memory access speed and overall system performance. This idea became a standard in later computer designs, with caches becoming an integral component of modern processors.

`IBM POWER1` introduced several advanced architectural features such as register renaming and out-of-order execution. These features improved the performance and efficiency of the processor, providing crucial examples for subsequent processor designs. Register renaming allowed the processor to rename registers during instruction execution, enhancing instruction-level parallelism and performance. Out-of-order execution enabled the processor to execute instructions in a more efficient manner, further improving performance.

Additionally, `IBM POWER1` IBM POWER1 adopted an open architecture and standards, providing a broad development space for partners and developers. IBM actively promoted the openness and collaboration of the `Power` architecture, enabling other vendors to develop their own products and solutions based on the `Power` architecture. This concept of openness and collaborative ecosystem persisted in later POWER series processors, offering increased choices and innovations to diverse market demands.

The `Apple M1` is a system-on-chip processor designed by Apple for use in their Mac computers. It is notable for being the first processor to use Apple's custom ARM-based architecture and for its impressive performance and power efficiency. The M1 is important because it represents a shift away from the x86 architecture that has dominated the personal computer industry for decades. It proved that ARM processors can al processors can also handle complex and high- performance work, while consuming far less power. The M1 has a complex cache hierarchy that includes multiple levels of caches, including a unified L2 cache.

A notable trend in the evolution of processors is the pursuit of wider and more complex cache

designs, along with an increase in the number of processor cores, higher clock frequencies, enhanced microarchitecture designs, and optimized instruction-level parallelism, among other factors. As the performance gains of individual processor cores face physical limitations, the significance of developing multi-core processors has grown considerably. Multi-core processors integrate multiple processor cores onto a single chip, enabling improved overall performance through parallel processing of tasks.

Reference:

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- # IBM System/360
- POWER1
- Apple M1
- M1芯片