ELEC3441 HW1 PartB Report

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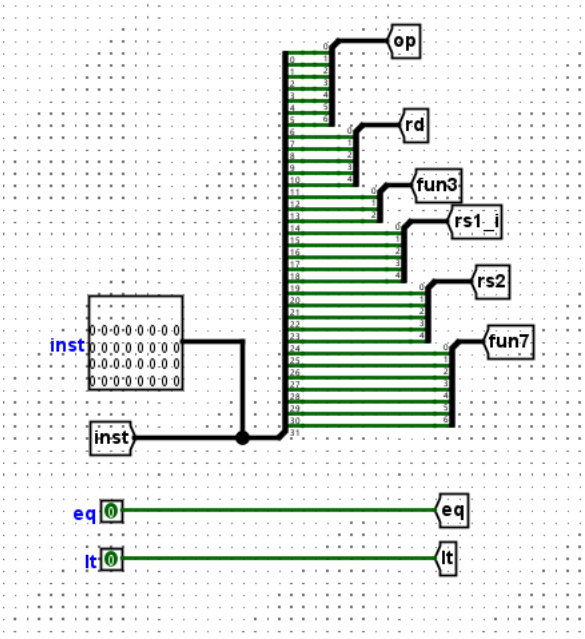
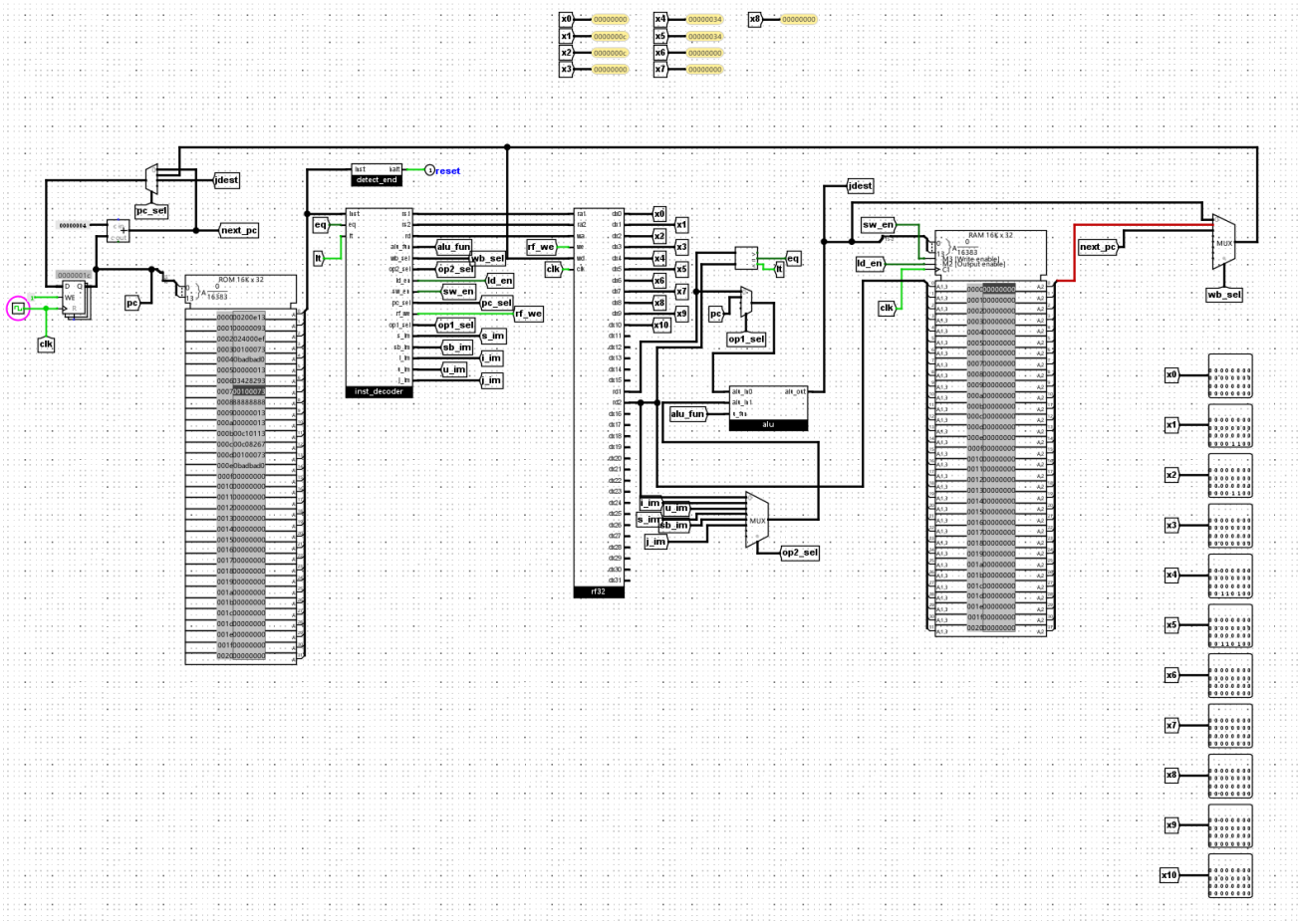
Implementations

All the instructions required, including addi , sw , lw , auipc , beq , bne , blt , bge , jal , jalr are implemented in rv32-full.circ.

Although 3 files are submitted as required, some bugs were found in rv32-full.circ .
When we load the test files to exam the processor, the instruction code sometimes present 0000…. While the instruction still can be processed in the processor.
e.g. When I load jaljalr.mem into the memory in my computer, the instruction in encoder presents 0000… The result is correct. While when I try it on another classmate's computer, the instruction works correctly.





Modifications

- An output pin op1_sel is added to the instruction decoder, as it's required by auipc .
- Only two input pins eq , lt is reserved for branch conditions, as they are enough for all branches. The names are changed to avoid confusion with the instruction names.
- A halt is added in B3. When halt is asserted, pc will be reset to 0.

Contribution

The workload of this project is equally distributed.