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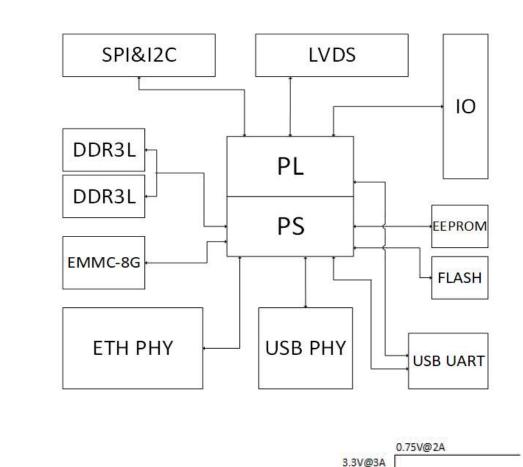
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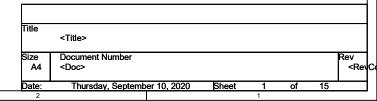


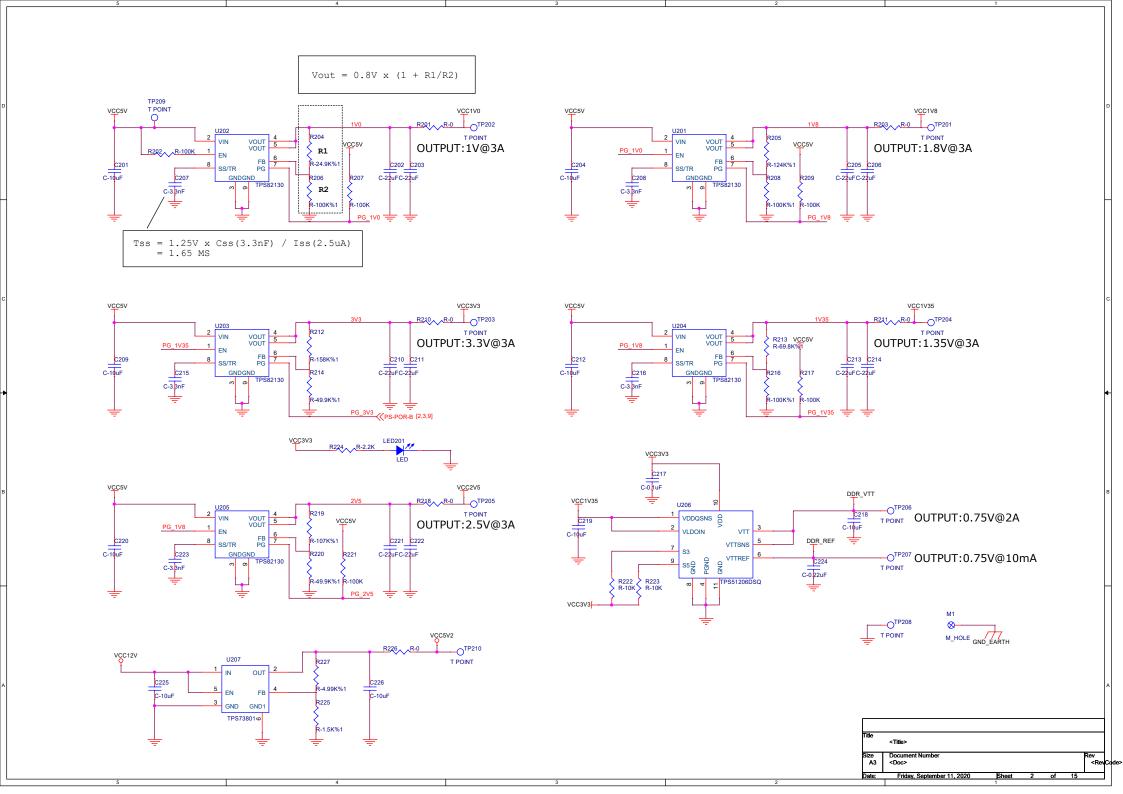
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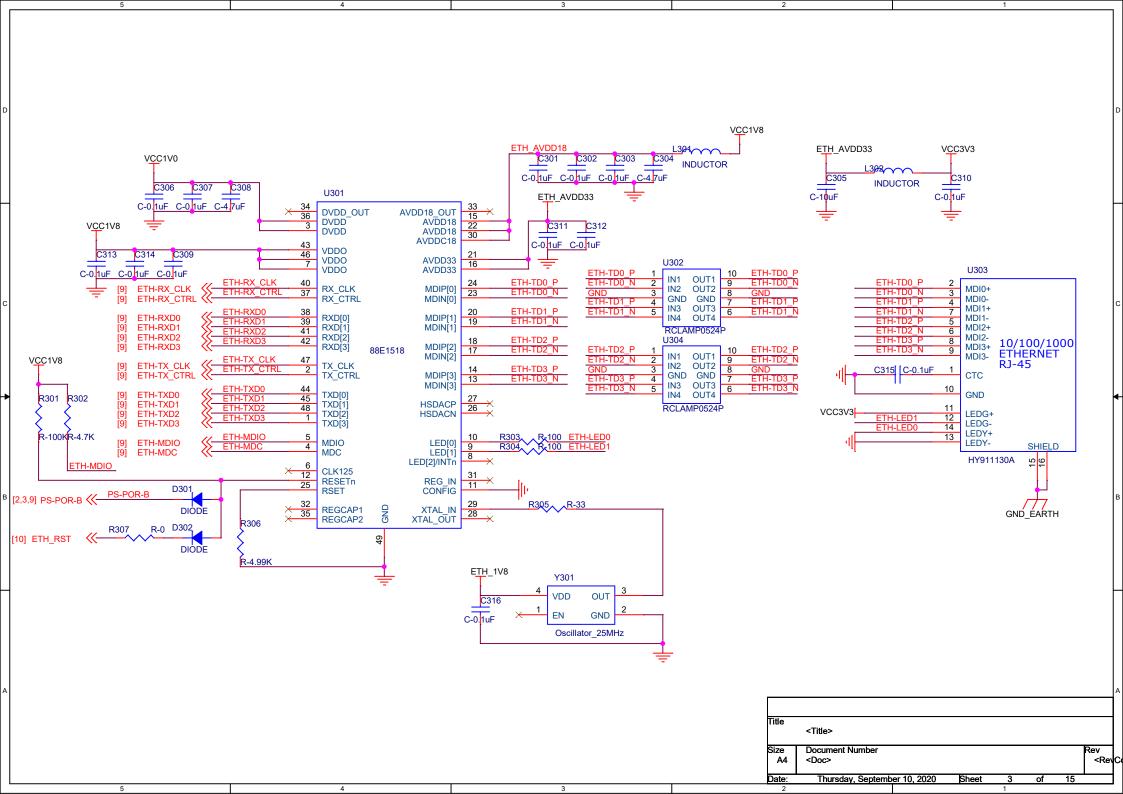
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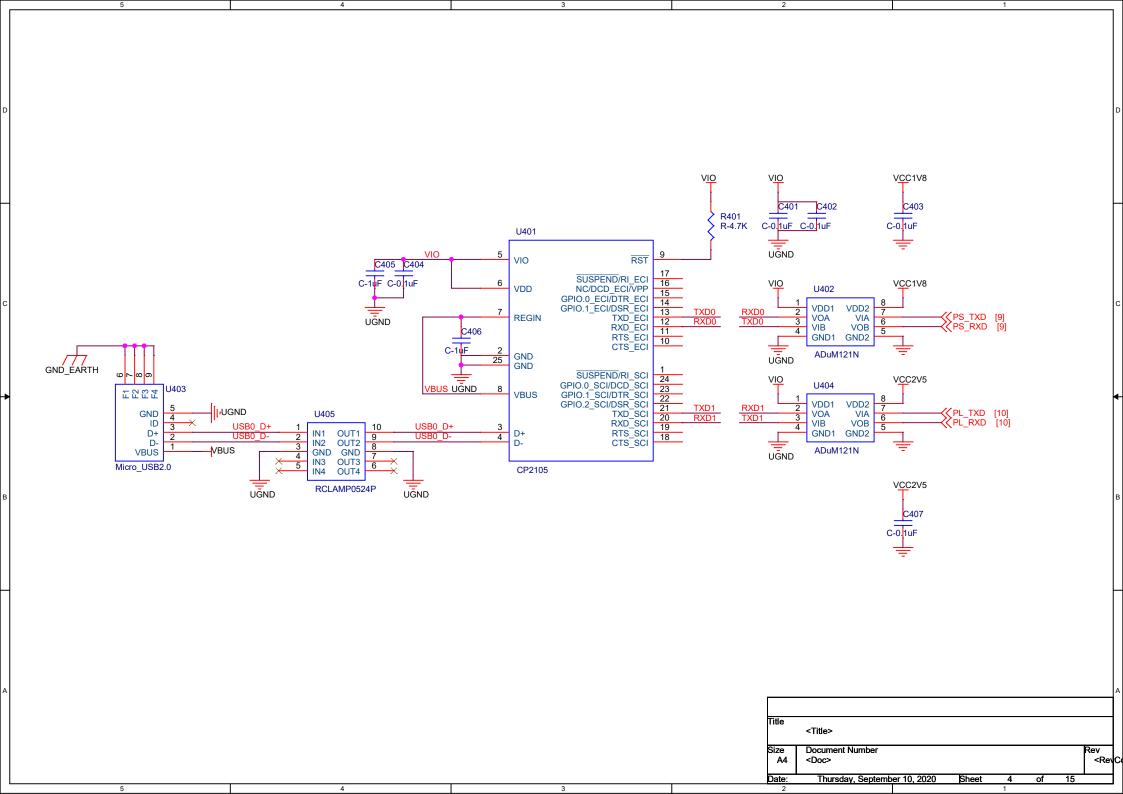
1.0V@3A

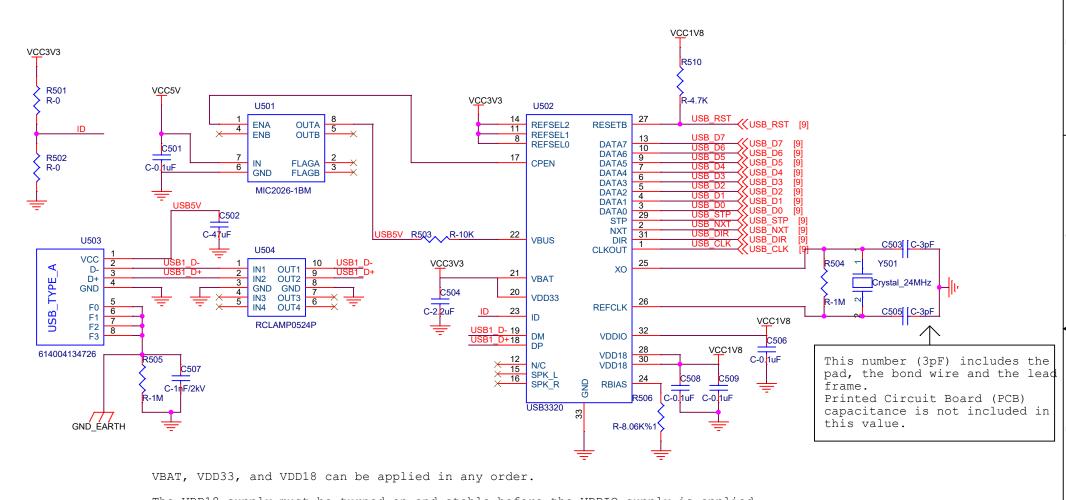
5V





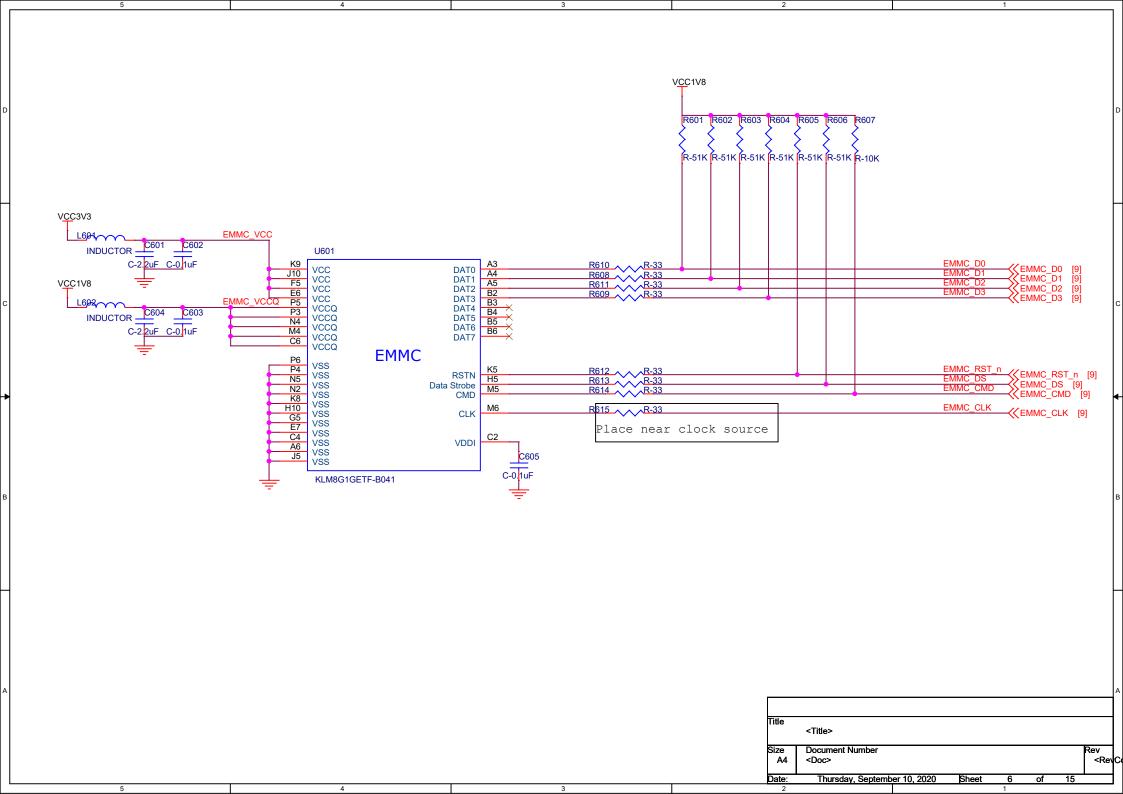


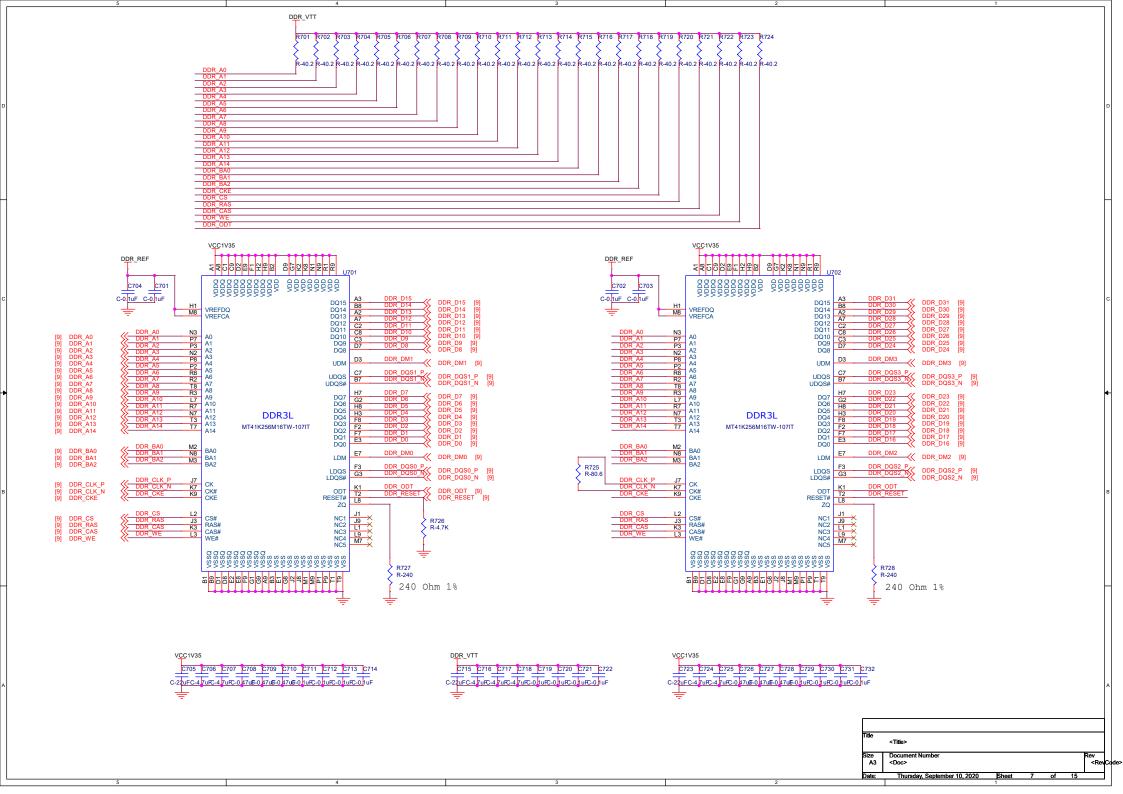


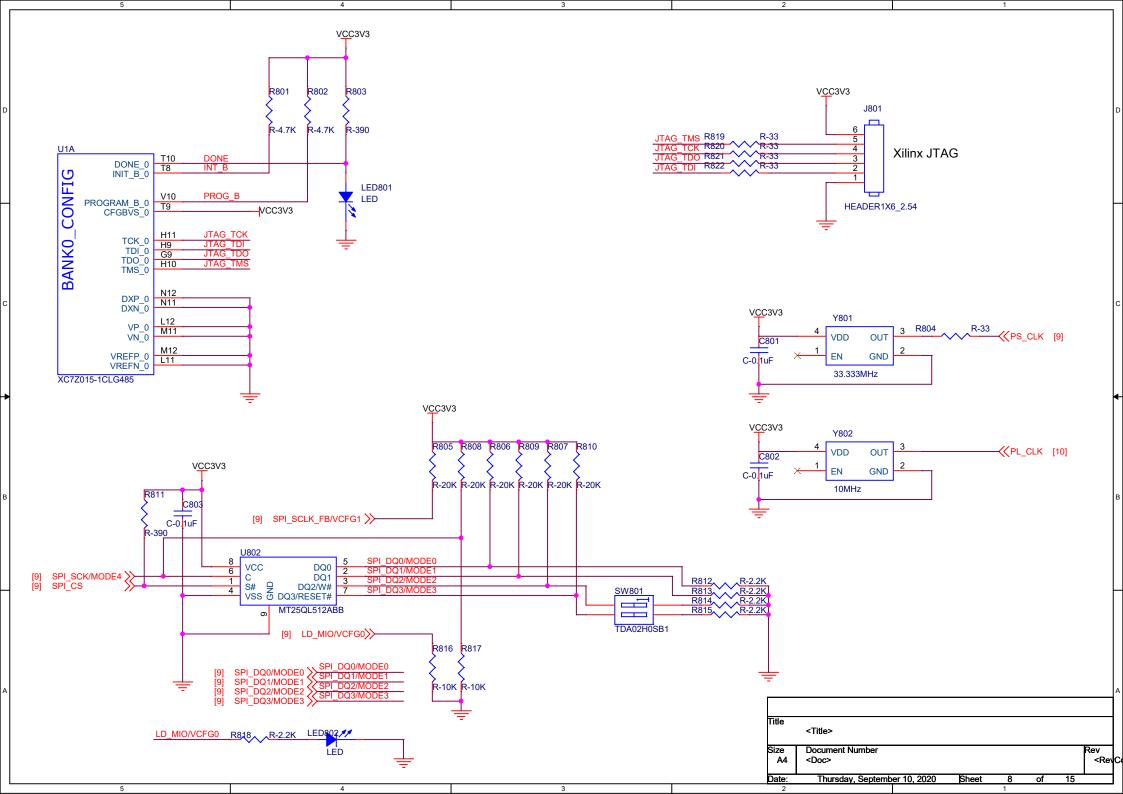


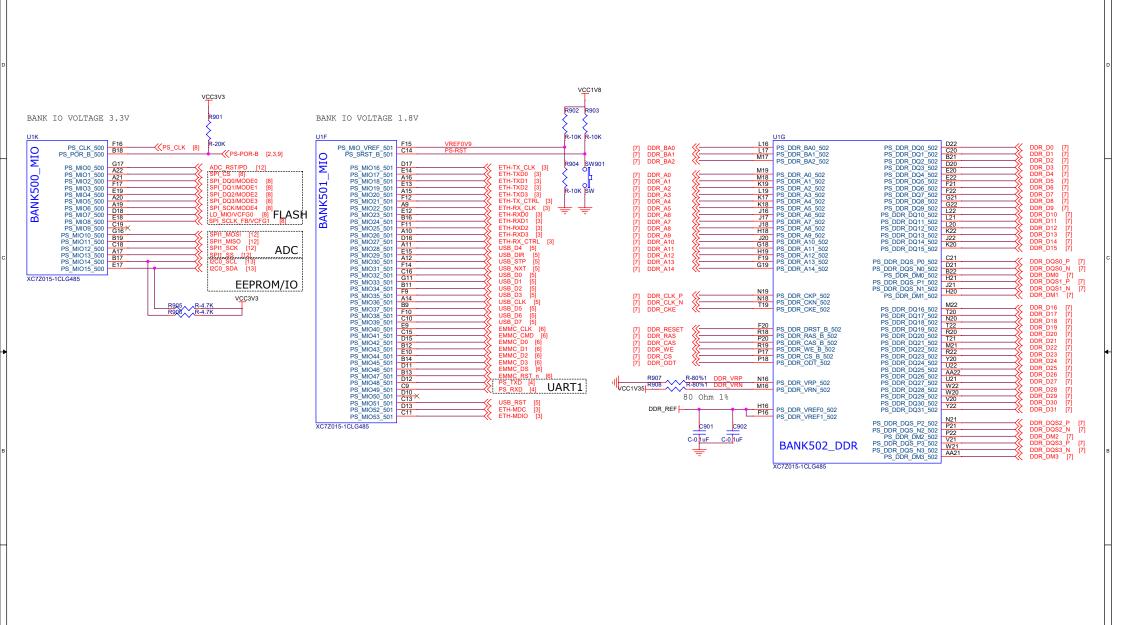
The VDD18 supply must be turned on and stable before the VDD10 supply is applied.

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Power on or Loader FW PUDC B: 1 = High, ALL IO Enable PULL UP Resistor PUDC_B: 0 = GND, ALL IO Disable PULL UP Resistor BANK IO VOLTAGE 2.5V BANK IO VOLTAGE 2.5V BANK IO VOLTAGE 3.3V VCC2V5 U1B R1002 R-0
LVDS_R0_P R1003 R-0
LVDS_R0_N R1005 R-0
LVDS_R1_P R1006 R-0
LVDS_R1_N R1008 R-0 R1015 B13_T16 [15] LVDS_DATA0_P LVDS_DATA0_N LVDS_DATA1_P LVDS_DATA1_N IO_0_34 IO_L1P_T0_34 IO_L1N_T0_34 IO_L2P_T0_34 B34_H8 [15] LVDS_REV0_P [15] LVDS_REV0_N [15] IO_0_35 IO_L1P_T0_AD0P_35 IO_L1N_T0_AD0N_35 IO_L2P_T0_AD8P_35 DPSA_ERR DPSB_ERR 至 뚶 DPSC_ERR DPSD_ERR R-10K IO_L2N_T0_AD8N_35 IO_L3P_T0_DQS_AD1P_35 BANK13 LVDS_DATA1_N
LVDS_DATA2_P
LVDS_DATA2_N
LVDS_DATA3_N
LVDS_DATA4_P
LVDS_DATA4_P
LVDS_DATA5_P
LVDS_DATA5_N
LVDS_DATA6_N
LVDS_DATA6_N
LVDS_DATA6_N
LVDS_DATA6_N
LVDS_DATA7_N
LVDS_DATA7_N
LVDS_DATA7_N
LVDS_DATA7_N
LVDS_DATA7_N IO_L2N_T0_34 IO_L3P_T0_DQS_PUDC_B_34 BANK34 DPSE_ERR DPSF_ERR VVDS R2 P R1018 R0
LVDS R2 N R1020 R0
LVDS R3 P R1024 R0
LVDS R3 N R1025 R0
LVDS R4 N R1027 R0
LVDS R4 N R1027 R0
LVDS R5 P R1028 R0 IO_L3N_T0_DQS_34 IO_L4P_T0_34 IO_L3N_T0_DQS_AD1N_35 IO_L4P_T0_35 16 R1011 LVDS_REV2_P [15] LVDS_REV2_N [15] LVDS_REV3_P [15] CFG0 CFG1 IO_L4P_10_35 IO_L4N_T0_35 IO_L5P_T0_AD9P_35 IO_L5N_T0_AD9N_35 IO_L6P_T0_35 IO_L4N_T0_34 IO_L5P_T0_34 CFG2 [14] [14] [14] [14] [14] [14] CFG3 CFG4 CFG5 CFG6 CFG7 LED0 IO_L5N_T0_34 IO_L6P_T0_34 LVDS REV3 N 115 R-10K M8 M7 IO_L6P_T0_35 IO_L6N_T0_VREF_35 IO_L7P_T1_AD2P_35 IO_L7N_T1_AD2N_35 IO_L8P_T1_AD10P_35 IO_L6N_T0_VREF_34 IO_L7P_T1_34 LVDS_REV4_N LVDS_REV5_P J5 K5 IO_L7N_T1_34 IO_L8P_T1_34 LVDS_REV5_N LVDS_REV6_P IO L8P T1 13
IO_L8N_T1 13
IO_L8P_T1 DQS 13
IO_L9N_T1 DQS 13
IO_L9N_T1 DQS 13
IO_L10P_T1 13
IO_L10P_T1 13
IO_L11P_T1 SRCC 13
IO_L11N_T1 SRCC 13 LVDS_REV6_N LVDS_REV7_P LVDS_REV7_N LVDS_REV8_P [14] [14] [14] [14] [14,15] LVDS_DATA7_N LVDS_DATA8_P LED1 LED2 IO_L8N_T1_34 IO_L8N_T1_AD10N_35 IO_L8N_I1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10P_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34 IO LBN_IT_ADJUNTS 35 IO LPN_TT_DQS_ADSP_35 IO_LPN_TT_DQS_ADSN_35 IO_LTOP_TT_ADJUNTS 35 IO_LTOP_TT_SRCC_35 IO_LTOP_TT_SRCC_35 IO_LTOP_TT_SRCC_35 IO_LTOP_TT_MRCC_35 IO_LTOP_TT_MRCC_35 K2 L2 LVDS_DATA8_N LVDS_DATA9_P LED3 SW0 LVDS_DATA9_P LVDS_DATA9_N LVDS_DATA10_P LVDS_DATA10_N LVDS_DATA11_P LVDS_DATA11_N LVDS_DATA12_P LVDS_DATA12_N LVDS_REV8_N LVDS_REV9_P SW1 [14,15] [14,15] [14,15] SW2 K3 SW3 IO L11N T1 SRCC 34 IO L12P T1 MRCC 34 IO L12N T1 MRCC 34 IO L13P T2 MRCC 34 IO L13P T2 MRCC 34 IO L14P T2 SRCC 34 IO L14P T2 SRCC 34 B34_L12_P B34_L12_N B34_L13_P B34_L13_N PL_CLK [8] B35_L12_N [15] IO0 [14] IO1 [14] IO_L12P_T1_MRCC_13 IO_L12N_T1_MRCC_13 IO_L12N_I1_MRCC_35 IO_L13P_T2_MRCC_35 IO_L13N_T2_MRCC_35 IO_L14P_T2_AD4P_SRCC_35 IO_L14N_T2_AD4N_SRCC_35 IO L13N T2 MRCC 13 IO L14P T2 SRCC 13 IO L14N T2 SRCC 13 LVDS_DATA12_N
LVDS_DATA13_P
LVDS_DATA13_N
LVDS_DATA14_N
LVDS_DATA14_N
LVDS_DATA15_N
LVDS_DATA15_N
LVDS_CLK0_N [
LVDS_CLK1_N [
LVDS_CLK1_N [
LVDS_CLK1_N [
LVDS_CLK2_P [
LVDS_CLK2_N [
LVDS_CLX_N [
LVDS_CLK2_N [
LVDS_CLX_N [
LVDS SPI5_MOSI SPI5_MISO IO2 IO3 R1060 R-0
R1022 R-0
R1024 R-0
R1024 R-0
R1024 R-0
R1068 R-0
R1068 R-0
R1072 R-0
R1072 R-0
R1074 R-0 M2 IO_L15P_T2_DQS_34 SPI5_SCK SPI5_SS IO_L15P_T2_DQS_AD12P_35 IO L15P T2 DQS 34 IO L15N T2 DQS 34 IO L16P T2 34 IO L16P T2 34 IO L17P T2 34 IO L17P T2 34 IO L18P T2 34 IO L18P T2 34 IO L18P T3 34 IO L19P T3 34 IO_L15P_T2_DQS_AD12P_35 IO_L15N_T2_DQS_AD12N_35 IO_L16P_T2_35 IO_L17P_T2_AD5P_35 IO_L17P_T2_AD5P_35 IO_L17P_T2_AD13P_35 IO_L18P_T2_AD13P_35 IO_L18P_T2_AD13N_35 IO_L18P_T3_AD12P_33 IO_L20P_T3_AD6P_35 IO_L20P_T3_AD6P_35 IO_L20P_T3_AD6P_35 SPI4_MOSI SPI4_MISO SPI4_MISO SPI4_SCK SPI4_SS [1 SPI3_MOSI Driver Board: SPI3 MISO SPI3_SCK LVDS_CLK2_P LVDS_CLK3_P LVDS_CLK3_P LVDS_CLK3_P LVDS_CLK4_P LVDS_CLK4_N LVDS_CLK5_N LVDS_CLK6_P LVDS_CLK6_P LVDS_CLK7_P LVDS_CLK7_P LVDS_CLK7_P LVDS_CLK7_P IO_L19N_T3_VREF_34 IO_L20P_T3_34 SPI3_SS [15] SPI2_MOSI [IO_L20P_T3_34 IO_L20N_T3_34 IO_L21P_T3_DQS_34 IO_L21N_T3_DQS_34 IO_L22P_T3_34 IO_L22N_T3_34 IO_L23P_T3_34 IO_L23P_T3_34 IO_L2Ur_13_AD6n_35 IO_L20N_T3_AD6N_35 IO_L21P_T3_DQS_AD14P_35 E3 SPI2 MISO N4 N3 SPI2_SCK IO_L21P_T3_DQS_AD14P_35 IO_L21N_T3_DQS_AD14N_35 IO_L22P_T3_AD7P_35 IO_L22N_T3_AD7N_35 UARTO O B35_L22_P B35_L22_N B35_L23_P B35_L23_N IO_L23P_T3_35 IO_L23N_T3_35 SPI0_MISO IO_L24P_T3_AD15P_35 IO_L24N_T3_AD15N_35 H5 IO_L24P_T3_34 R7 IO_L24N_T3_34 R8 Firmware **EMIO** R1098 R-0 B13_U16 [15] IO_25_34 IO_25_35 XC77015-1CL G485 XC77015-1CLG485 XC7Z015-1CLG485 LVDS_R8_P LVDS_R8_N LVDS_R9_P [15] [15] [15] [15] U7 MGTRREF 112 MGTPTXP3 112
MGTPTXP3 112
MGTPTXP2 112
MGTPTXP2 112
MGTPTXP1 112
MGTPTXN1 112
MGTPTXN0 112
MGTPTXN0 112
MGTPTXN0 112
MGTPTXN0 112 GTP LVDS_D13_N LVDS_D14_N SANK112 LVDS_D15_N LVDS_D15_N LVDS_C7_N LVDS_C6_N LVDS_C5_N LVDS_C4_N LVDS_C3_N LVDS_C2_N MGTPRXP3_112 W6
MGTPRXN3_112 MGTPRXP2_112 MGTPRXN2_112 W8
MGTPRXP1_112 LVDS_C1_N LVDS_C0_N MGTPRXP1 112 MGTPRXN1 LVDS_D14_P LVDS_D15_P LVDS_C7_P LVDS_D14_P [10] MGTPRXP0 112 AB7 LVDS_D15_P LVDS_C7_P LVDS_C6_P MGTPRXN0 112 MGTREFCLK0P_112 V9 X9 MGTREFCLK1P_112 V5 X LVDS_C3_P LVDS_C3_P LVDS_C2_P V5 🔆 MGTREFCLK1N_112 XC7Z015-1CLG485 LVDS_C1_P LVDS_C0_P <Title> Document Number A3 <Doc> <RevCo Thursday, September 10, 2020 Sheet 10

