1. Description

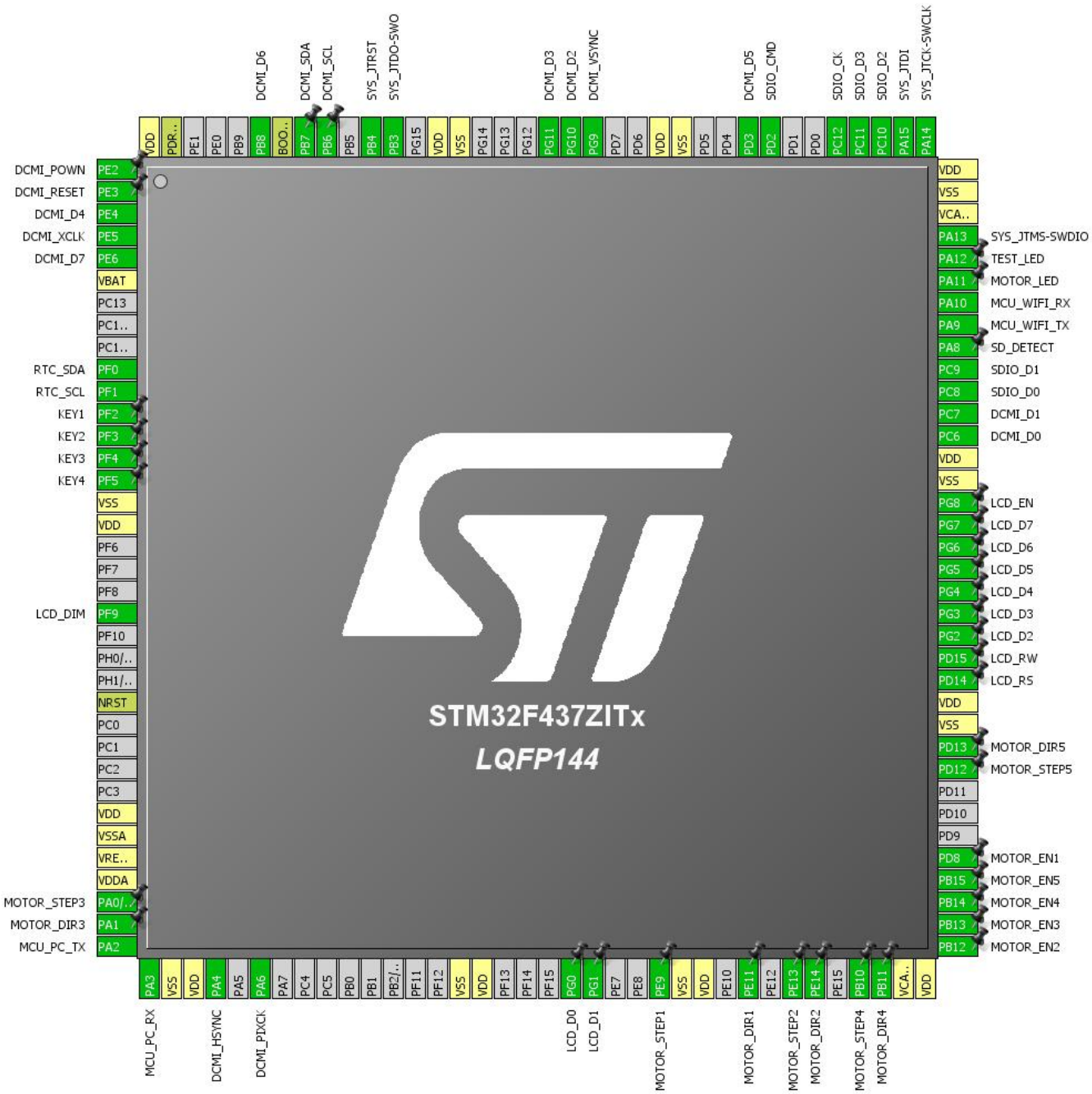
1.1. Project

Project Name	WiFi_Camera
Board Name	WiFi_Camera
Generated with:	STM32CubeMX 4.23.0
Date	11/14/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F427/437
MCU name	STM32F437ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

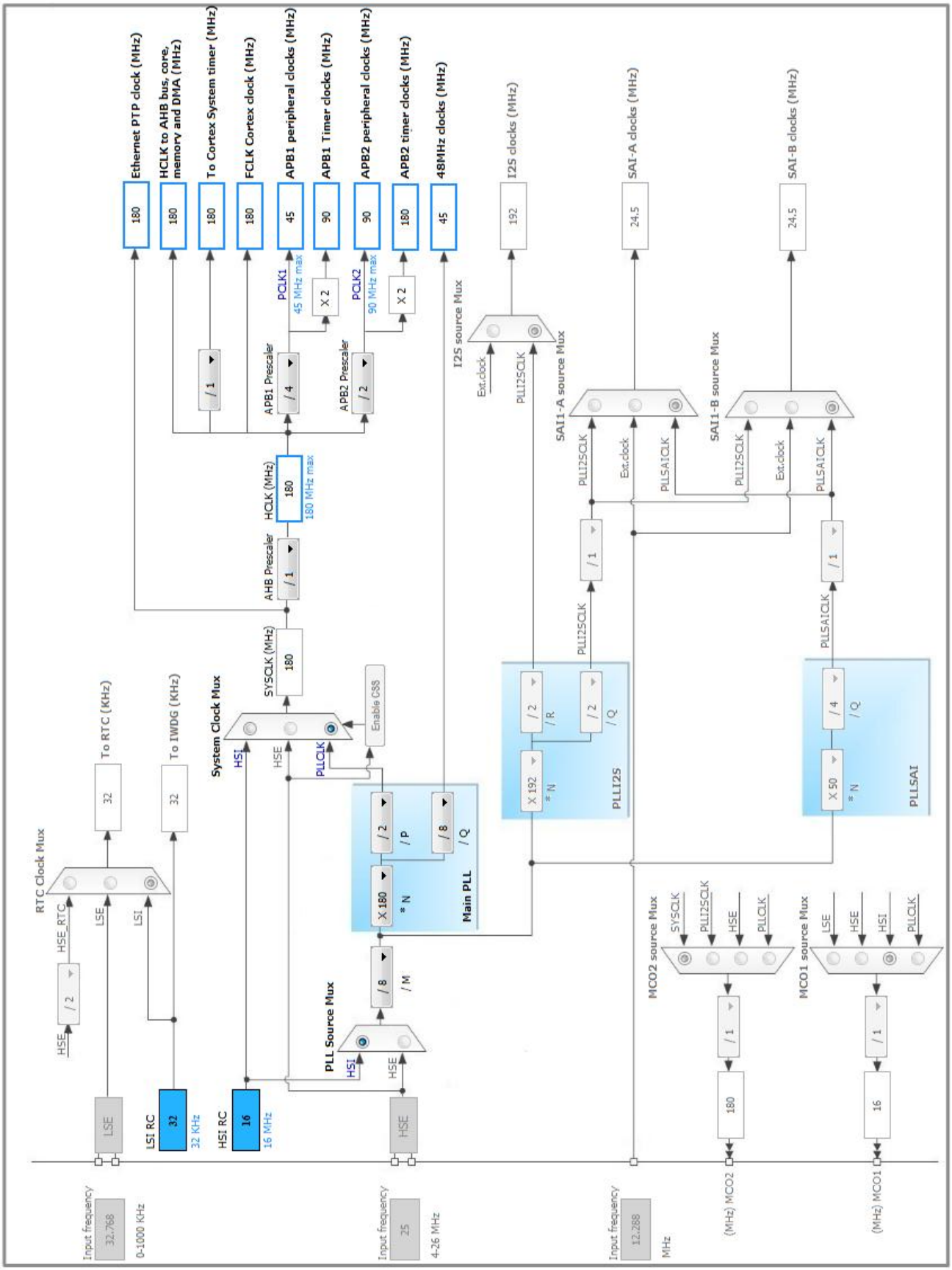
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	DCMI_POWN
2	PE3 *	I/O	GPIO_Output	DCMI_RESET
3	PE4	I/O	DCMI_D4	
4	PE5	I/O	TIM9_CH1	DCMI_XCLK
5	PE6	I/O	DCMI_D7	
6	VBAT	Power		
10	PF0	I/O	I2C2_SDA	RTC_SDA
11	PF1	I/O	I2C2_SCL	RTC_SCL
12	PF2 *	I/O	GPIO_Input	KEY1
13	PF3 *	I/O	GPIO_Input	KEY2
14	PF4 *	I/O	GPIO_Input	KEY3
15	PF5 *	I/O	GPIO_Input	KEY4
16	VSS	Power		
17	VDD	Power		
21	PF9	I/O	TIM14_CH1	LCD_DIM
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP *	I/O	GPIO_Output	MOTOR_STEP3
35	PA1 *	I/O	GPIO_Output	MOTOR_DIR3
36	PA2	I/O	USART2_TX	MCU_PC_TX
37	PA3	I/O	USART2_RX	MCU_PC_RX
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DCMI_HSYNC	
42	PA6	I/O	DCMI_PIXCK	
51	VSS	Power		
52	VDD	Power		
56	PG0 *	I/O	GPIO_Output	LCD_D0
57	PG1 *	I/O	GPIO_Output	LCD_D1
60	PE9 *	I/O	GPIO_Output	MOTOR_STEP1
61	VSS	Power		
62	VDD	Power		
64	PE11 *	I/O	GPIO_Output	MOTOR_DIR1

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
66	PE13 *	I/O	GPIO_Output	MOTOR_STEP2
67	PE14 *	I/O	GPIO_Output	MOTOR_DIR2
69	PB10 *	I/O	GPIO_Output	MOTOR_STEP4
70	PB11 *	I/O	GPIO_Output	MOTOR_DIR4
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Output	MOTOR_EN2
74	PB13 *	I/O	GPIO_Output	MOTOR_EN3
75	PB14 *	I/O	GPIO_Output	MOTOR_EN4
76	PB15 *	I/O	GPIO_Output	MOTOR_EN5
77	PD8 *	I/O	GPIO_Output	MOTOR_EN1
81	PD12 *	I/O	GPIO_Output	MOTOR_STEP5
82	PD13 *	I/O	GPIO_Output	MOTOR_DIR5
83	VSS	Power		
84	VDD	Power		
85	PD14 *	I/O	GPIO_Output	LCD_RS
86	PD15 *	I/O	GPIO_Output	LCD_RW
87	PG2 *	I/O	GPIO_Output	LCD_D2
88	PG3 *	I/O	GPIO_Output	LCD_D3
89	PG4 *	I/O	GPIO_Output	LCD_D4
90	PG5 *	I/O	GPIO_Output	LCD_D5
91	PG6 *	I/O	GPIO_Output	LCD_D6
92	PG7 *	I/O	GPIO_Output	LCD_D7
93	PG8 *	I/O	GPIO_Output	LCD_EN
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	DCMI_D0	
97	PC7	I/O	DCMI_D1	
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	SDIO_D1	
100	PA8 *	I/O	GPIO_Input	SD_DETECT
101	PA9	I/O	USART1_TX	MCU_WIFI_TX
102	PA10	I/O	USART1_RX	MCU_WIFI_RX
103	PA11 *	I/O	GPIO_Output	MOTOR_LED
104	PA12 *	I/O	GPIO_Output	TEST_LED
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15	I/O	SYS_JTDI	
111	PC10	I/O	SDIO_D2	
112	PC11	I/O	SDIO_D3	
113	PC12	I/O	SDIO_CK	
116	PD2	I/O	SDIO_CMD	
117	PD3	I/O	DCMI_D5	
120	VSS	Power		
121	VDD	Power		
124	PG9	I/O	DCMI_VSYNC	
125	PG10	I/O	DCMI_D2	
126	PG11	I/O	DCMI_D3	
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SYS_JTDO-SWO	
134	PB4	I/O	SYS_JTRST	
136	PB6 *	I/O	GPIO_Output	DCMI_SCL
137	PB7 *	I/O	GPIO_Output	DCMI_SDA
138	BOOT0	Boot		
139	PB8	I/O	DCMI_D6	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. DCMI

DCMI: Slave 8 bits External Synchro

5.1.1. Parameter Settings:

Mode Config:

Pixel clock polarity	**Active on Rising edge ***
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	**Enabled ***

5.2. I2C2

I2C: I2C

5.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.3. SDIO

Mode: SD 4 bits Wide bus

5.3.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made	Rising transition
SDIO Clock divider bypass	Disable
SDIO Clock output enable when the bus is idle	Disable the power save for the clock
SDIO hardware flow control	The hardware control flow is disabled
SDIOCLK clock divide factor	0

5.4. SYS

Debug: JTAG (5 pins)

Timebase Source: TIM1

5.5. TIM6

mode: Activated

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**180 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.6. TIM9

mode: Clock Source

Channel1: PWM Generation CH1

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**5 ***
Fast Mode	Disable
CH Polarity	High

5.7. TIM14

mode: Activated

Channel1: PWM Generation CH1

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**90 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. USART2

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.10. FREERTOS

mode: Enabled

5.10.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	**10 ***
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled

ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	**Enabled ***
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	**9 ***
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.10.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled

xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	**Enabled ***
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DCMI	PE4	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG9	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	RTC_SDA
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	RTC_SCL
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
	PB4	SYS_JTRST	n/a	n/a	n/a	
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	DCMI_XCLK
TIM14	PF9	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_DIM
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	MCU_WIFI_TX
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High**	MCU_WIFI_RX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	MCU_PC_TX
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	MCU_PC_RX
GPIO	PE2	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	DCMI_POWN
	PE3	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	DCMI_RESET
	PF2	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY1
	PF3	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY2
	PF4	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY3
	PF5	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY4
	PA0/WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_STEP3
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_DIR3
	PG0	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D0
	PG1	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D1
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_STEP1
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_DIR1
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_STEP2
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_DIR2
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_STEP4
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_DIR4
	PB12	GPIO_Output	Output Push Pull	**Pull-up ***	Low	MOTOR_EN2
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_EN3
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_EN4
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_EN5
	PD8	GPIO_Output	Output Push Pull	**Pull-up ***	Low	MOTOR_EN1
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_STEP5
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_DIR5
	PD14	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_RS
	PD15	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_RW
	PG2	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D2
	PG3	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D3
	PG4	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D4
	PG5	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D5
	PG6	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D6
	PG7	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LCD_D7

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG8	GPIO_Output	Output Push Pull	**Pull-up ***	Low	LCD_EN
	PA8	GPIO_Input	Input mode	**Pull-up ***	n/a	SD_DETECT
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_LED
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TEST_LED
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	DCMI_SCL
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DCMI_SDA

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
DCMI	DMA2_Stream1	Peripheral To Memory	Low

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

DCMI: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	Single
Memory Burst Size:	**4 Increment ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
USART1 global interrupt	true	5	0
USART2 global interrupt	true	5	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	5	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	5	0
DMA2 stream1 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
DCMI global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SDIO global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F427/437
MCU	STM32F437ZITx
Datasheet	024244_Rev10

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	WiFi_Camera
Project Folder	C:\Users\Dongyang.Xie\OSRAM\O06_Private\WiFi_Camera\FirmwareDev\WiFi_
Toolchain / IDE	EWARM
Firmware Package Name and Version	STM32Cube FW_F4 V1.17.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No