1. Multiple Access

(a) 100 Mbps = 100000000 bps

2200 m / 2 * 10^8 m/s + 8 * 30 bit / 100000000 bps = 1.34 * 10^-5 s

(b) Based on question a, propagation delay = 1.34 * 10^-5 s

250 bytes = 2000 bit

$Time_{transmit}$ = 2000 bit / 100000000 bps = 0.00002 s = 2 * 10^-5 s

$Time_{backoff}$ = 1500 / 100000000 bps = 1.5 * 10^-5 s

Thus, total time:

1.34 * 10^-5 s + 2 * 10^-5 s + 1.34 * 10^-5 s = 4.68 * 10^-5 s

(c) 2200 m / 2 * 10^8 m/s + 8 * (30+30) bit / 100000000 bps = 1.58 * 10^-5 s **-2**

2. Ethernet Timing

(a)

A does NOT finish transmitting the frame before it detects that there was a collision.
When B begins sending a frame, A has already sent 550 bit according to the propagation time. Total A. And A has to send total (1024 +128) bit. According to the calculation below, 602 > 550. It means A does not finish transmitting. There is still (602-550 = 52) bit need to be sent when A detects that there was a collision.

1024 + 128 – 550 = 602 > 550

(b)

When A detects the collision, it has already transmitted the 128 bit preamble. So it stops transmitting the frame and sends a 64 bit jamming sequence.

550 * 2 + 64 = 1164 bit

A: 1164 bit * (0.055 ms / 550 bit) = 0.1164 ms

When B detects the collision, it not finishes the 128bit preamble. So it finishes transmitting the 128 bit preamble and then sends a 64 bit jamming sequence. Also, the time B begins transmitting is at 0.055 ms.

128 + 64 = 192 bit

192 bit * (0.055 ms / 550 bit) = 0.0192 ms

B: 0.0192 ms + 0.055 ms = 0.0742 ms

(c)

After receiving all transmission, host hears an idle channel again. Based on question b, we get
A: 0.0742 ms + 0.055 ms = 0.1292 ms
B: 0.1164 ms + 0.055 ms = 0.1714 ms

(d)

Since each host next decides to retransmit immediately after hearing the channel idle, A retransmits at 0.1292 ms and B retransmits at 0.1714 ms.
Since 0.1292 + 0.055 = 0.1842 ms > 0.1714 ms, B detects collision before it retransmits.
Since 0.1714 + 0.055 = 0.2264 ms and 0.2264 – 0.1292 = 0.0972 = 972 bit durations < 128 + 1024, A detects collision and finishes preamble. So at 0.2264 ms, A transmits 64 bit jamming sequence.

A: Time_{B_start} + $\text{Time}_{B\_transmiting}$ + $\text{Time}_{propagation}$

0.1714 ms + (128 bit + 64 bit) * (0.055 ms / 550 bit) + 0.055 ms = 0.2456 ms

B: $\text{Time}_{A\_start\_jam}$ + $\text{Time}_{A\_ransmiting}$ + $\text{Time}_{propagation}$

0.2264 ms + (64 bit * (0.055 ms / 550 bit)) + 0.055ms = 0.2878 ms

(e) Success

Based on question d, A restarts at 0.2456 ms which means 2456 bit durations. B is at 2878 bit durations.

In e case, A restarts at

2456+1024 = 3480

and the time of transmission arrive A is

2878 + 550 = 3428

Since 3480>3428

It means before A retransmit, A knows B is transmitting. Then, A would not retransmit before channel becomes silent. So the transmission of host B is success.

(f) Based on question d, A hears sclience at 0.2456 ms.

0.2456 ms + 2 * 0.1024 ms + (128+1024) bit *(0.055 ms / 550 bit) = 0.5656 ms **-1**

3. Server Bandwidth

(a) Since each packet crosses the I/O bus twice and is written to and read from main memory once. (P&D, page268 line 5) We get

700Mbps / (2.4Mbps * 2) = 145

(b) Since half I/O bus speed is less than half memory bandwidth. The throughput is half I/O bus speed. And throughput = pps * (BitsPerPacket)

700 Mbps / 2 = 2200 * s   Assume packet size is s bits. **-1**

=> 350 Mbps = 2200 * s

(c) Since I/O bus speed is less than memory bandwidth, I/O bus becomes the limiting factor first.

If memory bandwidth becomes the limiting factor, we get

1.2 Gbps / 2 = 2200 * s   Assume packet size is s bits.

=> 6 * 10^8 bps = 2200 * s **-1**

=> s =272727 bit

4. Virtual Circuits

(a) A → D, A → J, H → C, E → F, D → B, B → D

VC Table Entry at Switch 1

Incoming Interface	Incoming VCI	Outgoing Interface	Outgoing VCI
1	0	3	0
1	0	0	0
0	1	3	0
3	2	2	0
2	1	3	1

VC Table Entry at Switch 2

Incoming Interface	Incoming VCI	Outgoing Interface	Outgoing VCI
1	0	3	0
1	0	2	0
3	1	1	2
1	1	3	1

VC Table Entry at Switch 3

Incoming Interface	Incoming VCI	Outgoing Interface	Outgoing VCI
1	0	2	0
3	0	0	0
2	1	1	1
1	1	2	1

VC Table Entry at Switch 4

Incoming Interface	Incoming VCI	Outgoing Interface	Outgoing VCI
2	0	1	0
3	0	2	1

(b)

	Port0	Port1	Port2	Port3
S1	1	0	1	3
S2	0	1	1	2
S3	1	1	2	0
S4	0	1	1	0

(c) H → C: 0 → 1 → 0 → 0
(d) D → B: 1 → 1 → 2 → 0

5. Spanning Tree Algorithm for Intelligent Bridges

(a) Root: B1

Bridge	Port
1	-
2	E
3	A
4	F
5	A
6	D
7	D
8	E
9	B

LAN	Designated Bridge
A	1
B	1
C	7
D	3
E	5
F	6
G	9

(b) Mars → Jupiter : A, B, C, D, E, F, G
Jupiter → Mars : C, D, F
Venus → Jupiter : A, B, D, E, F, G