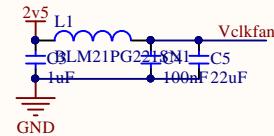
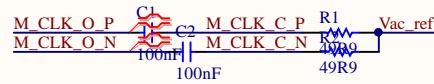
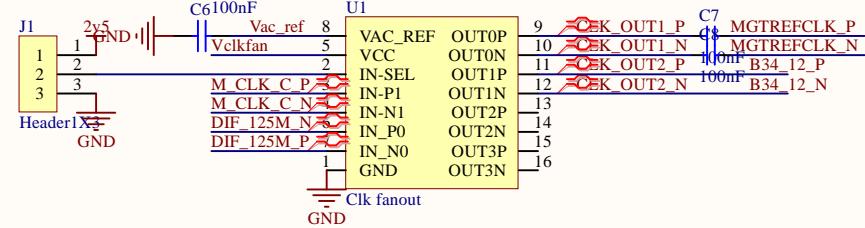
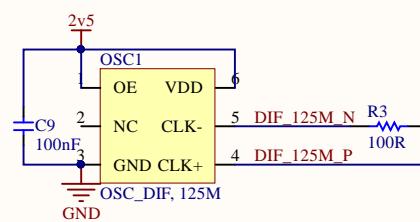


A



B



C

D

Title		
Clock network		
Size	Number	Revision
A4		
Date:	2019/6/4	Sheet of
File:	E:\ADproject..\CLOCK.SchDoc	Drawn By:

A

1 DP1_M1_P	B16_10_P
DPI_M1_N	B16_10_N
2 DP1_M2_P	B16_9_P
DPI_M2_N	B16_9_N
3 DP1_M3_P	B16_18_P
DPI_M3_N	B16_18_N
4 DP1_M4_P	B16_22_N
DPI_M4_N	B16_22_P
5 DP1_M5_P	B16_24_N
DPI_M5_N	B16_24_P
6 DP1_C1_P	B17_5_P
DPI_C1_N	B17_5_N
7 DP1_C2_P	B15_15_P
DPI_C2_N	B15_15_N
8 DP1_C3_P	B15_17_P
DPI_C3_N	B15_17_N
9 DP1_CCLK1_P	B18_15_P
DPI_CCLK1_N	B18_15_N
10 DP1_M9_P	B16_7_N
DPI_M9_N	B16_7_P
11 DP1_M8_P	B16_17_N
DPI_M8_N	B16_17_P
12 DP1_M7_P	B17_16_P
DPI_M7_N	B17_16_N
13 DP1_M6_P	B17_21_P
DPI_M6_N	B17_21_N
14 DP1_GTCLK1_P	B15_9_N
DPI_GTCLK1_N	B15_9_P
15 DP1_C9_P	B15_4_N
DPI_C9_N	B15_4_P
16 DP1_C8_P	B15_21_N
DPI_C8_N	B15_21_P
17 DP1_C7_P	B15_19_N
DPI_C7_N	B15_19_P
18 DP1_C6_P	B15_22_N
DPI_C6_N	B15_22_P

19 DP1_C0_P	B18_17_P
DPI_C0_N	B18_17_N
20 DP1_M0_P	B18_24_P
DPI_M0_N	B18_24_N
21 LA1_06_P	B18_9_P
LA1_06_N	B18_9_N
22 LA1_10_P	B17_22_N
LA1_10_N	B17_22_P
23 LA1_14_P	B16_1_P
LA1_14_N	B16_1_N
24 LA1_18_P	B15_5_P
LA1_18_N	B15_5_N
25 LA1_27_P	B15_24_P
LA1_27_N	B15_24_N
26 LA1_28_P	B15_7_N
LA1_28_N	B15_7_P
27 LA1_30_P	B15_12_N
LA1_30_N	B15_12_P
28 LA1_32_P	B15_23_N
LA1_32_N	B15_23_P
29 DP1_GTCLK0_P	B18_11_P
DPI_GTCLK0_N	B18_11_N
30 LA1_01_P	B18_19_P
LA1_01_N	B18_19_N
31 LA1_05_P	B17_20_P
LA1_05_N	B17_20_N
32 LA1_09_P	B17_19_P
LA1_09_N	B17_19_N
33 LA1_13_P	B17_23_P
LA1_13_N	B17_23_N
34 LA1_17_P	B16_8_P
LA1_17_N	B16_8_N
35 LA1_23_P	B15_6_N
LA1_23_N	B15_6_P
36 LA1_26_P	B15_20_P
LA1_26_N	B15_20_N
37 LA1_29_P	B16_6_N
LA1_29_N	B16_6_P
38 LA1_33_P	B15_14_N
LA1_33_N	B15_14_P

39 HA1_01_P	B18_6_P
HA1_01_N	B18_6_N
40 HA1_05_P	B18_3_P
HA1_05_N	B18_3_N
41 HA1_09_P	B18_5_N
HA1_09_N	B18_5_P
42 HA1_13_P	B18_1_P
HA1_13_N	B18_1_N
43 HA1_16_P	B17_1_P
HA1_16_N	B17_1_N
44 HA1_20_P	B17_6_P
HA1_20_N	B17_6_N
45 HB1_03_P	B17_7_P
HB1_03_N	B17_7_N
46 HB1_05_P	B15_1_P
HB1_05_N	B15_1_N
47 HB1_09_P	B15_10_N
HB1_09_N	B15_10_P
48 HB1_13_P	B15_2_N
HB1_13_N	B15_2_P

1 DP2_M1_P	B13_10_P
DP2_M1_N	B13_10_N
2 DP2_M2_P	B13_18_P
DP2_M2_N	B13_18_N
3 DP2_M3_P	B12_2_P
DP2_M3_N	B12_2_N
4 DP2_M4_P	B13_15_N
DP2_M4_N	B13_15_P
5 DP2_M5_P	B33_1_P
DP2_M5_N	B33_1_N
6 DP2_C1_P	B33_7_N
DP2_C1_N	B33_7_P
7 DP2_C2_P	B13_24_P
DP2_C2_N	B13_24_N
8 DP2_C3_P	B34_7_P
DP2_C3_N	B34_7_N
9 DP2_CCLK1_P	B13_5_P
DP2_CCLK1_N	B13_5_N
10 DP2_M9_P	B13_11_P
DP2_M9_N	B13_11_N
11 DP2_M8_P	B12_13_N
DP2_M8_N	B12_13_P
12 DP2_M7_P	B32_17_N
DP2_M7_N	B32_17_P
13 DP2_M6_P	B32_24_P
DP2_M6_N	B32_24_N
14 DP2_GTCLK1_P	B33_5_P
DP2_GTCLK1_N	B33_5_N
15 DP2_C9_P	B34_20_N
DP2_C9_N	B34_20_P
16 DP2_C8_P	B34_1_P
DP2_C8_N	B34_1_N
17 DP2_C7_P	B34_3_P
DP2_C7_N	B34_3_N
18 DP2_C6_P	B34_6_P
DP2_C6_N	B34_6_N

A

B

DP1_C4_P	SFP2_RX_P
DP1_C4_N	SFP2_RX_N
DP1_C5_P	SFP2_TX_P
DP1_C5_N	SFP2_TX_N

DP2_C4_P	SFP3_RX_P
DP2_C4_N	SFP3_RX_N

DP2_C5_P	SFP3_TX_P
DP2_C5_N	SFP3_TX_N

HB1_06_P
HB1_06_N

HB2_06_P
HB2_06_N

HB1_10_P
HB1_10_N

HB2_10_P
HB2_10_N

C

Title		
LVDS TX		Revision
Size	Number	
A4		
Date:	2019/6/4	Sheet of
File:	E:\ADproject\..\connection1.SchDoc	Drawn By:

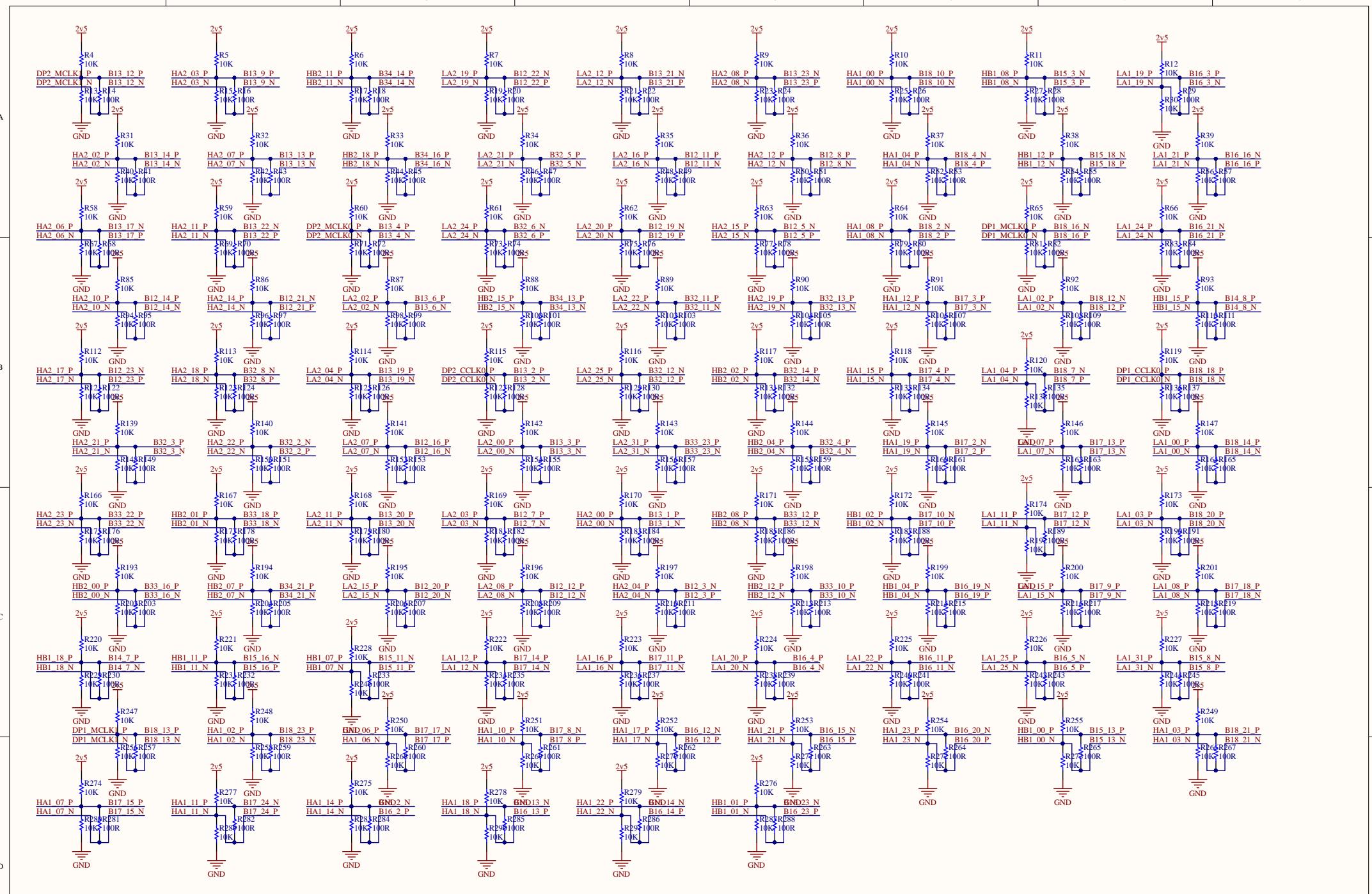
A

D

B

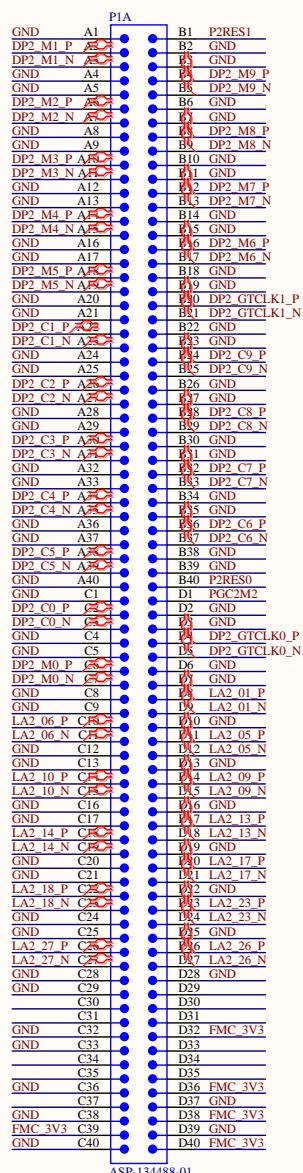
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D

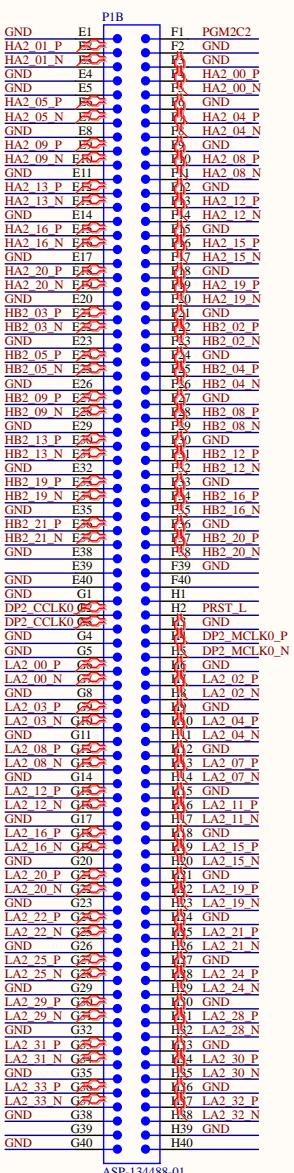


Title		
Size	Number	Revision
A3		
Date:	2019/6/4	Sheet of
File:	E:\ADproject\connection2.SchDoc	Drawn By:

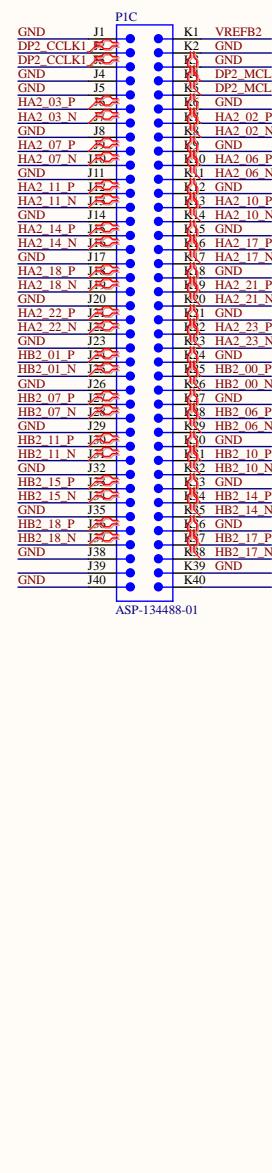
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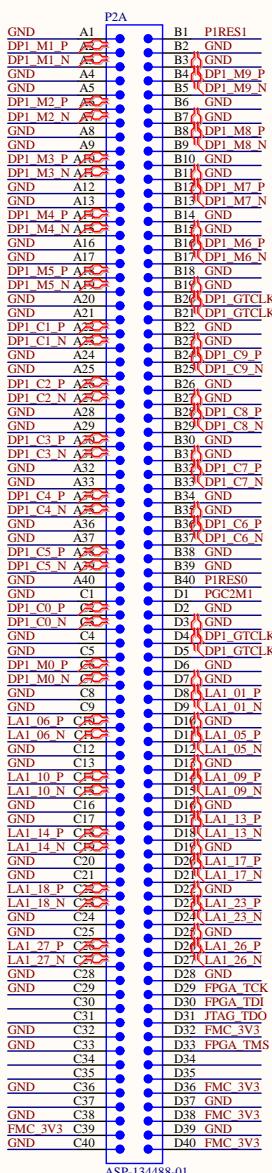
ASP-134488-01



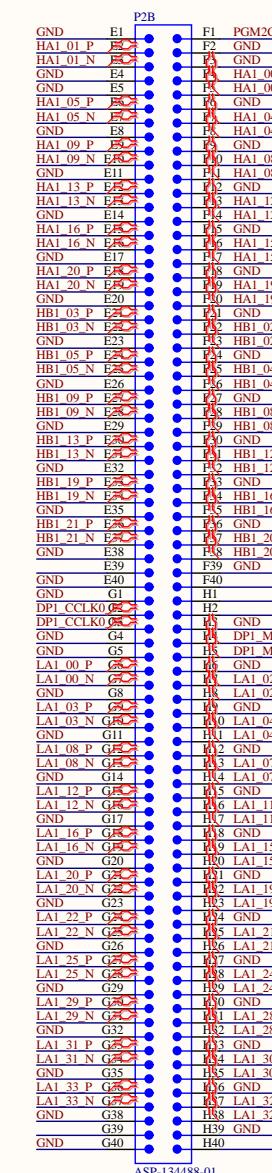
ASP-134488-01



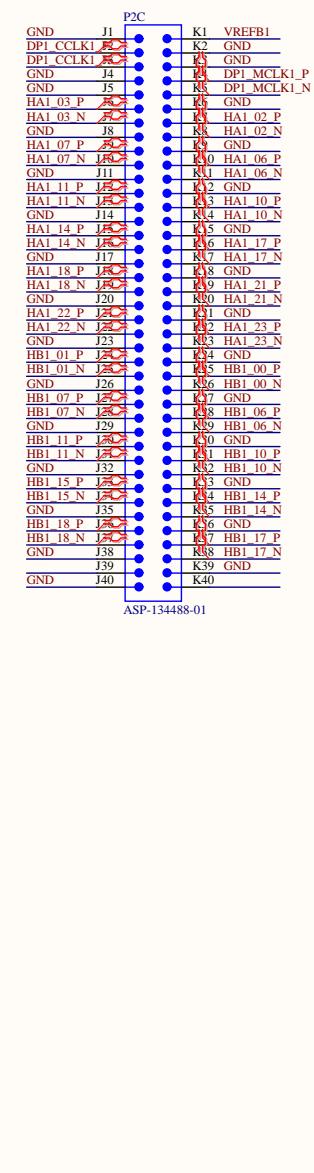
ASP-134488-01



ASP-134488-01



ASP-134488-01



ASP-134488-01

Title		
Size	Number	Revision
A3		
Date:	2019/6/4	Sheet of
File:	E:\ADProject\...\FMCs.SchDoc	Drawn By:

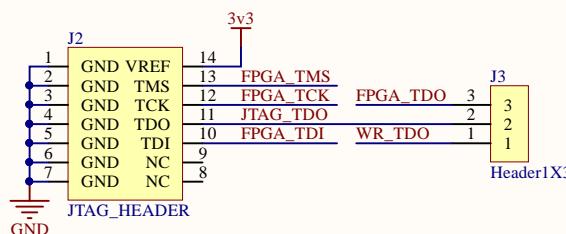
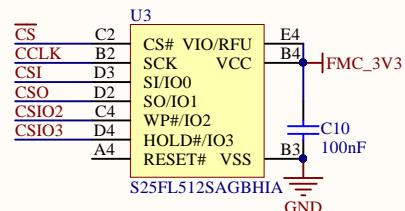
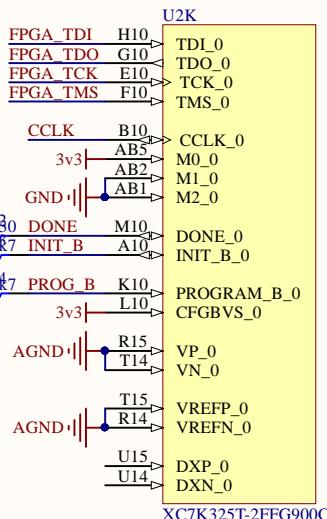
A

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C

D

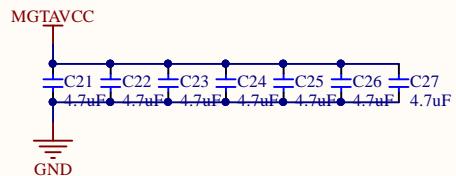
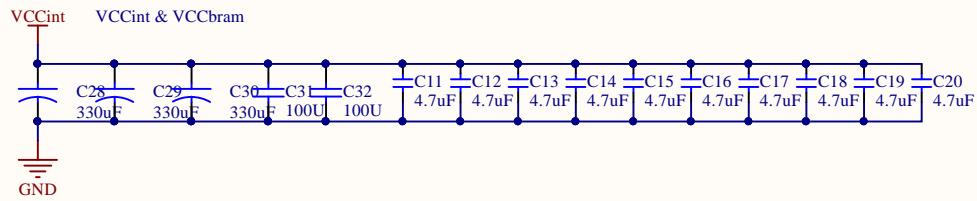
Mode: Master SPIx4



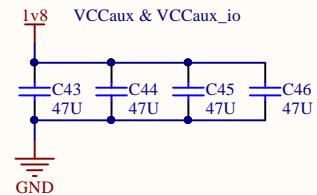
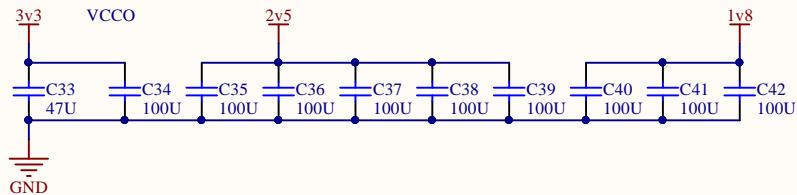
use jumper to select
including mini-WR or
JTAG chain or not

Title		
FPGA configure		
Size	Number	Revision
A4		
Date:	2019/6/4	Sheet of
File:	E:\ADproject\..\FPGA_config.SchDoc	Drawn By:

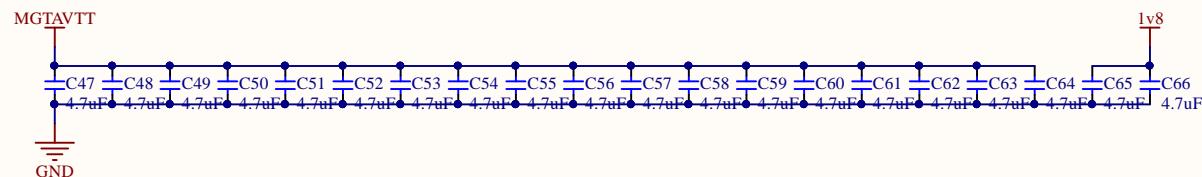
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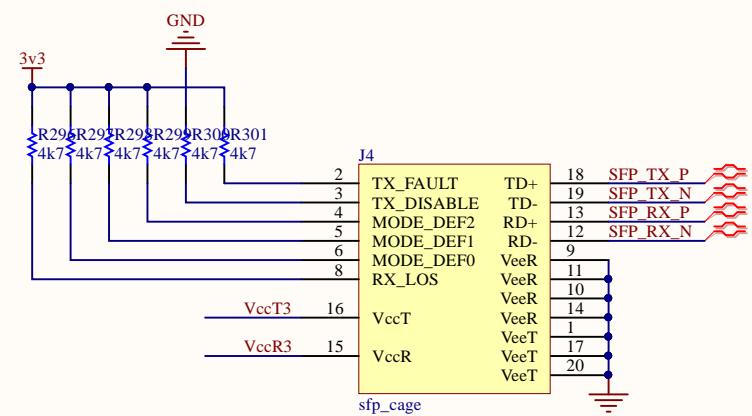
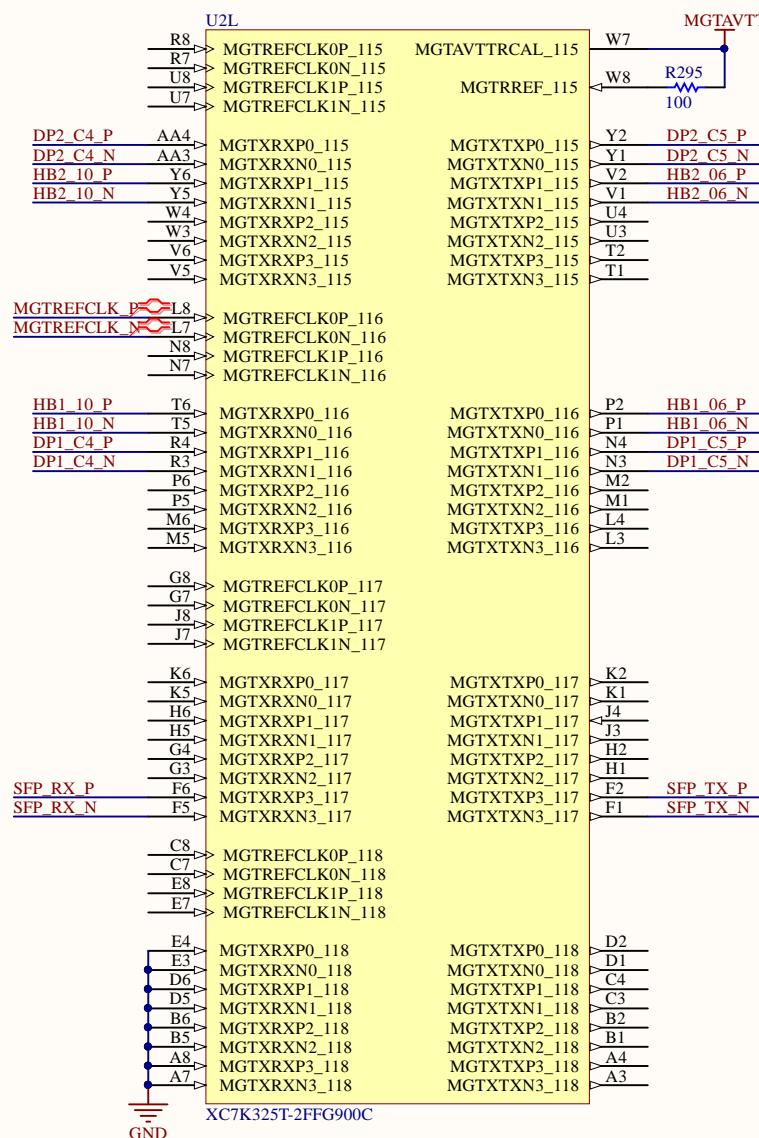
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C



Title Decoupling capacitors		
Size A4	Number	Revision
Date: 2019/6/4	Sheet of	
File: E:\ADproject..\FPGA_de_cap.SchDoc	Drawn By:	



Title		
FPGA GTx + SFP		
Size	Number	Revision
A4		
Date:	2019/6/4	Sheet of
File:	E:\ADproject..\FPGA_MGT.SchDoc	Drawn By:

XC7K325T bank12 to bank18 are HR banks.
I/O voltage range from 1.2V to 3.3V.

U2A

A	BANK 12	
	IO_0_12	Y20
	IO_L1P_T0_12	Y23
	IO_L1N_T0_12	Y24
	IO_L2P_T0_12	B12_1_N
	IO_L2N_T0_12	Y21
	IO_L3P_T0_DQS_12	AA21
	IO_L3N_T0_DQS_12	B12_2_N
	IO_L4P_T0_12	AB22
	IO_L4N_T0_12	B12_3_N
	IO_L5P_T0_12	AB23
	IO_L5N_T0_12	B12_4_N
	IO_L6P_T0_12	AA22
	IO_L6N_T0_VREF_12	AC23
	IO_L7P_T1_12	B12_5_P
	IO_L7N_T1_12	AC20
	IO_L8P_T1_12	AC21
	IO_L8N_T1_12	B12_6_P
	IO_L9P_T1_DQS_12	AB20
	IO_L9N_T1_DQS_12	B12_7_P
	IO_L10P_T1_12	AC25
	IO_L10N_T1_12	AC22
	IO_L11P_T1_SRCC_12	B12_8_P
	IO_L11N_T1_SRCC_12	AD22
	IO_L12P_T1_MRCC_12	B12_9_P
	IO_L12N_T1_MRCC_12	AD24
	IO_L13P_T2_MRCC_12	AC24
	IO_L13N_T2_MRCC_12	AE21
	IO_L14P_T2_SRCC_12	AD23
	IO_L14N_T2_SRCC_12	B12_10_N
	IO_L15P_T2_DQS_12	AE23
	IO_L15N_T2_DQS_12	B12_11_N
	IO_L16P_T2_12	AF23
	IO_L16N_T1_SRCC_12	B12_11_N
	IO_L12P_T1_MRCC_12	AD23
	IO_L12N_T1_MRCC_12	B12_12_P
	IO_L13P_T2_MRCC_12	AE24
	IO_L13N_T2_MRCC_12	AG23
	IO_L14P_T2_SRCC_12	B12_13_N
	IO_L14N_T2_SRCC_12	AD27
	IO_L15P_T2_DQS_13	B12_13_N
	IO_L15N_T2_DQS_13	AD28
	IO_L16P_T2_13	AB27
	IO_L12P_T1_MRCC_13	B12_13_N
	IO_L12N_T1_MRCC_13	AC27
	IO_L13P_T2_MRCC_13	AG29
	IO_L13N_T2_MRCC_13	AH29
	IO_L14P_T2_SRCC_13	AE28
	IO_L14N_T2_SRCC_13	AF28
	IO_L15P_T2_DQS_13	B12_14_N
	IO_L15N_T2_DQS_13	AK29
	IO_L16P_T2_13	AK30
	IO_L12P_T1_MRCC_13	B12_15_N
	IO_L12N_T1_MRCC_13	AE25
	IO_L13P_T2_MRCC_13	AK25
	IO_L13N_T2_MRCC_13	B12_15_N
	IO_L14P_T2_SRCC_13	AE25
	IO_L14N_T2_SRCC_13	AJ25
	IO_L15P_T2_DQS_13	B12_16_P
	IO_L15N_T2_DQS_13	AK25
	IO_L16P_T2_12	AE25
	IO_L16N_T2_12	AK23
	IO_L17P_T2_12	B12_17_P
	IO_L17N_T2_12	AK24
	IO_L18P_T2_12	B12_18_P
	IO_L18N_T2_12	AG25
	IO_L19P_T3_12	AH25
	IO_L19N_T3_VREF_12	AF20
	IO_L19N_T3_VREF_12	B12_19_P
	IO_L20P_T3_12	AF21
	IO_L20N_T3_12	B12_19_N
	IO_L21P_T3_DQS_12	AG22
	IO_L21N_T3_DQS_12	AK22
	IO_L22P_T3_12	B12_20_P
	IO_L22N_T3_12	AH22
	IO_L23P_T3_12	AK21
	IO_L23N_T3_12	B12_21_P
	IO_L24P_T3_12	AG20
	IO_L24N_T3_12	AK20
	IO_L25_12	AE20

XC7K325T-2FFG900C

U2B

B	BANK 13	
	IO_0_13	Y25
	IO_L1P_T0_13	Y26
	IO_L1N_T0_13	B13_1_P
	IO_L2P_T0_13	AA26
	IO_L2N_T0_13	B13_2_P
	IO_L3P_T0_DQS_13	W27
	IO_L3N_T0_DQS_13	W28
	IO_L4P_T0_13	B13_3_P
	IO_L5P_T0_13	Y28
	IO_L5N_T0_13	AA28
	IO_L6P_T0_13	B13_3_N
	IO_L6N_T0_VREF_13	W29
	IO_L7P_T1_13	Y29
	IO_L7N_T1_13	B13_4_N
	IO_L8P_T1_13	AA27
	IO_L8N_T1_13	IO_L4P_T0_D04_14
	IO_L9P_T1_DQS_13	AB28
	IO_L9N_T1_DQS_13	B13_5_N
	IO_L10P_T1_13	IO_L5N_T0_D07_14
	IO_L11P_T1_SRCC_13	AA25
	IO_L11N_T1_SRCC_13	B13_6_P
	IO_L12P_T1_MRCC_12	AB25
	IO_L12N_T1_MRCC_12	B13_6_N
	IO_L13P_T2_MRCC_12	AC29
	IO_L13N_T2_MRCC_12	AD21
	IO_L14P_T2_SRCC_12	AD24
	IO_L14N_T2_SRCC_12	B12_9_N
	IO_L15P_T2_DQS_12	AD24
	IO_L15N_T2_DQS_12	B12_10_P
	IO_L16P_T2_12	AE21
	IO_L17P_T2_12	AE23
	IO_L18P_T2_12	AF23
	IO_L19P_T3_12	AG23
	IO_L19N_T3_VREF_12	AG24
	IO_L20P_T3_12	AH24
	IO_L20N_T3_12	AK24
	IO_L21P_T3_DQS_12	AJ24
	IO_L21N_T3_DQS_12	B12_15_P
	IO_L22P_T3_12	AK25
	IO_L22N_T3_12	B12_16_P
	IO_L23P_T3_12	AE25
	IO_L23N_T3_12	AK25
	IO_L24P_T3_12	AE25
	IO_L24N_T3_12	AK25
	IO_25_13	IO_25_13

XC7K325T-2FFG900C

U2C

C	BANK 14	
	IO_0_14	R19
	IO_L1P_T0_D00_MOSI_14	B14_0
	IO_L1N_T0_D01_DIN_14	R24
	IO_L2P_T0_D02_14	CS1
	IO_L2N_T0_D03_14	R20
	IO_L3P_T0_DQS_PUDC_B_14	CS1
	IO_L3N_T0_DQS_EMCCCLK_14	R21
	IO_L4P_T0_D04_14	GND
	IO_L5P_T1_D05_14	R22
	IO_L5P_T0_D06_14	B14_4_P
	IO_L5N_T0_D07_14	U19
	IO_L6P_T0_FCS_B_14	CS
	IO_L6N_T0_D08_VREF_14	U20
	IO_L7P_T1_D09_14	B14_6_N
	IO_L7N_T1_D10_14	P29
	IO_L8P_T1_D11_14	B14_7_P
	IO_L8N_T1_D12_14	T20
	IO_L9P_T1_DQS_14	B14_8_P
	IO_L9N_T1_DQS_D13_14	T30
	IO_L10P_T1_D14_14	B14_9_P
	IO_L10N_T1_D15_14	P26
	IO_L11P_T1_SRCC_14	B14_10_P
	IO_L11N_T1_SRCC_14	U26
	IO_L12P_T1_MRCC_14	B14_11_P
	IO_L12N_T1_MRCC_14	U27
	IO_L13P_T2_MRCC_14	B14_12_N
	IO_L13N_T2_MRCC_14	U28
	IO_L14P_T2_SRCC_14	B14_13_N
	IO_L14N_T2_SRCC_14	U25
	IO_L15P_T2_DQS_RDWR_B_14	B14_14_N
	IO_L15N_T2_DQS_DOUT_CSO_B_14	U29
	IO_L16P_T2_CSI_B_14	B14_15_N
	IO_L16N_T2_A15_D31_14	V26
	IO_L17P_T2_A14_D30_14	B14_16_N
	IO_L17P_T2_A13_D29_14	V27
	IO_L18P_T2_A12_D28_14	B14_17_P
	IO_L18N_T2_A11_D27_14	V28
	IO_L19P_T3_A10_D26_14	B14_18_N
	IO_L19N_T3_A09_D25_VREF_14	V29
	IO_L20P_T3_A08_D24_14	B14_19_N
	IO_L20N_T3_A07_D23_14	W23
	IO_L21P_T3_DQS_14	B14_20_P
	IO_L21N_T3_DQS_A06_D22_14	W24
	IO_L22P_T3_A05_D21_14	V22
	IO_L22N_T3_A04_D20_14	B14_21_P
	IO_L23P_T3_A03_D19_14	U23
	IO_L23N_T3_A02_D18_14	B14_22_P
	IO_L24P_T3_A01_D17_14	V24
	IO_L24N_T3_A00_D16_14	W21
	IO_25_14	B14_23_P

XC7K325T-2FFG900C

U2D

D	BANK 15	
	IO_0_15	M19
	IO_L1P_T0_AD0P_15	B15_1_P
	IO_L1N_T0_AD0N_15	U24
	IO_L2P_T0_AD8P_15	B15_2_P
	IO_L2N_T0_AD8N_15	U23
	IO_L3P_T0_DQS_AD1P_15	K23
	IO_L3N_T0_DQS_AD1N_15	K24
	IO_L4P_T0_AD9P_15	B15_3_N
	IO_L4N_T0_AD9N_15	K21
	IO_L5P_T0_AD2P_15	B15_4_N
	IO_L5N_T0_AD2N_15	K22
	IO_L6P_T0_15	B15_5_N
	IO_L6N_T0_VREF_15	K20
	IO_L7P_T1_AD10P_15	B15_6_N
	IO_L7N_T1_AD10N_15	H29
	IO_L8P_T1_AD3P_15	B15_7_N
	IO_L8N_T1_AD4N_15	K27
	IO_L11P_T1_SRCC_AD12P_15	B15_8_N
	IO_L11N_T1_SRCC_AD12N_15	K30
	IO_L12P_T1_MRCC_AD5P_15	K25
	IO_L12N_T1_MRCC_AD5N_15	K28
	IO_L13P_T2_MRCC_15	K29
	IO_L13N_T2_MRCC_15	K31
	IO_L14P_T2_SRCC_15	M28
	IO_L14N_T2_SRCC_15	K28
	IO_L15P_T2_DQS_15	M29
	IO_L15N_T2_DQS_ADV_B_15	M30
	IO_L16P_T2_A28_15	N27
	IO_L16N_T2_A27_15	B15_16_N
	IO_L17P_T2_A26_15	N29
	IO_L17N_T2_A25_15	B15_17_P
	IO_L18P_T2_A24_15	N30
	IO_L18N_T2_A23_15	N25
	IO_L19P_T3_A22_15	N26
	IO_L19N_T3_A21_VREF_15	N19
	IO_L20P_T3_A20_15	N20
	IO_L20N_T3_A19_15	N21
	IO_L21P_T3_DQS_15	N22
	IO_L21N_T3_DQS_A18_15	N23
	IO_L22P_T3_A17_15	P21
	IO_L22N_T3_A16_15	P22
	IO_L23P_T3_FOE_B_15	M24
	IO_L23N_T3_FWE_B_15	M25
	IO_L24P_T3_RS1_15	M22
	IO_L24N_T3_RS0_15	M23
	IO_25_15	P19

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Title

FPGA bank 12 - 15

Size	Number	Revision
A4		
Date:	2019/6/4	Sheet of
File:	E:\ADproject\..\FPGA_part1.SchDoc	Drawn By:

XC7K325T bank12 to bank18 are HR banks.
I/O voltage range from 1.2V to 3.3V.

U2E
BANK 16

IO_0_16
IO_L1P_T0_16
IO_L1N_T0_16
IO_L2P_T0_16
IO_L2N_T0_16
IO_L3P_T0_DQS_16
IO_L3N_T0_DQS_16
IO_L4P_T0_16
IO_L4N_T0_16
IO_L5P_T0_16
IO_L5N_T0_16
IO_L6P_T0_16
IO_L6N_T0_VREF_16
IO_L7P_T1_16
IO_L7N_T1_16
IO_L8P_T1_16
IO_L8N_T1_16
IO_L9P_T1_DQS_16
IO_L9N_T1_DQS_16
IO_L10P_T1_16
IO_L10N_T1_16
IO_L11P_T1_SRCC_16
IO_L11N_T1_SRCC_16
IO_L12P_T1_MRCC_16
IO_L12N_T1_MRCC_16
IO_L13P_T2_MRCC_16
IO_L13N_T2_MRCC_16
IO_L14P_T2_SRCC_16
IO_L14N_T2_SRCC_16
IO_L15P_T2_DQS_16
IO_L15N_T2_DQS_16
IO_L16P_T2_16
IO_L16N_T2_16
IO_L17P_T2_16
IO_L17N_T2_16
IO_L18P_T2_16
IO_L18N_T2_16
IO_L19P_T3_16
IO_L19N_T3_VREF_16
IO_L20P_T3_16
IO_L20N_T3_16
IO_L21P_T3_DQS_16
IO_L21N_T3_DQS_16
IO_L22P_T3_16
IO_L22N_T3_16
IO_L23P_T3_16
IO_L23N_T3_16
IO_L24P_T3_16
IO_L24N_T3_16
IO_25_16

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U2F
BANK 17

IO_0_17
IO_L1P_T0_17
IO_L1N_T0_17
IO_L2P_T0_17
IO_L2N_T0_17
IO_L3N_T0_DQS_17
IO_L4P_T0_17
IO_L4N_T0_17
IO_L5P_T0_17
IO_L5N_T0_17
IO_L6P_T0_17
IO_L6N_T0_VREF_17
IO_L7P_T1_17
IO_L7N_T1_17
IO_L8P_T1_17
IO_L8N_T1_17
IO_L9P_T1_DQS_17
IO_L9N_T1_DQS_17
IO_L10P_T1_17
IO_L10N_T1_17
IO_L11P_T1_SRCC_17
IO_L11N_T1_SRCC_17
IO_L12P_T1_MRCC_17
IO_L12N_T1_MRCC_17
IO_L13P_T2_MRCC_17
IO_L13N_T2_MRCC_17
IO_L14P_T2_SRCC_17
IO_L14N_T2_SRCC_17
IO_L15P_T2_DQS_17
IO_L15N_T2_DQS_17
IO_L16P_T2_17
IO_L16N_T2_17
IO_L17P_T2_17
IO_L17N_T2_17
IO_L18P_T2_17
IO_L18N_T2_17
IO_L19P_T3_17
IO_L19N_T3_VREF_17
IO_L20P_T3_17
IO_L20N_T3_17
IO_L21P_T3_DQS_17
IO_L21N_T3_DQS_17
IO_L22P_T3_17
IO_L22N_T3_17
IO_L23P_T3_17
IO_L23N_T3_17
IO_L24P_T3_17
IO_L24N_T3_17
IO_25_17

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U2G
BANK 18

IO_0_18
IO_L1P_T0_18
IO_L1N_T0_18
IO_L2P_T0_18
IO_L2N_T0_18
IO_L3N_T0_DQS_18
IO_L4P_T0_18
IO_L4N_T0_18
IO_L5P_T0_18
IO_L5N_T0_18
IO_L6P_T0_18
IO_L6N_T0_VREF_18
IO_L7P_T1_18
IO_L7N_T1_18
IO_L8P_T1_18
IO_L8N_T1_18
IO_L9P_T1_DQS_18
IO_L9N_T1_DQS_18
IO_L10P_T1_18
IO_L10N_T1_18
IO_L11P_T1_SRCC_18
IO_L11N_T1_SRCC_18
IO_L12P_T1_MRCC_18
IO_L12N_T1_MRCC_18
IO_L13P_T2_MRCC_18
IO_L13N_T2_MRCC_18
IO_L14P_T2_SRCC_18
IO_L14N_T2_SRCC_18
IO_L15P_T2_DQS_18
IO_L15N_T2_DQS_18
IO_L16P_T2_18
IO_L16N_T2_18
IO_L17P_T2_18
IO_L17N_T2_18
IO_L18P_T2_18
IO_L18N_T2_18
IO_L19P_T3_18
IO_L19N_T3_VREF_18
IO_L20P_T3_18
IO_L20N_T3_18
IO_L21P_T3_DQS_18
IO_L21N_T3_DQS_18
IO_L22P_T3_18
IO_L22N_T3_18
IO_L23P_T3_18
IO_L23N_T3_18
IO_L24P_T3_18
IO_L24N_T3_18
IO_25_18

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Title

FPGA bank 16 - 18

Size	Number	Revision
A4		
Date:	2019/6/4	Sheet of
File:	E:\ADproject..\FPGA_part2.SchDoc	Drawn By:

XC7K325T bank32 to bank34 are HP banks.
I/O voltage range from 1.2V to 1.8V.

A

U2H	
BANK 32	
IO_0_VRN_32	Y14
IO_L1P_T0_32	AK16 B32_1_P TP0
IO_L1N_T0_32	AK15 B32_1_N TP1
IO_L2P_T0_32	AG15 B32_2_P
IO_L2N_T0_32	AH15 B32_2_N
IO_L3P_T0_DQS_32	AH16 B32_3_P
IO_L3N_T0_DQS_32	AJ16 B32_3_N
IO_L4P_T0_32	AF15 B32_4_P
IO_L4N_T0_32	AG14 B32_4_N
IO_L5P_T0_32	AH17 B32_5_P
IO_L5N_T0_32	AJ17 B32_5_N
IO_L6P_T0_32	AE16 B32_6_P
IO_L6N_T0_VREF_32	AF16 B32_6_N
IO_L7P_T1_32	AJ19 B32_7_P
IO_L7N_T1_32	AK19 B32_7_N
IO_L8P_T1_32	AG19 B32_8_P
IO_L8N_T1_32	AH19 B32_8_N
IO_L9P_T1_DQS_32	AJ18 B32_9_P
IO_L9N_T1_DQS_32	AK18 B32_9_N
IO_L10P_T1_32	AD19 B32_10_P
IO_L10N_T1_32	AE19 B32_10_N
IO_L11P_T1_SRCC_32	AF18 B32_11_P
IO_L11N_T1_SRCC_32	AG18 B32_11_N
IO_L12P_T1_MRCC_32	AF17 B32_12_P
IO_L12N_T1_MRCC_32	AG17 B32_12_N
IO_L13P_T2_MRCC_32	AD18 B32_13_P
IO_L13N_T2_MRCC_32	AE18 B32_13_N
IO_L14P_T2_SRCC_32	AD17 B32_14_P
IO_L14N_T2_SRCC_32	AD16 B32_14_N
IO_L15P_T2_DQS_32	Y19 B32_15_P
IO_L15N_T2_DQS_32	Y18 B32_15_N
IO_L16P_T2_32	AA18 B32_16_P
IO_L16N_T2_32	AB18 B32_16_N
IO_L17P_T2_32	AB19 B32_17_P
IO_L17N_T2_32	AC19 B32_17_N
IO_L18P_T2_32	AB17 B32_18_P
IO_L18N_T2_32	AC17 B32_18_N
IO_L19P_T3_32	AE15 B32_19_P
IO_L19N_T3_VREF_32	AE14 B32_19_N
IO_L20P_T3_32	AA15 B32_20_P
IO_L20N_T3_32	AB15 B32_20_N
IO_L21P_T3_DQS_32	AC16 B32_21_P
IO_L21N_T3_DQS_32	AC15 B32_21_N
IO_L22P_T3_32	AC14 B32_22_P
IO_L22N_T3_32	AD14 B32_22_N
IO_L23P_T3_32	AA17 B32_23_P
IO_L23N_T3_32	AA16 B32_23_N
IO_L24P_T3_32	Y16 B32_24_P
IO_L24N_T3_32	Y15 B32_24_N
IO_25_VRP_32	AB14

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B

U2I	
BANK 33	
IO_0_VRN_33	Y13
IO_L1P_T0_33	AA12 B33_1_P
IO_L1N_T0_33	AB12 B33_1_N
IO_L2P_T0_33	AA8 B33_2_P
IO_L2N_T0_33	AB8 B33_2_N
IO_L3P_T0_DQS_33	AB9 B33_3_P
IO_L3N_T0_DQS_33	AC9 B33_3_N
IO_L4P_T0_33	Y11 B33_4_P
IO_L4N_T0_33	Y10 B33_4_N
IO_L5P_T0_33	AA11 B33_5_P
IO_L5N_T0_33	AA10 B33_5_N
IO_L6P_T0_33	AA13 B33_6_P
IO_L6N_T0_VREF_33	AB13 B33_6_N
IO_L7P_T1_33	AB10 B33_7_P
IO_L7N_T1_33	AC10 B33_7_N
IO_L8P_T1_33	AD8 B33_8_P
IO_L8N_T1_33	AE8 B33_8_N
IO_L9P_T1_DQS_33	AC12 B33_9_P
IO_L9N_T1_DQS_33	AD9 B33_10_P
IO_L10P_T1_33	AE9 B33_10_N
IO_L10N_T1_33	AE11 B33_11_P
IO_L11P_T1_SRCC_33	AF11 B33_11_N
IO_L11N_T1_SRCC_33	AD12 B33_12_P
IO_L12P_T1_MRCC_33	AD11 B33_12_N
IO_L12N_T1_MRCC_33	AG10 B33_13_P
IO_L13P_T2_MRCC_33	AH10 B33_13_N
IO_L13N_T2_MRCC_33	AE10 B33_14_P
IO_L14P_T2_SRCC_33	AF10 B33_14_N
IO_L14N_T2_SRCC_33	AJ9 B33_15_P
IO_L15P_T2_DQS_33	AK9 B33_15_N
IO_L15N_T2_DQS_33	AG9 B33_16_P
IO_L16P_T2_33	AH9 B33_16_N
IO_L16N_T2_33	AK11 B33_17_P
IO_L17P_T2_33	AK10 B33_17_N
IO_L17N_T2_33	AH11 B33_18_P
IO_L18P_T2_33	AJ11 B33_18_N
IO_L18N_T2_33	AE13 B33_19_P
IO_L19P_T3_33	AF13 B33_19_N
IO_L19N_T3_VREF_33	AK14 B33_20_P TP2
IO_L20P_T3_33	AK13 B33_20_N TP3
IO_L20N_T3_33	AK14 B33_21_P
IO_L21P_T3_DQS_33	AJ14 B33_21_N
IO_L21N_T3_DQS_33	AJ13 B33_22_P
IO_L22P_T3_33	AJ12 B33_22_N
IO_L22N_T3_33	AF12 B33_23_P
IO_L23P_T3_33	AG12 B33_23_N
IO_L23N_T3_33	AG13 B33_24_P
IO_L24P_T3_33	AH12 B33_24_N
IO_L24N_T3_33	AD13
IO_25_VRP_33	

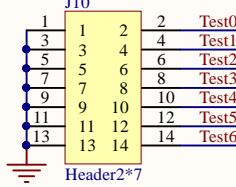
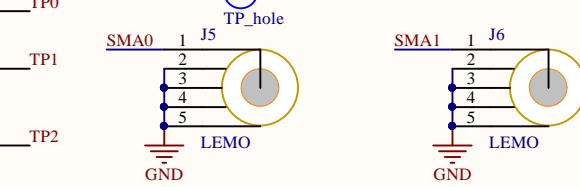
XC7K325T-2FFG900C

C

U2J	
BANK 34	
IO_0_VRN_34	AC6
IO_L1P_T0_34	AD4 B34_1_P
IO_L1N_T0_34	AD3 B34_1_N
IO_L2P_T0_34	AC2 B34_2_P
IO_L2N_T0_34	AC1 B34_2_N
IO_L3P_T0_DQS_34	AD2 B34_3_P
IO_L3N_T0_DQS_34	AD1 B34_3_N
IO_L4P_T0_34	AC5 B34_4_P
IO_L4N_T0_34	AD6 B34_4_N
IO_L5P_T0_34	AE6 B34_5_N
IO_L5N_T0_34	AC7 B34_6_P
IO_L6P_T0_34	AD7 B34_6_N
IO_L6N_T0_VREF_34	AF3 B34_7_P
IO_L7P_T1_34	AF2 B34_7_N
IO_L7N_T1_34	AE1 B34_8_P Test1
IO_L8P_T1_34	AF1 B34_8_N Test0
IO_L8N_T1_34	AG4 B34_9_P
IO_L9P_T1_DQS_34	AG3 B34_9_N
IO_L9N_T1_DQS_34	AE4 B34_10_P
IO_L10P_T1_34	AE3 B34_10_N
IO_L10N_T1_34	AE5 B34_11_P
IO_L11P_T1_SRCC_34	AF5 B34_11_N
IO_L11N_T1_SRCC_34	AF6 B34_12_P
IO_L12P_T1_MRCC_34	AG5 B34_12_N
IO_L12N_T1_MRCC_34	AH4 B34_13_P
IO_L13P_T2_MRCC_34	AJ4 B34_13_N
IO_L13N_T2_MRCC_34	AH6 B34_14_P
IO_L14P_T2_SRCC_34	AH5 B34_14_N
IO_L14N_T2_SRCC_34	AG2 B34_15_P
IO_L15P_T2_DQS_34	AG1 B34_15_N Test3
IO_L15N_T2_DQS_34	AH2 B34_16_P
IO_L16P_T2_34	AJ2 B34_16_N
IO_L16N_T2_34	AJ1 B34_17_P Test6
IO_L17P_T2_34	AK1 B34_17_N Test5
IO_L17N_T2_34	AJ3 B34_18_P
IO_L18P_T2_34	AK3 B34_18_N Test2
IO_L18N_T2_34	AF8 B34_19_P
IO_L19P_T3_34	AG8 B34_19_N
IO_L19N_T3_VREF_34	AF7 B34_20_P
IO_L20P_T3_34	AG7 B34_20_N
IO_L20N_T3_34	AH7 B34_21_P
IO_L21P_T3_DQS_34	AJ7 B34_21_N
IO_L21N_T3_DQS_34	AJ6 B34_22_P
IO_L22P_T3_34	AK6 B34_22_N SMA0
IO_L22N_T3_34	AJ8 B34_23_P
IO_L23P_T3_34	AK8 B34_23_N
IO_L23N_T3_34	AK5 B34_24_P SMA1
IO_L24P_T3_34	AK4 B34_24_N Test4
IO_L24N_T3_34	AB7
IO_25_VRP_34	

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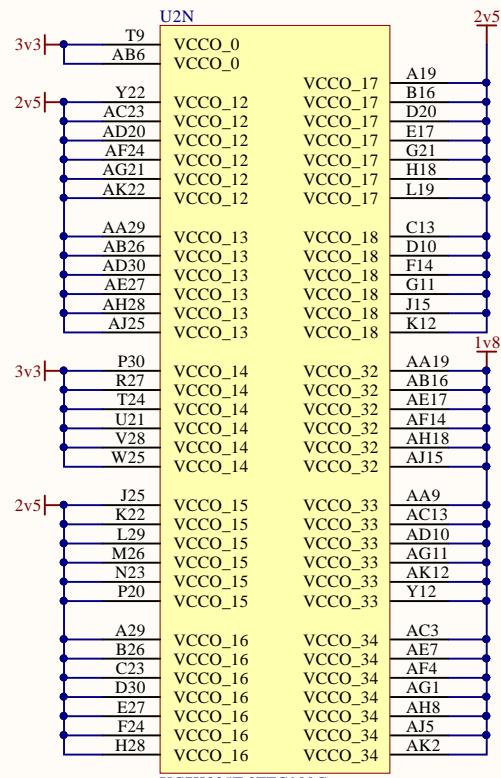
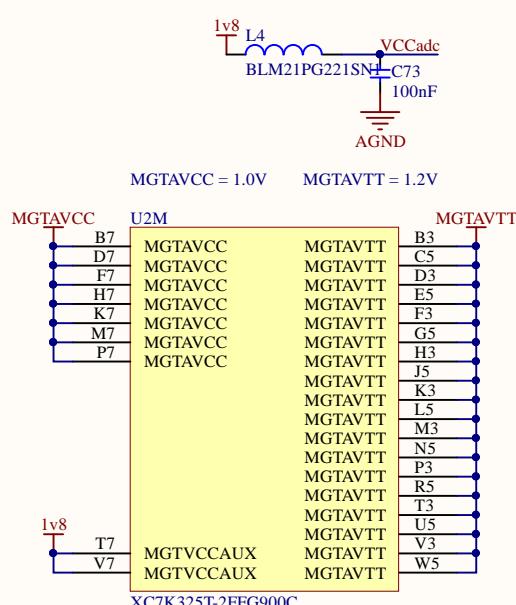
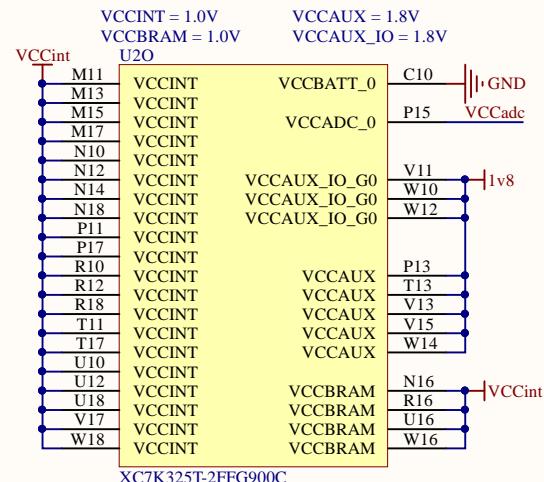
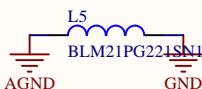
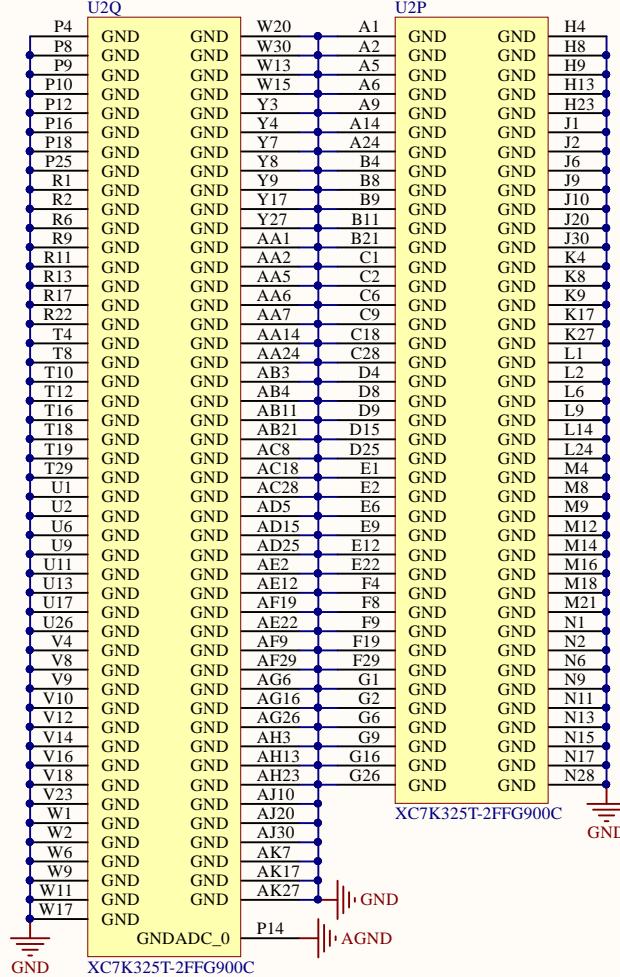
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Size	Number	Revision
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File:	E:\ADproject\..\FPGA_part3.SchDoc	Drawn By:

A

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D



Title		FPGA VCCO settings	
Size A4	Number	Revision	
Date:	2019/6/4	Sheet	of
File:	E:\ADproject..\FPGA_power.SchDoc	Drawn By:	

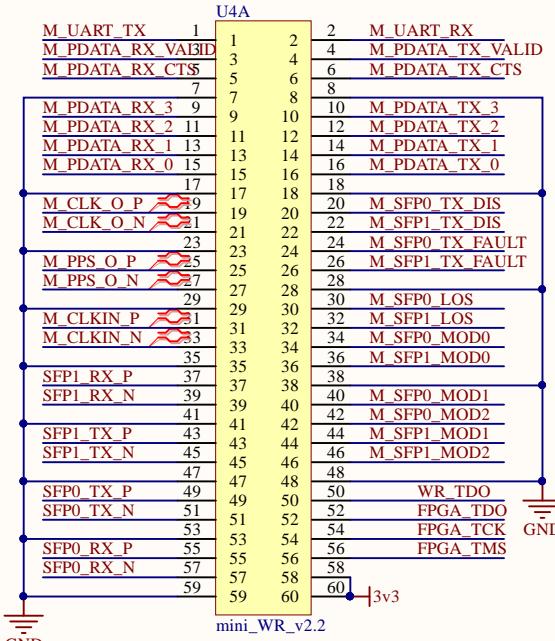
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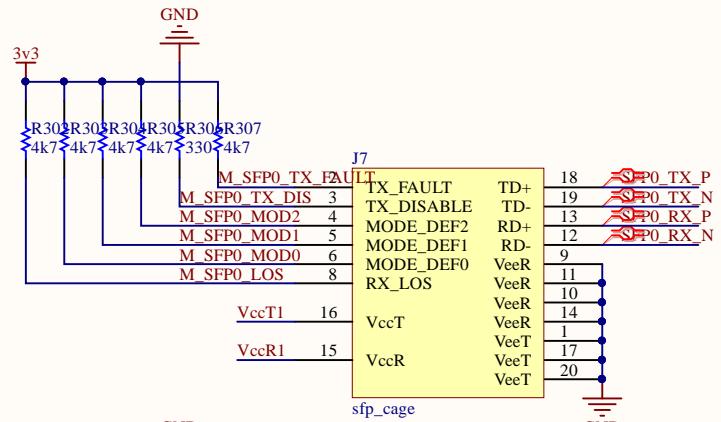
A

B34_2_P
B34_2_N

M_PDATA_TX_VALID B14_21_P
M_PDATA_TX_CTS B14_4_P

M_PDATA_TX_3 B14_19_P
M_PDATA_TX_2 B14_22_P
M_PDATA_TX_1 B14_19_N
M_PDATA_TX_0 B14_16_P

R_PDATA_TX_7 B14_14_P
R_PDATA_TX_6 B14_5_N
R_PDATA_TX_5 B14_3_N
R_PDATA_TX_4 B14_0

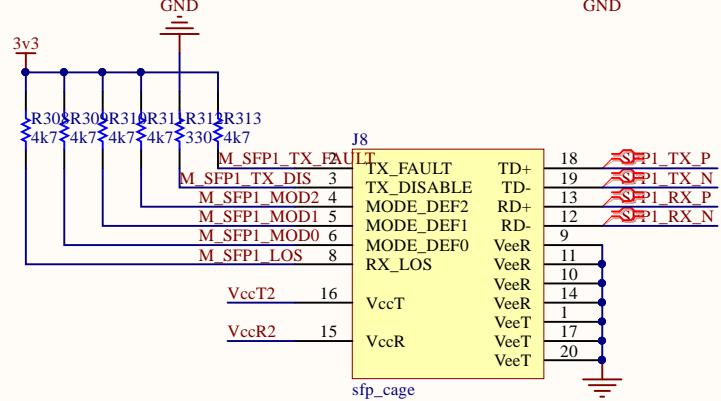


B

M_PDATA_RX_VALID B14_22_N
M_PDATA_RX_CTS B14_24_N

M_PDATA_RX_3 B14_20_P
M_PDATA_RX_2 B14_20_N
M_PDATA_RX_1 B14_24_P
M_PDATA_RX_0 B14_18_N

R_PDATA_RX_7 B14_21_N
R_PDATA_RX_6 B14_4_N
R_PDATA_RX_5 B14_23_P
R_PDATA_RX_4 B14_5_P



C

R_NSS 61 62 R_MOSI
WR_LOCKED 63 64 R_MISO
WR_RESET 65 66 R_SCLK

R_PDATA_RX_7 69 70 R_PDATA_RX_7
R_PDATA_RX_6 71 72 R_PDATA_RX_6
R_PDATA_RX_5 73 74 R_PDATA_RX_5
R_PDATA_RX_4 75 76 R_PDATA_RX_4

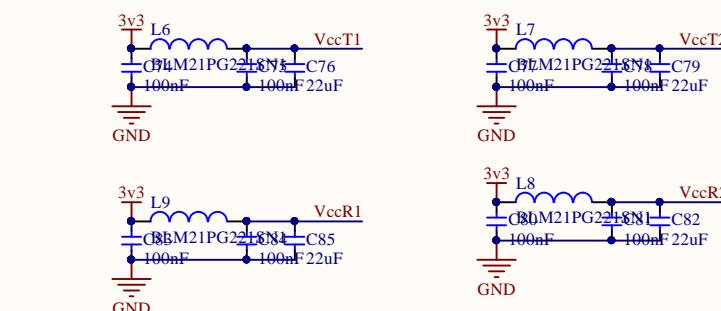
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R_RSV0_N 81 82 R_RSV1
R_RSV1_P 85 84 R_RSV2
R_RSV1_N 87 86 R_RSV3

R_CLK_O_P 91 90 R_CLK_I
R_CLK_O_N 93 92 R_TOD_I
R_TOD_I_P 97 98 R_TOD_O

R_TOD_I_N 99 100 R_PPS_O
R_PPS_O_P 101 102 R_TOD_O
R_PPS_O_N 103 104 R_CLK125_O_P
R_PPS_O_N 105 106 R_CLK125_O_N

R_TOD_O_P 107 108 R_CLK_I_P
R_TOD_O_N 111 112 R_CLK_I_N

R_PPS_I_P 113 114 R_REFCLK_P
R_PPS_I_N 117 118 R_REFCLK_N



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mini_WR_v2.2

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