



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	5/18	J.W.
B	INC. ECN NO. 8680		

LTR	MIN	MAX
A IN. MM	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.009 0.229	0.013 0.33
D IN. MM	—→	
e IN. MM	.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN. MM	0.398 10.11	0.416 10.57
L IN. MM	0.016 0.40	0.040 1.02
$\Theta$	0°	8°

16 PIN MIN	16 PIN MAX	18 PIN MIN	18 PIN MAX	20 PIN MIN	20 PIN MAX	24 PIN MIN	24 PIN MAX	28 PIN MIN	28 PIN MAX
0.398 10.11	0.412 10.46	0.448 11.38	0.462 11.73	0.498 12.65	0.511 12.99	0.598 15.19	0.612 15.54	0.698 17.73	0.712 18.08

THE CHAMFER ON THE BODY IS OPTIONAL.  
IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER  
MUST BE POSITIONED SO THAT 1/2 OR MORE OF  
IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

SIGNATURE		DATE	 <b>DALLAS SEMICONDUCTOR</b> 	
DOC. CONTROL: J.WILKINS		5/94		
ENGR. MGR: B.W.MCARTY		5/94	TITLE PACKAGE OUTLINE .300" SOIC 16,18,20,24&28 LD.	
MFG. ENGR: C.M.SELLS		5/94		
CHECKED BY: C.M.SELLS		5/94		
DRAWN BY: M.W.C.		5/94		
SIZE A	FSCM NO	PART NO. 56-G4009-001		REV B
DO NOT SCALE DWG.		SCALE N/A		SHEET 1 OF 1