EE 599 Spring 2020

Homework2

Jianqi Zhang<jianqiz@usc.edu>, 1052509893

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Github URL: https://github.com/JianqiZhang/EE599_Jianqi-Zhang_1052509893

1 Barrel Shifter [50 Points]

A Barrel Shifter is a logic circuit for shifting a word by a varying amount. It has a control input (select bits) that specifies the number of bit positions that it shifts. A Barrel Shifter is implemented with a sequence of shift multiplexers, each shifting a word by 2k bit positions for different values of k. The diagram below (Figure 1) shows a pipeline clock-wise barrel shifter for 8 inputs.

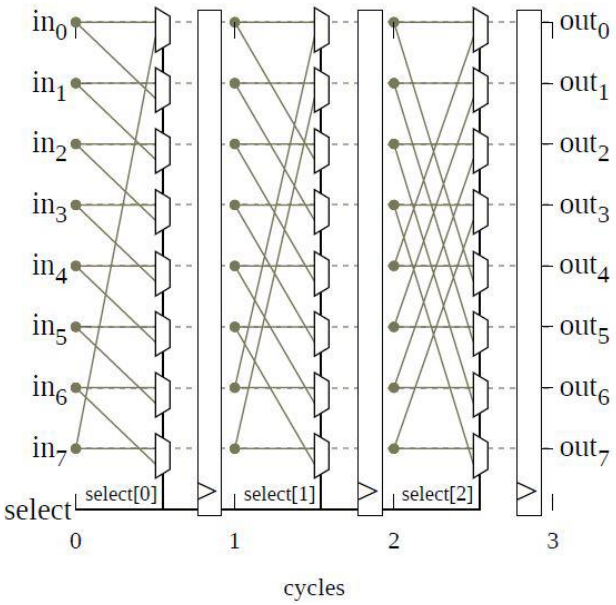


Figure 1: An Example Pipeline Barrel Shifter

Notice that we can shift the input elements by 0 - 7 elements using an implementation like Figure 1. Table 1 shows all the shifting possibilities for the above example. Similarly, a scalable Barrel Shifter with N inputs and maximum shift of N-1 can be implemented.

Table 1: All the shifting possibilities for the given example

Select[2]	Select[1]	Select[0]	Shift
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

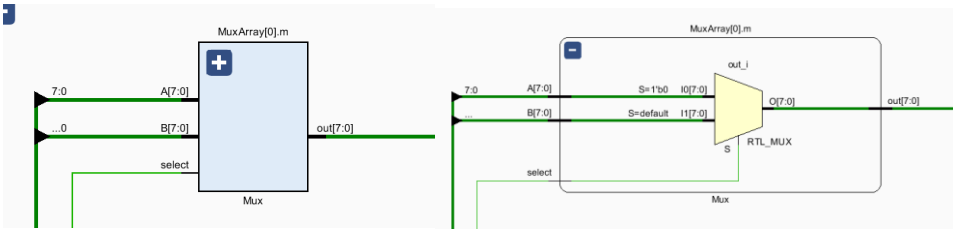
- **Implementation: Using Xilinx Vivado Software (Use Zynq-7000 xc7z007 sclg225-2 FPGA)**

Consider only 8-bit arithmetic. **You must implement a scalable design.**

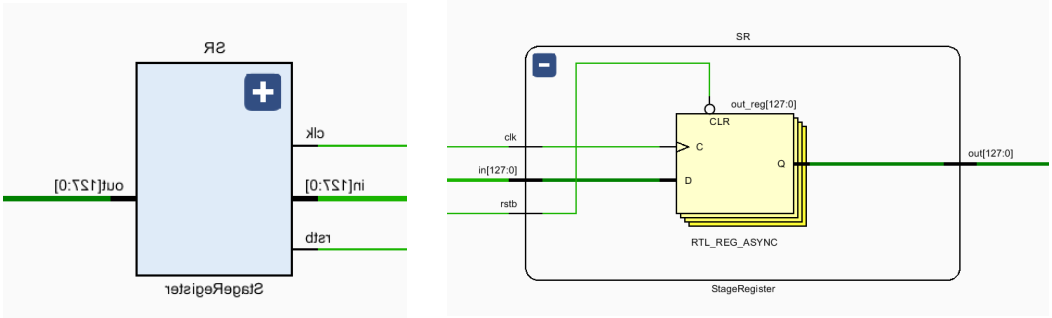
1. Implement a barrel shifter design in Verilog which takes n inputs with 8 bits and shift them by r (value of r is passed to select bits and $r_{max} = (n-1)$).
2. For a 16 elements design with a maximum shift of 15, write a testbench and verify the waveforms.
3. Elaborate the design and include all the schematics screenshots of the modules in the report.
4. Synthesis the design and include the schematics screenshots in the report.
5. Generate Resource and timing estimations and include them in the report.
6. Redo parts 3, 4, 5 for 64 elements (with maximum shift of 63).

Schematics' screenshots are shown below:

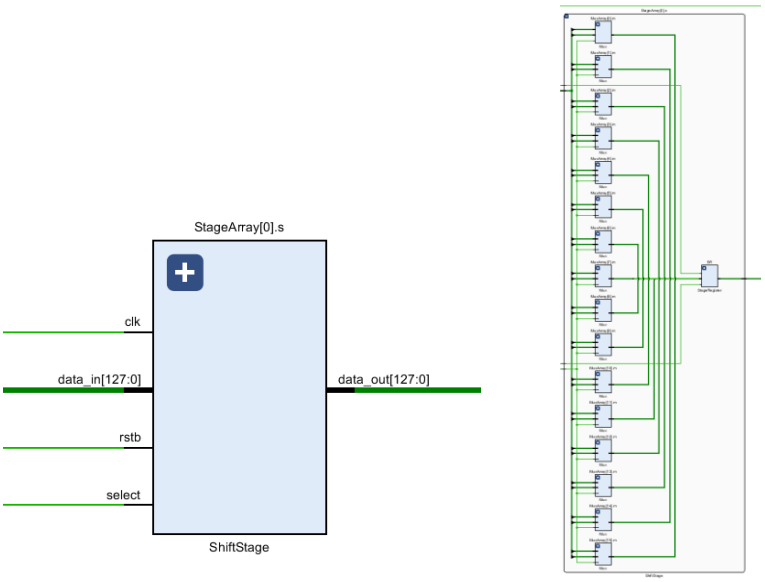
a. **2 Inputs Mux** is designed to select one 8 bits-input to output by the control signal.



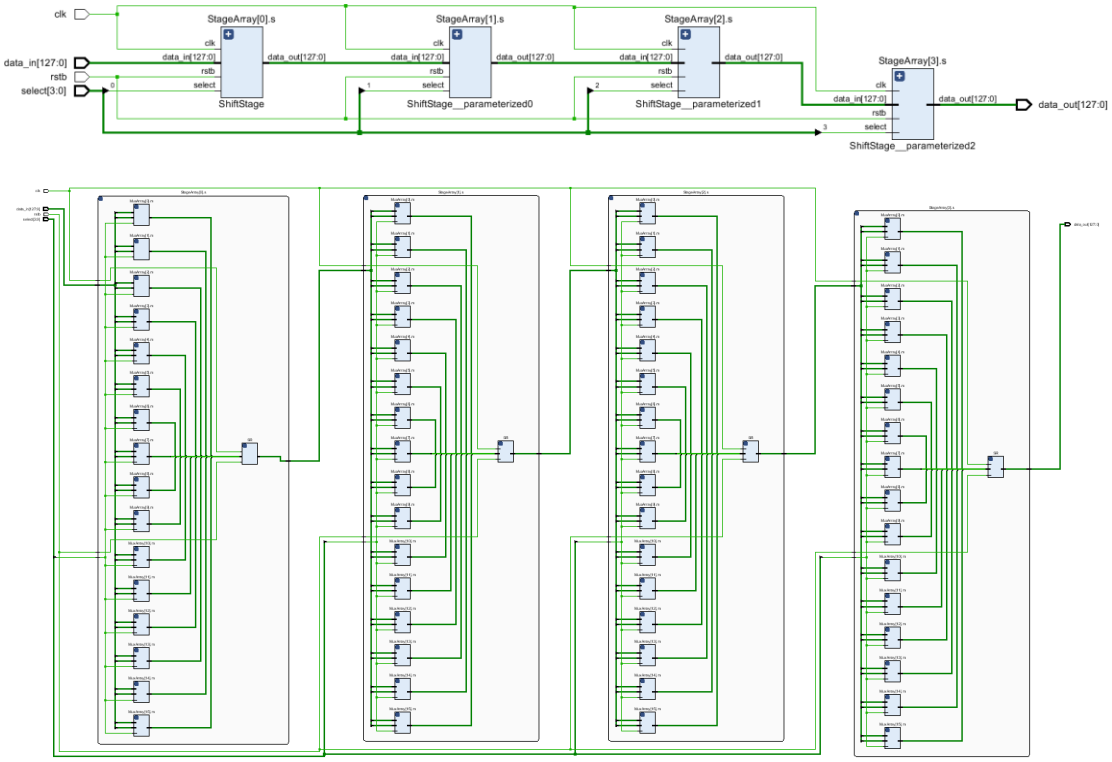
b. **Stage Register** is acted as D Filp-Flop. In every stage, all 16 elements will go through the stage register to next stage so that build a pipeline architecture.



c. **StageArray** contains 16 Muxes and 1 stage register.

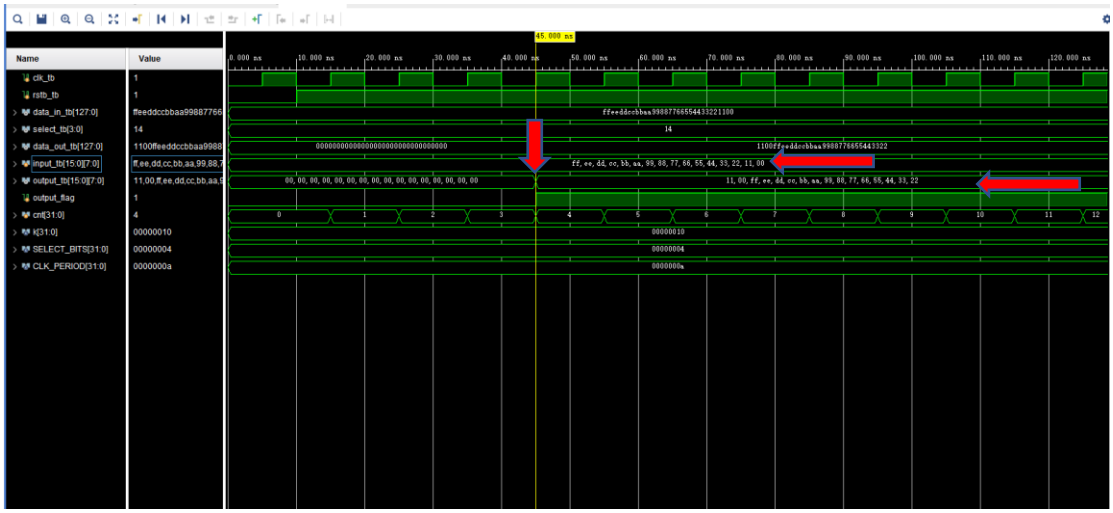


d. **BarrelShifter** is the top module of the design. For 16 elements barrel shifter, we need 4 stages connected end to end.



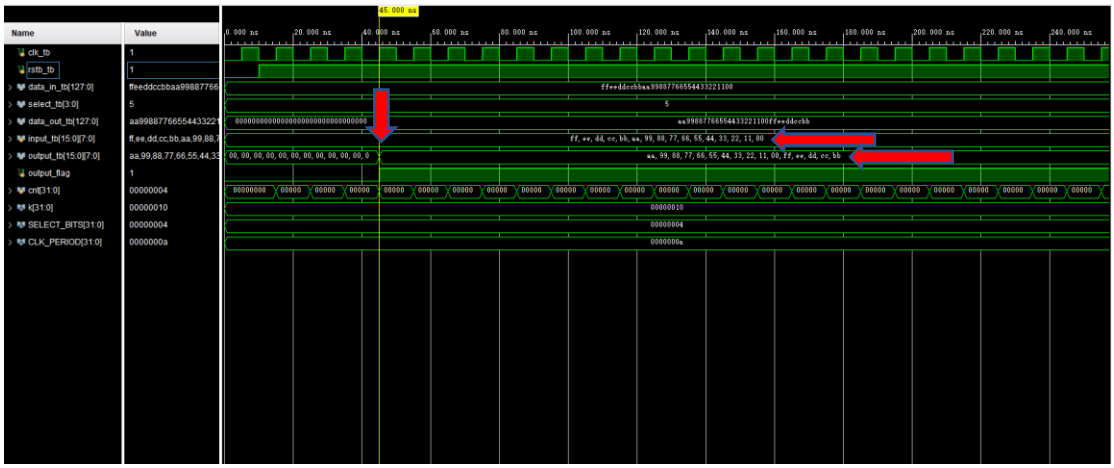
The total schematic is shown in the Appendix.

For a 16 elements test bench, we give 16 8-bit numbers as input, and after 2*16 = 32 clocks, the module will output sorted results. The waveform is shown as followed:



We can see input_tb includes 16 8-bit numbers, after 4 clocks, output_tb gives the number array which shift by 14.

Then, we change the number of shifting.



We can see input_tb includes 16 8-bit numbers, after 4 clocks, output_tb gives the number array which shift by 5.

The full synthesis schematic please see in the Appendix.

Resource Estimations:

```
Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
------------------------------------------------------------------------------------
| Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec  5 04:49:17 MST 2019
| Date         : Thu Apr  2 20:45:41 2020
| Host         : DESKTOP-06TLU5M running 64-bit major release  (build 9200)
| Command      : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb
| Design       : BarrelShifter
| Device       : 7z007sclg225-2
| Design State : Synthesized
------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents
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1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists

1. Slice Logic
--------------

+----------------------------+------+-------+-----------+-------+
|          Site Type         | Used | Fixed | Available | Util% |
+----------------------------+------+-------+-----------+-------+
| Slice LUTs*                |  257 |     0 |     14400 |  1.78 |
|   LUT as Logic             |  257 |     0 |     14400 |  1.78 |
|   LUT as Memory            |    0 |     0 |      6000 |  0.00 |
| Slice Registers            |  512 |     0 |     28800 |  1.78 |
|   Register as Flip Flop    |  512 |     0 |     28800 |  1.78 |
|   Register as Latch        |    0 |     0 |     28800 |  0.00 |
| F7 Muxes                   |    0 |     0 |      8800 |  0.00 |
| F8 Muxes                   |    0 |     0 |      4400 |  0.00 |
+----------------------------+------+-------+-----------+-------+
* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type
--------------------------------

+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     | _            | -           | -            |
| 0     | _            | -           | Set          |
| 0     | _            | -           | Reset        |
| 0     | _            | Set         | -            |
| 0     | _            | Reset       | -            |
| 0     | Yes          | -           | -            |
| 0     | Yes          | -           | Set          |
| 512   | Yes          | -           | Reset        |
| 0     | Yes          | Set         | -            |
| 0     | Yes          | Reset       | -            |
+-------+--------------+-------------+--------------+
```

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	262	0	54	485.19
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT3	512	LUT
FDCE	512	Flop & Latch
IBUF	134	IO
OBUF	128	IO
LUT1	1	LUT
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.609 ns	Worst Hold Slack (WHS):	0.127 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	384	Total Number of Endpoints:	384	Total Number of Endpoints:	513

All user specified timing constraints are met.

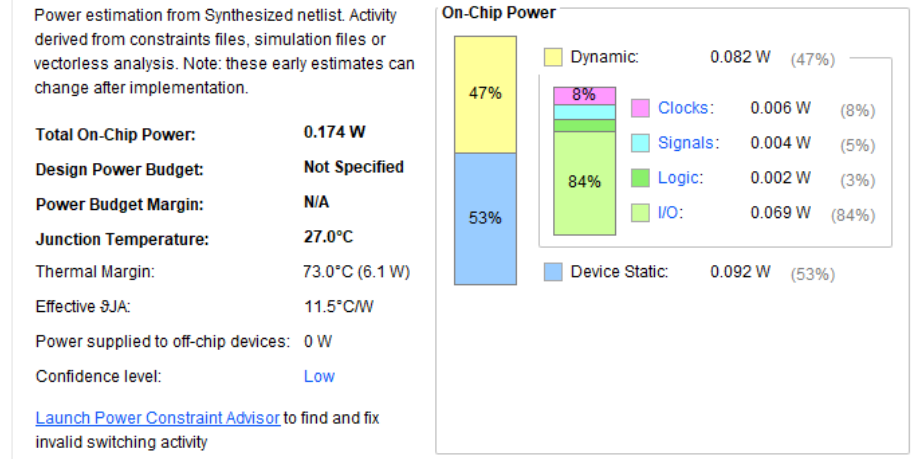
Power Estimation:

Summary

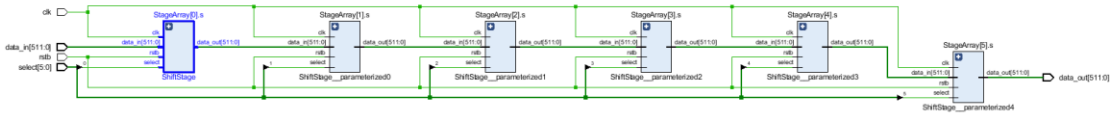
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

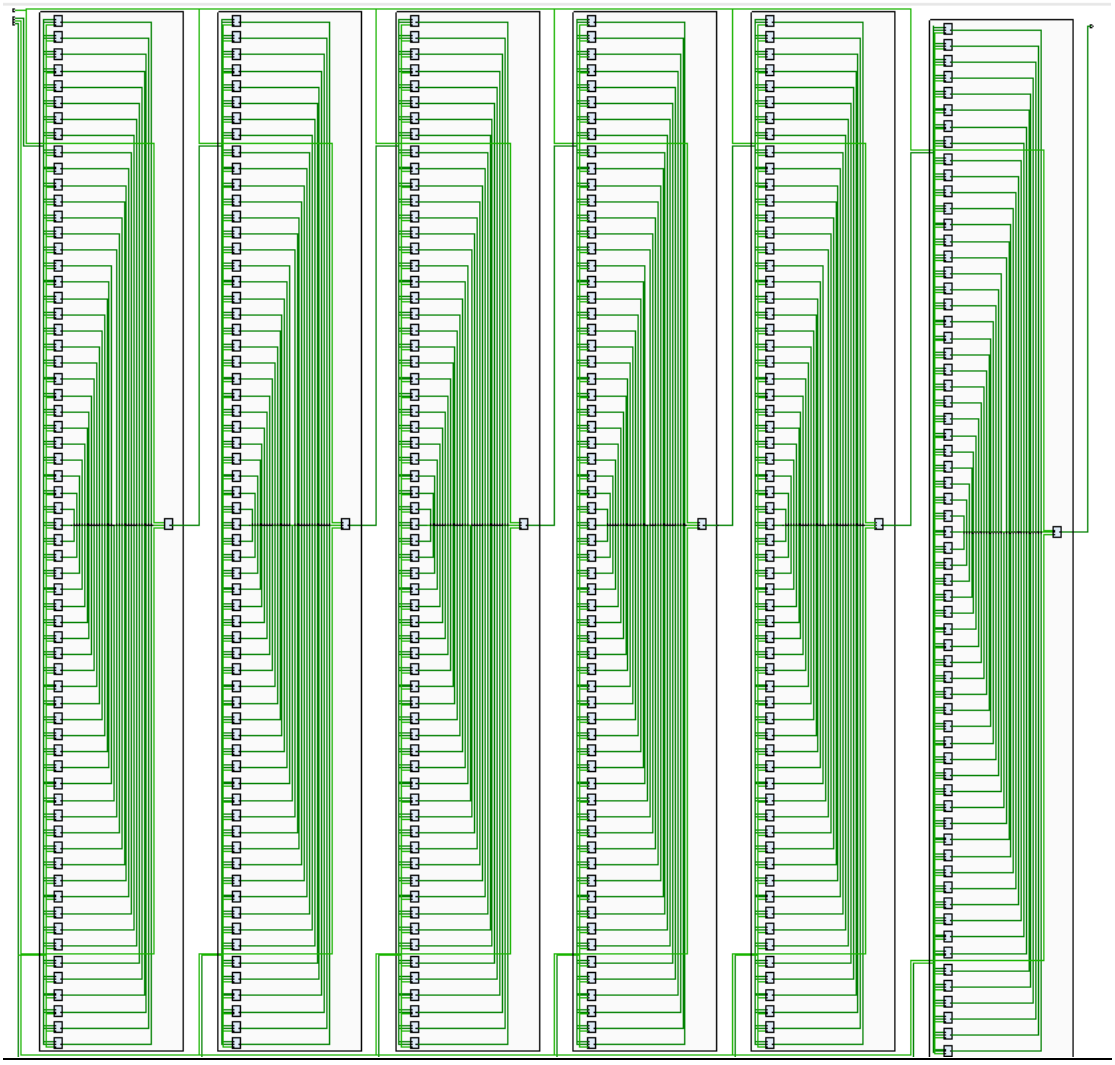
Total On-Chip Power:	**0.174 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.0°C**
Thermal Margin:	73.0°C (6.1 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Now redo for 64 inputs.





The full synthesis schematic please see in the Appendix.

Resource Estimation:

| Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec 5 04:49:17 MST 2019
| Date : Thu Apr 2 21:06:07 2020
| Host : DESKTOP-06TLU5M running 64-bit major release (build 9200)
| Command : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb
| Design : BarrelShifter
| Device : 7z007sclg225-2
| Design State : Synthesized

Utilization Design Information

Table of Contents

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1537	0	14400	10.67
LUT as Logic	1537	0	14400	10.67
LUT as Memory	0	0	6000	0.00
Slice Registers	3072	0	28800	10.67
Register as Flip Flop	3072	0	28800	10.67
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
3072	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic avail

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	1032	0	54	1911.11
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT3	3072	LUT
FDCE	3072	Flop & Latch
IBUF	520	IO
OBUF	512	IO
LUT1	1	LUT
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.609 ns	Worst Hold Slack (WHS):	0.188 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2560	Total Number of Endpoints:	2560	Total Number of Endpoints:	3073

All user specified timing constraints are met.

Power Estimation:

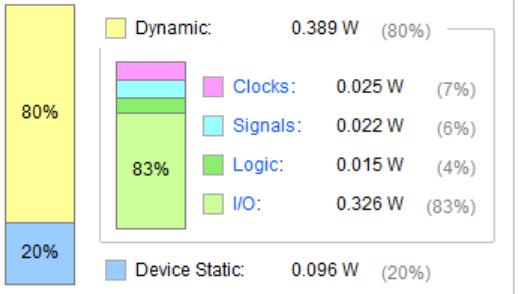
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

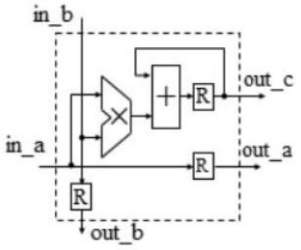
Total On-Chip Power:	**0.485 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.6°C**
Thermal Margin:	69.4°C (5.8 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

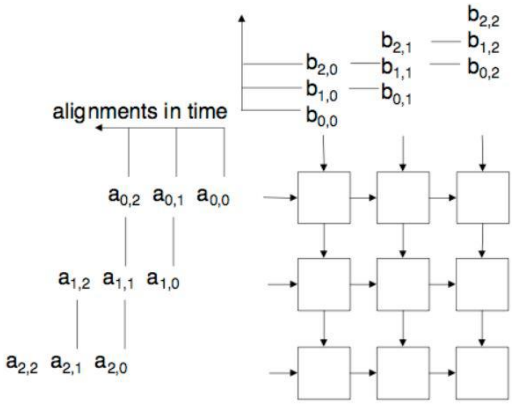
On-Chip Power



2 Systolic Array for Dense Matrix-Matrix Multiplicatio n [50 Points]



Internals of the PE



Example 3 × 3 Systolic Array

The Systolic Architecture consists of an array of processing elements, where data flows between neighboring elements, synchronously, from different directions. Processing element takes data from Top, Left, and output the results to Right, Bottom.

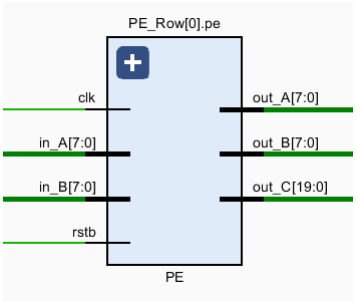
One of the main applications of Systolic Architecture is matrix multiplication. As the following figure depicts, in a, in b are inputs to the processing element and out a, out bare output to the processing element. out c is to get the output result of each processing element.

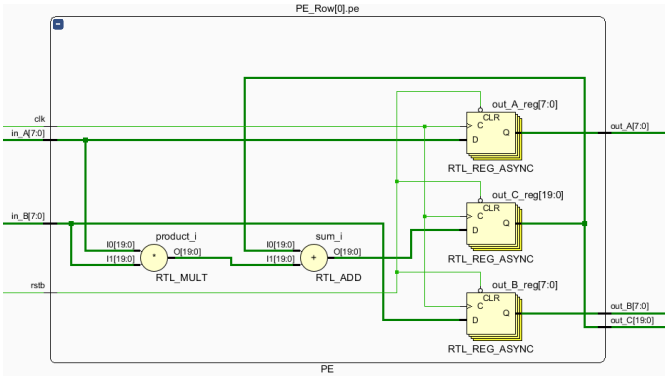
Processing elements are arranged in the form of an array. In the following example, we analyze, multiplication of 3 × 3 matrices, which can be easily extended. Let say the two matrices are A and B. Figure above depicts how matrix A and B are fed into PE array.

2.1 Implementation

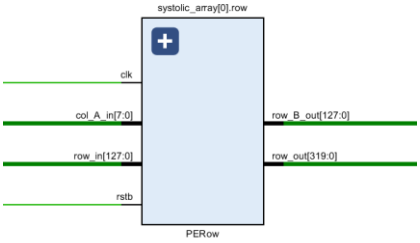
Schematics' screenshots are shown below:

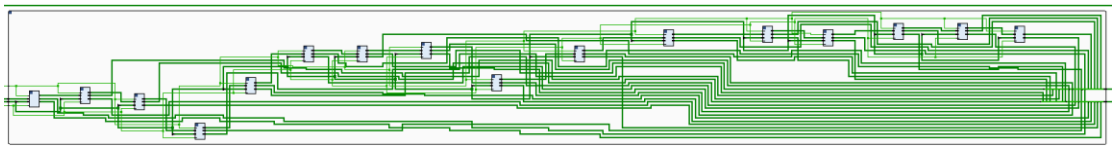
PE is designed to calculate the product of two 8 bits-input A and B, and accumulate all the products produced by own. Also, each PE will also transfer the two inputs to the next every clock. So there are a multiplier, an adder and three output register.



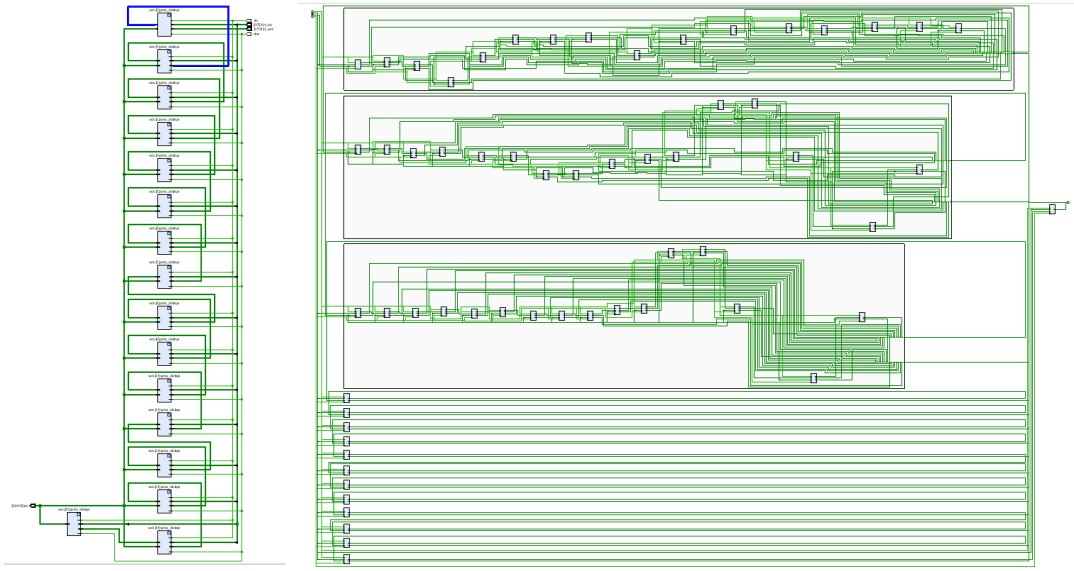


PERow is designed to build a row of systolic array. For a systolic array of n × n size, PERow contains n PEs.

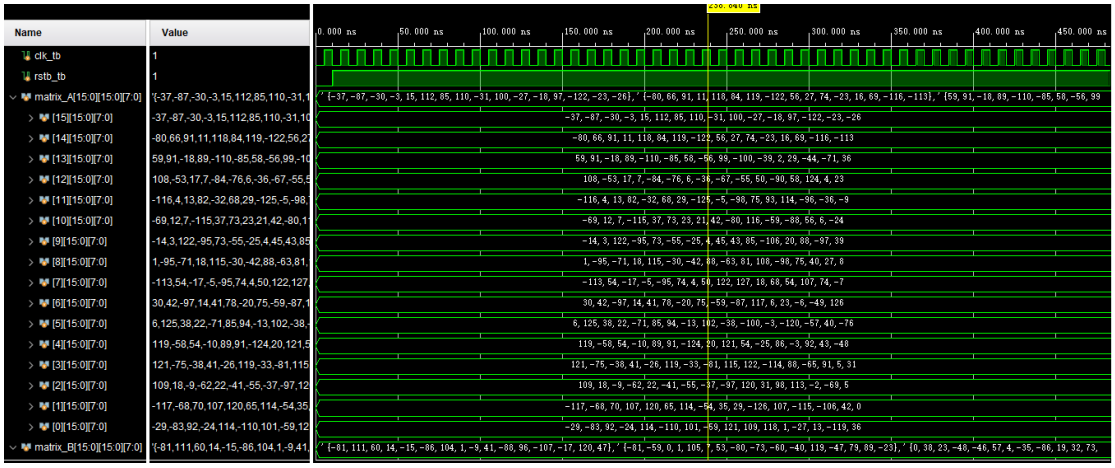


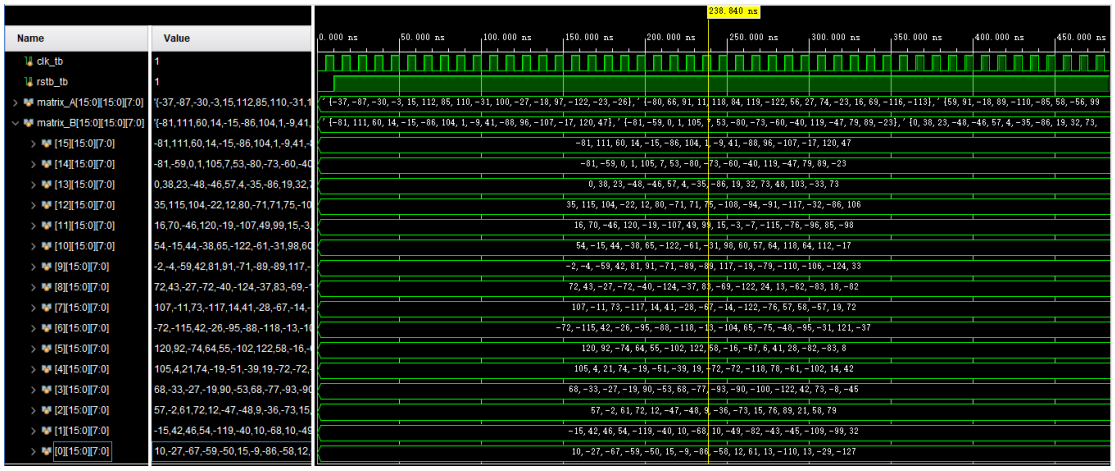


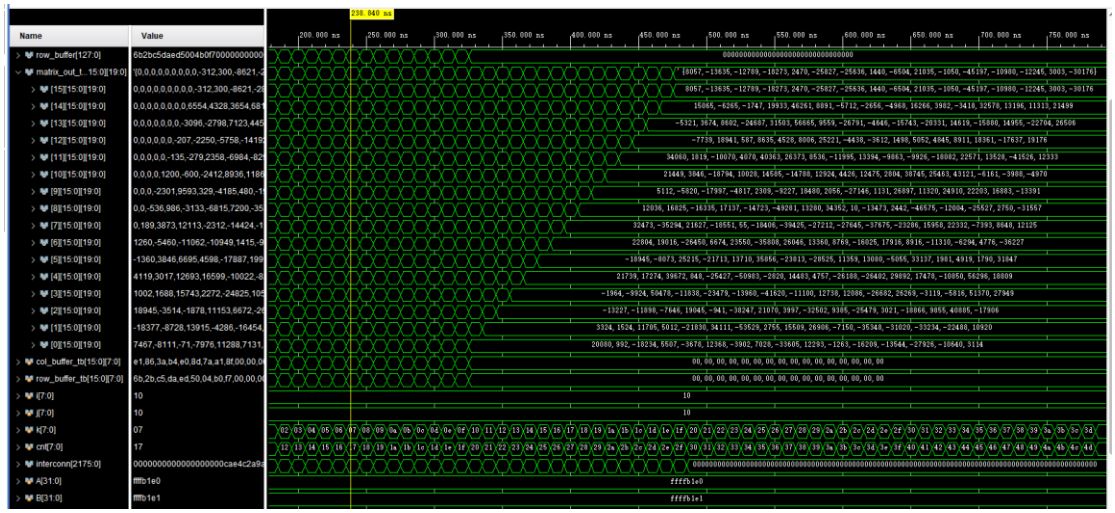
The Top Module, which is **SystolicArray** consist of n PERows.

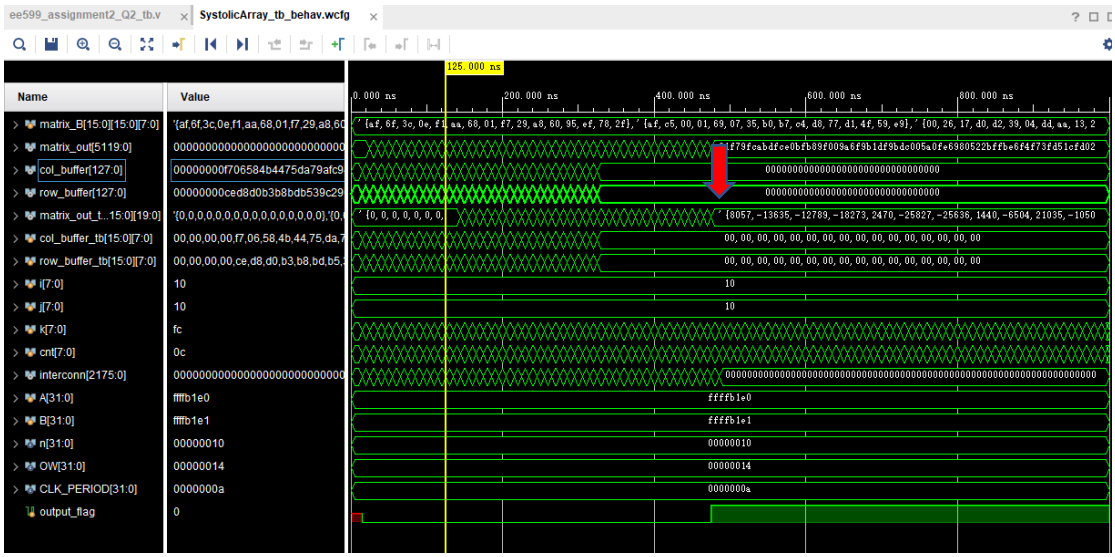


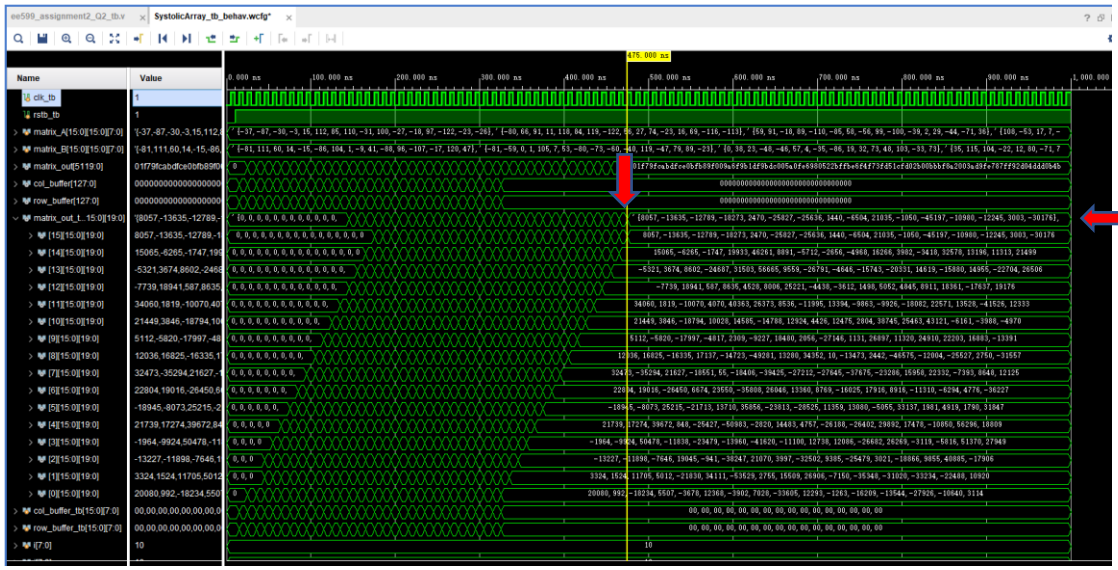
For a 16 × 16 size systolic array test bench, we give two 16 × 16 size matrices as input, and after 3 × n − 1 = 47 clocks, the module will output results. The waveform is shown as followed:


Name
Value
clk_tb
rstb_tb
matrix_A[15:0][15:0][7:0]
matrix_B[15:0][15:0][7:0]
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns


Name
Value
clk_tb
rstb_tb
matrix_A[15:0][15:0][7:0]
matrix_B[15:0][15:0][7:0]
238.040 ns
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns

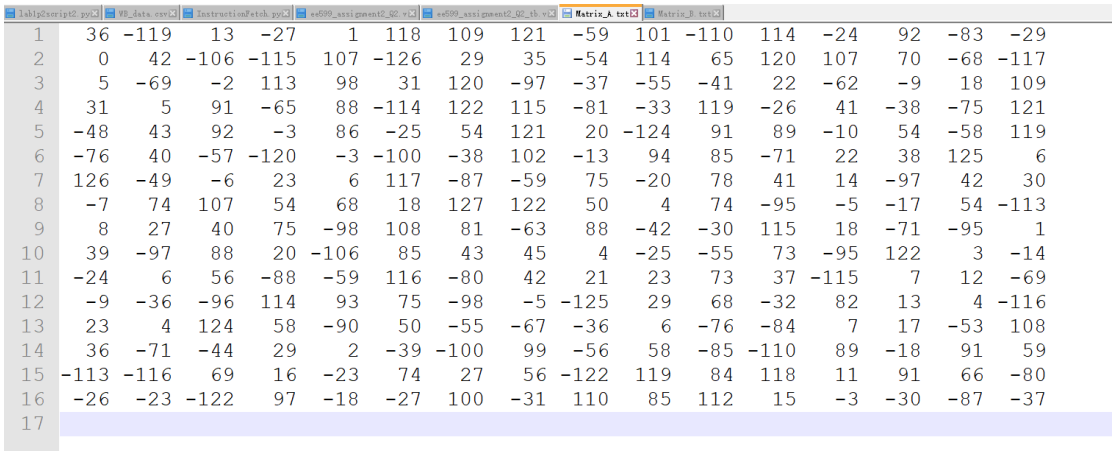

Name
Value
row_buffer[127:0]
matrix_out_t...15:0][19:0]
col_buffer_tb[15:0][7:0]
row_buffer_tb[15:0][7:0]
i[7:0]
j[7:0]
k[7:0]
cnt[7:0]
interconn[2175:0]
A[31:0]
B[31:0]
238.040 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns
500.000 ns
550.000 ns
600.000 ns
650.000 ns
700.000 ns
750.000 ns





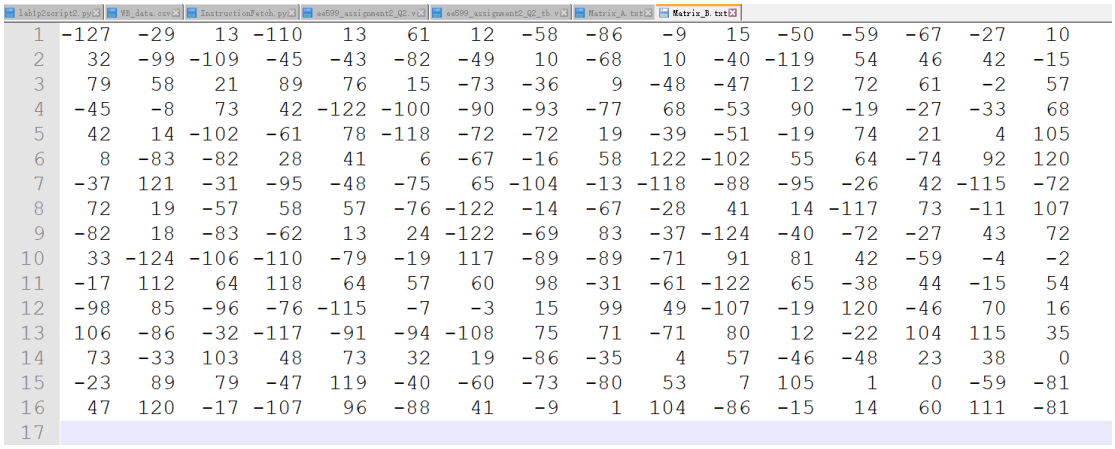
Here, we generate the two matrices by random. Using Verilog system function, we can easily generate the data and store them into two files Matrix_A.txt and Matrix_B.txt.

```
initial
    begin : MATRIX_GENERATOR
    A = $fopen("../../../../Matrix_A.txt", "w");
    B = $fopen("../../../../Matrix_B.txt", "w");
    for (i = 0; i < n; i = i + 1)
        begin
        for (j = 0; j < n; j = j + 1)
            begin
                matrix_A[i][j] = $random % 128;
                matrix_B[i][j] = $random % 128;
                col_buffer_tb[i] = 0;
                row_buffer_tb[i] = 0;
                $fwrite(A, "%d ", matrix_A[i][j]);
                $fwrite(B, "%d ", matrix_B[i][j]);
            end
            $fwrite(A, "\n");$fwrite(B, "\n");
        end
    $fclose(A);
    $fclose(B);
    end
```



1	36	-119	13	-27	1	118	109	121	-59	101	-110	114	-24	92	-83	-29
2	0	42	-106	-115	107	-126	29	35	-54	114	65	120	107	70	-68	-117
3	5	-69	-2	113	98	31	120	-97	-37	-55	-41	22	-62	-9	18	109
4	31	5	91	-65	88	-114	122	115	-81	-33	119	-26	41	-38	-75	121
5	-48	43	92	-3	86	-25	54	121	20	-124	91	89	-10	54	-58	119
6	-76	40	-57	-120	-3	-100	-38	102	-13	94	85	-71	22	38	125	6
7	126	-49	-6	23	6	117	-87	-59	75	-20	78	41	14	-97	42	30
8	-7	74	107	54	68	18	127	122	50	4	74	-95	-5	-17	54	-113
9	8	27	40	75	-98	108	81	-63	88	-42	-30	115	18	-71	-95	1
10	39	-97	88	20	-106	85	43	45	4	-25	-55	73	-95	122	3	-14
11	-24	6	56	-88	-59	116	-80	42	21	23	73	37	-115	7	12	-69
12	-9	-36	-96	114	93	75	-98	-5	-125	29	68	-32	82	13	4	-116
13	23	4	124	58	-90	50	-55	-67	-36	6	-76	-84	7	17	-53	108
14	36	-71	-44	29	2	-39	-100	99	-56	58	-85	-110	89	-18	91	59
15	-113	-116	69	16	-23	74	27	56	-122	119	84	118	11	91	66	-80
16	-26	-23	-122	97	-18	-27	100	-31	110	85	112	15	-3	-30	-87	-37
17																

Matrix_A.txt



1	-127	-29	13	-110	13	61	12	-58	-86	-9	15	-50	-59	-67	-27	10
2	32	-99	-109	-45	-43	-82	-49	10	-68	10	-40	-119	54	46	42	-15
3	79	58	21	89	76	15	-73	-36	9	-48	-47	12	72	61	-2	57
4	-45	-8	73	42	-122	-100	-90	-93	-77	68	-53	90	-19	-27	-33	68
5	42	14	-102	-61	78	-118	-72	-72	19	-39	-51	-19	74	21	4	105
6	8	-83	-82	28	41	6	-67	-16	58	122	-102	55	64	-74	92	120
7	-37	121	-31	-95	-48	-75	65	-104	-13	-118	-88	-95	-26	42	-115	-72
8	72	19	-57	58	57	-76	-122	-14	-67	-28	41	14	-117	73	-11	107
9	-82	18	-83	-62	13	24	-122	-69	83	-37	-124	-40	-72	-27	43	72
10	33	-124	-106	-110	-79	-19	117	-89	-89	-71	91	81	42	-59	-4	-2
11	-17	112	64	118	64	57	60	98	-31	-61	-122	65	-38	44	-15	54
12	-98	85	-96	-76	-115	-7	-3	15	99	49	-107	-19	120	-46	70	16
13	106	-86	-32	-117	-91	-94	-108	75	71	-71	80	12	-22	104	115	35
14	73	-33	103	48	73	32	19	-86	-35	4	57	-46	-48	23	38	0
15	-23	89	79	-47	119	-40	-60	-73	-80	53	7	105	1	0	-59	-81
16	47	120	-17	-107	96	-88	41	-9	1	104	-86	-15	14	60	111	-81
17																

Matrix_B.txt

We can get the result from waveform, and we can also read from the output file Matrix_Result.txt. Then we write a Python script to verify the result.

ResultVerification.py

D: > XilinxPorject > Assignment2_Q2_SystolicArrayforDMM > ResultVerification.py > ...

```python
import numpy as np

matrix_A = np.loadtxt('Matrix_A.txt')
matrix_B = np.loadtxt('Matrix_B.txt')
print (matrix_A)

print(matrix_B)
result = np.dot(matrix_A, matrix_B)
np.set_printoptions(suppress=True)

print (result)
```

And use python we can get the result as below.

```
[[  3114. -10640. -27926. -13544. -16209.  -1263.  12293. -33605.   7028.
   -3902.  12368.  -3678.   5507. -18234.    992.  20080.]
 [ 10920. -22488. -33234. -31020. -35348.  -7150.  26906.  15509.   2755.
  -53529.  34111. -21830.   5012.  11705.   1524.   3324.]
 [-17906.  40885.   9855. -18866.   3021. -25479.   9385. -32502.   3997.
   21070. -38247.   -941.  19045.  -7646. -11898. -13227.]
 [ 27949.  51370.  -5816.  -3119.  26269. -26682.  12086.  12738. -11100.
  -41620. -13960. -23479. -11838.  50478.  -9924.  -1964.]
 [ 18809.  56296. -10850.  17478.  29892. -26402. -26188.   4757.  14483.
   -2820. -50983. -25427.    848.  39672.  17274.  21739.]
 [ 31847.   1790.   4919.   1981.  33137.  -5055.  13080.  11359. -28525.
  -23813.  35856.  13710. -21713.  25215.  -8073. -18945.]
 [-36227.   4776.  -6294. -11310.   8916.  17916. -16025.   8769.  13360.
   26046. -35808.  23550.   6674. -26450.  19016.  22804.]
 [ 12125.   8648.  -7393.  22332.  15958. -23286. -37675. -27645. -27212.
  -39425. -18406.     55. -18551.  21627. -35294.  32473.]
 [-31557.   2750. -25527. -12004. -46575.   2442. -13473.     10.  34352.
   13280. -49281. -14723.  17137. -16335.  16825.  12036.]
 [-13391.  16883.  22203.  24910.  11320.  26897.   1131. -27146.   2056.
   18480.  -9227.   2309.  -4817. -17997.  -5820.   5112.]
 [ -4970.  -3988.  -6161.  43121.  25463.  38745.   2804.  12475.   4426.
   12924. -14788.  14585.  10028. -18794.   3846.  21449.]
 [ 12333. -41526.  13528.  22571. -18082.  -9926.  -9863.  13394. -11995.
    8536.  26373.  40363.   4070. -10070.   1819.  34060.]
 [ 19176. -17637.  18361.   8911.   4845.   5052.   1498.  -3612.  -4438.
   25221.   8006.   4528.   8635.    587.  18941.  -7739.]
 [ 26506. -22704.  14955. -15880.  14619. -20331. -15743.  -4646. -26791.
    9559.  56665.  31503. -24687.   8602.   3674.  -5321.]
 [ 21499.  11313.  13196.  32578.  -3418.   3982.  16266.  -4968.  -2656.
   -5712.   8891.  46261.  19933.  -1747.  -6265.  15065.]
 [-30176.   3003. -12245. -10980. -45197.  -1050.  21035.  -6504.   1440.
  -25636. -25827.   2470. -18273. -12789. -13635.   8057.]]
PS D:\XilinxPorject\Assignment2_Q2_SystolicArrayforDMM>
```

And compare the output file or waveform from the simulation, we can verify the correctness of systolic array.

1	3114	-10640	-27926	-13544	-16209	-1263	12293	-33605	7028	-3902	12368	-3678	5507	-18234	992	20080
2	10920	-22488	-33234	-31020	-35348	-7150	26906	15509	2755	-53529	34111	-21830	5012	11705	1524	3324
3	-17906	40885	9855	-18866	3021	-25479	9385	-32502	3997	21070	-38247	-941	19045	-7646	-11898	-13227
4	27949	51370	-5816	-3119	26269	-26682	12086	12738	-11100	-41620	-13960	-23479	-11838	50478	-9924	-1964
5	18809	56296	-10850	17478	29892	-26402	-26188	4757	14483	-2820	-50983	-25427	848	39672	17274	21739
6	31847	1790	4919	1981	33137	-5055	13080	11359	-28525	-23813	35856	13710	-21713	25215	-8073	-18945
7	-36227	4776	-6294	-11310	8916	17916	-16025	8769	13360	26046	-35808	23550	6674	-26450	19016	22804
8	12125	8648	-7393	22332	15958	-23286	-37675	-27645	-27212	-39425	-18406	55	-18551	21627	-35294	32473
9	-31557	2750	-25527	-12004	-46575	2442	-13473	10	34352	13280	-49281	-14723	17137	-16335	16825	12036
10	-13391	16883	22203	24910	11320	26897	1131	-27146	2056	18480	-9227	2309	-4817	-17997	-5820	5112
11	-4970	-3988	-6161	43121	25463	38745	2804	12475	4426	12924	-14788	14585	10028	-18794	3846	21449
12	12333	-41526	13528	22571	-18082	-9926	-9863	13394	-11995	8536	26373	40363	4070	-10070	1819	34060
13	19176	-17637	18361	8911	4845	5052	1498	-3612	-4438	25221	8006	4528	8635	587	18941	-7739
14	26506	-22704	14955	-15880	14619	-20331	-15743	-4646	-26791	9559	56665	31503	-24687	8602	3674	-5321
15	21499	11313	13196	32578	-3418	3982	16266	-4968	-2656	-5712	8891	46261	19933	-1747	-6265	15065
16	-30176	3003	-12245	-10980	-45197	-1050	21035	-6504	1440	-25636	-25827	2470	-18273	-12789	-13635	8057
17																

Matrix_Result.txt

The synthesis schematic please see in the Appendix.

Resource Estimation for 16x16 size:

```
Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
------------------------------------------------------------------------------------
| Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec  5 04:49:17 MST 2019
| Date         : Thu Apr  2 23:28:40 2020
| Host         : DESKTOP-O6TLU5M running 64-bit major release  (build 9200)
| Command      : report_utilization -file SystolicArray_utilization_synth.rpt -pb SystolicArray_utilization_synth.pb
| Design       : SystolicArray
| Device       : 7z007sclg225-2
| Design State : Synthesized
------------------------------------------------------------------------------------


Utilization Design Information

Table of Contents
-----------------

1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists

1. Slice Logic
```

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	20992	0	14400	145.78
LUT as Logic	20992	0	14400	145.78
LUT as Memory	0	0	6000	0.00
Slice Registers	8960	0	28800	31.11
Register as Flip Flop	8960	0	28800	31.11
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
8960	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic availab

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	5378	0	54	9959.26
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	11264	LUT
FDCE	8960	Flop & Latch
LUT6	6656	LUT
LUT4	6400	LUT
OBUF	5120	IO
CARRY4	4608	CarryLogic
LUT5	1536	LUT
LUT3	1536	LUT
IBUF	258	IO
LUT1	1	LUT
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.935 ns	Worst Hold Slack (WHS):	0.165 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8704	Total Number of Endpoints:	8704	Total Number of Endpoints:	8961

All user specified timing constraints are met.

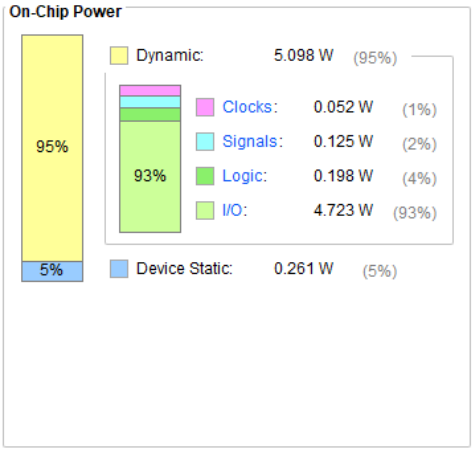
Power Estimation:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**5.359 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**86.8°C**
Thermal Margin:	13.2°C (1.1 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



<u>Now redo for 32x32 size.</u>

The full synthesis schematic please see in the Appendix.

Resource Estimation:

```
Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
------------------------------------------------------------------------------------
| Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec  5 04:49:17 MST 2019
| Date         : Thu Apr  2 23:57:00 2020
| Host         : DESKTOP-06TLU5M running 64-bit major release  (build 9200)
| Command      : report_utilization -file SystolicArray_utilization_synth.rpt -pb SystolicArray_utilization_synth.pb
| Design       : SystolicArray
| Device       : 7z007sclg225-2
| Design State : Synthesized
------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents
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1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists
```

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	84992	0	14400	590.22
LUT as Logic	84992	0	14400	590.22
LUT as Memory	0	0	6000	0.00
Slice Registers	37376	0	28800	129.78
Register as Flip Flop	37376	0	28800	129.78
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and f

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
37376	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic availa

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	22018	0	54	40774.07
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	46080	LUT
FDCE	37376	Flop & Latch
LUT6	26624	LUT
LUT4	25600	LUT
OBUF	21504	IO
CARRY4	19456	CarryLogic
LUT5	6144	LUT
LUT3	6144	LUT
IBUF	514	IO
LUT1	1	LUT
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.923 ns	Worst Hold Slack (WHS):	0.165 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	36864	Total Number of Endpoints:	36864	Total Number of Endpoints:	37377

All user specified timing constraints are met.

Power Estimation:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**22.079 W (Junction temp exceeded!)**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**125.0°C**
Thermal Margin:	-179.6°C (-15.1 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity