EE 599 Spring 2020

Homework1

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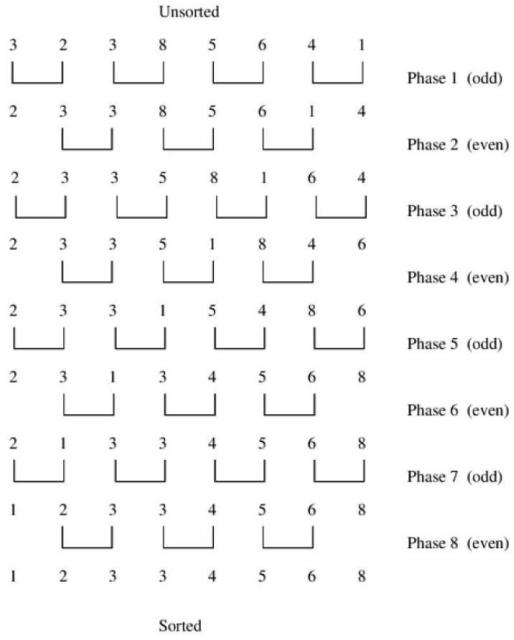
2020/03/05

1 Odd-even transposition sort[40 Points]

Odd-even transposition sort algorithm is a parallel sorting algorithm. It sorts n elements in n clocks (n is even), each of which requires n/2 compare-exchange operations. This algorithm alternates between two phases, called the odd and even phases. Let $< a_1; a_2; \ldots ; a_n >$ be the sequence to be sorted. During the odd phase, elements with odd indices are compared with their right neighbors, and if they are out of sequence they are exchanged; thus, the pairs $(a_1; a_2)$; $(a_3; a_4)$; ...; $(a_{n-1}; a_n)$ are compare-exchanged (assuming n is even). Similarly, during the even phase, elements with even indices are compared with their right neighbors, and if they are out of sequence they are exchanged; thus, the pairs $(a_2; a_3)$; $(a_4; a_5)$; :::; $(a_{n-2}; a_{n-1})$ are compare-exchanged. After n phases of odd-even exchanges, the sequence is sorted. An example sorting instance is shown in Figure 1.

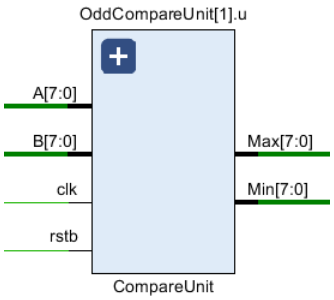


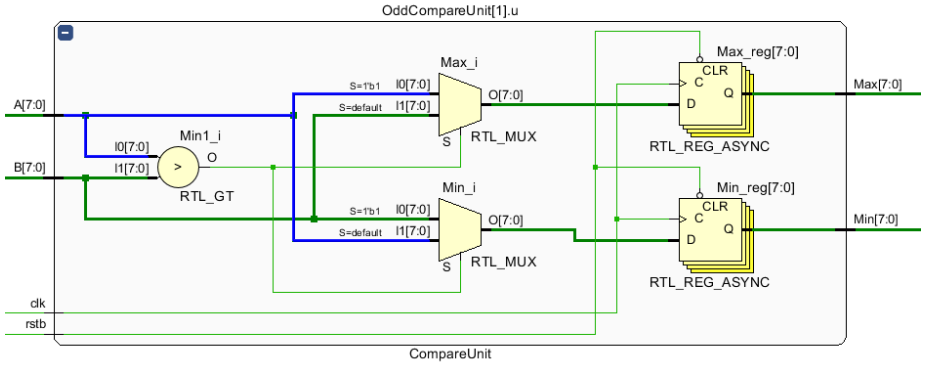
- **Implementation: Using Xilinx Vivado Software (Use Zynq-7000 xc7z007 sclg225-2 FPGA)**

1. Using Verilog, implement odd-even transposition circuit, which takes n, 8 bit inputs and sort them.
2. For a 16 elements write a test bench and verify the waveforms.
3. Elaborate the design and include all the schematics' screenshots of the modules in the report.
4. Synthesis the design and include the screenshots.
5. Generate Resource and timing estimations and include them in the report.
6. Redo part 3, 4, 5 for 32, 64, 128.

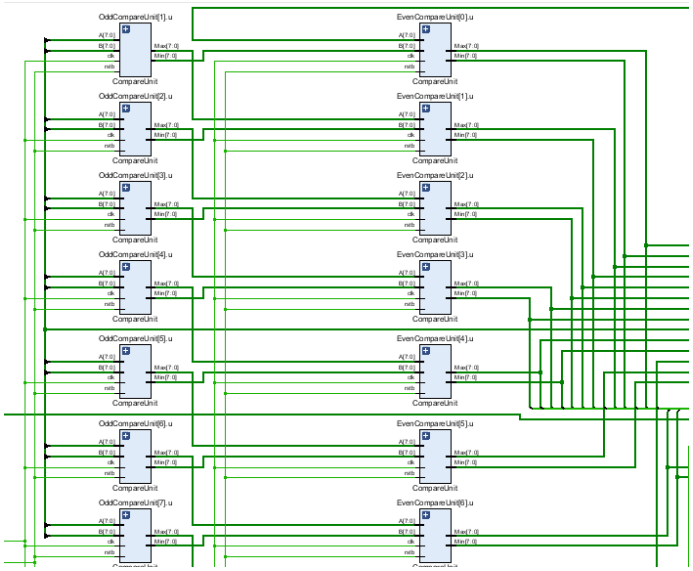
Schematics' screenshots are shown below:

a. **OddCompareUnit** is designed to compare two 8-bit number A and B, and output the maximum one and minimum one between them.



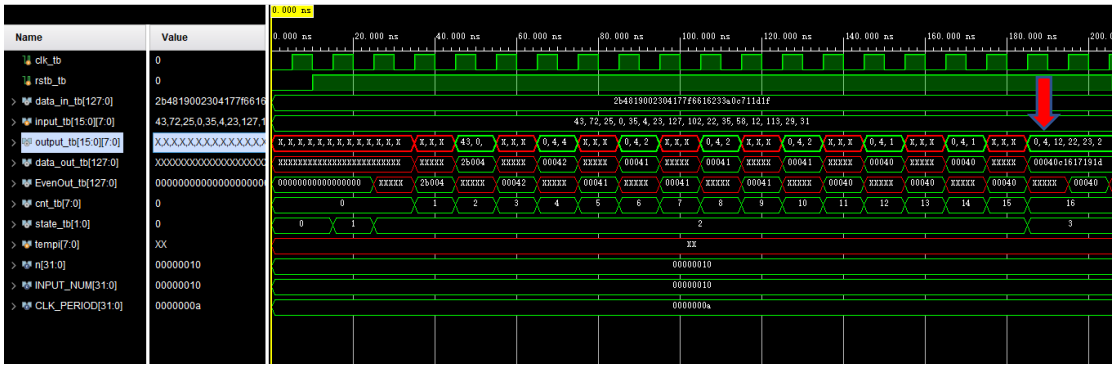


b. **OddevenSort** is the top module of the design. The main part of this module is an array of compare unit, which consist of 8 odd compare units and 7 even compare units.

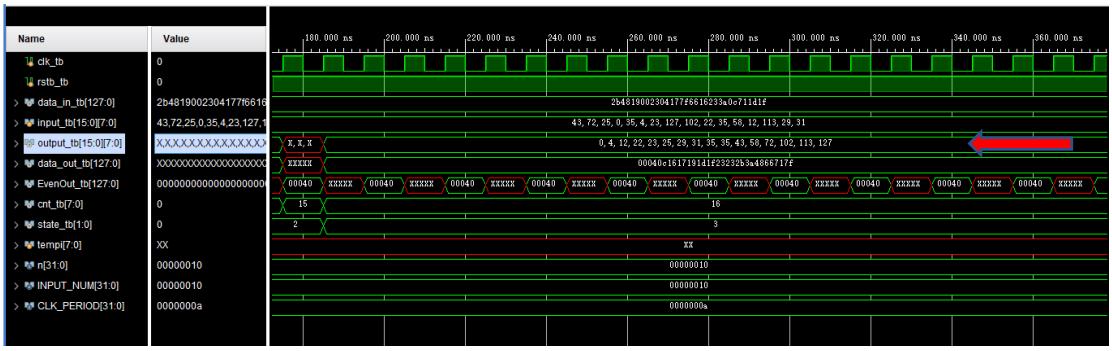


<u>The total schematic is shown in the Appendix.</u>

For a 16 elements test bench, we give 16 8-bit numbers as input, and after 2*16 = 32 clocks, the module will output sorted results. The waveform is shown as followed:



We can see input_tb includes 16 8-bit numbers, after 16 clocks, output_tb gives the sorted number array.



Then, we give another sets of input.

The full synthesis schematic please see in the Appendix.

Resource Estimations:

| Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec 5 04:49:17 MST 2019
| Date : Thu Mar 5 21:23:41 2020
| Host : DESKTOP-06TLU5M running 64-bit major release (build 9200)
| Command : report_utilization -file OddevenSort_utilization_synth.rpt -pb OddevenSort_utilization_synth.pb
| Design : OddevenSort
| Device : 7z007sclg225-2
| Design State : Synthesized

Utilization Design Information

Table of Contents

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	322	0	14400	2.24
LUT as Logic	322	0	14400	2.24
LUT as Memory	0	0	6000	0.00
Slice Registers	396	0	28800	1.38
Register as Flip Flop	396	0	28800	1.38
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
266	Yes	-	Reset
0	Yes	Set	-
130	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore c

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	258	0	54	477.78
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDCE	266	Flop & Latch
LUT6	195	LUT
IBUF	130	IO
FDRE	130	Flop & Latch
OBUF	128	IO
LUT4	125	LUT
LUT3	115	LUT
CARRY4	15	CarryLogic
LUT5	3	LUT
LUT2	3	LUT
LUT1	1	LUT
BUFG	1	Clock

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used

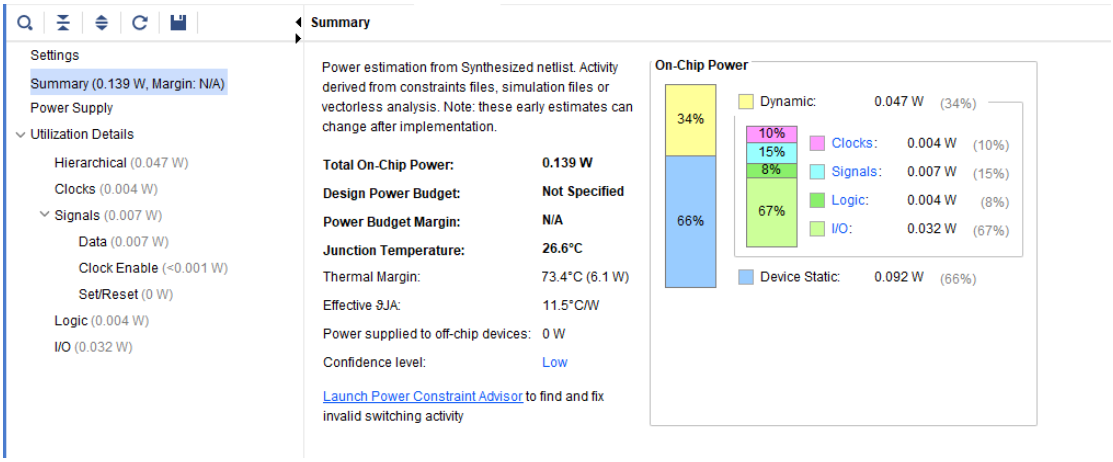
Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.547 ns	Worst Hold Slack (WHS):	0.136 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	532	Total Number of Endpoints:	532	Total Number of Endpoints:	397

All user specified timing constraints are met.

Power Estimation:



Now redo for 32 inputs.

The full synthesis schematic please see in the Appendix.

Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	642	0	14400	4.46
LUT as Logic	642	0	14400	4.46
LUT as Memory	0	0	6000	0.00
Slice Registers	781	0	28800	2.71
Register as Flip Flop	781	0	28800	2.71
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
522	Yes	-	Reset
0	Yes	Set	-
259	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	514	0	54	951.85
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDCE	522	Flop & Latch
LUT6	386	LUT
FDRE	259	Flop & Latch
IBUF	258	IO
OBUF	256	IO
LUT4	253	LUT
LUT3	243	LUT
CARRY4	31	CarryLogic
LUT5	3	LUT
LUT2	3	LUT
LUT1	1	LUT
BUFG	1	Clock

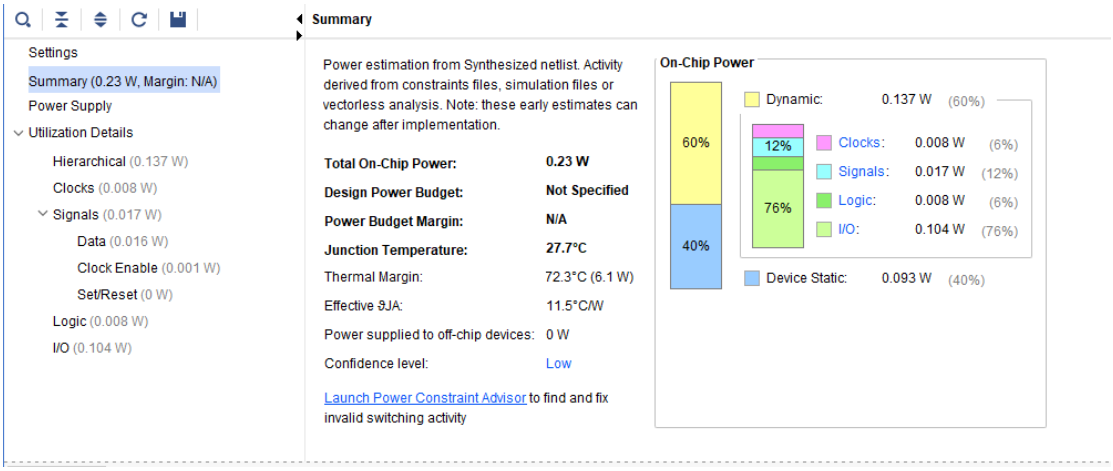
Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.547 ns	Worst Hold Slack (WHS):	0.127 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1045	Total Number of Endpoints:	1045	Total Number of Endpoints:	782

All user specified timing constraints are met.

Power Estimation:



Now redo for 64 inputs.

The full synthesis schematic please see in the Appendix.

Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1430	0	14400	9.93
LUT as Logic	1430	0	14400	9.93
LUT as Memory	0	0	6000	0.00
Slice Registers	1556	0	28800	5.40
Register as Flip Flop	1556	0	28800	5.40
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
1034	Yes	-	Reset
0	Yes	Set	-
522	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic av

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	1026	0	54	1900.00
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDCE	1034	Flop & Latch
LUT3	884	LUT
LUT6	770	LUT
FDRE	522	Flop & Latch
IBUF	514	IO
OBUF	512	IO
LUT4	260	LUT
LUT5	131	LUT
CARRY4	63	CarryLogic
LUT2	3	LUT
LUT1	1	LUT
BUFG	1	Clock

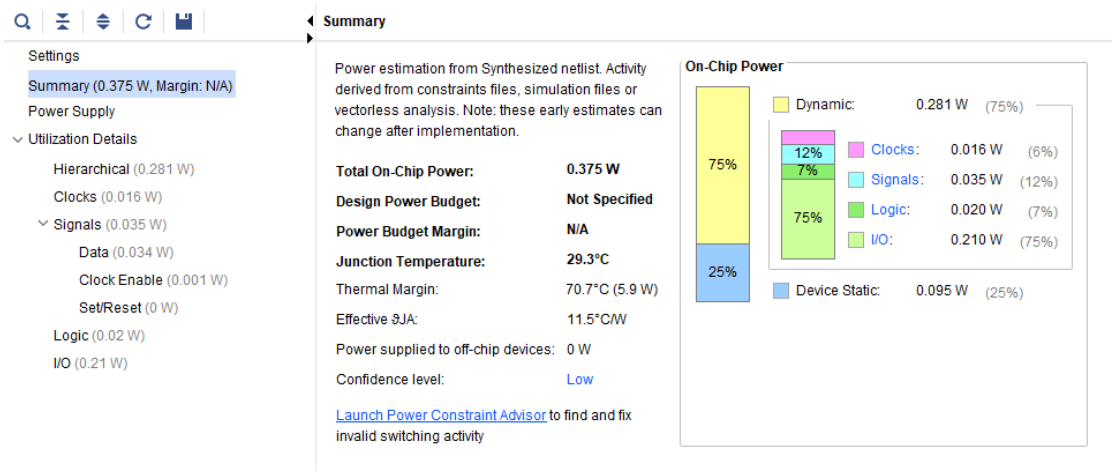
Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.040 ns	Worst Hold Slack (WHS):	0.131 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2076	Total Number of Endpoints:	2076	Total Number of Endpoints:	1557

All user specified timing constraints are met.

Power Estimation:



Now redo for 128 inputs.

The full synthesis schematic please see in the Appendix.

Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2860	0	14400	19.86
LUT as Logic	2860	0	14400	19.86
LUT as Memory	0	0	6000	0.00
Slice Registers	3102	0	28800	10.77
Register as Flip Flop	3102	0	28800	10.77
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
2058	Yes	-	Reset
0	Yes	Set	-
1044	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic ava

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	2050	0	54	3796.30
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDCE	2058	Flop & Latch
LUT3	1780	LUT
LUT6	1538	LUT
FDRE	1044	Flop & Latch
IBUF	1026	IO
OBUF	1024	IO
LUT4	526	LUT
LUT5	259	LUT
CARRY4	127	CarryLogic
LUT2	3	LUT
LUT1	1	LUT
BUFG	1	Clock

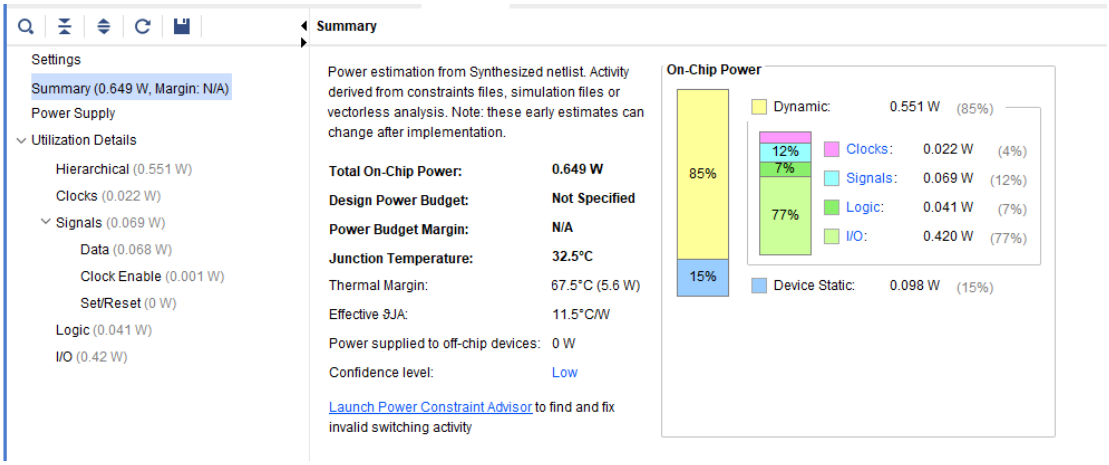
Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.040 ns	Worst Hold Slack (WHS):	0.131 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4134	Total Number of Endpoints:	4134	Total Number of Endpoints:	3103

All user specified timing constraints are met.

Power Estimation:



2 Dense Matrix-Matrix Multiplication [60 Points]

2.1 Scalable Multiply and adder tree

If A is an $m \times n$ matrix and B is an $n \times p$ matrix, the matrix product $C = AB$ (denoted without multiplication signs or dots) is defined to be the $m \times p$ matrix such that,

$$c_{i,j} = a_{i,1}b_{1,j} + a_{i,2}b_{2,j} + ... + a_{i,n}b_{n,j} = \sum_{k=1}^{n} a_{i,k}b_{k,j};$$

where for i = 1, ..., m and j = 1, ..., p

Consider two matrices A and B, each having the size of $n \times n$ where n = 2^r.

Figure 3 shows an example design of Multiply and Adder Tree. The adder tree consists of a Multiplication Step following Adder Steps. Given the size of matrices is $n \times n$, there are n multipliers in the first stage. Assume that matrix A saved in row order, and matrix B saved in column order in the memory. In the beginning, the first row of A and the first column of B loaded and multiplied together. Then in each Adder Step, partial sums are added together until it produces the final result corresponding to an element in the output matrix. Adder steps consist of 2 element adders as shown in Figure 2. Notice that Multiply and adder tree is a pipeline process. Notice that in each step, after corresponding rows and columns of A and B going through the pipe, it produces one element of the output matrix.

2.1.1 Design Problems

Consider simple Multiply and Adder Tree design with n element multiplication,

1. How many Multiply units needed for the entire design?

$$n$$

2. Consider an adder stage r, how many adder modules needed for that stage (Assume multiplication stage as stage 0)?

$$2^{\log n - r}$$

3. If all the inputs to the design represented using k bits, how many bits are needed to represent the final result of the Multiply and Adder Tree?

$$2k - 1 + \log n$$

4. How may Adder modules need for the entire multiply and adder tree design?

$$n - 1$$

5. How many clock cycles need to produce the first output element in the adder tree?

$$\log n + 1$$

6. How many clock cycles need to multiply two n×n matrices?

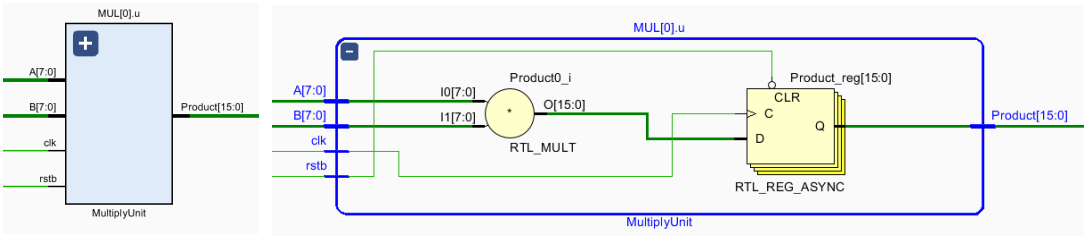
$$n^2 + \log n$$

2.1.2 Implementation

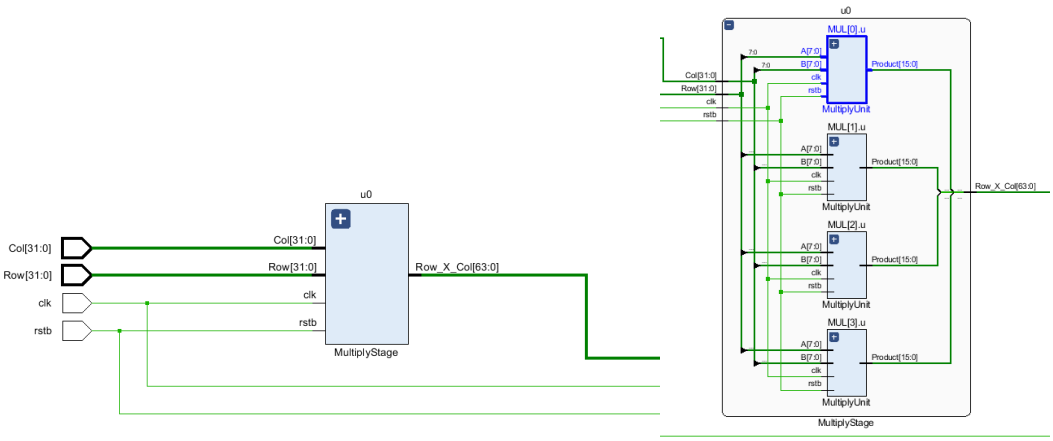
1. Write a testbench which provides two 4X4 matrices to the design and takes output final 4X4 resultant matrix.
2. Simulate the design using the simulator and include the waveform in the report (Clearly indicate the locations where final outputs produced)
3. Elaborate the design and include all the schematics' screenshots of the modules (MulandAddTree, adder, and multiply) in the report.
4. Synthesis the design and include the screenshots like part 3.
5. Generate Resource and timing estimations and include them in the report.

6. Generate power estimation reports and include them in the report.
7. How many of parallel *MulandAddTrees* can be implemented in this FPGA (Provide resource utilization reports with parallel *MulandAddTres*)?
8. Redo part 4,5,6 for 8x8, 16x16 and 32x32 matrices.

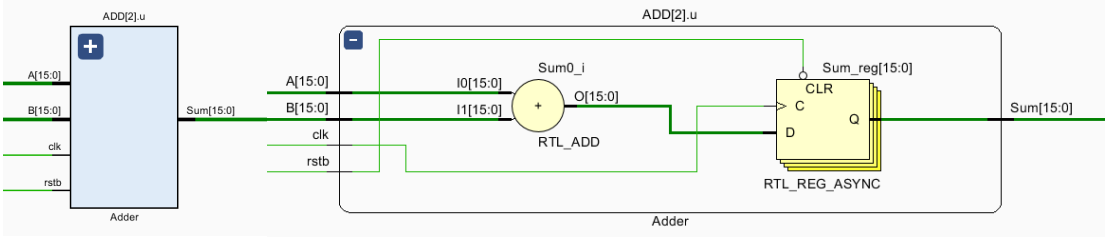
Schematics' screenshots are shown below:
MultiplyUnit is designed to get the product of two 8-bit number A and B.



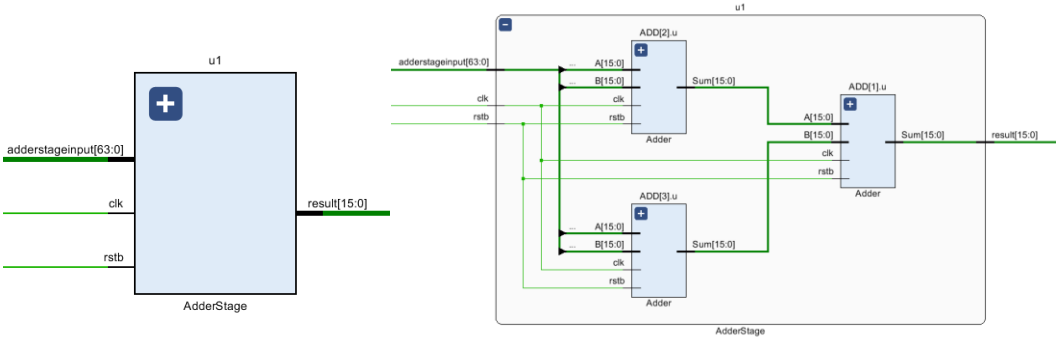
And according to the number of elements of matrix, combine all of the multiply units into **MultiplyStage**



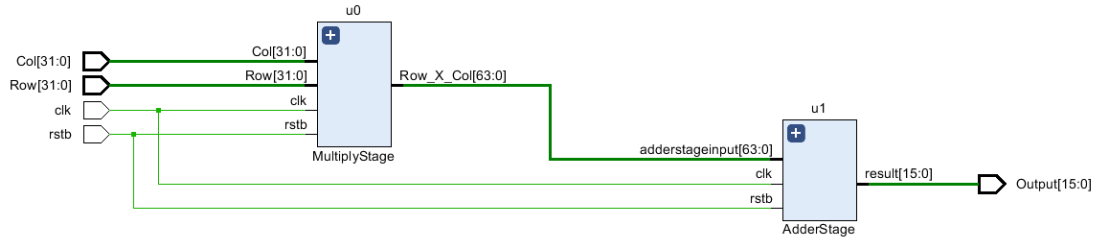
As for **Adder**, it computes the sum of two 16-bit numbers A and B.

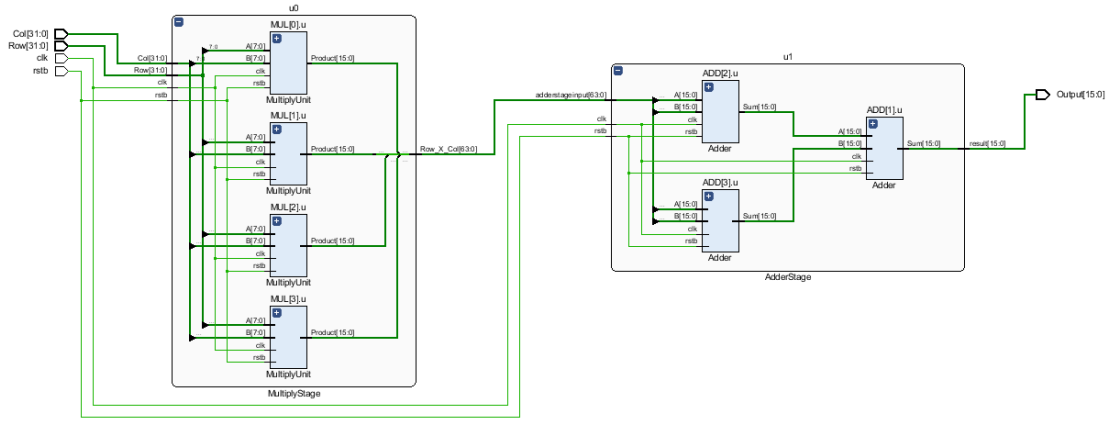


And $n-1$ **Adder**s make up the **AdderStage** module.



The Top Module, which is **MulandAddTree** consist of **MultiplyStage** and **AdderStage**.





// matrix1:

// 1 2 3 4

// 2 3 4 5

// 3 4 5 6

// 4 5 6 7

// matrix2:

// 1 0 0 0

// 0 1 0 0

// 0 0 1 0

// 0 0 0 1

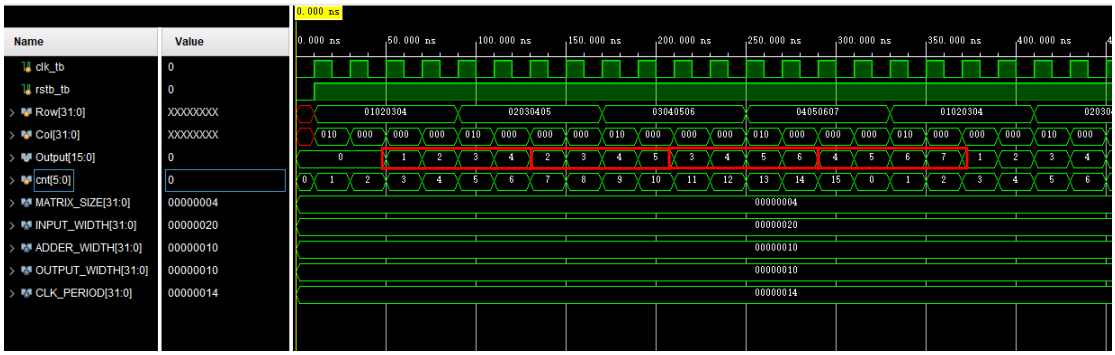
Result:

1 2 3 4

2 3 4 5

3 4 5 6

4 5 6 7



// matrix3:

// 1 2 3 4

// 2 3 4 5

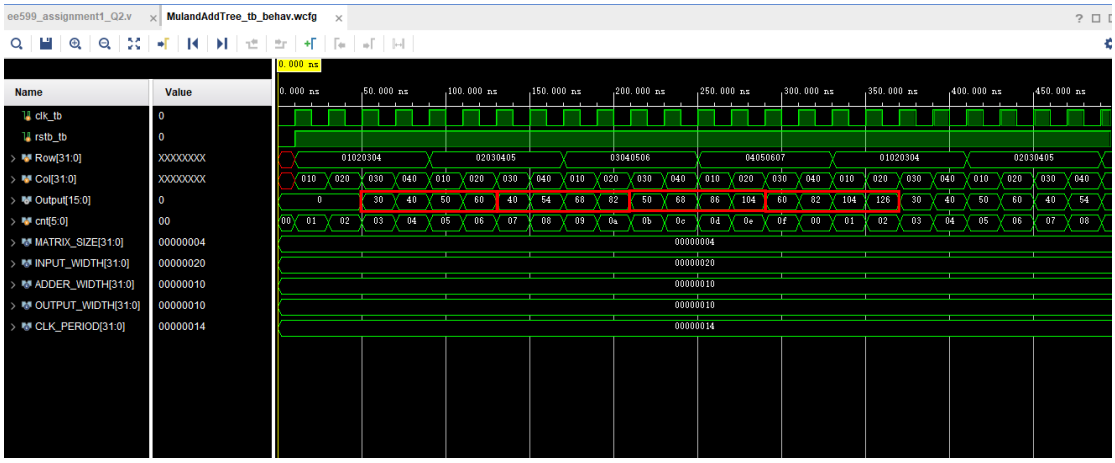
Result:

30 40 50 60

40 54 68 82

// 3 4 5 6 50 68 86 104
// 4 5 6 7 60 82 104 126

// matrix4:
// 1 2 3 4
// 2 3 4 5
// 3 4 5 6
// 4 5 6 7



The synthesis schematic please see in the Appendix.

Resource Estimation for 4x4 size:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	293	0	14400	2.03
LUT as Logic	293	0	14400	2.03
LUT as Memory	0	0	6000	0.00
Slice Registers	112	0	28800	0.39
Register as Flip Flop	112	0	28800	0.39
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
112	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic avail

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	82	0	54	151.85
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	144	LUT
FDCE	112	Flop & Latch
LUT6	104	LUT
LUT4	100	LUT
IBUF	66	IO
CARRY4	64	CarryLogic
LUT5	24	LUT
LUT3	24	LUT
OBUF	16	IO
LUT1	1	LUT
BUFG	1	Clock

8. Black Boxes

Ref Name	Used

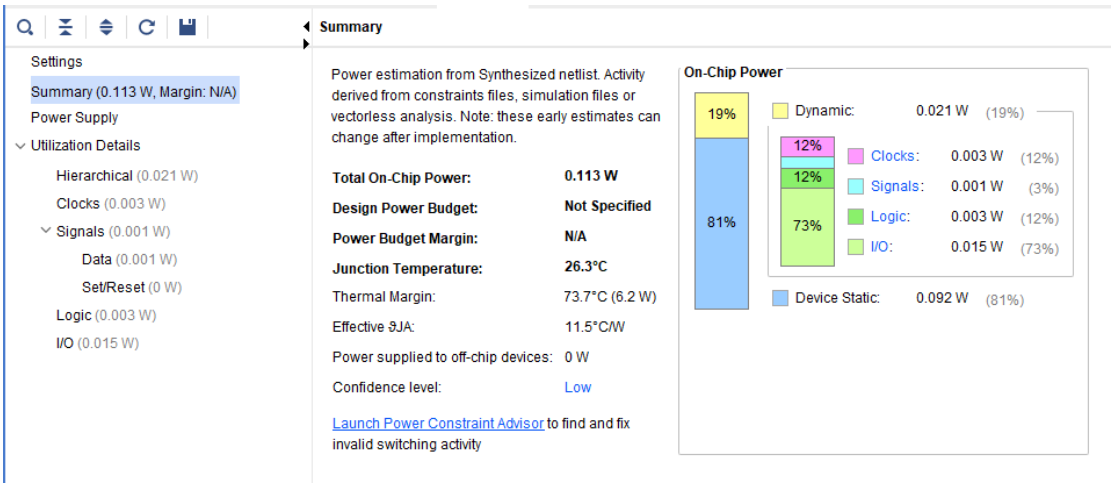
9. Instantiated Netlists

Ref Name	Used

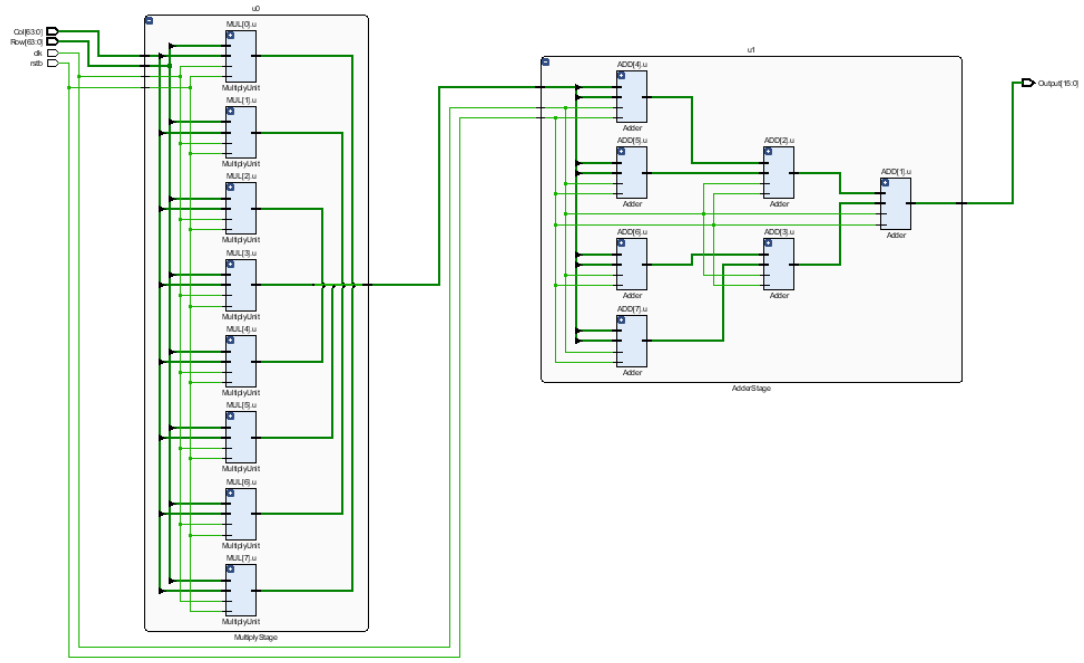
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.965 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	48	Total Number of Endpoints:	48	Total Number of Endpoints:	113

All user specified timing constraints are met.



Now redo for 8x8 size.



The full synthesis schematic please see in the Appendix.

Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	601	0	14400	4.17
LUT as Logic	601	0	14400	4.17
LUT as Memory	0	0	6000	0.00
Slice Registers	240	0	28800	0.83
Register as Flip Flop	240	0	28800	0.83
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
240	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic availab

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	146	0	54	270.37
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	304	LUT
FDCE	240	Flop & Latch
LUT6	208	LUT
LUT4	200	LUT
CARRY4	132	CarryLogic
IBUF	130	IO
LUT5	48	LUT
LUT3	48	LUT
OBUF	16	IO
LUT1	1	LUT
BUFG	1	Clock

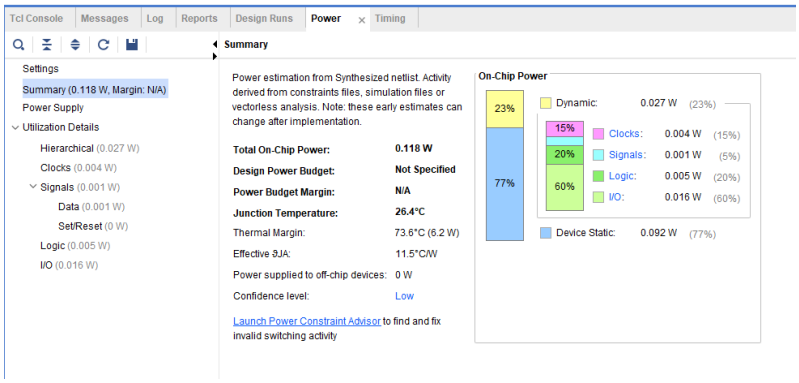
Timing Estimation:

Design Timing Summary

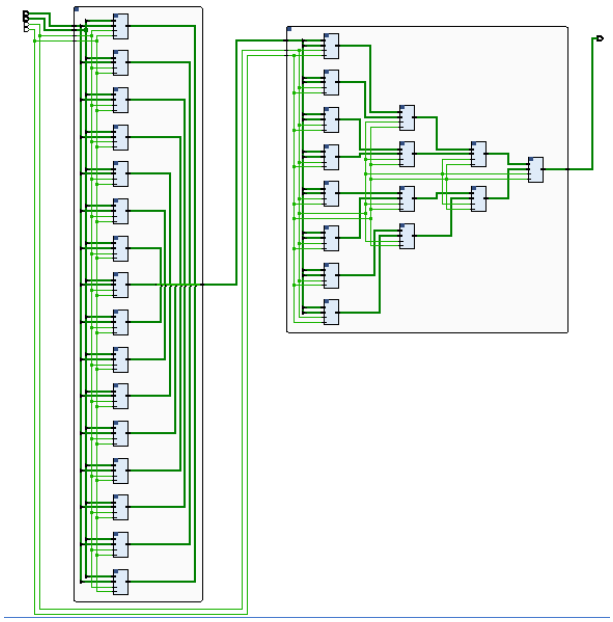
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.965 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	112	Total Number of Endpoints:	112	Total Number of Endpoints:	241

All user specified timing constraints are met.

Power Estimation:



Now redo for 16x16 size.



The full synthesis schematic please see in the Appendix.

Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1217	0	14400	8.45
LUT as Logic	1217	0	14400	8.45
LUT as Memory	0	0	6000	0.00
Slice Registers	496	0	28800	1.72
Register as Flip Flop	496	0	28800	1.72
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
496	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	274	0	54	507.41
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	624	LUT
FDCE	496	Flop & Latch
LUT6	416	LUT
LUT4	400	LUT
CARRY4	268	CarryLogic
IBUF	258	IO
LUT5	96	LUT
LUT3	96	LUT
OBUF	16	IO
LUT1	1	LUT
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.965 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	240	Total Number of Endpoints:	240	Total Number of Endpoints:	497

All user specified timing constraints are met.

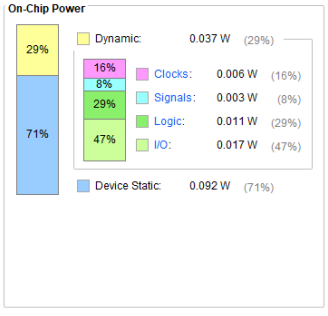
Power Estimation:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.128 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.5°C**
Thermal Margin:	73.5°C (6.2 W)
Effective ΘJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Now redo for 32x32 size.

The full synthesis schematic please see in the Appendix.

Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2449	0	14400	17.01
LUT as Logic	2449	0	14400	17.01
LUT as Memory	0	0	6000	0.00
Slice Registers	1008	0	28800	3.50
Register as Flip Flop	1008	0	28800	3.50
Register as Latch	0	0	28800	0.00
F7 Muxes	0	0	8800	0.00
F8 Muxes	0	0	4400	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
1008	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	66	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	530	0	54	981.48
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	54	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	54	0.00
OLOGIC	0	0	54	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	1264	LUT
FDCE	1008	Flop & Latch
LUT6	832	LUT
LUT4	800	LUT
CARRY4	540	CarryLogic
IBUF	514	IO
LUT5	192	LUT
LUT3	192	LUT
OBUF	16	IO
LUT1	1	LUT
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.965 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	496	Total Number of Endpoints:	496	Total Number of Endpoints:	1009

All user specified timing constraints are met.

Power Estimation: