

EE 599 Spring 2020

Homework2

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2020/04/02

Github URL: https://github.com/JianqiZhang/EE599_Jianqi-Zhang_1052509893

1 Barrel Shifter [50 Points]

A Barrel Shifter is a logic circuit for shifting a word by a varying amount. It has a control input (select bits) that specifies the number of bit positions that it shifts. A Barrel Shifter is implemented with a sequence of shift multiplexers, each shifting a word by 2^k bit positions for different values of k . The diagram below (Figure 1) shows a pipeline clock-wise barrel shifter for 8 inputs.

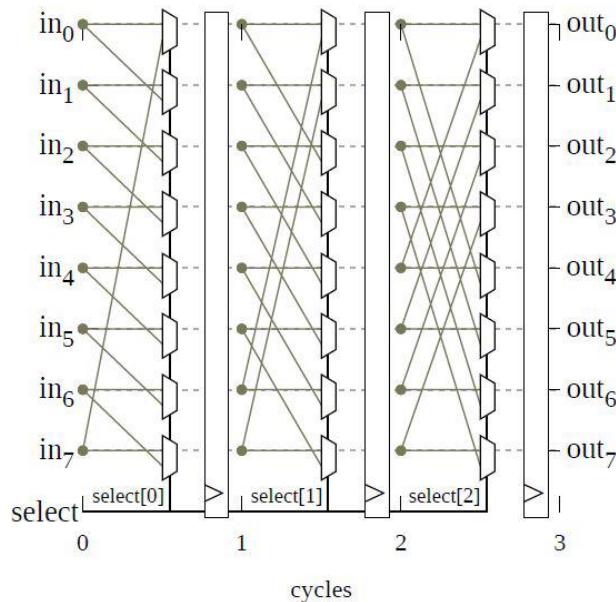


Figure 1: An Example Pipeline Barrel Shifter

Notice that we can shift the input elements by 0 - 7 elements using an implementation like Figure 1. Table 1 shows all the shifting possibilities for the above example. Similarly, a scalable Barrel Shifter with N inputs and maximum shift of $N-1$ can be implemented.

Table 1: All the shifting possibilities for the given example

Select[2]	Select[1]	Select[0]	Shift
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

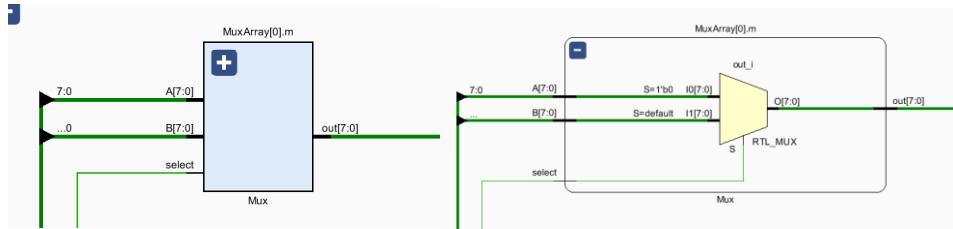
- Implementation: Using Xilinx Vivado Software (Use Zynq-7000 xc7z007 sclg225-2 FPGA)

Consider only 8-bit arithmetic. You must implement a scalable design.

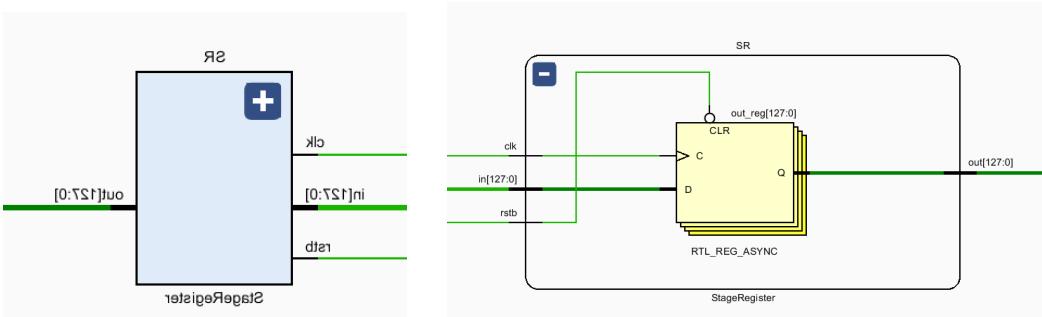
1. Implement a barrel shifter design in Verilog which takes n inputs with 8 bits and shift them by r (value of r is passed to select bits and $r_{max} = (n - 1)$).
2. For a 16 elements design with a maximum shift of 15, write a testbench and verify the waveforms.
3. Elaborate the design and include all the schematics screenshots of the modules in the report.
4. Synthesis the design and include the schematics screenshots in the report.
5. Generate Resource and timing estimations and include them in the report.
6. Redo parts 3, 4, 5 for 64 elements (with maximum shift of 63).

Schematics' screenshots are shown below:

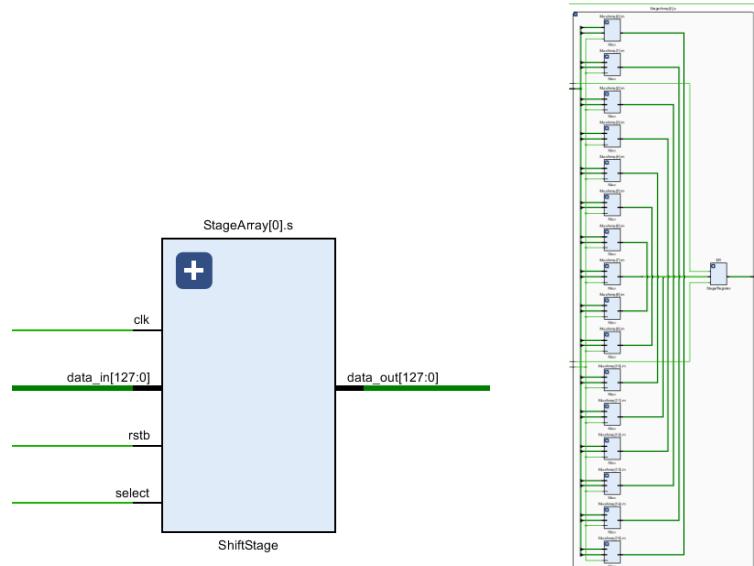
- a. **2 Inputs Mux** is designed to select one 8 bits-input to output by the control signal.



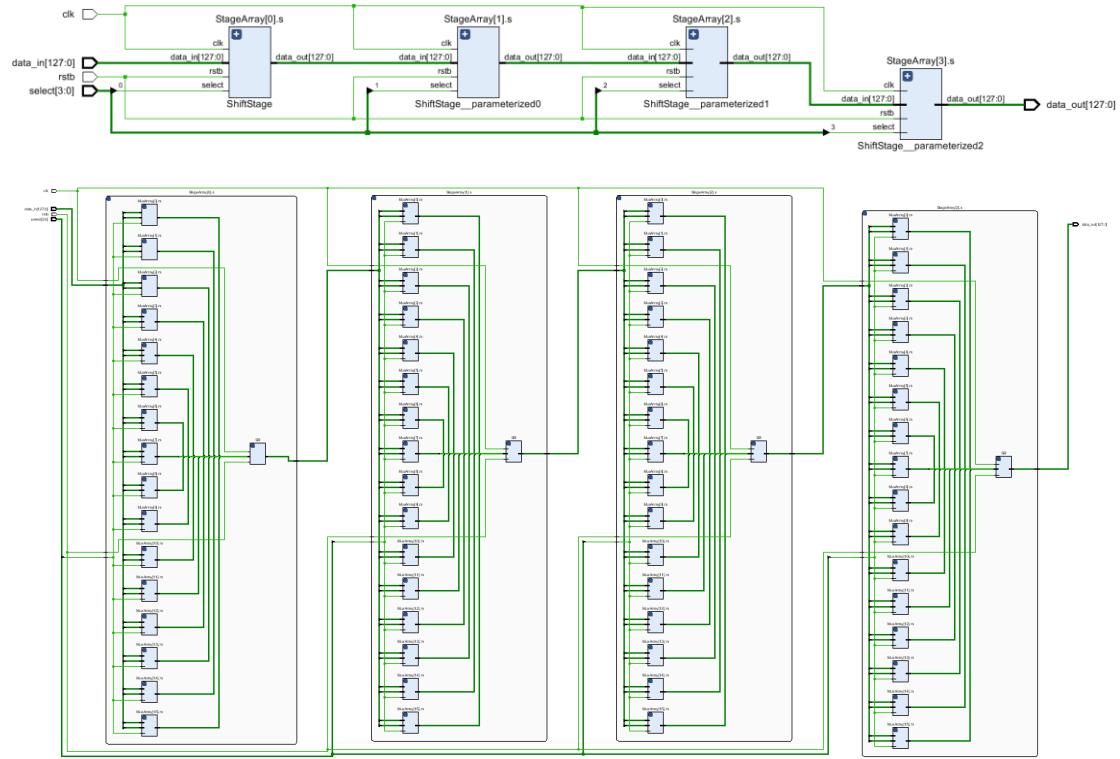
- b. **Stage Register** is acted as D Filp-Flop. In every stage, all 16 elements will go through the stage register to next stage so that build a pipeline architecture.



- c. **StageArray** contains 16 Muxes and 1 stage register.

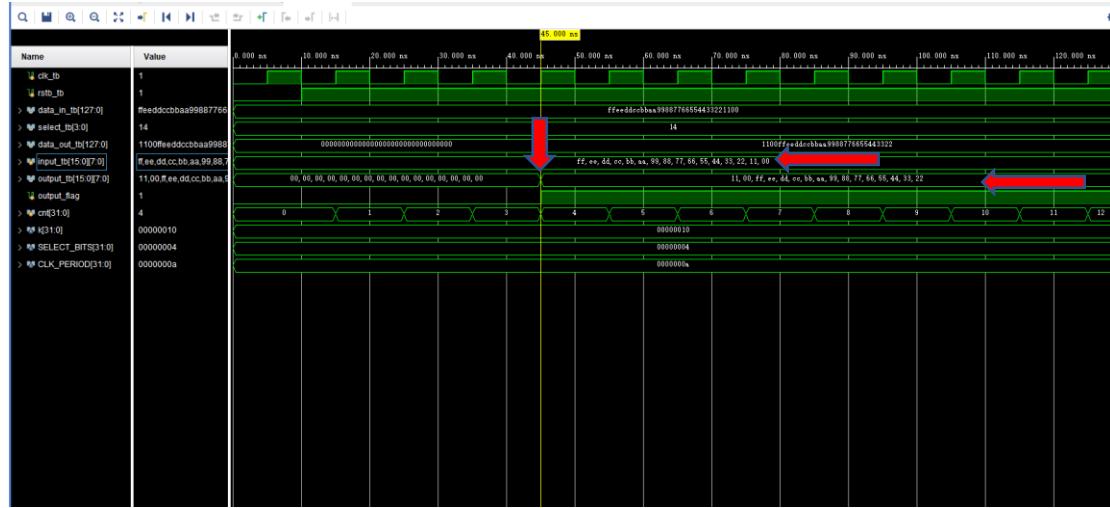


- d. **BarrelShifter** is the top module of the design. For 16 elements barrel shifter, we need 4 stages connected end to end.



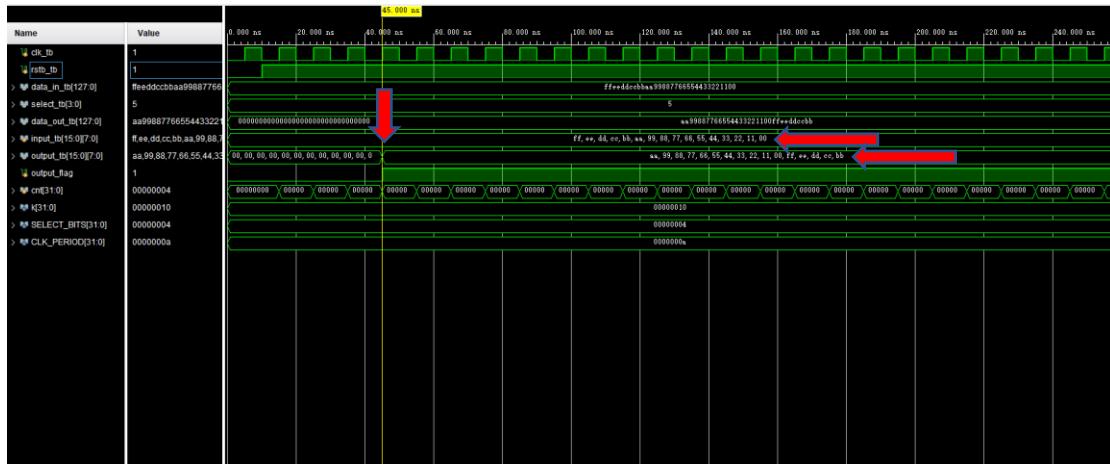
The total schematic is shown in the Appendix.

For a 16 elements test bench, we give 16 8-bit numbers as input, and after $2 \times 16 = 32$ clocks, the module will output sorted results. The waveform is shown as followed:



We can see input_tb includes 16 8-bit numbers, after 4 clocks, output_tb gives the number array which shift by 14.

Then, we change the number of shifting.



We can see input_tb includes 16 8-bit numbers, after 4 clocks, output_tb gives the number array which shift by 5.

The full synthesis schematic please see in the Appendix.

Resource Estimations:

```

1 Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
2
3 | Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec 5 04:49:17 MST 2019
4 | Date       : Thu Apr 2 20:45:41 2020
5 | Host       : DESKTOP-06TLUJM running 64-bit major release (build 9200)
6 | Command    : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb
7 | Design     : BarrelShifter
8 | Device     : 7z007sclg225-2
9 | Design State: Synthesized
10
11 Utilization Design Information
12
13 Table of Contents
14
15 1. Slice Logic
16 1.1 Summary of Registers by Type
17 2. Memory
18 3. DSP
19 4. IO and GT Specific
20 5. Clocking
21 6. Specific Feature
22 7. Primitives
23 8. Black Boxes
24 9. Instantiated Netlists
25
26
27 1. Slice Logic
28
29
30 +-----+-----+-----+-----+
31 | Site Type | Used | Fixed | Available | Util% |
32 +-----+-----+-----+-----+
33 | Slice LUTs* | 257 | 0 | 14400 | 1.78 |
34 | LUT as Logic | 257 | 0 | 14400 | 1.78 |
35 | LUT as Memory | 0 | 0 | 6000 | 0.00 |
36 | Slice Registers | 512 | 0 | 28800 | 1.78 |
37 | Register as Flip Flop | 512 | 0 | 28800 | 1.78 |
38 | Register as Latch | 0 | 0 | 28800 | 0.00 |
39 | F7 Muxes | 0 | 0 | 8800 | 0.00 |
40 | F8 Muxes | 0 | 0 | 4400 | 0.00 |
41 +-----+-----+-----+-----+
42 * Warning! The Final LUT count, after physical optimizations and full implementation.
43
44
45 1.1 Summary of Registers by Type
46
47
48 +-----+-----+-----+-----+
49 | Total | Clock Enable | Synchronous | Asynchronous |
50 +-----+-----+-----+-----+
51 | 0 | - | - | - |
52 | 0 | - | - | Set |
53 | 0 | - | - | Reset |
54 | 0 | - | Set | - |
55 | 0 | - | Reset | - |
56 | 0 | Yes | - | - |
57 | 0 | Yes | - | Set |
58 | 512 | Yes | - | Reset |
59 | 0 | Yes | Set | - |
60 | 0 | Yes | Reset | - |
61 +-----+-----+-----+-----+

```

64	2. Memory
<hr/>	
65	
66	+-----+-----+-----+-----+-----+
67	Site Type Used Fixed Available Util%
68	+-----+-----+-----+-----+-----+
69	Block RAM Tile 0 0 50 0.00
70	RAMB36/FIFO* 0 0 50 0.00
71	RAMB18 0 0 100 0.00
72	+-----+-----+-----+-----+-----+
73	* Note: Each Block RAM Tile only has one FIFO logic available and
74	75
76	3. DSP
77	<hr/>
78	+-----+-----+-----+-----+-----+
79	Site Type Used Fixed Available Util%
80	+-----+-----+-----+-----+-----+
81	DSPs 0 0 66 0.00
82	+-----+-----+-----+-----+-----+
83	84
85	+-----+-----+-----+-----+-----+
86	87
87	4. IO and GT Specific
88	<hr/>
89	+-----+-----+-----+-----+-----+
90	Site Type Used Fixed Available Util%
91	+-----+-----+-----+-----+-----+
92	Bonded IOB 262 0 54 485.19
93	Bonded IPADs 0 0 2 0.00
94	Bonded IOPADs 0 0 130 0.00
95	PHY_CONTROL 0 0 2 0.00
96	PHASER_REF 0 0 2 0.00
97	OUT_FIFO 0 0 8 0.00
98	IN_FIFO 0 0 8 0.00
99	IDELAYCTRL 0 0 2 0.00
100	IBUFDS 0 0 54 0.00
101	PHASER_OUT/PHASER_OUT_PHY 0 0 8 0.00
102	PHASER_IN/PHASER_IN_PHY 0 0 8 0.00
103	IDELAY2/IDELAY2_FINEDELAY 0 0 100 0.00
104	ILOGIC 0 0 54 0.00
105	OLOGIC 0 0 54 0.00
106	+-----+-----+-----+-----+-----+
107	107
108	110
110	5. Clocking
111	<hr/>
112	+-----+-----+-----+-----+-----+
113	Site Type Used Fixed Available Util%
114	+-----+-----+-----+-----+-----+
115	BUFGCTRL 1 0 32 3.13
116	BUFI0 0 0 8 0.00
117	MMCME2_ADV 0 0 2 0.00
118	PLL2_ADV 0 0 2 0.00
119	BUFMRC 0 0 4 0.00
120	BUFPDCE 0 0 48 0.00
121	BUFPDCE 0 0 8 0.00
122	+-----+-----+-----+-----+-----+
123	123
124	126
126	6. Specific Feature
127	<hr/>
128	+-----+-----+-----+-----+-----+
129	Site Type Used Fixed Available Util%
130	+-----+-----+-----+-----+-----+
131	BSCANE2 0 0 4 0.00
132	CAPTUREE2 0 0 1 0.00
133	DNA_PORT 0 0 1 0.00
134	EFUSE_USR 0 0 1 0.00
135	FRAME_ECC 0 0 1 0.00
136	ICAPPE2 0 0 2 0.00
137	STARTUP2 0 0 1 0.00
138	XADC 0 0 1 0.00
139	+-----+-----+-----+-----+-----+
140	140
141	143
143	7. Primitives
144	<hr/>
145	+-----+-----+-----+
146	Ref Name Used Functional Category
147	+-----+-----+-----+
148	LUT3 512 LUT
149	FDCE 512 Flop & Latch
150	IBUF 134 IO
151	OBUF 128 IO
152	LUT1 1 LUT
153	BUFPG 1 Clock
154	+-----+-----+-----+
155	155

Timing Estimation:

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.609 ns	Worst Hold Slack (WHS): 0.127 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWNS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 384	Total Number of Endpoints: 384	Total Number of Endpoints: 513

All user specified timing constraints are met.

Power Estimation:

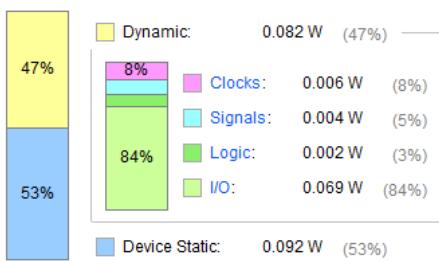
◀ Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

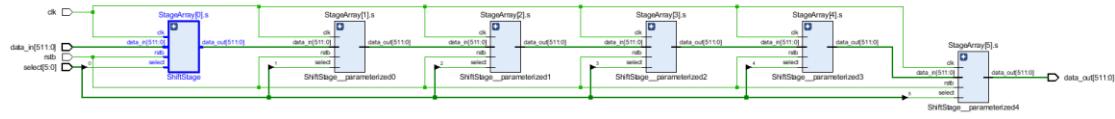
Total On-Chip Power:	0.174 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	27.0°C
Thermal Margin:	73.0°C (6.1 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

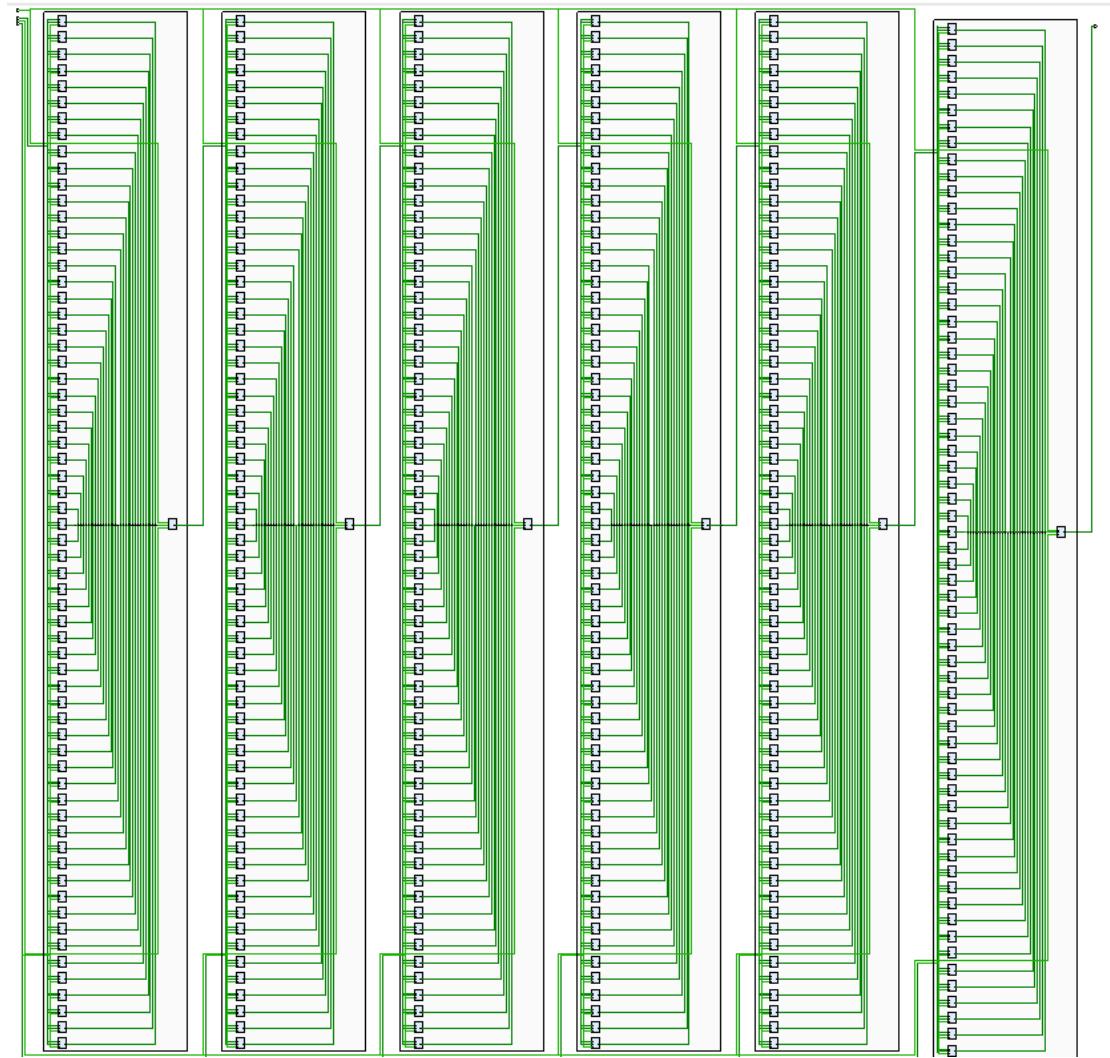
[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power



Now redo for 64 inputs.





The full synthesis schematic please see in the Appendix.

Resource Estimation:

```

1 Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
2
3 | Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec 5 04:49:17 MST 2019
4 | Date       : Thu Apr 2 21:06:07 2020
5 | Host       : DESKTOP-06TLU5M running 64-bit major release (build 9200)
6 | Command    : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb
7 | Design     : BarrelShifter
8 | Device     : 7z007sc1g225-2
9 | Design State : Synthesized
10
11
12 Utilization Design Information
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14 Table of Contents
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16 1. Slice Logic
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18 2. Memory
19 3. DSP
20 4. IO and GT Specific
21 5. Clocking
22 6. Specific Feature
23 7. Primitives
24 8. Black Boxes
25 9. Instantiated Netlists
26
27 1. Slice Logic
28
29
30 +-----+-----+-----+-----+
31 | Site Type | Used | Fixed | Available | Util% |
32 +-----+-----+-----+-----+
33 | Slice LUTs* | 1537 | 0 | 14400 | 10.67 |
34 | LUT as Logic | 1537 | 0 | 14400 | 10.67 |
35 | LUT as Memory | 0 | 0 | 6000 | 0.00 |
36 | Slice Registers | 3072 | 0 | 28800 | 10.67 |
37 | Register as Flip Flop | 3072 | 0 | 28800 | 10.67 |
38 | Register as Latch | 0 | 0 | 28800 | 0.00 |
39 | F7 Muxes | 0 | 0 | 8800 | 0.00 |
40 | F8 Muxes | 0 | 0 | 4400 | 0.00 |
41 +-----+-----+-----+-----+
42 * Warning! The Final LUT count, after physical optimizations and
43
44
45 1.1 Summary of Registers by Type
46
47
48 +-----+-----+-----+-----+
49 | Total | Clock Enable | Synchronous | Asynchronous |
50 +-----+-----+-----+-----+
51 | 0 | - | - | - |
52 | 0 | - | - | Set |
53 | 0 | - | - | Reset |
54 | 0 | - | Set | - |
55 | 0 | - | Reset | - |
56 | 0 | Yes | - | - |
57 | 0 | Yes | - | Set |
58 | 3072 | Yes | - | Reset |
59 | 0 | Yes | Set | - |
60 | 0 | Yes | Reset | - |
61 +-----+-----+-----+-----+
62
63
64 2. Memory
65
66
67 +-----+-----+-----+-----+
68 | Site Type | Used | Fixed | Available | Util% |
69 +-----+-----+-----+-----+
70 | Block RAM Tile | 0 | 0 | 50 | 0.00 |
71 | RAMB36/FIFO* | 0 | 0 | 50 | 0.00 |
72 | RAMB18 | 0 | 0 | 100 | 0.00 |
73 +-----+-----+-----+-----+
74 * Note: Each Block RAM Tile only has one FIFO logic avail
75
76
77 3. DSP
78
79
80 +-----+-----+-----+-----+
81 | Site Type | Used | Fixed | Available | Util% |
82 +-----+-----+-----+-----+
83 | DSPs | 0 | 0 | 66 | 0.00 |
84 +-----+-----+-----+-----+
85
86
87 4. IO and GT Specific
88
89
90 +-----+-----+-----+-----+
91 | Site Type | Used | Fixed | Available | Util% |
92 +-----+-----+-----+-----+
93 | Bonded IOB | 1032 | 0 | 54 | 1911.11 |
94 | Bonded IPADs | 0 | 0 | 2 | 0.00 |
95 | Bonded IOPADs | 0 | 0 | 130 | 0.00 |
96 | PHY_CONTROL | 0 | 0 | 2 | 0.00 |
97 | PHASER_REF | 0 | 0 | 2 | 0.00 |
98 | OUT_FIFO | 0 | 0 | 8 | 0.00 |
99 | IN_FIFO | 0 | 0 | 8 | 0.00 |
100 | IDELAYCTRL | 0 | 0 | 2 | 0.00 |
101 | IBUFDS | 0 | 0 | 54 | 0.00 |
102 | PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 8 | 0.00 |
103 | PHASER_IN/PHASER_IN_PHY | 0 | 0 | 8 | 0.00 |
104 | IDELAY2/IDELAY2_FINEDELAY | 0 | 0 | 100 | 0.00 |
105 | ILOGIC | 0 | 0 | 54 | 0.00 |
106 | OLOGIC | 0 | 0 | 54 | 0.00 |
107 +-----+-----+-----+-----+

```

5. Clocking						6. Specific Feature					
<hr/>						<hr/>					
<hr/>						<hr/>					
Site Type	Used	Fixed	Available	Util%		Site Type	Used	Fixed	Available	Util%	
BUFGCTRL	1	0	32	3.13		BSCANE2	0	0	4	0.00	
BUFIO	0	0	8	0.00		CAPTUREE2	0	0	1	0.00	
MMCME2_ADV	0	0	2	0.00		DNA_PORT	0	0	1	0.00	
PLLE2_ADV	0	0	2	0.00		EFUSE_USR	0	0	1	0.00	
BUFMRCE	0	0	4	0.00		FRAME_ECC2	0	0	1	0.00	
BUFHCE	0	0	48	0.00		ICAPE2	0	0	2	0.00	
BUFR	0	0	8	0.00		STARTUPE2	0	0	1	0.00	
						XADC	0	0	1	0.00	

7. Primitives		
<hr/>		
<hr/>		
Ref Name Used Functional Category		
<hr/>		
LUT3	3072	LUT
FDCE	3072	Flop & Latch
IBUF	520	IO
OBUF	512	IO
LUT1	1	LUT
BUFG	1	Clock

Timing Estimation:

Design Timing Summary			
Setup		Hold	
Worst Negative Slack (WNS):	8.609 ns	Worst Hold Slack (WHS):	0.188 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2560	Total Number of Endpoints:	2560
All user specified timing constraints are met.			

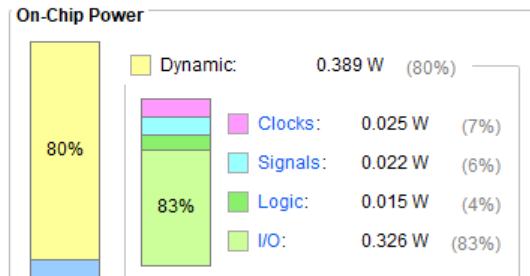
Power Estimation:

Summary

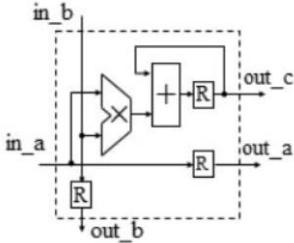
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.485 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 30.6°C
 Thermal Margin: 69.4°C (5.8 W)
 Effective θJA: 11.5°C/W
 Power supplied to off-chip devices: 0 W
 Confidence level: Low

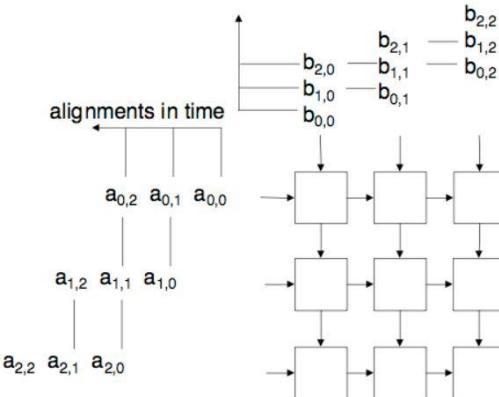
[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



2 Systolic Array for Dense Matrix-Matrix Multiplication [50 Points]



Internals of the PE



Example 3×3 Systolic Array

The Systolic Architecture consists of an array of processing elements, where data flows between neighboring elements, synchronously, from different directions. Processing element takes data from Top, Left, and output the results to Right, Bottom.

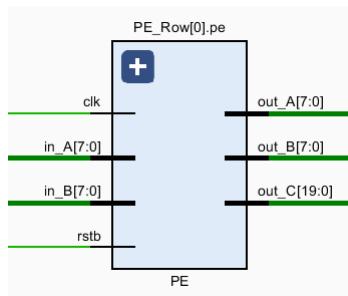
One of the main applications of Systolic Architecture is matrix multiplication. As the following figure depicts, in *a*, *in_b* are inputs to the processing element and *out_a*, *out_b* bare output to the processing element. *out_c* is to get the output result of each processing element.

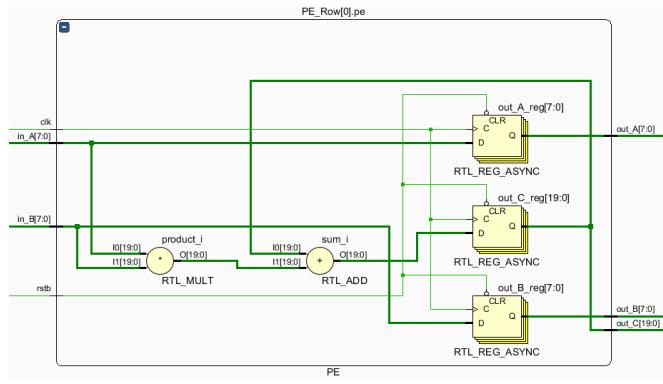
Processing elements are arranged in the form of an array. In the following example, we analyze, multiplication of 3×3 matrices, which can be easily extended. Let say the two matrices are *A* and *B*. Figure above depicts how matrix *A* and *B* are fed into PE array.

2.1 Implementation

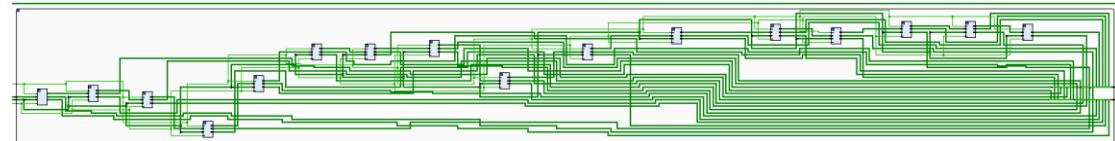
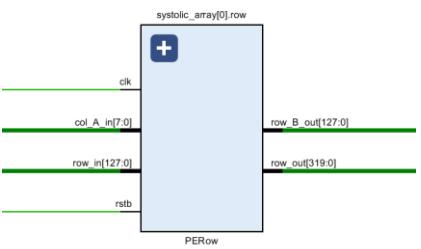
Schematics' screenshots are shown below:

PE is designed to calculate the product of two 8 bits-input *A* and *B*, and accumulate all the products produced by own. Also, each PE will also transfer the two inputs to the next every clock. So there are a multiplier, an adder and three output register.

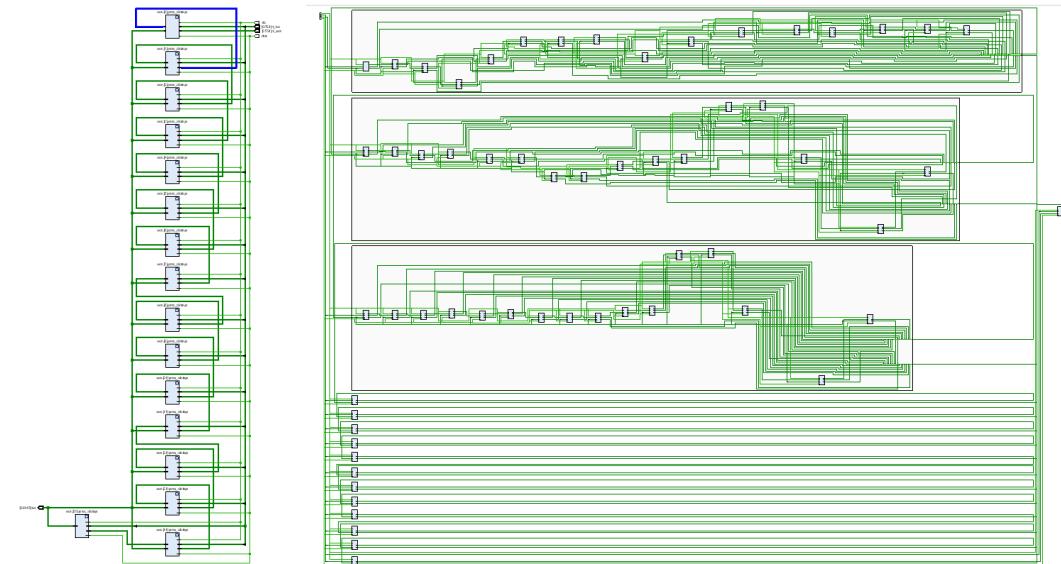




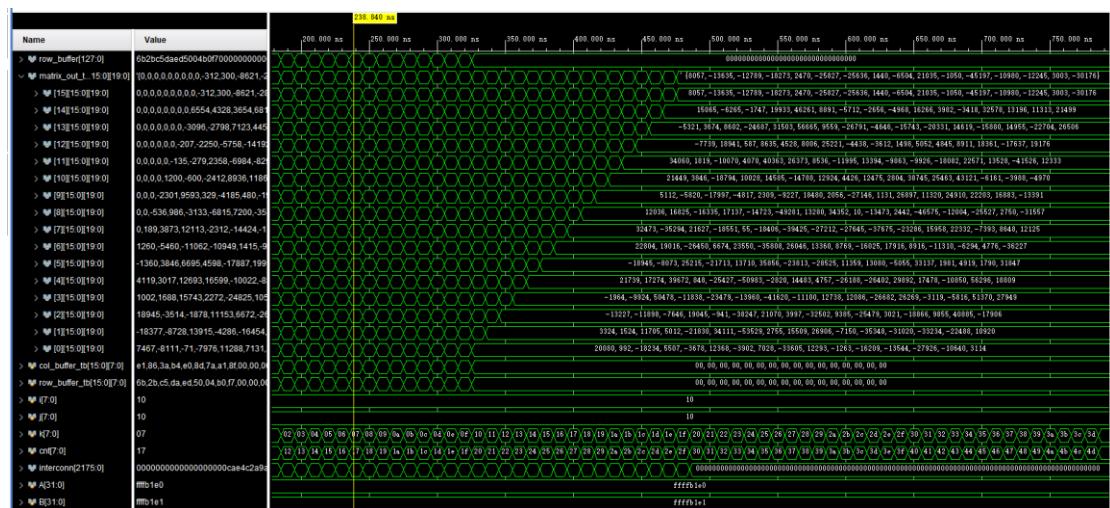
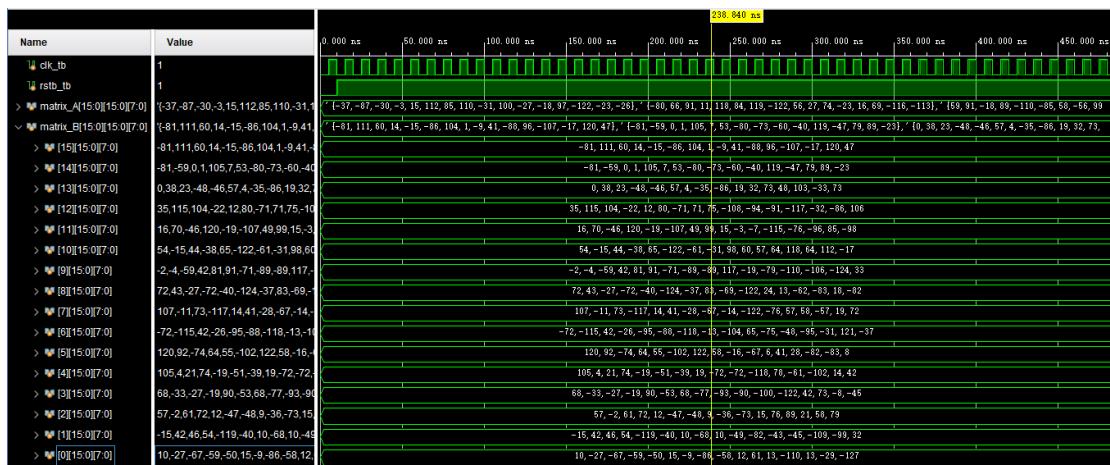
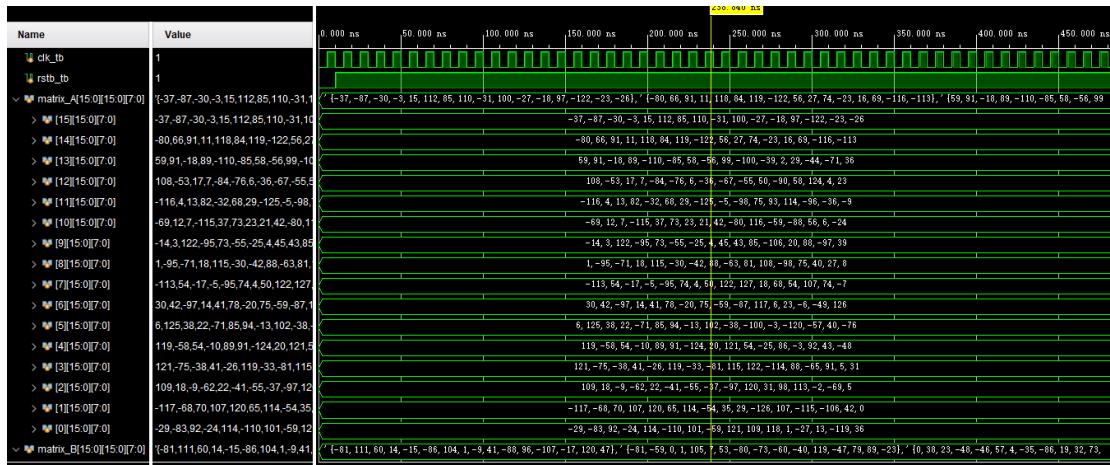
PERow is designed to build a row of systolic array. For a systolic array of $n \times n$ size, PERow contains n PEs.

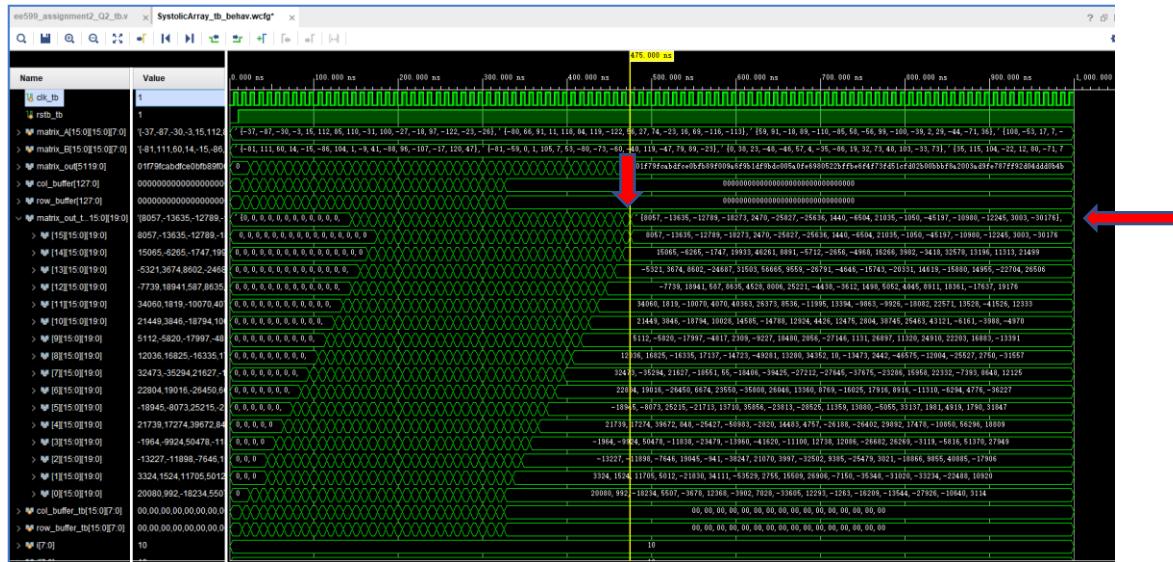
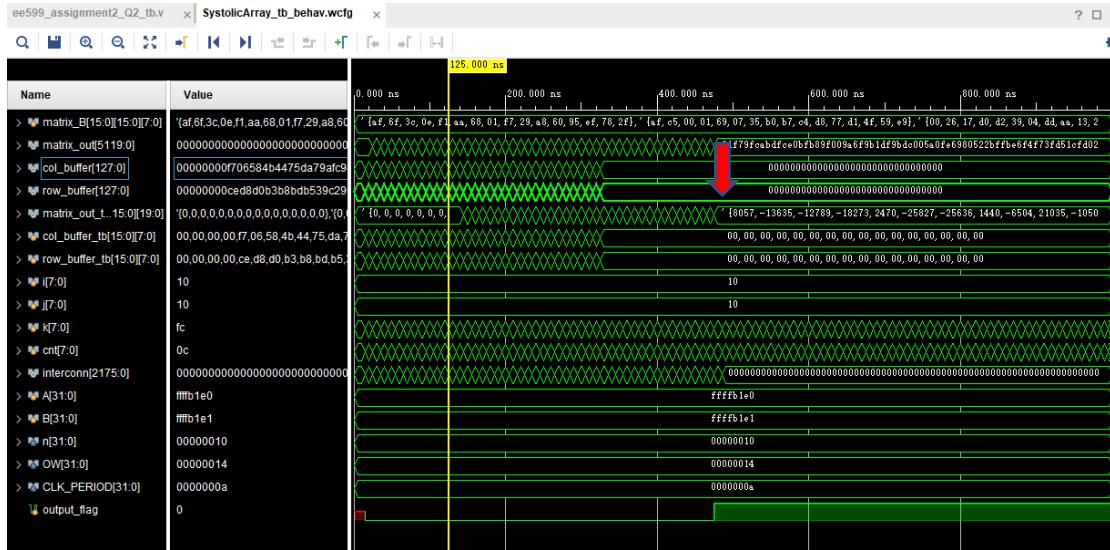


The Top Module, which is **SystolicArray** consist of n PERows.



For a 16×16 size systolic array test bench, we give two 16×16 size matrices as input, and after $3 \times n - 1 = 47$ clocks, the module will output results. The waveform is shown as followed:





Here, we generate the two matrices by random. Using Verilog system function, we can easily generate the data and store them into two files Matrix_A.txt and Matrix_B.txt.

```

initial
begin : MATRIX_GENERATOR
    A = $fopen("../..../..../Matrix_A.txt", "w");
    B = $fopen("../..../..../Matrix_B.txt", "w");
    for (i = 0; i < n; i = i + 1)
        begin
            for (j = 0; j < n; j = j + 1)
                begin
                    matrix_A[i][j] = $random % 128;
                    matrix_B[i][j] = $random % 128;
                    col_buffer_tb[i] = 0;
                    row_buffer_tb[i] = 0;
                    $fwrite(A, "%d ", matrix_A[i][j]);
                    $fwrite(B, "%d ", matrix_B[i][j]);
                end
            $fwrite(A, "\n");$fwrite(B, "\n");
        end
    $fclose(A);
    $fclose(B);
end

```

	lalp2script2.py[3]	VB_data.csv[3]	InstructionFetch.py[3]	es699_assignment2_Q2.vi[3]	es699_assignment2_Q2_tb.vi[3]	Matrix_A.txt	Matrix_B.txt
1	36 -119 13 -27	1 118 109 121	-59 101 -110 114	-24 92 -83 -29			
2	0 42 -106 -115	107 -126 29 35	-54 114 65 120	107 70 -68 -117			
3	5 -69 -2 113	98 31 120 -97	-37 -55 -41 22	-62 -9 18 109			
4	31 5 91 -65	88 -114 122 115	-81 -33 119 -26	41 -38 -75 121			
5	-48 43 92 -3	86 -25 54 121	20 -124 91 89	-10 54 -58 119			
6	-76 40 -57 -120	-3 -100 -38 102	-13 94 85 -71	22 38 125 6			
7	126 -49 -6 23	6 117 -87 -59	75 -20 78 41	14 -97 42 30			
8	-7 74 107 54	68 18 127 122	50 4 74 -95	-5 -17 54 -113			
9	8 27 40 75	-98 108 81 -63	88 -42 -30 115	18 -71 -95 1			
10	39 -97 88 20	-106 85 43 45	4 -25 -55 73	-95 122 3 -14			
11	-24 6 56 -88	-59 116 -80 42	21 23 73 37	-115 7 12 -69			
12	-9 -36 -96 114	93 75 -98 -5	-125 29 68 -32	82 13 4 -116			
13	23 4 124 58	-90 50 -55 -67	-36 6 -76 -84	7 17 -53 108			
14	36 -71 -44 29	2 -39 -100 99	-56 58 -85 -110	89 -18 91 59			
15	-113 -116 69 16	-23 74 27 56	-122 119 84 118	11 91 66 -80			
16	-26 -23 -122 97	-18 -27 100 -31	110 85 112 15	-3 -30 -87 -37			
17							

Matrix_A.txt

	lalp2script2.py[3]	VB_data.csv[3]	InstructionFetch.py[3]	es699_assignment2_Q2.vi[3]	es699_assignment2_Q2_tb.vi[3]	Matrix_A.txt	Matrix_B.txt
1	-127 -29 13 -110	13 61 12 -58	-86 -9 15 -50	-59 -67 -27 10			
2	32 -99 -109 -45	-43 -82 -49 10	-68 10 -40 -119	54 46 42 -15			
3	79 58 21 89	76 15 -73 -36	9 -48 -47 12	72 61 -2 57			
4	-45 -8 73 42	-122 -100 -90 -93	-77 68 -53 90	-19 -27 -33 68			
5	42 14 -102 -61	78 -118 -72 -72	19 -39 -51 -19	74 21 4 105			
6	8 -83 -82 28	41 6 -67 -16	58 122 -102 55	64 -74 92 120			
7	-37 121 -31 -95	-48 -75 65 -104	-13 -118 -88 -95	-26 42 -115 -72			
8	72 19 -57 58	57 -76 -122 -14	-67 -28 41 14	-117 73 -11 107			
9	-82 18 -83 -62	13 24 -122 -69	83 -37 -124 -40	-72 -27 43 72			
10	33 -124 -106 -110	-79 -19 117 -89	-89 -71 91 81	42 -59 -4 -2			
11	-17 112 64 118	64 57 60 98	-31 -61 -122 65	-38 44 -15 54			
12	-98 85 -96 -76	-115 -7 -3 15	99 49 -107 -19	120 -46 70 16			
13	106 -86 -32 -117	-91 -94 -108 75	71 -71 80 12	-22 104 115 35			
14	73 -33 103 48	73 32 19 -86	-35 4 57 -46	-48 23 38 0			
15	-23 89 79 -47	119 -40 -60 -73	-80 53 7 105	1 0 -59 -81			
16	47 120 -17 -107	96 -88 41 -9	1 104 -86 -15	14 60 111 -81			
17							

Matrix_B.txt

We can get the result from waveform, and we can also read from the output file Matrix_Result.txt. Then we write a Python script to verify the result.

```
ResultVerification.py ×

D: > XilinxPorject > Assignment2_Q2_SystolicArrayforDMM > ResultVerification.py > ...
1 import numpy as np
2
3 matrix_A = np.loadtxt('Matrix_A.txt')
4 matrix_B = np.loadtxt('Matrix_B.txt')
5 print (matrix_A)
6
7 print(matrix_B)
8 result = np.dot(matrix_A, matrix_B)
9 np.set_printoptions(suppress=True)
10
11 print (result)
```

And use python we can get the result as below.

```

[[ 3114. -10640. -27926. -13544. -16209. -1263. 12293. -33605. 7028.
-3902. 12368. -3678. 5507. -18234. 992. 20080.]
[ 10920. -22488. -33234. -31020. -35348. -7150. 26906. 15509. 2755.
-53529. 34111. -21830. 5012. 11705. 1524. 3324.]
[-17906. 40885. 9855. -18866. 3021. -25479. 9385. -32502. 3997.
21070. -38247. -941. 19045. -7646. -11898. -13227.]
[ 27949. 51370. -5816. -3119. 26269. -26682. 12086. 12738. -11100.
-41620. -13960. -23479. -11838. 50478. -9924. -1964.]
[ 18809. 56296. -10850. 17478. 29892. -26402. -26188. 4757. 14483.
-2820. -50983. -25427. 848. 39672. 17274. 21739.]
[ 31847. 1790. 4919. 1981. 33137. -5055. -13080. 11359. -28525.
-23813. 35856. 13710. -21713. 25215. -8073. -18945.]
[-36227. 4776. -6294. -11310. 8916. 17916. -16025. 8769. 13360.
26846. -35888. 23558. 6674. -26450. 19016. 22804.]
[ 12125. 8648. -7393. 22332. 15958. -23286. -37675. -27645. -27212.
-39425. -18406. 55. -18551. 21627. -35294. 32473.]
[-31557. 2750. -25527. -12004. -46575. 2442. -13473. 10. 34352.
13280. -49281. -14723. 17137. -16335. 16825. 12036.]
[-13391. 16883. 22203. 24910. 11320. 26897. 1131. -27146. 2056.
18480. -9227. 2309. -4817. -17997. -5820. 5112.]
[-4970. -3988. -6161. 43121. 25463. 38745. 2804. 12475. 4426.
12924. -14788. 14585. 10028. -18794. 3846. 21449.]
[ 12333. -41526. 13528. 22571. -18082. -9926. -9863. 13394. -11995.
8536. 26373. 40363. 4070. -10070. 1819. 34060.]
[ 19176. -17637. 18361. 8911. 4845. 5052. 1498. -3612. -4438.
25221. 8006. 4528. 8635. 587. 18941. -7739.]
[ 26506. -22704. 14955. -15880. 14619. -20331. -15743. -4646. -26791.
9559. 56665. 31503. -24687. 8602. 3674. -5321.]
[ 21499. 11313. 13196. 32578. -3418. 3982. 16266. -4968. -2656.
-5712. 8891. 46261. 19933. -1747. -6265. 15065.]
[-30176. 3003. -12245. -10980. -45197. -1050. 21035. -6504. 1440.
-25636. -25827. 2470. -18273. -12789. -13635. 8057.]]
PS D:\XilinxProject\Assignment2_Q2_SystolicArrayforDM> 

```

And compare the output file or waveform from the simulation, we can verify the correctness of systolic array.

	Matrix_A[0][0]	Matrix_A[0][1]	Matrix_A[0][2]	Matrix_A[0][3]	Matrix_A[0][4]	Matrix_A[0][5]	Matrix_A[0][6]	Matrix_A[0][7]	Matrix_A[0][8]	Matrix_A[0][9]	Matrix_A[0][10]	Matrix_A[0][11]	Matrix_A[0][12]	Matrix_A[0][13]	Matrix_A[0][14]	Matrix_A[0][15]	Matrix_A[1][0]	Matrix_A[1][1]	Matrix_A[1][2]	Matrix_A[1][3]	Matrix_A[1][4]	Matrix_A[1][5]	Matrix_A[1][6]	Matrix_A[1][7]	Matrix_A[1][8]	Matrix_A[1][9]	Matrix_A[1][10]	Matrix_A[1][11]	Matrix_A[1][12]	Matrix_A[1][13]	Matrix_A[1][14]	Matrix_A[1][15]	Matrix_A[2][0]	Matrix_A[2][1]	Matrix_A[2][2]	Matrix_A[2][3]	Matrix_A[2][4]	Matrix_A[2][5]	Matrix_A[2][6]	Matrix_A[2][7]	Matrix_A[2][8]	Matrix_A[2][9]	Matrix_A[2][10]	Matrix_A[2][11]	Matrix_A[2][12]	Matrix_A[2][13]	Matrix_A[2][14]	Matrix_A[2][15]	Matrix_A[3][0]	Matrix_A[3][1]	Matrix_A[3][2]	Matrix_A[3][3]	Matrix_A[3][4]	Matrix_A[3][5]	Matrix_A[3][6]	Matrix_A[3][7]	Matrix_A[3][8]	Matrix_A[3][9]	Matrix_A[3][10]	Matrix_A[3][11]	Matrix_A[3][12]	Matrix_A[3][13]	Matrix_A[3][14]	Matrix_A[3][15]	Matrix_A[4][0]	Matrix_A[4][1]	Matrix_A[4][2]	Matrix_A[4][3]	Matrix_A[4][4]	Matrix_A[4][5]	Matrix_A[4][6]	Matrix_A[4][7]	Matrix_A[4][8]	Matrix_A[4][9]	Matrix_A[4][10]	Matrix_A[4][11]	Matrix_A[4][12]	Matrix_A[4][13]	Matrix_A[4][14]	Matrix_A[4][15]	Matrix_A[5][0]	Matrix_A[5][1]	Matrix_A[5][2]	Matrix_A[5][3]	Matrix_A[5][4]	Matrix_A[5][5]	Matrix_A[5][6]	Matrix_A[5][7]	Matrix_A[5][8]	Matrix_A[5][9]	Matrix_A[5][10]	Matrix_A[5][11]	Matrix_A[5][12]	Matrix_A[5][13]	Matrix_A[5][14]	Matrix_A[5][15]	Matrix_A[6][0]	Matrix_A[6][1]	Matrix_A[6][2]	Matrix_A[6][3]	Matrix_A[6][4]	Matrix_A[6][5]	Matrix_A[6][6]	Matrix_A[6][7]	Matrix_A[6][8]	Matrix_A[6][9]	Matrix_A[6][10]	Matrix_A[6][11]	Matrix_A[6][12]	Matrix_A[6][13]	Matrix_A[6][14]	Matrix_A[6][15]	Matrix_A[7][0]	Matrix_A[7][1]	Matrix_A[7][2]	Matrix_A[7][3]	Matrix_A[7][4]	Matrix_A[7][5]	Matrix_A[7][6]	Matrix_A[7][7]	Matrix_A[7][8]	Matrix_A[7][9]	Matrix_A[7][10]	Matrix_A[7][11]	Matrix_A[7][12]	Matrix_A[7][13]	Matrix_A[7][14]	Matrix_A[7][15]	Matrix_A[8][0]	Matrix_A[8][1]	Matrix_A[8][2]	Matrix_A[8][3]	Matrix_A[8][4]	Matrix_A[8][5]	Matrix_A[8][6]	Matrix_A[8][7]	Matrix_A[8][8]	Matrix_A[8][9]	Matrix_A[8][10]	Matrix_A[8][11]	Matrix_A[8][12]	Matrix_A[8][13]	Matrix_A[8][14]	Matrix_A[8][15]	Matrix_A[9][0]	Matrix_A[9][1]	Matrix_A[9][2]	Matrix_A[9][3]	Matrix_A[9][4]	Matrix_A[9][5]	Matrix_A[9][6]	Matrix_A[9][7]	Matrix_A[9][8]	Matrix_A[9][9]	Matrix_A[9][10]	Matrix_A[9][11]	Matrix_A[9][12]	Matrix_A[9][13]	Matrix_A[9][14]	Matrix_A[9][15]	Matrix_A[10][0]	Matrix_A[10][1]	Matrix_A[10][2]	Matrix_A[10][3]	Matrix_A[10][4]	Matrix_A[10][5]	Matrix_A[10][6]	Matrix_A[10][7]	Matrix_A[10][8]	Matrix_A[10][9]	Matrix_A[10][10]	Matrix_A[10][11]	Matrix_A[10][12]	Matrix_A[10][13]	Matrix_A[10][14]	Matrix_A[10][15]	Matrix_A[11][0]	Matrix_A[11][1]	Matrix_A[11][2]	Matrix_A[11][3]	Matrix_A[11][4]	Matrix_A[11][5]	Matrix_A[11][6]	Matrix_A[11][7]	Matrix_A[11][8]	Matrix_A[11][9]	Matrix_A[11][10]	Matrix_A[11][11]	Matrix_A[11][12]	Matrix_A[11][13]	Matrix_A[11][14]	Matrix_A[11][15]	Matrix_A[12][0]	Matrix_A[12][1]	Matrix_A[12][2]	Matrix_A[12][3]	Matrix_A[12][4]	Matrix_A[12][5]	Matrix_A[12][6]	Matrix_A[12][7]	Matrix_A[12][8]	Matrix_A[12][9]	Matrix_A[12][10]	Matrix_A[12][11]	Matrix_A[12][12]	Matrix_A[12][13]	Matrix_A[12][14]	Matrix_A[12][15]	Matrix_A[13][0]	Matrix_A[13][1]	Matrix_A[13][2]	Matrix_A[13][3]	Matrix_A[13][4]	Matrix_A[13][5]	Matrix_A[13][6]	Matrix_A[13][7]	Matrix_A[13][8]	Matrix_A[13][9]	Matrix_A[13][10]	Matrix_A[13][11]	Matrix_A[13][12]	Matrix_A[13][13]	Matrix_A[13][14]	Matrix_A[13][15]	Matrix_A[14][0]	Matrix_A[14][1]	Matrix_A[14][2]	Matrix_A[14][3]	Matrix_A[14][4]	Matrix_A[14][5]	Matrix_A[14][6]	Matrix_A[14][7]	Matrix_A[14][8]	Matrix_A[14][9]	Matrix_A[14][10]	Matrix_A[14][11]	Matrix_A[14][12]	Matrix_A[14][13]	Matrix_A[14][14]	Matrix_A[14][15]	Matrix_A[15][0]	Matrix_A[15][1]	Matrix_A[15][2]	Matrix_A[15][3]	Matrix_A[15][4]	Matrix_A[15][5]	Matrix_A[15][6]	Matrix_A[15][7]	Matrix_A[15][8]	Matrix_A[15][9]	Matrix_A[15][10]	Matrix_A[15][11]	Matrix_A[15][12]	Matrix_A[15][13]	Matrix_A[15][14]	Matrix_A[15][15]	Matrix_A[16][0]	Matrix_A[16][1]	Matrix_A[16][2]	Matrix_A[16][3]	Matrix_A[16][4]	Matrix_A[16][5]	Matrix_A[16][6]	Matrix_A[16][7]	Matrix_A[16][8]	Matrix_A[16][9]	Matrix_A[16][10]	Matrix_A[16][11]	Matrix_A[16][12]	Matrix_A[16][13]	Matrix_A[16][14]	Matrix_A[16][15]	Matrix_A[17][0]	Matrix_A[17][1]	Matrix_A[17][2]	Matrix_A[17][3]	Matrix_A[17][4]	Matrix_A[17][5]	Matrix_A[17][6]	Matrix_A[17][7]	Matrix_A[17][8]	Matrix_A[17][9]	Matrix_A[17][10]	Matrix_A[17][11]	Matrix_A[17][12]	Matrix_A[17][13]	Matrix_A[17][14]	Matrix_A[17][15]	Matrix_A[18][0]	Matrix_A[18][1]	Matrix_A[18][2]	Matrix_A[18][3]	Matrix_A[18][4]	Matrix_A[18][5]	Matrix_A[18][6]	Matrix_A[18][7]	Matrix_A[18][8]	Matrix_A[18][9]	Matrix_A[18][10]	Matrix_A[18][11]	Matrix_A[18][12]	Matrix_A[18][13]	Matrix_A[18][14]	Matrix_A[18][15]	Matrix_A[19][0]	Matrix_A[19][1]	Matrix_A[19][2]	Matrix_A[19][3]	Matrix_A[19][4]	Matrix_A[19][5]	Matrix_A[19][6]	Matrix_A[19][7]	Matrix_A[19][8]	Matrix_A[19][9]	Matrix_A[19][10]	Matrix_A[19][11]	Matrix_A[19][12]	Matrix_A[19][13]	Matrix_A[19][14]	Matrix_A[19][15]	Matrix_A[20][0]	Matrix_A[20][1]	Matrix_A[20][2]	Matrix_A[20][3]	Matrix_A[20][4]	Matrix_A[20][5]	Matrix_A[20][6]	Matrix_A[20][7]	Matrix_A[20][8]	Matrix_A[20][9]	Matrix_A[20][10]	Matrix_A[20][11]	Matrix_A[20][12]	Matrix_A[20][13]	Matrix_A[20][14]	Matrix_A[20][15]	Matrix_A[21][0]	Matrix_A[21][1]	Matrix_A[21][2]	Matrix_A[21][3]	Matrix_A[21][4]	Matrix_A[21][5]	Matrix_A[21][6]	Matrix_A[21][7]	Matrix_A[21][8]	Matrix_A[21][9]	Matrix_A[21][10]	Matrix_A[21][11]	Matrix_A[21][12]	Matrix_A[21][13]	Matrix_A[21][14]	Matrix_A[21][15]	Matrix_A[22][0]	Matrix_A[22][1]	Matrix_A[22][2]	Matrix_A[22][3]	Matrix_A[22][4]	Matrix_A[22][5]	Matrix_A[22][6]	Matrix_A[22][7]	Matrix_A[22][8]	Matrix_A[22][9]	Matrix_A[22][10]	Matrix_A[22][11]	Matrix_A[22][12]	Matrix_A[22][13]	Matrix_A[22][14]	Matrix_A[22][15]	Matrix_A[23][0]	Matrix_A[23][1]	Matrix_A[23][2]	Matrix_A[23][3]	Matrix_A[23][4]	Matrix_A[23][5]	Matrix_A[23][6]	Matrix_A[23][7]	Matrix_A[23][8]	Matrix_A[23][9]	Matrix_A[23][10]	Matrix_A[23][11]	Matrix_A[23][12]	Matrix_A[23][13]	Matrix_A[23][14]	Matrix_A[23][15]	Matrix_A[24][0]	Matrix_A[24][1]	Matrix_A[24][2]	Matrix_A[24][3]	Matrix_A[24][4]	Matrix_A[24][5]	Matrix_A[24][6]	Matrix_A[24][7]	Matrix_A[24][8]	Matrix_A[24][9]	Matrix_A[24][10]	Matrix_A[24][11]	Matrix_A[24][12]	Matrix_A[24][13]	Matrix_A[24][14]	Matrix_A[24][15]	Matrix_A[25][0]	Matrix_A[25][1]	Matrix_A[25][2]	Matrix_A[25][3]	Matrix_A[25][4]	Matrix_A[25][5]	Matrix_A[25][6]	Matrix_A[25][7]	Matrix_A[25][8]	Matrix_A[25][9]	Matrix_A[25][10]	Matrix_A[25][11]	Matrix_A[25][12]	Matrix_A[25][13]	Matrix_A[25][14]	Matrix_A[25][15]	Matrix_A[26][0]	Matrix_A[26][1]	Matrix_A[26][2]	Matrix_A[26][3]	Matrix_A[26][4]	Matrix_A[26][5]	Matrix_A[26][6]	Matrix_A[26][7]	Matrix_A[26][8]	Matrix_A[26][9]	Matrix_A[26][10]	Matrix_A[26][11]	Matrix_A[26][12]	Matrix_A[26][13]	Matrix_A[26][14]	Matrix_A[26][15]	Matrix_A[27][0]	Matrix_A[27][1]	Matrix_A[27][2]	Matrix_A[27][3]	Matrix_A[27][4]	Matrix_A[27][5]	Matrix_A[27][6]	Matrix_A[27][7]	Matrix_A[27][8]	Matrix_A[27][9]	Matrix_A[27][10]	Matrix_A[27][11]	Matrix_A[27][12]	Matrix_A[27][13]	Matrix_A[27][14]	Matrix_A[27][15]	Matrix_A[28][0]	Matrix_A[28][1]	Matrix_A[28][2]	Matrix_A[28][3]	Matrix_A[28][4]	Matrix_A[28][5]	Matrix_A[28][6]	Matrix_A[28][7]	Matrix_A[28][8]	Matrix_A[28][9]	Matrix_A[28][10]	Matrix_A[28][11]	Matrix_A[28][12]	Matrix_A[28][13]	Matrix_A[28][14]	Matrix_A[28][15]	Matrix_A[29][0]	Matrix_A[29][1]	Matrix_A[29][2]	Matrix_A[29][3]	Matrix_A[29][4]	Matrix_A[29][5]	Matrix_A[29][6]	Matrix_A[29][7]	Matrix_A[29][8]	Matrix_A[29][9]	Matrix_A[29][10]	Matrix_A[29][11]	Matrix_A[29][12]	Matrix_A[29][13]	Matrix_A[29][14]	Matrix_A[29][15]	Matrix_A[30][0]	Matrix_A[30][1]	Matrix_A[30][2]	Matrix_A[30][3]	Matrix_A[30][4]	Matrix_A[30][5]	Matrix_A[30][6]	Matrix_A[30][7]	Matrix_A[30][8]	Matrix_A[30][9]	Matrix_A[30][10]	Matrix_A[30][11]	Matrix_A[30][12]	Matrix_A[30][13]	Matrix_A[30][14]	Matrix_A[30][15]	Matrix_A[31][0]	Matrix_A[31][1]	Matrix_A[31][2]	Matrix_A[31][3]	Matrix_A[31][4]	Matrix_A[31][5]	Matrix_A[31][6]	Matrix_A[31][7]	Matrix_A[31][8]	Matrix_A[31][9]	Matrix_A[31][10]	Matrix_A[31][11]	Matrix_A[31][12]	Matrix_A[31][13]	Matrix_A[31][14]	Matrix_A[31][15]	Matrix_A[32][0]	Matrix_A[32][1]	Matrix_A[32][2]	Matrix_A[32][3]	Matrix_A[32][4]	Matrix_A[32][5]	Matrix_A[32][6]	Matrix_A[32][7]	Matrix_A[32][8]	Matrix_A[32][9]	Matrix_A[32][10]	Matrix_A[32][11]	Matrix_A[32][12]	Matrix_A[32][13]	Matrix_A[32][14]	Matrix_A[32][15]	Matrix_A[33][0]	Matrix_A[33][1]	Matrix_A[33][2]	Matrix_A[33][3]	Matrix_A[33][4]	Matrix_A[33][5]	Matrix_A[33][6]	Matrix_A[33][7]	Matrix_A[33][8]	Matrix_A[33][9]	Matrix_A[33][10]	Matrix_A[33][11]	Matrix_A[33][12]	Matrix_A[33][13]	Matrix_A[33][14]	Matrix_A[33][15]	Matrix_A[34][0]	Matrix_A[34][1]	Matrix_A[34][2]	Matrix_A[34][3]	Matrix_A[34][4]	Matrix_A[34][5]	Matrix_A[34][6]	Matrix_A[34][7]	Matrix_A[34][8]	Matrix_A[34][9]	Matrix_A[34][10]	Matrix_A[34][11]	Matrix_A[34][12]	Matrix_A[34][13]	Matrix_A[34][14]	Matrix_A[34][15]	Matrix_A[35][0]	Matrix_A[35][1]	Matrix_A[35][2]	Matrix_A[35][3]	Matrix_A[35][4]	Matrix_A[35][5]	Matrix_A[35][6]	Matrix_A[35][7]	Matrix_A[35][8]	Matrix_A[35][9]	Matrix_A[35][10]	Matrix_A[35][11]	Matrix_A[35][12]	Matrix_A[35][13]	Matrix_A[35][14]	Matrix_A[35][15]	Matrix_A[36][0]	Matrix_A[36][1]	Matrix_A[36][2]	Matrix_A[36][3]	Matrix_A[36][4]	Matrix_A[36][5]	Matrix_A[36][6]	Matrix_A[36][7]	Matrix_A[36][8]	Matrix_A[36][9]	Matrix_A[36][10]	Matrix_A[36][11]	Matrix_A[36][12]	Matrix_A[36][13]	Matrix_A[36][14]	Matrix_A[36][15]	Matrix_A[37][0]	Matrix_A[37][1]	Matrix_A[37][2]	Matrix_A[37][3]	Matrix_A[37][4]	Matrix_A[37][5]	Matrix_A[37][6]	Matrix_A[37][7]	Matrix_A[37][8]	Matrix_A[37][9]	Matrix_A[37][10]	Matrix_A[37][11]	Matrix_A[37][12]	Matrix_A[37][13]	Matrix_A[37][14]	Matrix_A[37][15]	Matrix_A[38][0]	Matrix_A[38][1]	Matrix_A[38][2]	Matrix_A[38][3]	Matrix_A[38][4]	Matrix_A[38][5]	Matrix_A[38][6]	Matrix_A[38][7]	Matrix_A[38][8]	Matrix_A[38][9]	Matrix_A[38][10]	Matrix_A[38][11]	Matrix_A[38][12]	Matrix_A[38][13]	Matrix_A[38][14]	Matrix_A[38][15]	Matrix_A[39][0]	Matrix_A[39][1]	Matrix_A[39][2]	Matrix_A[39][3]	Matrix_A[39][4]	Matrix_A[39][5]	Matrix_A[39][6]	Matrix_A[39][7]	Matrix_A[39][8]	Matrix_A[39][9]	Matrix_A[39][10]	Matrix_A[39][11]	Matrix_A[39][12]	Matrix_A[39][13]	Matrix_A[39][14]	Matrix_A[39][15]	Matrix_A[40][0]	Matrix_A[40][1]	Matrix_A[40][2]	Matrix_A[40][3]	Matrix_A[40][4]	Matrix_A[40][5]	Matrix_A[40][6]	Matrix_A[40][7]	Matrix_A[40][8]	Matrix_A[40][9]	Matrix_A[40][10]	Matrix_A[40][11]	Matrix_A[40][12]	Matrix_A[40][13]	Matrix_A[40][14]	Matrix_A[40][15]	Matrix_A[41][0]	Matrix_A[41][1]	Matrix_A[41][2]	Matrix_A[41][3]	Matrix_A[41][4]	Matrix_A[41][5]	Matrix_A[41][6]	Matrix_A[41][7]	Matrix_A[41][8]	Matrix_A[41][9]	Matrix_A[41][10]	Matrix_A[41][11]	Matrix_A[41][12]	Matrix_A[41][13]	Matrix_A[41][14]	Matrix_A[41][15]	Matrix_A[42][0]	Matrix_A[42][1]	Matrix_A[42][2]	Matrix_A[42][3]	Matrix_A[42][4]	Matrix_A[42][5]	Matrix_A[42][6]	Matrix_A[42][7]	Matrix_A[42][8]	Matrix_A[42][9]	Matrix_A[42][10]	Matrix_A[42][11]	Matrix_A[42][12]	Matrix_A[42][13]	Matrix_A[42][14]	Matrix_A[42][15]	Matrix_A[43][0]	Matrix_A[43][1]	Matrix_A[43][2]	Matrix_A[43][3]	Matrix_A[43][4]	Matrix_A[43][5]	Matrix_A[43][6]	Matrix_A[43][7]	Matrix_A[43][8]	Matrix_A[43][9]	Matrix_A[43][10]	Matrix_A[43][11]	Matrix_A[43][12]	Matrix_A[43][13]	Matrix_A[43][14]	Matrix_A[43][15]	Matrix_A[44][0]	Matrix_A[44][1]	Matrix_A[44][2]	Matrix_A[44][3]	Matrix_A[44][4]	Matrix_A[44][5]	Matrix_A[44][6]	Matrix_A[44][7]	Matrix_A[44][8]	Matrix_A[44][9]	Matrix_A[44][10]	Matrix_A[44][11]	Matrix_A[44][12]	Matrix_A[44][13]	Matrix_A[44][14]	Matrix_A[44][15]	Matrix_A[45][0]	Matrix_A[45][1]	Matrix_A[45][2]	Matrix_A[45][3]	Matrix_A[45][4]	Matrix_A[45][5]	Matrix_A[45][6]	Matrix_A[45][7]	Matrix_A[45][8]	Matrix_A[45][9]	Matrix_A[45][10]	Matrix_A[45][11]	Matrix_A[45][12]	Matrix_A[45][13]	Matrix_A[45][14]	Matrix_A[45][15]	Matrix_A[46][0]	Matrix_A[46][1]	Matrix_A[46][2]	Matrix_A[46][3]	Matrix_A[46][4]	Matrix_A[46][5]	Matrix_A[46][6]	Matrix_A[46][7]	Matrix_A[46][8]	Matrix_A[46][9]	Matrix_A[46][10]	Matrix_A[46][11]	Matrix_A[46][12]	Matrix_A[46][13]	Matrix_A[46][14]	Matrix_A[46][15]	Matrix_A[47][0]	Matrix_A[47][1]	Matrix_A[47][2]	Matrix_A[47][3]	Matrix_A[47][4]	Matrix_A[47][5]	Matrix_A[47][6]	Matrix_A[47][7]	Matrix_A[47][8]	Matrix_A[47][9]	Matrix_A[47][10]	Matrix_A[47][11]	Matrix_A[47][12]	Matrix_A[47][13]	Matrix_A

1. Slice Logic					
Site Type	Used	Fixed	Available	Util%	
Slice LUTs*	20992	0	14400	145.78	
LUT as Logic	20992	0	14400	145.78	
LUT as Memory	0	0	6000	0.00	
Slice Registers	8960	0	28800	31.11	
Register as Flip Flop	8960	0	28800	31.11	
Register as Latch	0	0	28800	0.00	
F7 Muxes	0	0	8800	0.00	
F8 Muxes	0	0	4400	0.00	

* Warning! The Final LUT count, after physical optimizations and full

1.1 Summary of Registers by Type					
Total	Clock Enable	Synchronous	Asynchronous		
0	-	-	-	Set	
0	-	-	-	Reset	
0	-	Set	-		
0	-	Reset	-		
Yes	-	-			
Yes	-	Set			
Yes	-	Reset			
8960	Yes	-	Reset		
0	Yes	Set	-		
0	Yes	Reset	-		

2. Memory					
Site Type	Used	Fixed	Available	Util%	
Block RAM Tile	0	0	50	0.00	
RAMB36/FIFO*	0	0	50	0.00	
RAMB18	0	0	100	0.00	

* Note: Each Block RAM Tile only has one FIFO logic available

3. DSP					
Site Type	Used	Fixed	Available	Util%	
DSPs	0	0	66	0.00	

4. IO and GT Specific					
Site Type	Used	Fixed	Available	Util%	
Bonded IOB	5378	0	54	9959.26	
Bonded IPADs	0	0	2	0.00	
Bonded IOPADs	0	0	130	0.00	
PHV_CONTROL	0	0	2	0.00	
PHASER_REF	0	0	2	0.00	
OUT_FIFO	0	0	8	0.00	
IN_FIFO	0	0	8	0.00	
IDELAYCTRL	0	0	2	0.00	
IBUFDS	0	0	54	0.00	
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00	
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00	
IDELAY2/IDELAY2_FINEDELAY	0	0	100	0.00	
ILOGIC	0	0	54	0.00	
OLOGIC	0	0	54	0.00	

5. Clocking					
Site Type	Used	Fixed	Available	Util%	
BUFGCTRL	1	0	32	3.13	
BUFI0	0	0	8	0.00	
MMCME2_ADV	0	0	2	0.00	
PLLE2_ADV	0	0	2	0.00	
BUFMRCB	0	0	4	0.00	
BUFHCE	0	0	48	0.00	
BUFR	0	0	8	0.00	

6. Specific Feature					
Site Type	Used	Fixed	Available	Util%	
BSCANE2	0	0	4	0.00	
CAPTUREE2	0	0	1	0.00	
DNA_PORT	0	0	1	0.00	
EFUSE_USR	0	0	1	0.00	
FRAME_ECCE2	0	0	1	0.00	
ICAPE2	0	0	2	0.00	
STARTUPE2	0	0	1	0.00	
XADC	0	0	1	0.00	

7. Primitives					
Ref Name	Used	Functional Category			
LUT2	11264	LUT			
FDCE	8960	Flop & Latch			
LUT6	6656	LUT			
LUT4	6400	LUT			
OBUF	5120	IO			
CARRY4	4608	CarryLogic			
LUT5	1536	LUT			
LUT3	1536	LUT			
IBUF	258	IO			
LUT1	1	LUT			
BUFG	1	Clock			

Timing Estimation:

Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 3.935 ns	Worst Hold Slack (WHS): 0.165 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:	0
Total Number of Endpoints: 8704	Total Number of Endpoints: 8704	Total Number of Endpoints:	8961

All user specified timing constraints are met.

Power Estimation:

Summary		On-Chip Power							
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.		<table border="1"> <tr> <td>Dynamic: 5.098 W (95%)</td> </tr> <tr> <td>Clocks: 0.052 W (1%)</td> </tr> <tr> <td>Signals: 0.125 W (2%)</td> </tr> <tr> <td>Logic: 0.198 W (4%)</td> </tr> <tr> <td>I/O: 4.723 W (93%)</td> </tr> <tr> <td>Device Static: 0.261 W (5%)</td> </tr> </table>		Dynamic: 5.098 W (95%)	Clocks: 0.052 W (1%)	Signals: 0.125 W (2%)	Logic: 0.198 W (4%)	I/O: 4.723 W (93%)	Device Static: 0.261 W (5%)
Dynamic: 5.098 W (95%)									
Clocks: 0.052 W (1%)									
Signals: 0.125 W (2%)									
Logic: 0.198 W (4%)									
I/O: 4.723 W (93%)									
Device Static: 0.261 W (5%)									
Total On-Chip Power: 5.359 W									
Design Power Budget: Not Specified									
Power Budget Margin: N/A									
Junction Temperature: 86.8°C									
Thermal Margin: 13.2°C (1.1 W)									
Effective QJA: 11.5°C/W									
Power supplied to off-chip devices: 0 W									
Confidence level: Low									
Launch Power Constraint Advisor to find and fix invalid switching activity									

Now redo for 32x32 size.

The full synthesis schematic please see in the Appendix.

Resource Estimation:

```

1 | Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
2 |
3 | Tool Version : Vivado v.2019.2.1 (win64) Build 2729669 Thu Dec 5 04:49:17 MST 2019
4 | Date       : Thu Apr 2 23:57:00 2020
5 | Host       : DESKTOP-0GTLU5M running 64-bit major release (build 9200)
6 | Command    : report_utilization -file SystolicArray_utilization_synth.rpt -pb SystolicArray_utilization_synth.pb
7 | Design     : SystolicArray
8 | Device     : 7z007sclg225-2
9 | Design State: Synthesized
10 |
11
12 Utilization Design Information
13
14 Table of Contents
15
16 1. Slice Logic
17 1.1 Summary of Registers by Type
18 2. Memory
19 3. DSP
20 4. IO and GT Specific
21 5. Clocking
22 6. Specific Feature
23 7. Primitives
24 8. Black Boxes
25 9. Instantiated Netlists
26

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1. Slice Logic						1.1 Summary of Registers by Type				
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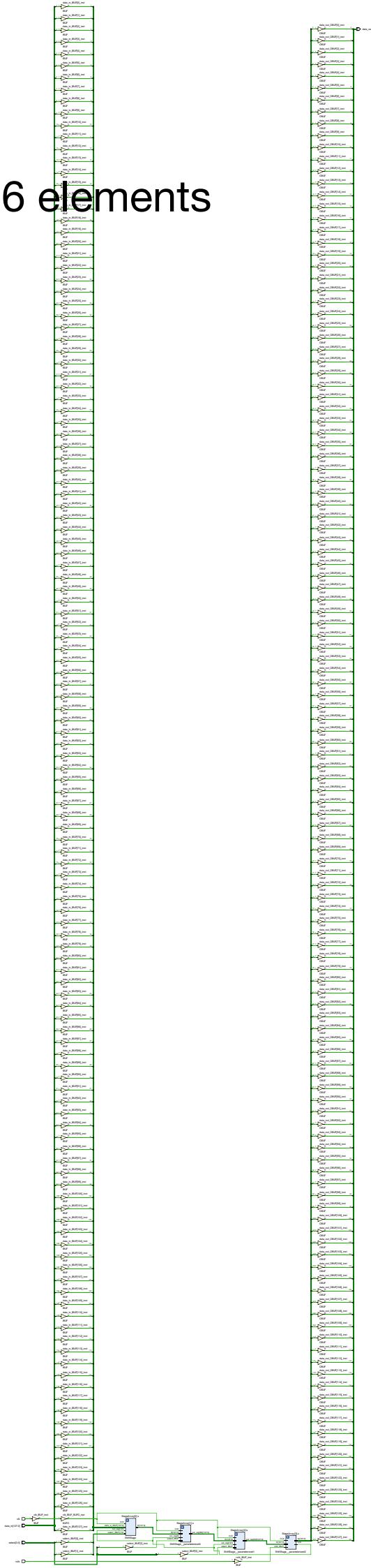
Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.923 ns	Worst Hold Slack (WHS): 0.165 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 36864	Total Number of Endpoints: 36864	Total Number of Endpoints: 37377

All user specified timing constraints are met.

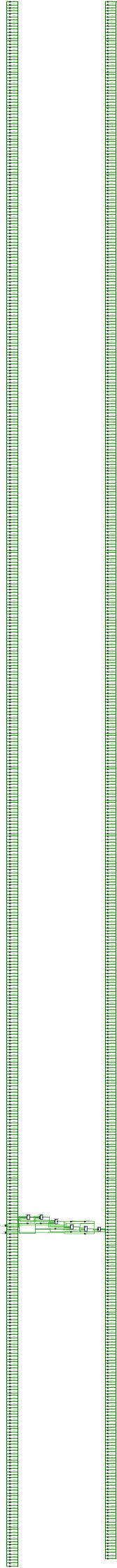
Power Estimation:

Summary													
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.													
Total On-Chip Power:	22.079 W (Junction temp exceeded!)												
Design Power Budget:	Not Specified												
Power Budget Margin:	N/A												
Junction Temperature:	125.0°C												
Thermal Margin:	-179.6°C (-15.1 W)												
Effective θJA:	11.5°C/W												
Power supplied to off-chip devices:	0 W												
Confidence level:	Low												
Launch Power Constraint Advisor to find and fix invalid switching activity													
On-Chip Power <table border="1"> <tr> <td>Dynamic:</td> <td>21.330 W (97%)</td> </tr> <tr> <td>Clocks:</td> <td>0.153 W (1%)</td> </tr> <tr> <td>Signals:</td> <td>0.510 W (2%)</td> </tr> <tr> <td>Logic:</td> <td>0.809 W (4%)</td> </tr> <tr> <td>I/O:</td> <td>19.858 W (93%)</td> </tr> <tr> <td>Device Static:</td> <td>0.747 W (3%)</td> </tr> </table>		Dynamic:	21.330 W (97%)	Clocks:	0.153 W (1%)	Signals:	0.510 W (2%)	Logic:	0.809 W (4%)	I/O:	19.858 W (93%)	Device Static:	0.747 W (3%)
Dynamic:	21.330 W (97%)												
Clocks:	0.153 W (1%)												
Signals:	0.510 W (2%)												
Logic:	0.809 W (4%)												
I/O:	19.858 W (93%)												
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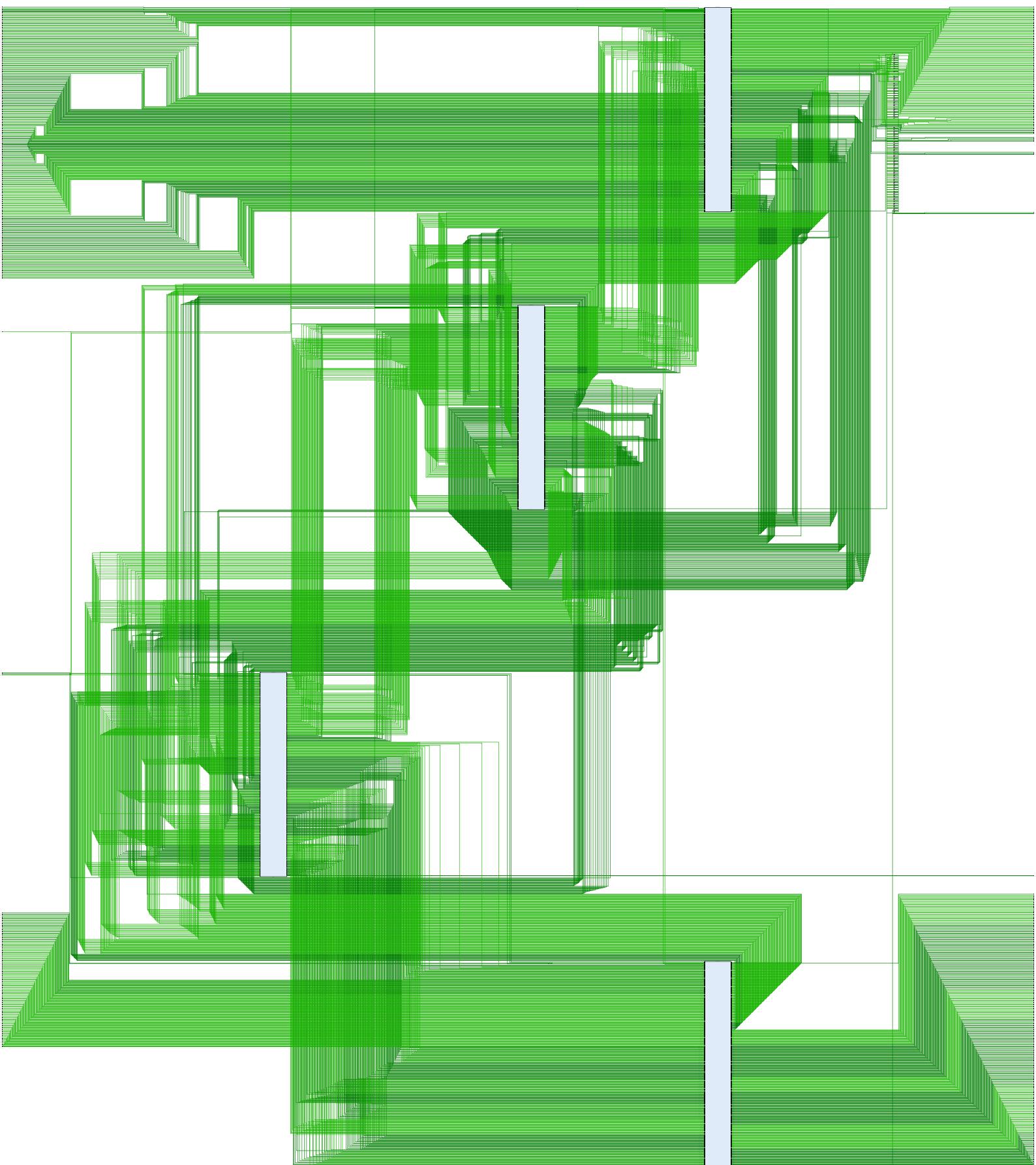
Barrel Shifter-16 elements

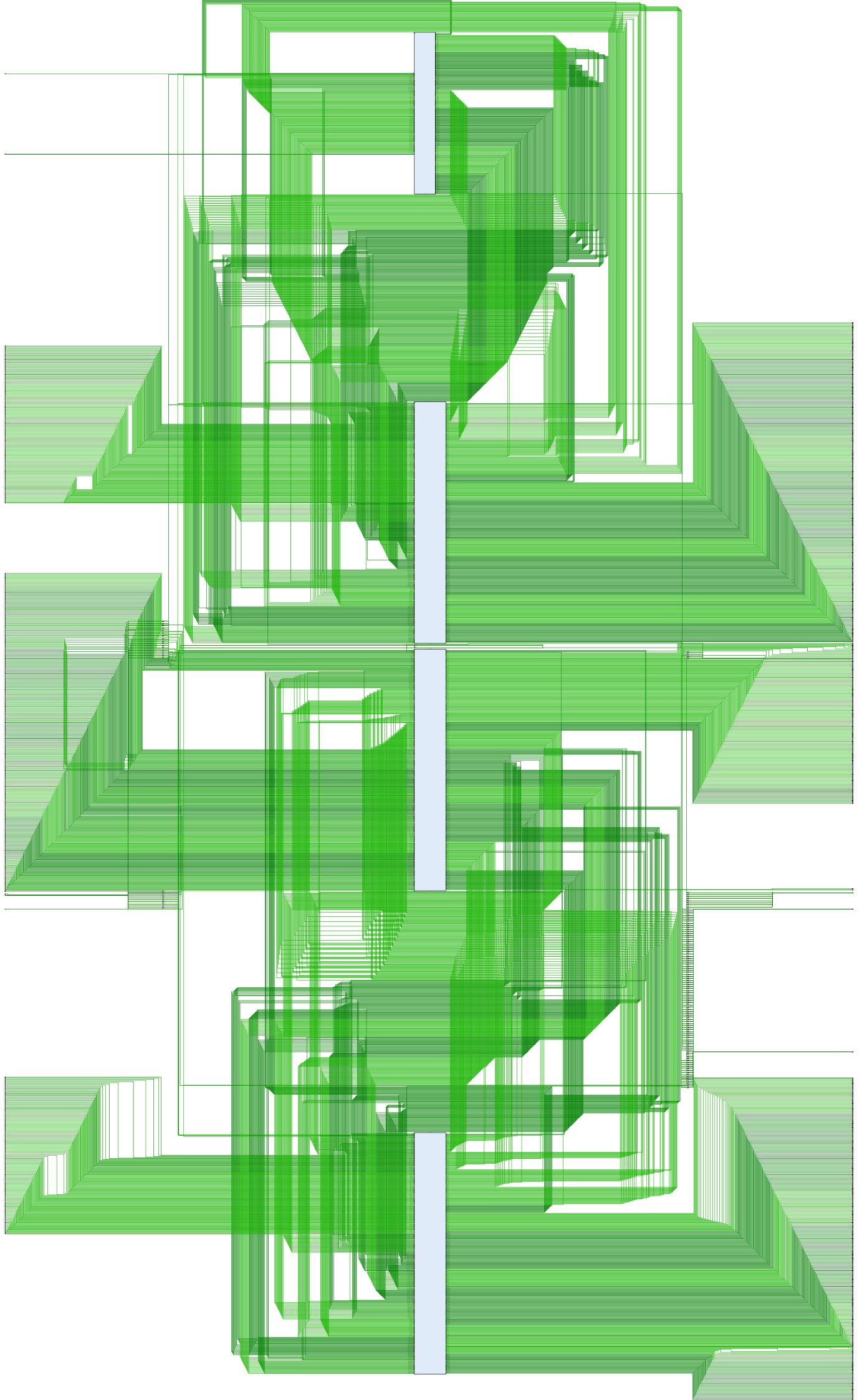


Barrel Shifter-64 elements

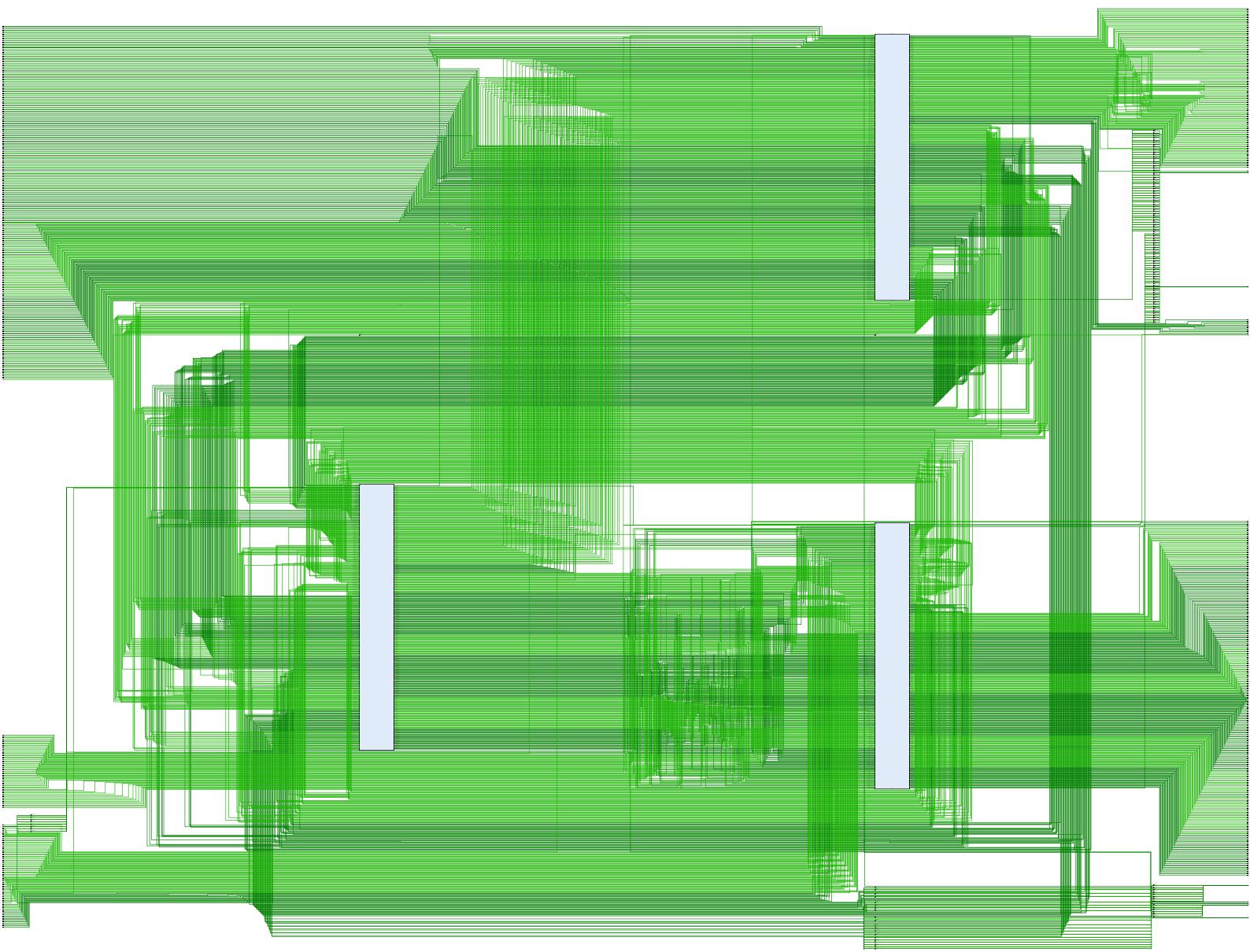


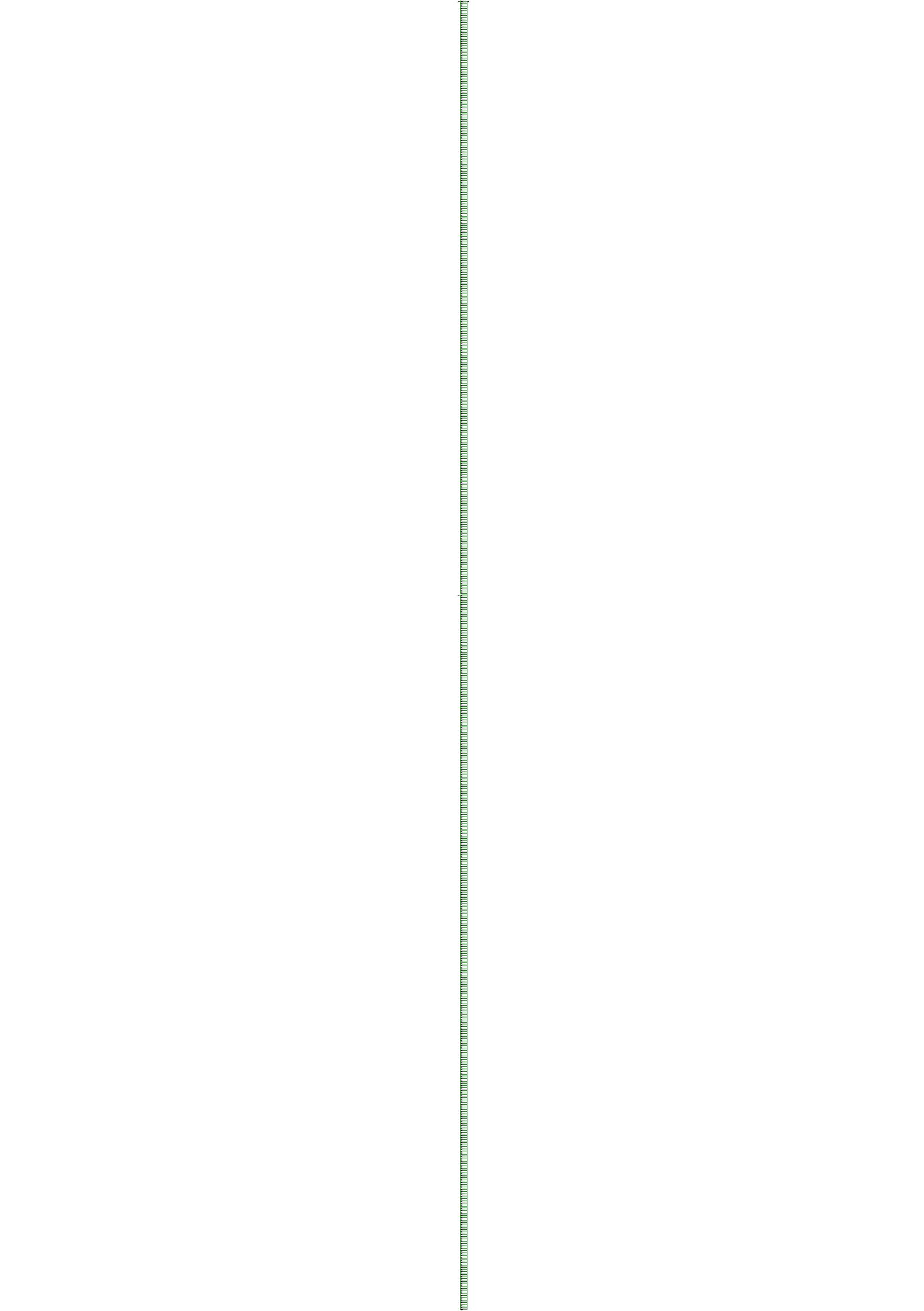
Systolic Array-16X16

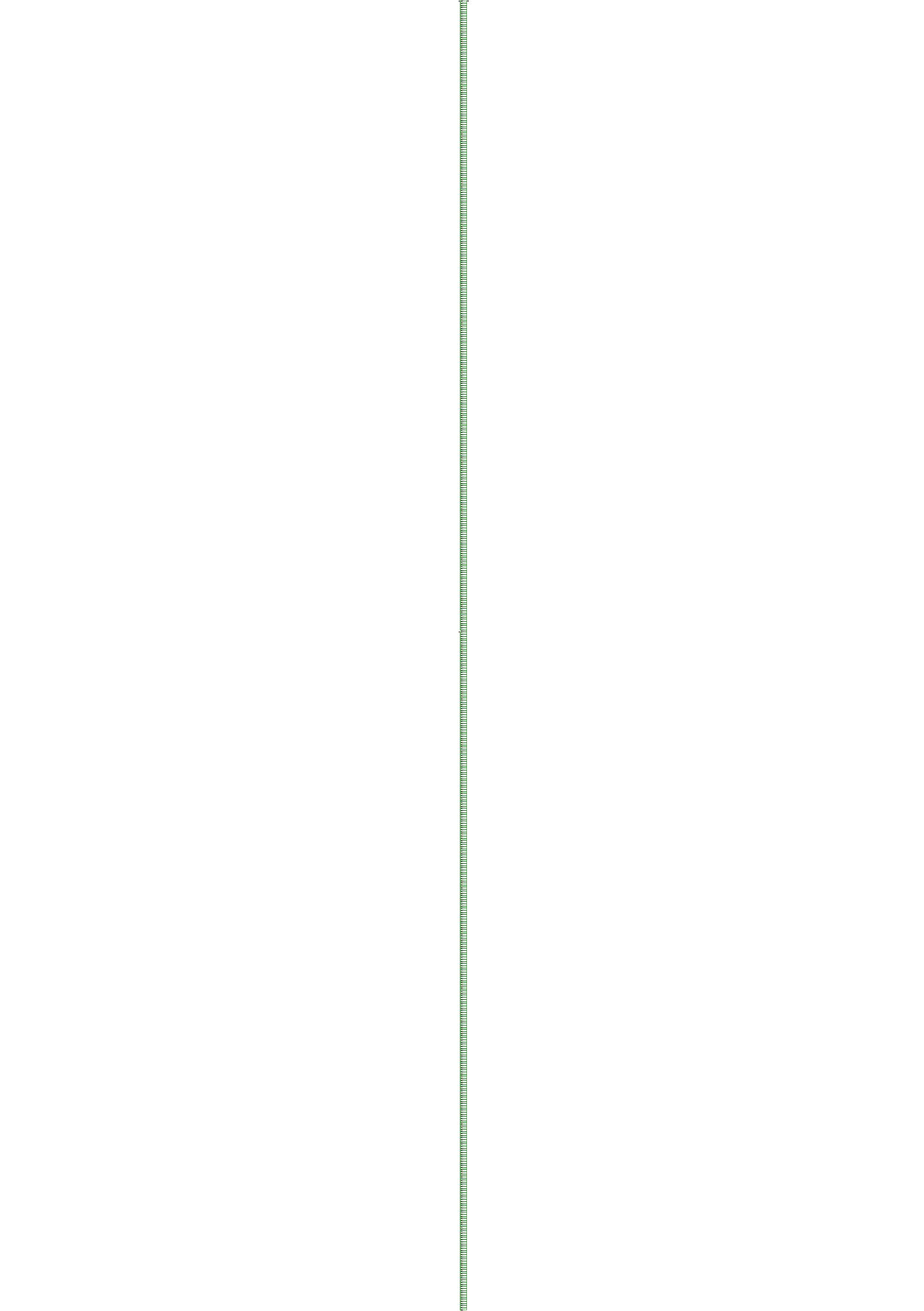


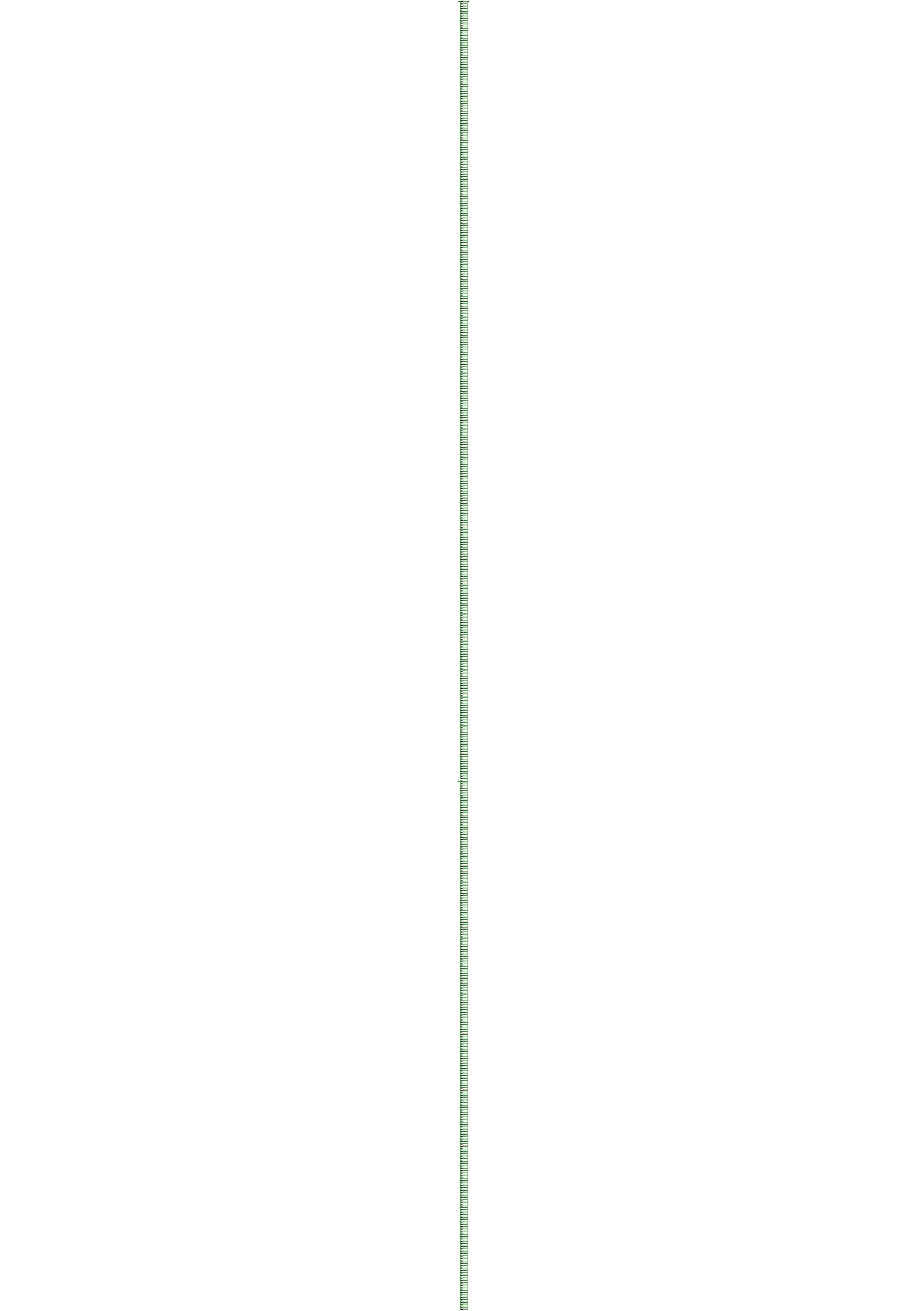


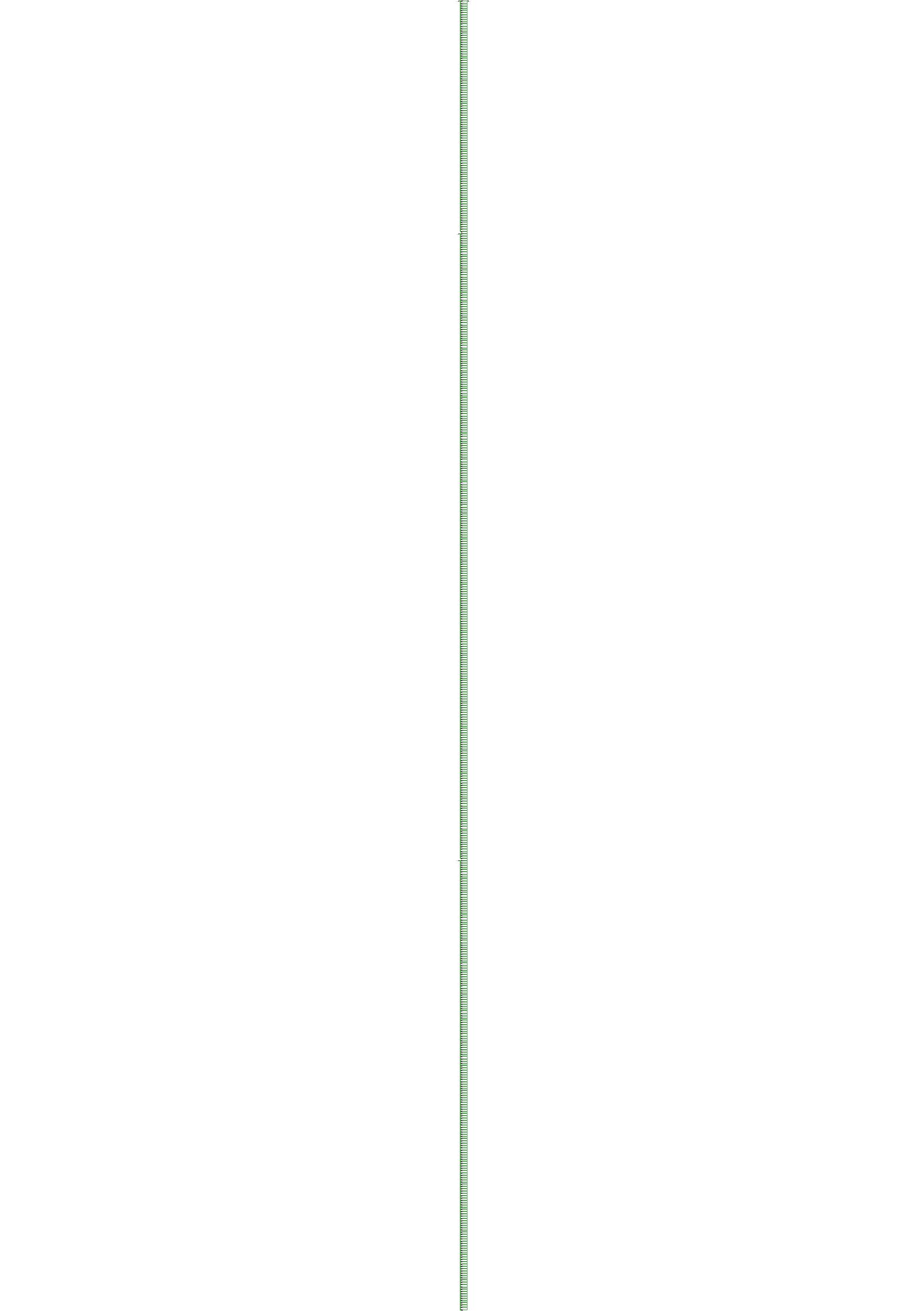


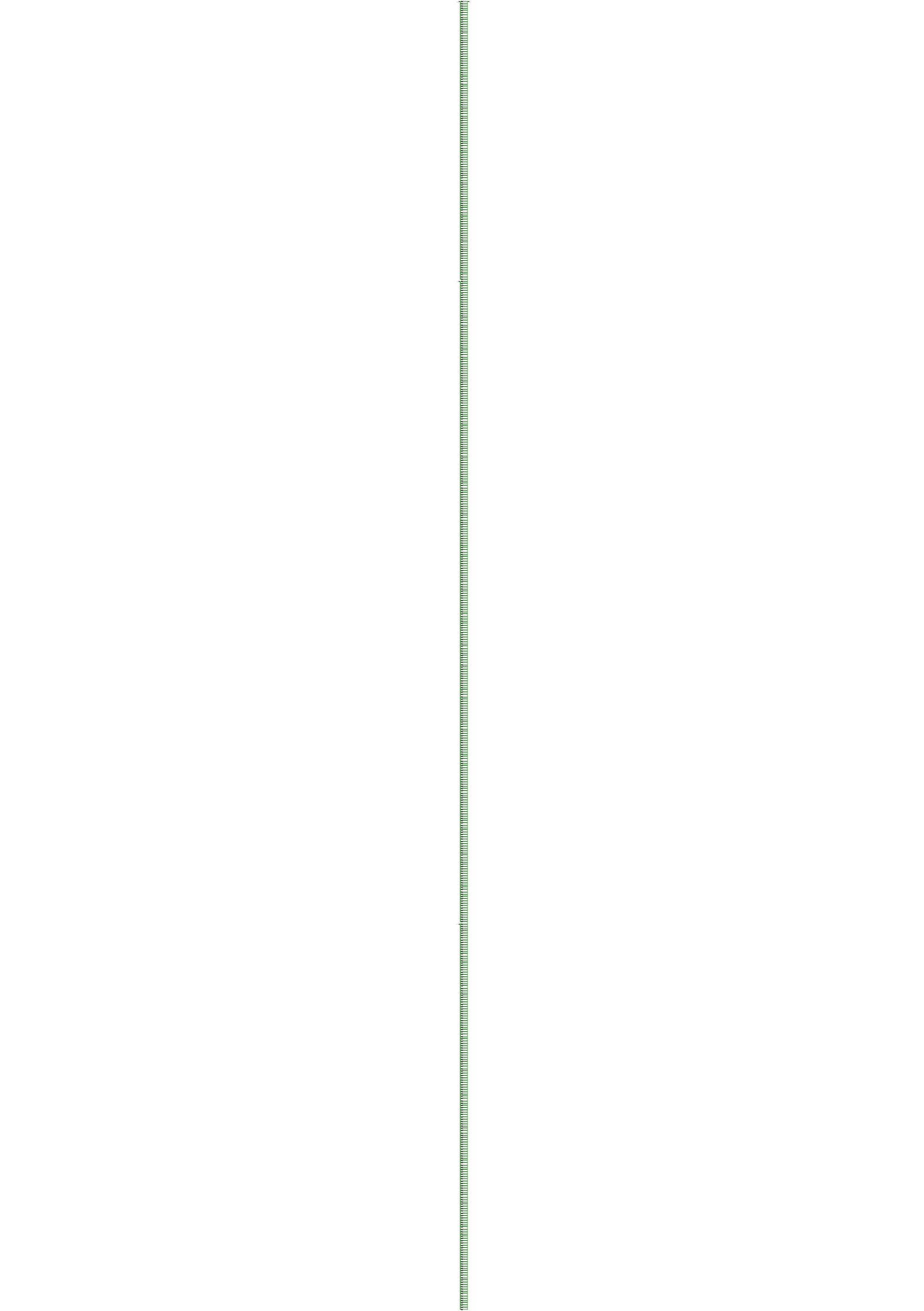


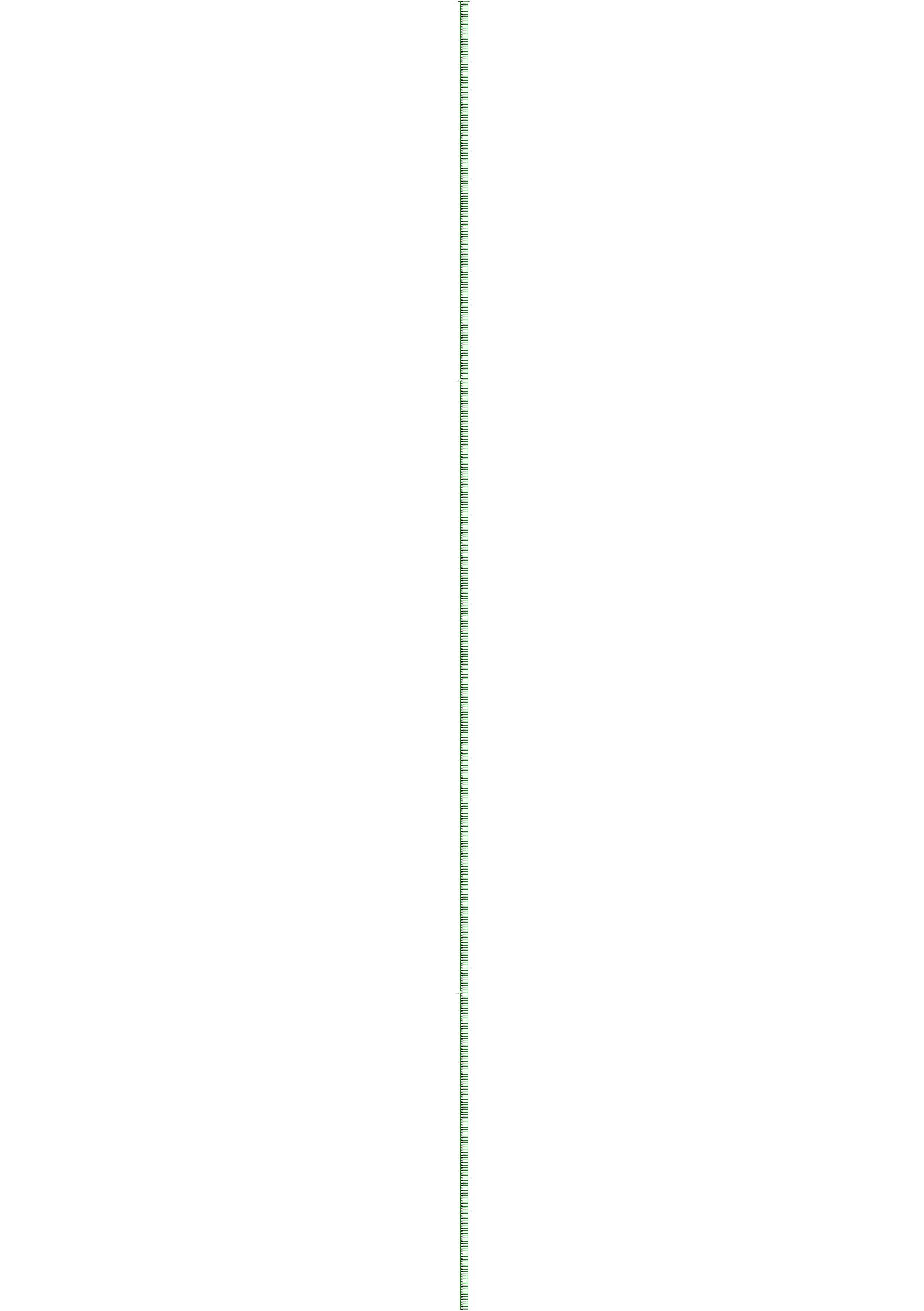


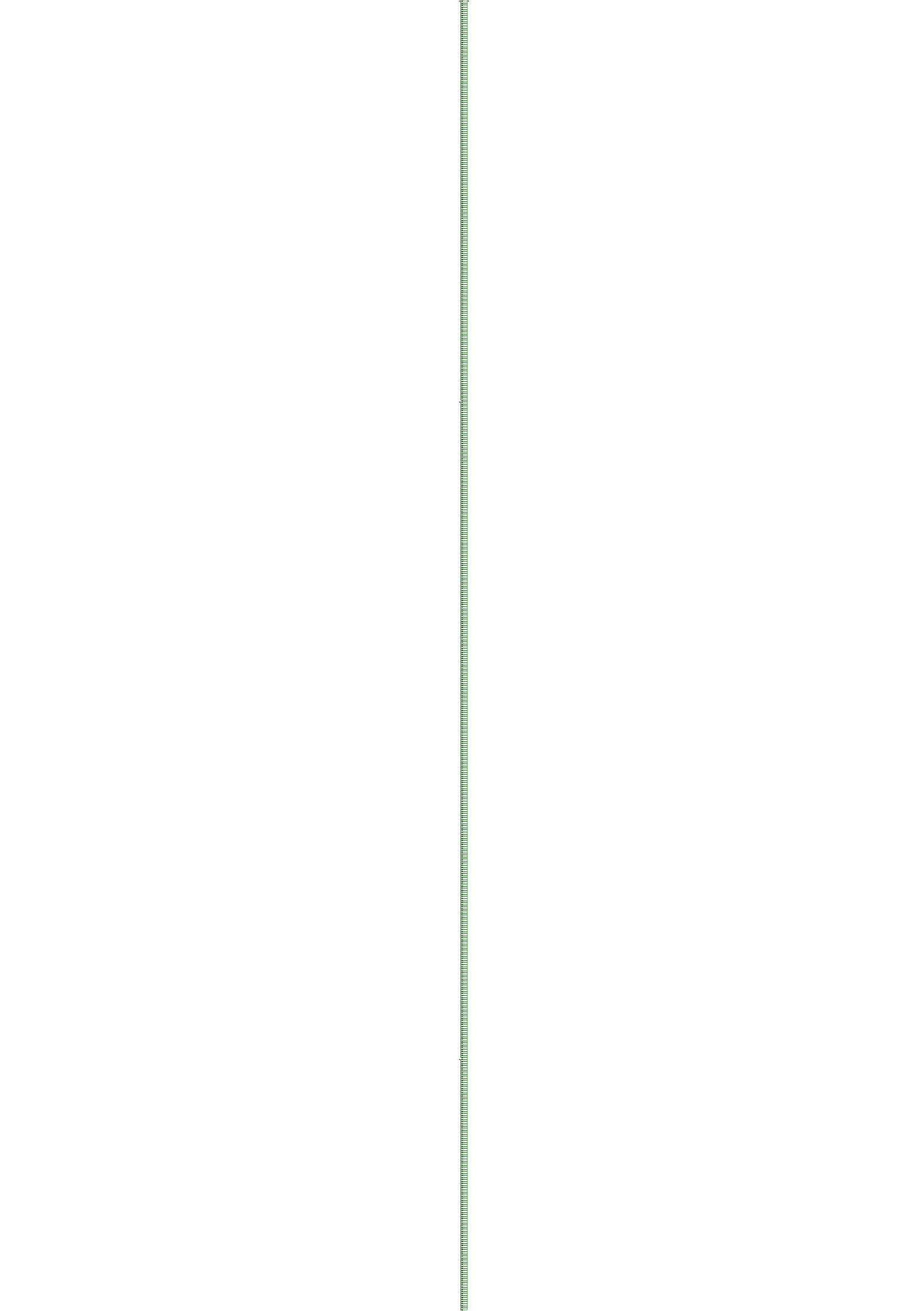


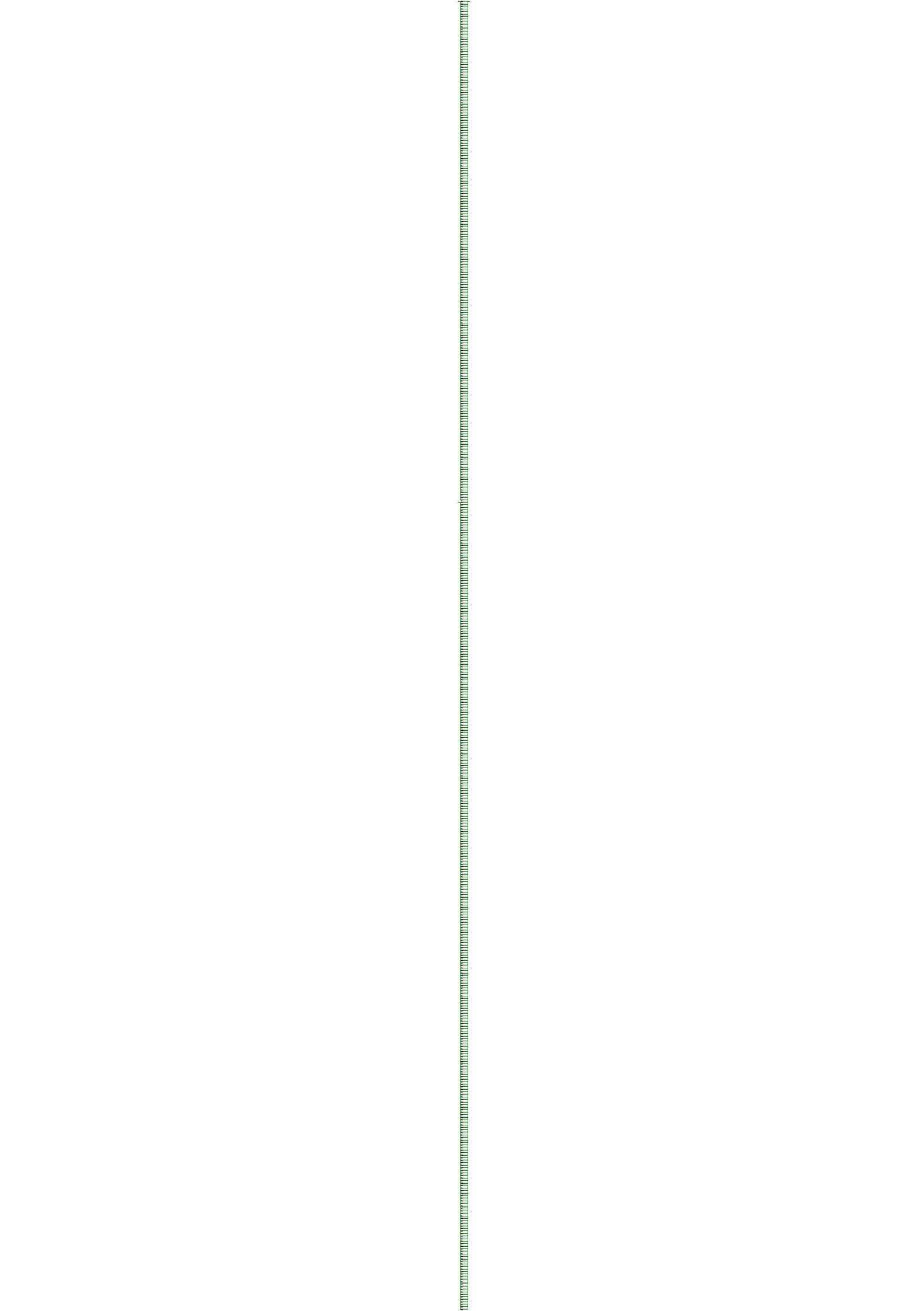


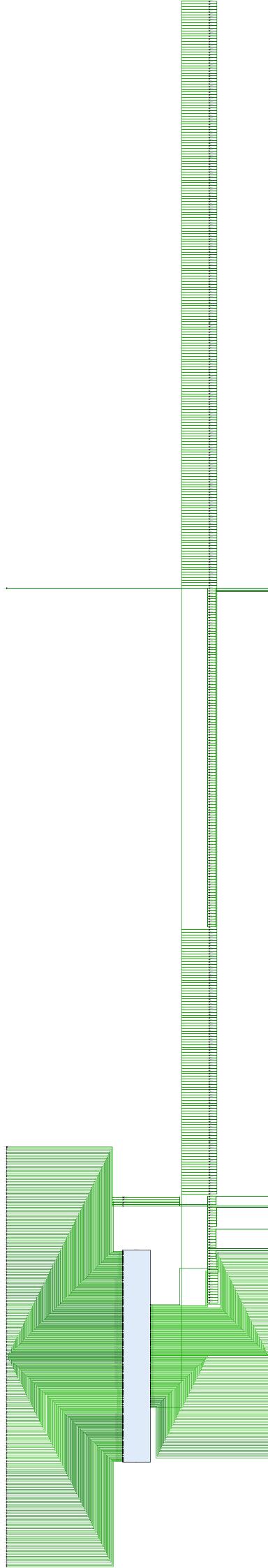












Systolic Array-32X32

