Lab Report No. 01:

Simple Circuit

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I. INTRODUCTION

A. Purpose

The purpose of today's experiments are familiar with the use and operation of AlteraQuartus software, and learn to use simulation tools to build the foundation for future learning VHDL.

At the completion of this lab, the student will be able to:

- Set up a Quartus II project, specify a revision, create graphical files, and compile a design
- Create a force file used in ModelSim, simulate, and verify the correct functional operation
- Program the Altera FPGA board with the correct pin assignments and demonstrate the correct operation of the circuit

B. Equipment

There is a minimal amount of equipment to be used in this lab. The few requirements are listed below:

- Quartus II Software (v13.0 or others)
- Computer capable of running the software mentioned
- The DE1_ SoC Developer Board (For Hardware Simulation)

C. Part I: Simulation and realization of a simple two-input OR gate

1. Block diagram

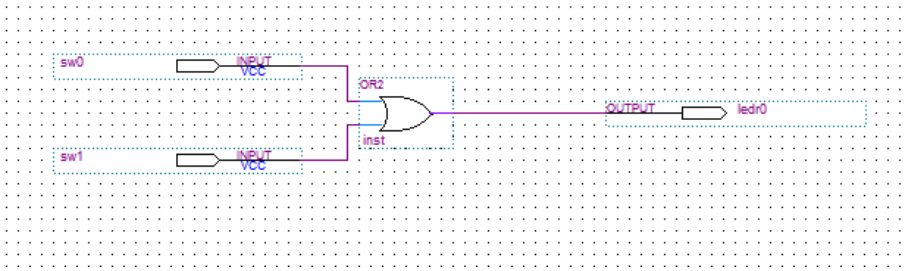


FIG. 1: or2in.bdf

2. VHDL code

```
1  LIBRARY ieee;
   USE ieee.std_logic_1164.all;
3
   LIBRARY work;
5
   ENTITY or2in IS
7     PORT
      (
9        sw0 :  IN  STD_LOGIC;
         sw1 :  IN  STD_LOGIC;
11       ledr0 :  OUT  STD_LOGIC
      );
13 END or2in;

15 ARCHITECTURE bdf_type OF or2in IS


17


19 BEGIN


21


23 ledr0 <= sw1 OR sw0;


25
   END bdf_type;
```

3. Functional simulation results

Write the test code:

```
# force file for two-input logic gate
# comment: need a # followed by a space
force sw0 0;# comment: after a command, need a semicolon
force sw1 0
run 100ns
force sw0 1
run 100ns
force sw1 1
run 100ns
force sw0 0
run 100ns
force sw1 0
run 100ns
```

The results are as follows:

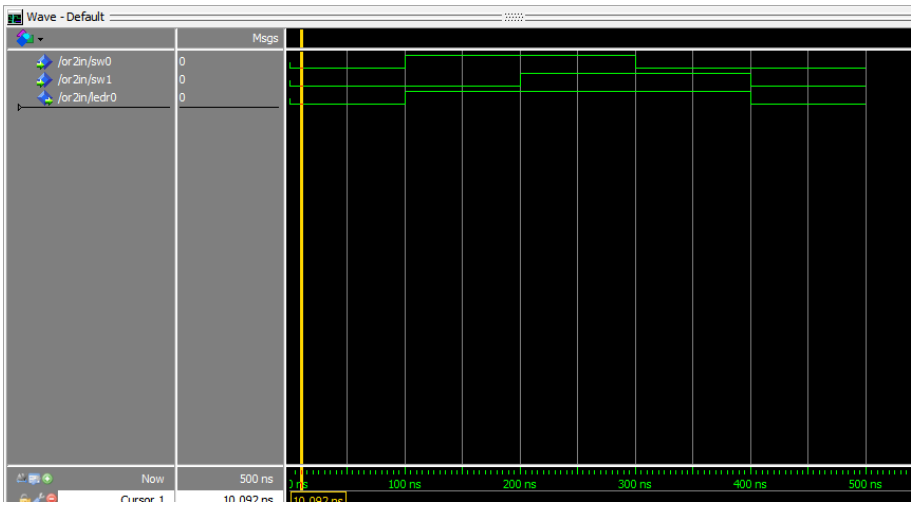


FIG. 2: or2in wave

D. Part II: Simulation and realization of a three-input AND gate

1. In the same project, create a new revision named **and3in** based on revision **or2in.**

2. Set **and3in** as current revision and generate the block diagram.

3. Set **and3in** as top-level entity by going to **Project> Set as top-level entity**.

4. Compile your diagram and run functional simulation following the Altera tutorial.

5. Download your design to the Altera board and demonstrate your result.

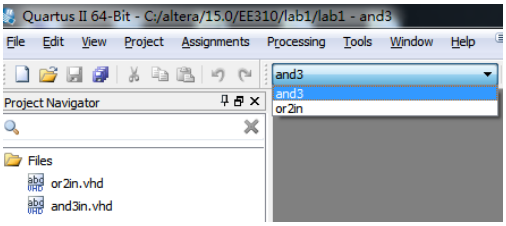
Write VHDL code:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY work;

ENTITY and3in IS
    PORT
    (
        sw0 :  IN  STD_LOGIC;
        sw1 :  IN  STD_LOGIC;
        sw2 :  IN  STD_LOGIC;
        ledr1 :  OUT  STD_LOGIC
    );
END and3in;

ARCHITECTURE bdf_type OF and3in IS



BEGIN



ledr1 <= sw0 AND sw1 AND sw2;


END bdf_type;
```

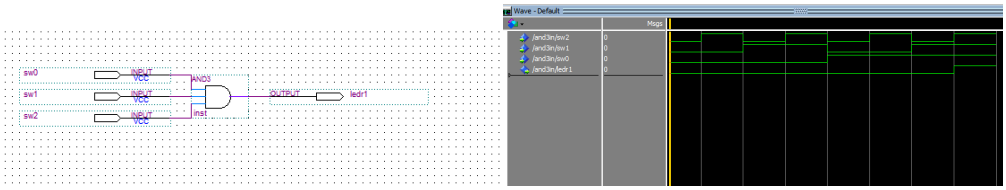
Write the test code:

```
# force file for two-input logic gate
# comment: need a # followed by a space
force sw0 0;# comment: after a command, need a semicolon
force sw1 0
force sw2 0
run 100ns

force sw0 0
force sw1 0
force sw2 1
run 100ns

force sw0 0
force sw1 1
force sw2 0
run 100ns

force sw0 0
force sw1 1
force sw2 1
run 100ns

force sw0 1
force sw1 0
force sw2 0
run 100ns

```

```
force sw0 1
force sw1 0
force sw2 1
run 100ns

force sw0 1
force sw1 1
force sw2 0
run 100ns

force sw0 1
force sw1 1
force sw2 1
run 100ns
```



(a) revision



(b) block diagram (c) wave

FIG. 3: All the needed FIG

II. DISCUSSION & CONCLUSION

Through this experiment, I learned how to install Quartus and ModelSim associated simulation, I am more familiar with the operation of Quartus software, a preliminary understanding of the VHDL language written. This experiment is very fun.

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Name (Pin Yin): Wan, Jiaqing Group: ZM1501 NAU ID: _____ Grade: 24

Name (Chinese): 万家庆

CQUPT EE310 2017 Fall Quiz 1a

(20min, 30pts)

I. (5pts) True or false

1. You can discuss the quiz questions with your classmates.
   True False ✓
2. If you catch a flu and can't come to class, it won't be counted as absence if you talked to the instructor.
   True ✓ False
3. If you sign in when you come to class but forget to sign out, it will be counted as absence
   True ✓ False
4. To pass the class with an 'C', you have to score at least 66 by the end of the semester
   True ✓ False
5. If you submit your lab report 1 week later than the due date, you will receive 10% off your lab grade.
   True ✓ False

II. Multiple answers (one or more correct answers)

6. (2pts) Which of the following behaviors are not allowed during the exams?
   A. Discuss exam questions with classmates
   B. Show your answers to other students
   C. Using cell phone as calculator
   D. borrow your note sheets or calculator to other students
   E. All of above

7. (2pts) Which of the following are improper behaviors in class?
   A. Eating snacks
   B. Taking a nap
   C. Playing your cell phone
   D. Leaving the classroom before the class is over
   E. All of above

8. (4pts) Which of the following are proper behaviors for a successful problem solver
   A. Can clearly define the problems ✓
   B. Can think of general or alternative solutions ✓
   C. Tend to manipulate symbols and equations to figure out what's going on ✓
   D. Search for similar problems, depend on pattern matching ✓
   E. Adapt their approach to the situation as needed ✓
   F. Flexible and willing to revise hypotheses to match situation ✓
   G. Can't plan how to test a hypothesis