Lab Report No. 02:

Introduction to VHDL

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I. INTRODUCTION

A. Objectives

At the completion of this lab, we will be able to:

1. Set up a Quartus II project, specify a revision, create VHDL files, and compile a design

2. Simulate and verify the correct functional operation

3. Program the Cyclone V GX Starter board with the correct pin assignments and demonstrate the correct operation of the circuit

B. Background knowledge

C. Design strategy

a. VHDL Design of an AND Gate.

b.Sequential Logic in VHDL: D Flip-flop.

c.Sequential logic in VHDL: JK flip-flop.

D. Simulation strategy

D Flip-flop			
input			output
reset	clk	d	q
key0	key1	sw0	ledr0
PIN_AA14	PIN_AA15	PIN_AB12	PIN_V16

FIG. 1: D filp-flop set

JK Flip-flop			
input			output
J	K	CLK	Q
sw0	sw1	key0	ledr0

FIG. 2: JK filp-flop set

E. Demonstration strategy

D flip-flop demonstration strategy:

In the case of key0 "0", and then press key1, if sw0 is "0",LED will not lighting, if sw0 is "1", LED will lighting. In the case of key0 "1",whenever what's others input are,the LED will not lighting.

JK flip-flop demonstration strategy:

In the case of sw0 "0" and sw1 "0", when pressed the key0, the state of LED will hold.

In the case of sw0 "0" and sw1 "1", when pressed the key0, the state of LED will clear.

In the case of sw0 "1" and sw1 "0", when pressed the key0, the state of LED will hold.

In the case of sw0 "1" and sw1 "1", when pressed the key0, the state of LED will toggle.

II. LAB DETAILS

A. Instructor questions in the lab instruction

D flip-flop question 1. Describe the operation of this circuit in terms of the effect of each input on the output.

A: Please see section I-E.

2. Why is the signal d not on the sensitivity list for the process?

A: Because the function of input signal d can store its state, only we press the clk, and d will change it's store state to new state. So it's not on the sensitivity list for the process.

JK flip-flop question 1. Describe the operation of this circuit in terms of the effect of each input on the output.

A: Please the section I-E.

2. Which signals should be included in the sensitivity list for your design? Why ?

A: the clk signal should be included in the sensitivity list for my design, because the state can only change when the clk is falling edge.

B. VHDL code

D flip-flop

```
library IEEE;
use IEEE.std_logic_1164.all;

entity d_ff is
    port(
        clk, d, reset : in std_logic;
        q : out std_logic
    );
end d_ff;

architecture basic of d_ff is
begin
   process (clk, reset)
   begin
        IF reset = '1' then                --when not press key0  led will be 0
        q <= '0';
        ELSIF clk'event AND clk = '1' then  --when pressed key0 amd click key1
        q <= d;                             --the state is what sw0 is.
        END IF;
   end process;
end basic;
```

JK flip-flop

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY jk_ff IS
  PORT (J,K:IN STD_LOGIC;
        clk : IN std_logic;
        Q: out STD_LOGIC);
end jk_ff;
ARCHITECTURE behave OF jk_ff IS
signal S:STD_LOGIC;---set another signal for output can't assignment to input
  BEGIN
    S<= (J and (not S)) or (S and (not K))  when clk'event and clk='0' ;
    Q<=S ; ---function of JK flip-flop realize
end  behave;
```

C. Block diagram

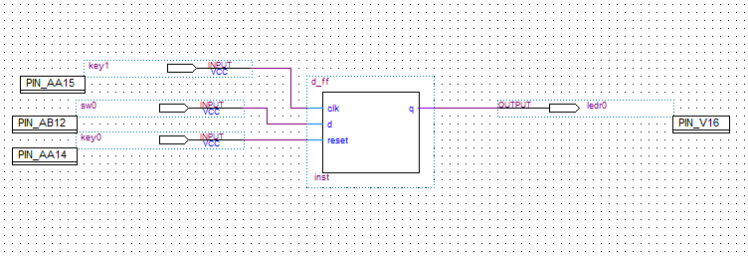

FIG. 3: D filp-flop Block diagram

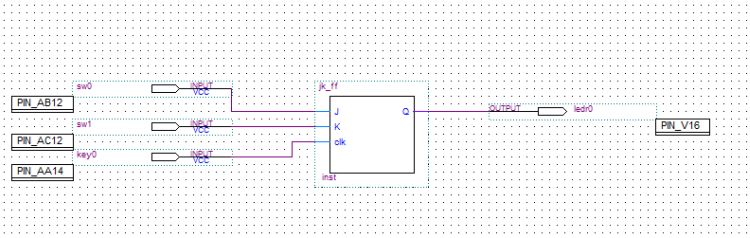

FIG. 4: JK filp-flop Block diagram

D. ModelSim force file

D Flip-flop:

```
force clk 0 0ns, 1 50ns -r 100ns
force d 0 0ns, 1 100ns -r 200ns
force reset 0 0ns,1 200ns -r 400ns
run 1600ns
```

JK Flip-flop:

```
force clk 0 0ns, 1 50ns -r 100ns
force J 0 0ns, 1 100ns -r 200ns
force K 0 0ns,1 200ns -r 400ns
run 1600ns
```

E. imulation results and detailed explanation

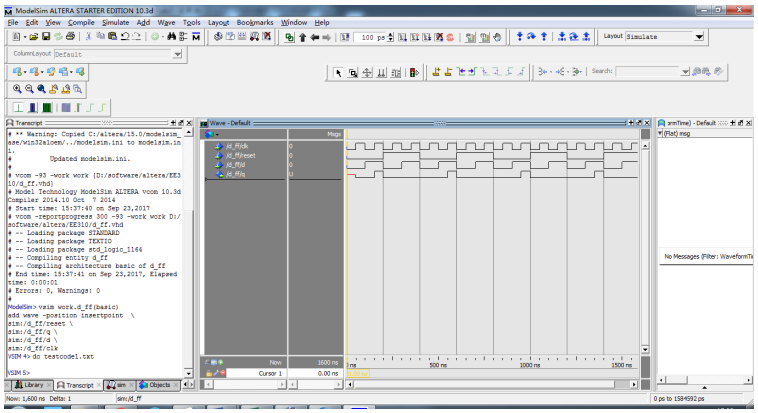

FIG. 5: D Filp-flop Wave

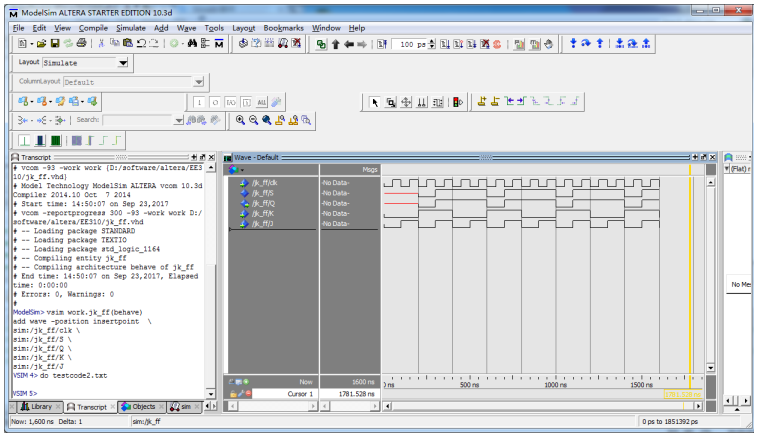

FIG. 6: JK Filp-flop Wave

F. Board demonstration result

key0	key1	**sw0**	ledr
1	x	**x**	0
0	↑	0	0
0	↑	1	1

FIG. 7: D Filp-flop Board demonstration result

J	K	CLK	Q
sw0	sw1	key0	ledr0
0	0	↓	Q
0	1	↓	0
1	0	↓	1
1	1	↓	NQ

FIG. 8: JK Filp-flop Board demonstration result

III. CONCLUSION

The lab is successful.

I realize all function we should achieve. The most difficulty things is the Instructor questions.

I refer to manual and ask classmates that I solved it.