**EE310 Fundamental of Computer Engineering**

Spring 2017 NAU

Lab 02 Quiz (15min, 20pts)

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. (10pts) Finish the following VHDL program to realize a 2-input OR gate. 3+3+4 pts

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entity or2in is*

*port(*



*)*



*end or2in;*

*architecture alu\_arch of or2in is*

*begin*



*end*

1. (5pts) Write the states table (truth table) for a falling-edge triggered D flip-flop with asynchronous reset input 1pt each line



1. (5pts) How would you modify the following VHDL to realize a falling-edge triggered D flip-flop

*process (clk, reset)*

*begin*

*IF reset = '1' then*



*q <= '0';*



*ELSIF clk'event AND clk = '1' then*



*q <= d;*

*END IF;*

*end process;*

1. (10pts) Which of following are valid identifiers, Y or N? If not, identify why.

|  |  |  |
| --- | --- | --- |
| **Y** | A |  |
| **Y** | X0 |  |
| **N** | 5bit\_counter | **must start with an alphabetic character** |
| **Y** | A0 |  |
| **N** | A0\_ | **cannot end with underline** |
| **Y** | counter |  |
| **Y** | Next\_Value |  |
| **N** | last@value | **can only use letters, digits and underline** |
| **N** | clock\_\_pulse | **cannot have two successive underline characters** |