**CQUPT EE310 2017 Fall Quiz 2b**

**(20min, 30pts)**

1. (10pts) Finish the following VHDL program to realize a 2-input AND gate.

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entity and2in is*

*port(*

*a, b : in std\_logic; 3pts*

*y : out std\_logic 3pts*

*);*

*end and2in;*

*architecture alu\_arch of and2in is*

*begin*

*y <= a and b; 4pts*

*end*

1. (5pts) Write the states table (truth table) for a rising-edge triggered JK flip-flop with asynchronous set (active low) input

1pt per combination

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Set | CLK | J | K |  |
| 0 | X | X | X | 1 |
| 1 |  | 0 | 0 |  |
| 1 |  | 0 | 1 | 0 |
| 1 |  | 1 | 0 | 1 |
| 1 |  | 1 | 1 |  |

1. (5pts) what signals should be included in the sensitivity list? -2 if miss/add one

*process (****reset, clk****)*

*begin*

*IF reset = '1' then*

*q <= '0';*

*ELSIF clk'event AND clk = '1' then*

*q <= d;*

*END IF;*

*end process;*

1. (10pts) Which of following are valid identifiers, Y or N? If not, identify why.

-1pt per mistake

|  |  |  |
| --- | --- | --- |
| **N** | \_A1 | **must start with an alphabetic character** |
| **Y** | Axd\_123 |  |
| **Y** | bit\_counter |  |
| **N** | X3\_ | **cannot end with underline** |
| **N** | A&B | **can only use letters, digits and underline** |
| **Y** | counter |  |
| **N** | Next\_\_Value | **cannot have two successive underline characters** |
| **Y** | Last12value |  |
| **Y** | clock\_pulse |  |