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**CQUPT EE310 2017 Fall Quiz 3a**

**(20min, 30pts)**

1. (4pts) For a 7-seg LED display, all outputs are active LOW.
   1. Write the input binary code to display the hexadecimal number ‘E’.
   2. What is the logic level for each output in order of abcdefg?
2. 1110
3. 0110000
4. (8pts) Read the following VHDL program and answer the questions.
   1. How many input and output ports in the entity named dec1?

1 input port and 1 output port

* 1. How many input and output pins in this circuit?

2 input pins and 4 output pins

* 1. What is the official name of the circuit realized by this VHDL code?

2-to-4 decoder

* 1. Is the output active low or active high?

Active high

library ieee;

use ieee.std\_logic\_1164.all;

entity dec1 is

port( I: in std\_logic\_vector(1 downto 0);

O: out std\_logic\_vector(3 downto 0)

);

end dec1;

architecture behv of dec1 is

begin

process (I)

begin

case I is

when "00" => O <= "0001";

when "01" => O <= "0010";

when "10" => O <= "0100";

when "11" => O <= "1000";

when others => O <= "XXXX";

end case;

end process;

end behv;

1. (5pts) Rewrite the architecture in question 2 using if statement.

architecture behv of dec1 is

begin

process (I)

begin

if I=”00” then

O <= "0001";

elsif I=”01” then

O <= "0010";

elsif I=”01” then

O <= "0100";

else

O <= "1000";

end if;

end process;

end behv;

1. (4pts) Define a variable ***pick*** of integer type, then assign value 38 to it using a separate statement.

variable pick : integer;

pick := 38;

1. (9pts) A signal is defined as std\_logic type, please explain what the following values mean.

‘U’: \_uninitialized\_\_\_\_\_\_\_\_\_\_\_\_\_ ‘X’: \_\_force unknown\_\_\_\_\_\_\_\_\_\_\_\_

‘0’: \_\_force logic 0\_\_\_\_\_\_\_\_\_\_\_\_ ‘1’: \_\_\_force logic 1 \_\_\_\_\_\_\_\_\_\_\_\_\_

‘Z’: \_\_high impedance\_\_\_\_\_\_\_\_\_ ‘W’: \_\_weak unknown\_\_\_\_\_\_\_\_\_\_\_

‘L’: \_\_\_weak zero\_\_\_\_\_\_\_\_\_\_\_\_\_ ‘H’: \_\_weak one\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

‘-‘ : \_\_don’t care\_\_\_\_\_\_\_\_\_\_\_\_\_\_