**EE310 Fundamental of Computer Engineering**

Spring 2017 NAU

Lab 04 Quiz (20min, 30pts)

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. (5pts) What are the main differences between a microprocessor and microcontroller?

Microprocessor has only the ALU, registers and control unit, microcontroller has its own memory and bus on chip!

1. (10pts) Explain the main function of following registers in a microprocessor.
   1. Program counter (PC): contains the memory address of the (current/next) instruction
   2. Instruction register (IR): holds the current instruction that has been fetched from memory
   3. Accumulator (AC): holds one operand for ALU; receives result from ALU
   4. Memory address register (MAR): holds address of memory location to be accessed
   5. Memory data register (MDR): holds data coming from/going to memory; other operand for ALU
2. (15pts) Read the following VHDL program for a IR register and finish the truth table below (binary or hex)

*entity ir is*

*port(clk,reset,load\_iru\_in,load\_irl\_in: in std\_logic;*

*data\_in: in std\_logic\_vector(7 downto 0);*

*opcode\_out,add\_val\_out: out std\_logic\_vector(7 downto 0));*

*end ir;*

*architecture syn of ir is*

*begin*

*process(clk,reset,load\_iru\_in,load\_irl\_in)*

*begin*

*if (reset='1') then*

*opcode\_out <= X"00";*

*add\_val\_out <= X"00";*

*elsif (clk'event and clk='1') then*

*if (load\_iru\_in='1' and load\_irl\_in='0') then*

*opcode\_out <= data\_in;*

*elsif (load\_iru\_in='0' and load\_irl\_in='1') then*

*add\_val\_out <= data\_in;*

*end if;*

*end if;*

*end process;*

*end syn;*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| clk | reset | Load\_iru\_in | Load\_irl\_in | Data\_in | Opcode\_out | Add\_val\_out |
| X | 1 | X | X | XX | 00 (0000 0000) | 00 (0000 0000) |
| 1st | 0 | 0 | 1 | A9 | 00 (0000 0000) | A9 (1010 1001) |
| 2nd | 0 | 1 | 0 | B8 | B8 (1011 1000) | A9 (1010 1001) |
| 3rd | 0 | 1 | 1 | 11 | B8 (1011 1000) | A9 (1010 1001) |
| 4th | 0 | 0 | 0 | CD | B8 (1011 1000) | A9 (1010 1001) |
| 5th | 0 | 1 | 0 | 35 | 35 (0011 0101) | A9 (1010 1001) |
| NOT | 0 | 0 | 1 | 35 | 35( 0011 0101) | A9 (1010 1001) |