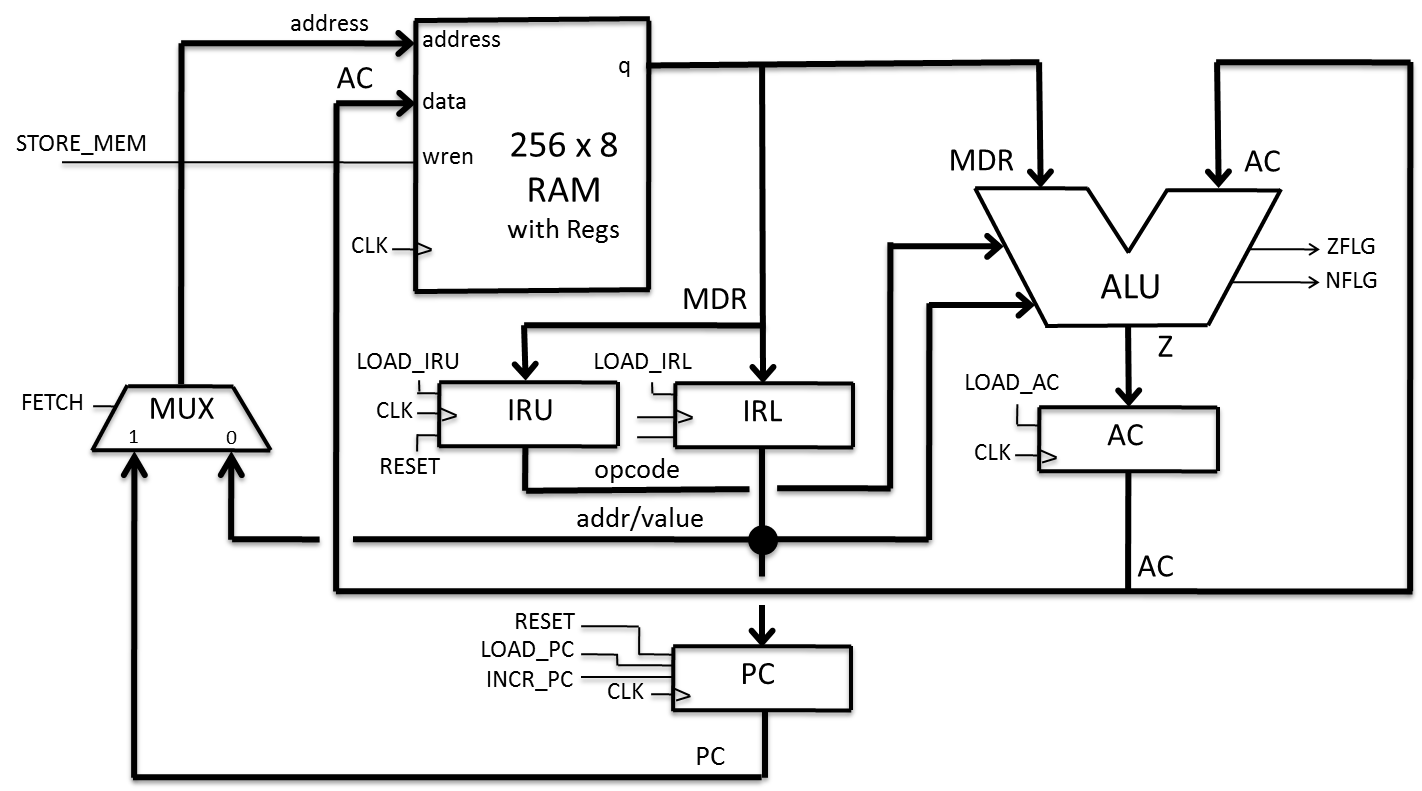
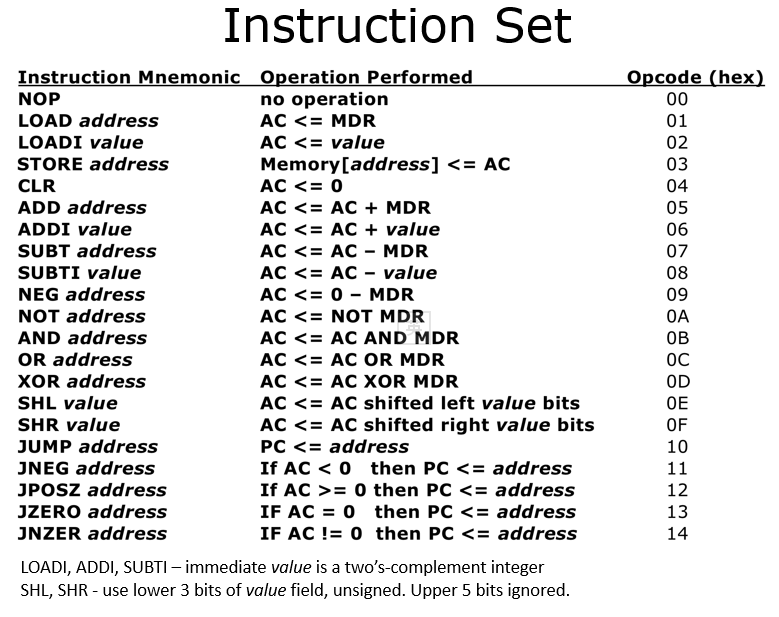
Name (Pin Yin): \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Assin. No.: \_\_\_\_\_\_

**CQUPT EE310 2017 Fall Quiz 7a**

**(20min, 30pts)**



|  |  |
| --- | --- |
| **FETCH** | **address[7..0]** source |
| **0** | **addr/value** bus |
| **1** | **PC** bus |



1. (4pts) In the picture on page 1, identify all the control signals and status signals.

Control: STORE\_MEM, LOAD\_AC, LOAD\_IRU, LOAD\_IRL, LOAD\_PC, INCR\_PC, FETCH, RESET

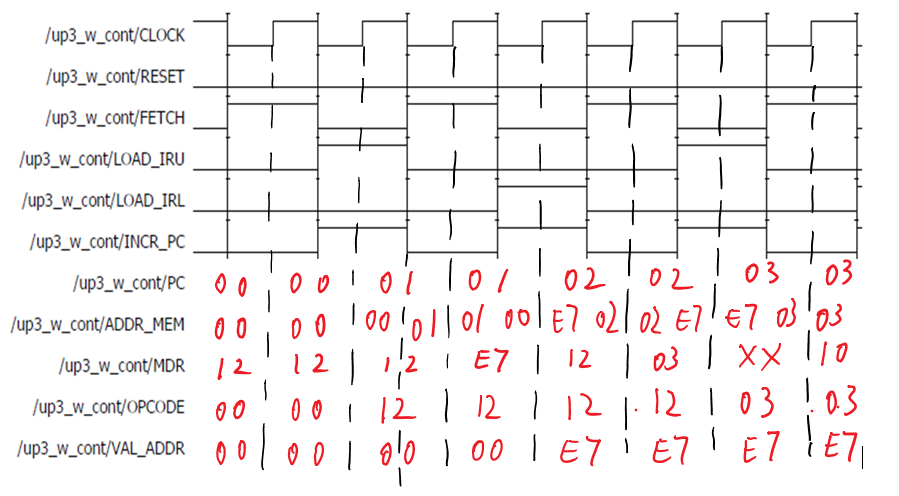
Status: NFLG, ZFLG

1. (4pts) For the following values in AC, determine the output value for ZFLG and NFLG.

|  |  |  |
| --- | --- | --- |
| AC | ZFLG | NFLG |
| 00 | 1 | 0 |
| E9 | 0 | 1 |

1. (12pts) Read the data path diagram on page 1. If the first eight memory locations contain the following hex data: 12, E7, 03, 10, 09, EE, 0A, 0E, finish the timing diagram below. (assume all registers are cleared at the beginning and use “XX” for unknown values)

4pts each waveform, check each value in each clock cycle, -1pt each error.





1. In the instruction fetch cycle, our control unit has 5 states: Start, PrepU, FetchU, PrepL, and FetchL, and our control input is RESET, outputs are FETCH, LOAD\_IRU, LOAD\_IRL, and INCR\_PC.
   1. (5pts) Read the description of each state, finish the table below 1pt each blank

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| States | **Description** | RESET | FETCH | LOAD\_IRU | LOAD\_IRL | INCR\_PC |
| Start | Reset all registers except AC | 1 | 0 | 0 | 0 | 0 |
| PrepU | Prepare for upper byte instruction fetch | 0 | 1 | 0 | 0 | 0 |
| FetchU | Fetch upper byte of instruction | 0 | 0 | 1 | 0 | 1 |
| PrepL | Prepare for lower byte instruction fetch | 0 | 1 | 0 | 0 | 0 |
| FetchL | Fetch lower byte of instruction | 0 | 0 | 0 | 1 | 1 |

* 1. (5pts) Draw the state diagram -1pts each error

