University of Washington
Department of Electrical Engineering
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Laboratory Project Design #1:
Capacitance Meter

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Objective

The objective of this project is to design a digital capacitance meter which can accurately separate the capacitance of a device under test (DUT) from its overall admittance, which may have both a conductance and capacitive part, $Y = G + j\omega C$. The meter will operate by applying a test excitation sine wave to the DUT, measuring the resulting current that flows, and then demodulating this current with a synchronous phase detector that will separate the real and imaginary parts. Low pass filtering of the output from the phase detector will then create a DC voltage that is proportional to either the real or imaginary parts of the DUT admittance. This DC voltage can then be displayed on an LCD digital panel meter and scaled to read the capacitance of the DUT in units of nanofarads (nF).

Introduction

There are many ways to measure capacitance, including charging the capacitor with a known current and measuring the resulting voltage, or inserting the capacitor in a bridge circuit. This project employs another method, namely applying an oscillating voltage of a known frequency and amplitude and measuring the resulting current through the capacitor.

This can be accomplished by taking advantage of the trigonometric double-angle formula:

$$cos(2\theta) = 2cos^2(\theta) - 1$$

Multiplying two sinusoidal voltages of the same frequency and phase will result in another voltage waveform with twice the frequency. If one waveform input is selected as the reference voltage, the second input will be the output of the capacitor. Since the current through a capacitor leads the voltage by 90 degrees, the input voltage should have a 90 degree phase shift relative to the reference voltage.

Reference Voltage:	$Acos(\theta)\ V$
Input Voltage to Capacitor	$Acos(\theta - 90^o)\ V$

The current through the capacitor will need to be converted to a voltage before being multiplied with the reference voltage; this can be accomplished by using a current-to-voltage converter.

Then finally, once the two waveforms are multiplied, the output should be filtered to remove the oscillation resulting in a DC signal that is proportional to the capacitor tested.

More detail about the circuit can be found in the “Circuit Design” section following.

Equipment and Materials Used

- AD633JNZ IC Analog Multiplier 8-DIP
- NE5532 Dual Low-Noise Operational Amplifier (2)
- 1N4148 Diode (2)
- Resistors
- Capacitors

- Power Supply
- Function Generator
- Oscilloscope

Procedures

1. Multiply the input signal and the reference signal
2. In order to achieve high degree of phase accuracy, create the in-phase signal and the quadrature signal at the same time using the quadrature oscillator.
3. Make sure that the excitation and reference signals have no DC offsets in order for the analog multiplication to perform properly.
4. Make sure that the excitation and reference signals are bipolar and symmetrical signals(i.e the sine wave that is centered about zero)
5. Use the low pass filter to remove the irrelevant modulation components.
6. Multiply two sinusoids of the same frequency together in order to obtain a DC component and a component that is doubled from the original frequency.
7. Set the input at 10 kHz in order for the DC component and the 20 kHz component to be created.
8. Use the low pass filter to remove the 20 kHz component.
9. Send the DC component to the digital panel meter.
10. Have one terminal of the DUT connected to the output of the sine wave oscillator.
11. Have the other terminal of the DUT connected to the input to a I-V converter. Make sure that the virtual short at the input to the I-V converter will keep this terminal at ground level, and make sure it allows the sinusoidal voltage across the device to remain undisturbed by the resulting current level.

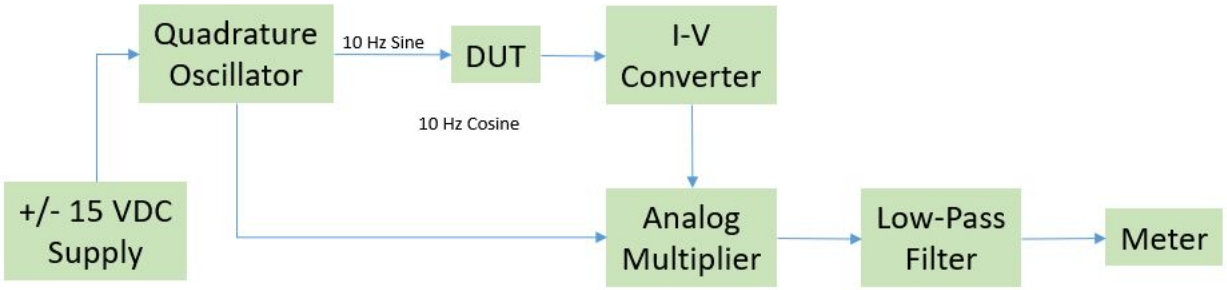
Circuit Design

The system requirements are provided in the table below, as well as a description of which portions of the circuit would meet the requirements:

Reqt ID	Reqt Text	Implementation Plan
1	The entire system must operate from only a bipolar +/- 15 VDC power supply. (No batteries are needed.)	Use bench power supply.
2	The output of the meter will be displayed on a 3.5 digit LCD panel meter with correct positioning of the decimal point or bench meter.	Scale circuit output to be compatible with range of 3.5 digit LCD panel meter (1 VDC reference voltage)
3	The excitation signal must be a 10 kHz sine wave with a peak amplitude of 1.0 Volt, created by an oscillator that is part of the system.	Use quadrature oscillator subcircuit.
4	The reference signal must be a symmetrical bipolar signal that is in quadrature (90 degrees) phase with, and derived from, the excitation signal.	Use quadrature oscillator subcircuit.
5	The meter must have 3 ranges with displays of N.NNN, NN.NN, and NNN.N nanofarads. Switching between ranges must be accomplished by changing no more than three wires on the breadboard. (Range switching does not have to be automatic.)	Operational Amplifier with discrete selectable gains.
6	The meter must display the capacitance of the device under test (DUT) to an accuracy of 5% over a range of shunt conductances which are 1/10th to 10 times the susceptance of the DUT.	Component value selection
7	The system must have one potentiometer that can be used to zero the meter when the input is open circuited (zero adjust).	Voltage Bias
8	The system must have one additional potentiometer that can be used to calibrate the reading to a known capacitor (span or gain adjust).	Operational Amplifier with discrete selectable gains

9	The cost of the parts to create this system must be minimized.	Use supplied parts.

The capacitance metering system is comprised of several subcircuits, as illustrated in the figure below:



Quadrature Oscillator

The quadrature oscillator produces two sinusoidal outputs with a phase difference of 90 degrees. The example circuit provided in the textbook[1] was selected as a template. The example circuit was designed to operate with a rail-to-rail voltage of +/-10 VDC and the output signal had an amplitude of 5 VDC and a frequency of 1 kHz. Since the requirements specify a rail-tail voltage of +/- 15VDC, an amplitude of 1 VDC and a frequency of 10 kHZ, the circuit was modified by selecting different values for C1 and C2 to produce the desired frequency, and the value of R7 was modified experimentally in the simulation until the output signal was at the desired amplitude.

It should be noted that while the textbook problems frequently refer to the use of standard resistor values, the values specified in the example circuit, namely 159 kΩ, are not standard values. The standard 1% value of 158 kΩ was used instead. To reduce the expense of the system, the provide op-amps, NE5332, were selected.

The output of this subscircuit:

Reference Voltage: $A\cos(\theta)\ V$

Input Voltage to Capacitor $A\cos(\theta - 90^o)\ V$

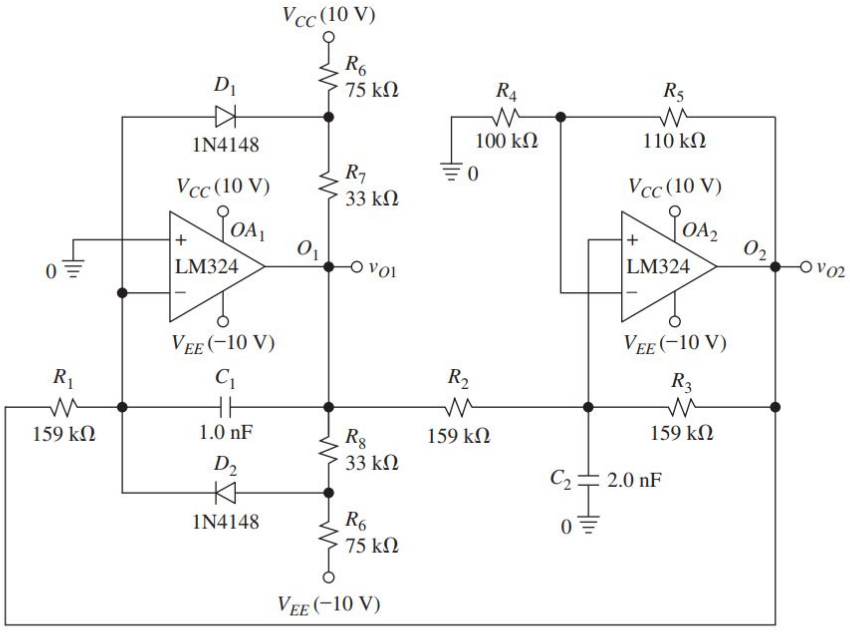


Figure 1. Example Quadrature Oscillator Circuit from Textbook.

[1] "Design with Operational Amplifiers and Analog Integrated Circuits", Franco, Sergio. Figure 10.6

Device Under Test (DUT) and Current-to-Voltage (I-V) Converter

The DUT for purposes of this project were 1, 10 and 100 nF capacitors. To provide a voltage input to the multiplier, one of the oscillator's outputs is applied to the DUT, and the resulting current converted to a voltage by means of a simple Current to Voltage Converter, as shown below.

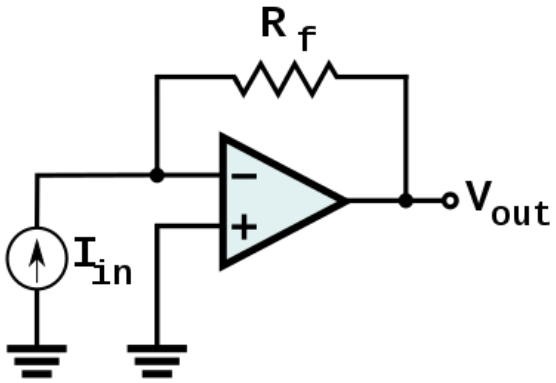


Figure 2. Simple Current-to-Voltage Converter Schematic (Source: Wikipedia)

The output, Vout is equal to I_in * Rf. The value of Rf can be selected or adjusted to change the value of the converter's output to calibrate the system.

The current through the capacitor is equal to the input voltage divided by the impedance shifted by 90 degrees:

$$Icap = \frac{A(cos\theta)}{\frac{1}{\omega C}} = AC\omega(cos\theta)$$

And the output of the I-V Converter:

$$V\,out = ARC\omega(cos\theta)$$

Analog Multiplier

The output of the I-V converter and the second output of the quadrature oscillator are multiplied by the analog multiplier subcircuit. Again, to reduce the cost of the system, the provided multiplier AD633 was selected. The basic connections are shown below.

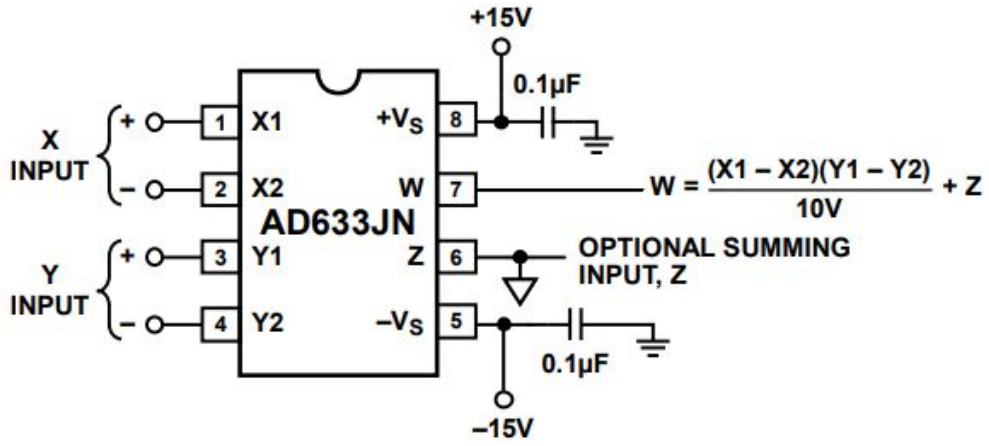


Figure 3. Basic AD633 Connections (Source: Analog Devices Datasheet)

The output from the oscillator was connected to Pin 1 (X1) and the output of the I-V connector was connected to Pin 3 (Y1). Pins 2 (X2) and 4 (Y2) were grounded. Pin 6 (Z) can be connected to a variable voltage divider to provide an offset to the output. This can be used to zero the output when no DUT is installed.

The output of the analog multiplier:

$$V\,out = ARC\omega(cos\theta) * A(cos\theta)/10 = A^2RC\omega(cos\theta)^2 = (1/2)(A^2RC\omega)(cos(2\theta) + 1)$$

The above expression has two parts: an oscillating component $(1/2)(A^2RC\omega cos(2\theta)$, and a DC component: $(1/2)(A^2RC\omega)$

Low-Pass Filter

The output of the multiplier is an oscillating signal with twice the frequency of the input signals and a DC offset that is proportional to the capacitance value. Filtering out the high-frequency portion of the signal will result in the DC value which can be used to represent the capacitance of the DUT.

To accomplish this an active single-stage non-inverting low pass filter is used. The general schematic of this filter is shown below.

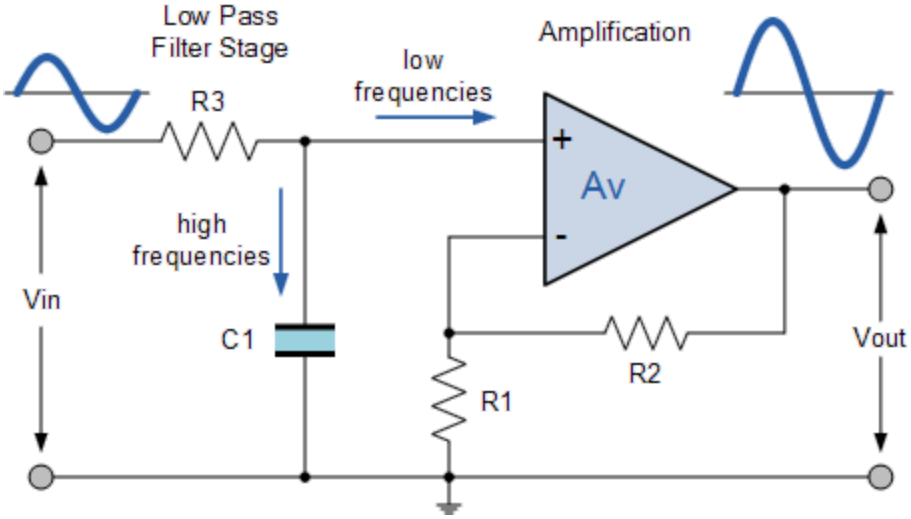


Figure 4. Generic Single-Stage Active Low-Pass Filter Amplifier Schematic
(Source: www.electronics-tutorials.ws)

The cut-off frequency is equal to 1/(2*π*R3*C1). Since it is desired to remove the 20 kHz component of the multiplier output, a cutoff frequency of 10 kHZ was selected. Selecting a value of 10nF for C1 results in a standard 1% resistor value of 1.58 kΩ for R3.

The output gain is equal to (1+R2/R1). Initially a value of 1 kΩ was selected for both R1 and R2 to produce a unity gain, but the value of R2 can be modified to adjust the output of the circuit to accommodate different voltage ranges.

So, the value of the output of the low-pass filter is: $(1/2)(A^2RC\omega)$

Since A is specified as 1 volt, and the frequency is specified as 10 kHz, then the value of R (the feedback resistor in the I-V converter) should be 31.8 ohms if the voltage output is desired to be 1 mV per nanofarad of capacitance.

Simulation

Multisim was used to simulate the circuit prior to its layout on a breadboard. Since it wasn't practical to simulate the entire system at once, the simulation was divided into two parts: the oscillator and everything else.

Quadrature Oscillator

A schematic of the simulated Quadrature Oscillator is shown below.

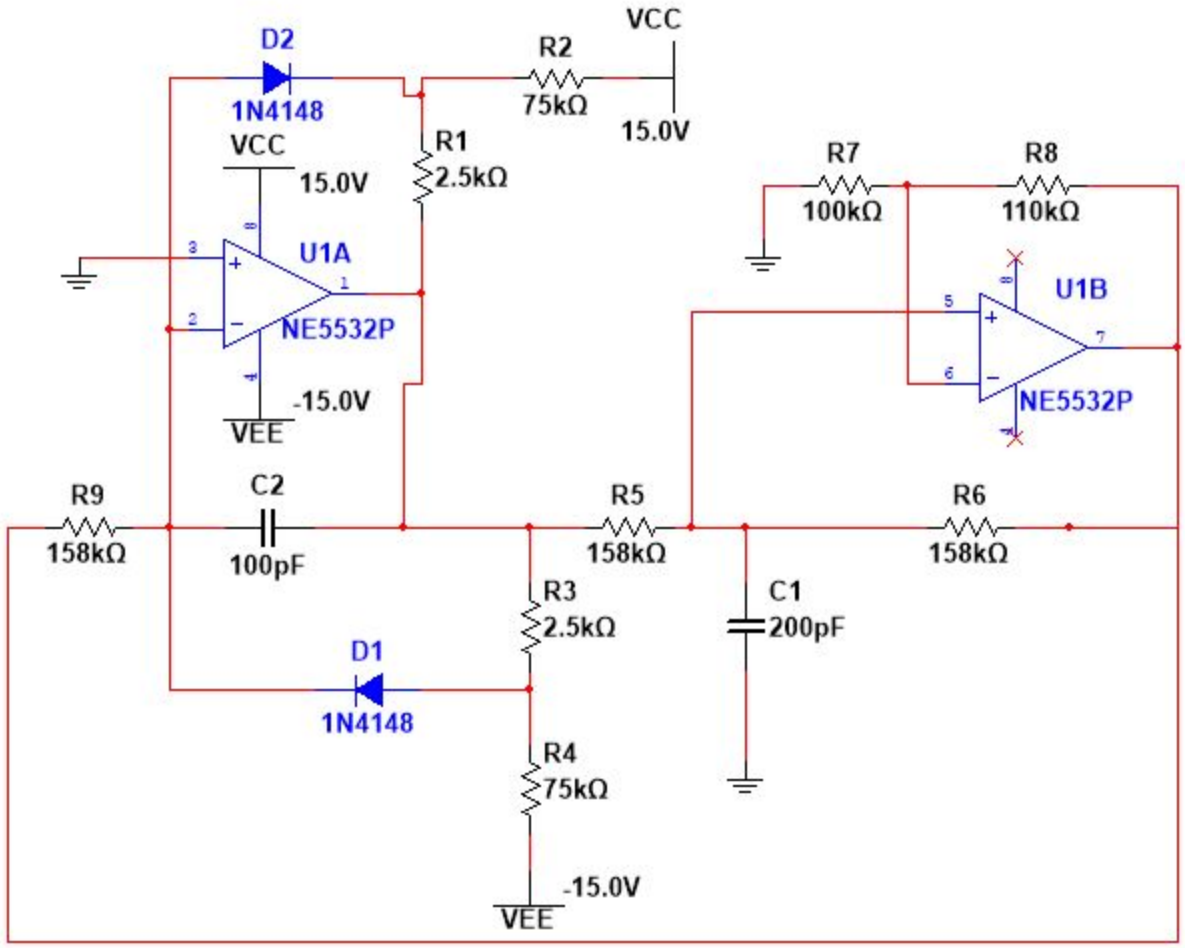


Figure 5. Quadrature Oscillator Circuit as Modeled in Multisim

The output of UIA (Pin 1) and UIB (Pin 7) are shown below, demonstrating the two 1 kHz, 1 V amplitude signals, with 90 degrees of phase difference:

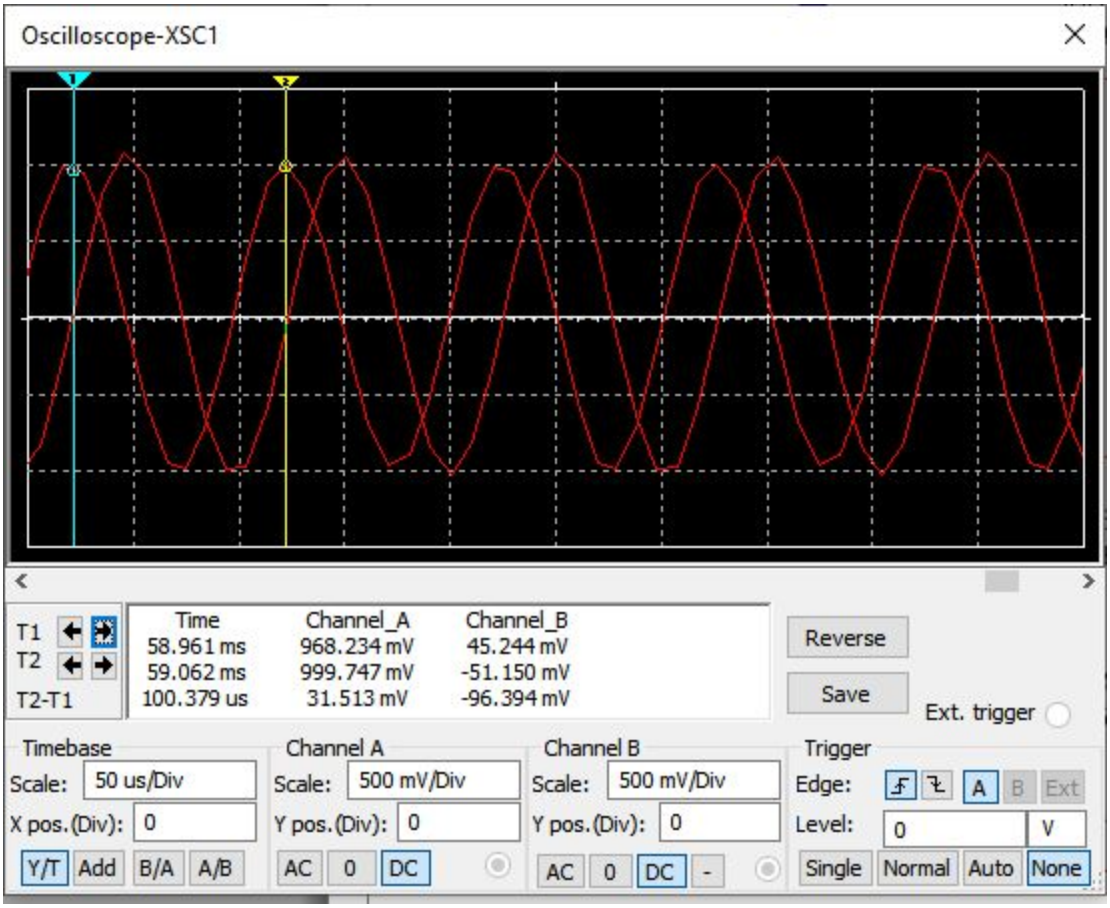


Figure 6. Multisim Quadrature Oscillator Simulation Output

The values of R1 and R3 were changed experimentally with potentiometers until the desired amplitude was achieved.

I-V Converter, Analog Multiplier and Low-Pass FIlter

This portion of the simulation was less definitive. Since the output of the quadrature oscillator could not be used in this portion, the Multisim function generators were used. However, the phase difference could not be simulated, and so the same signal was applied to both the I-V converter and multiplier. The function of the individual subcircuits could be validated, but not the end-to-end function. The circuit as simulated in Multisim is shown below:

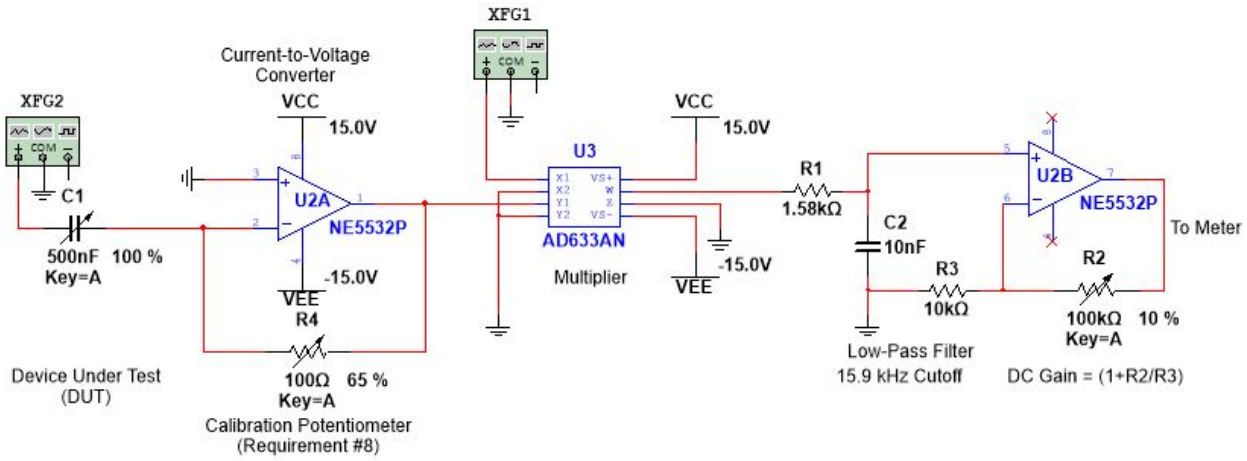


Figure 7. I-V Converter, Analog Multiplier and Low-Pass Filter as Modeled in Multisim

The circuit behaviour in the simulation, while not exactly representative of the actual circuit, did demonstrate the DC signal proportional to the capacitive value of the DUT:

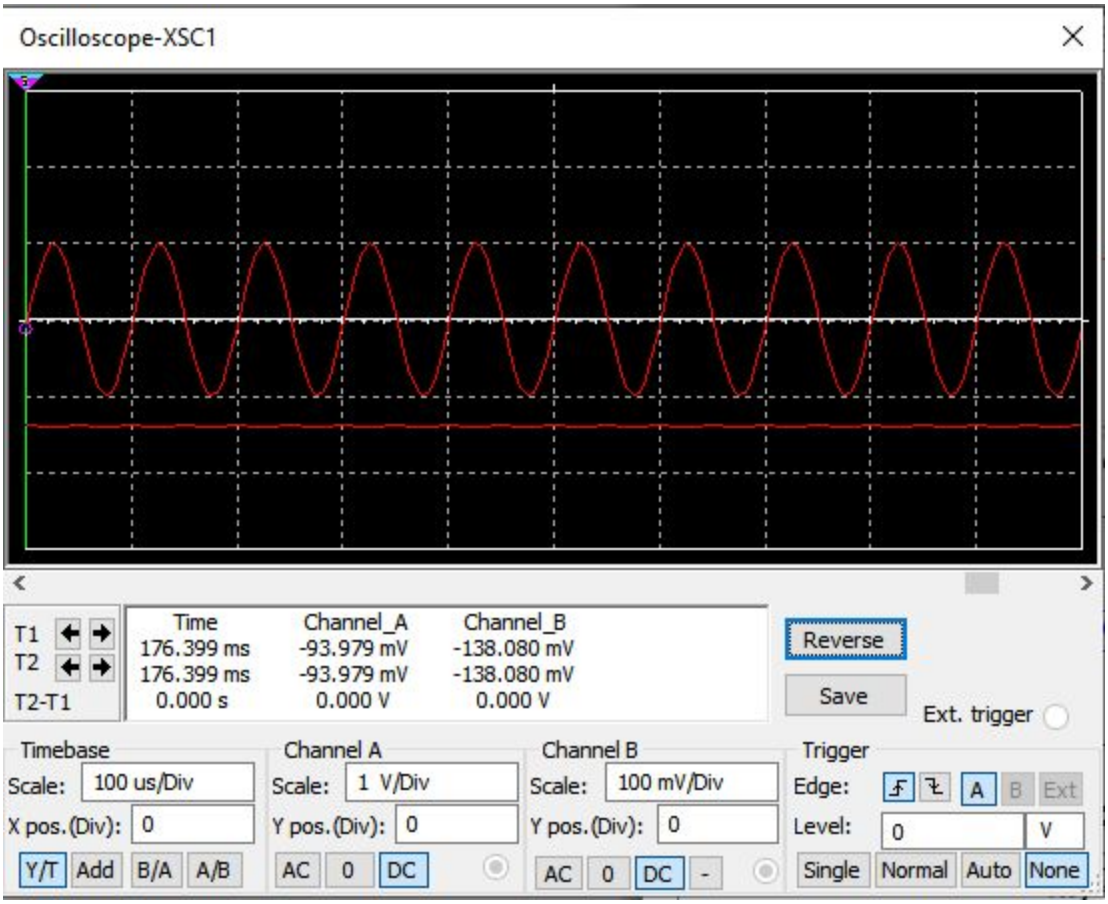


Figure 8. Multisim I-V Converter, Multiplier and Filter Simulation Output

Circuit Construction

The circuit was prototyped on solderless breadboards with the oscillator on one breadboard, and the I-V converter, analog multiplier and low-pass filter on another breadboard.

The oscillator proved problematic to prototype due to its complexity. Additional frustration was experienced due to a faulty breadboard--they are limited in the number of times they can be used before they begin to stop working. Some resistor values had to be changed on the board to get the desired amplitude, but in the end two nice, clean oscillating waveforms were achieved.

The multiplier circuit also proved challenging, mainly due to the fact that the test team was provided a faulty AD633 IC, and many hours were spent vainly trying to troubleshoot the circuit. However, on the last day of the project period a new AD633 chip was obtained and a working multiplier circuit was constructed.

Circuit Verification

Quadratic Oscillator

We built our quadratic oscillator designed in Figure 5 to create a sine and cosine wave with amplitude of 1 V and frequency of 10 kHz. Measuring the outputs of the two op-amps on our NE5532 IC, we see they match with our simulations.

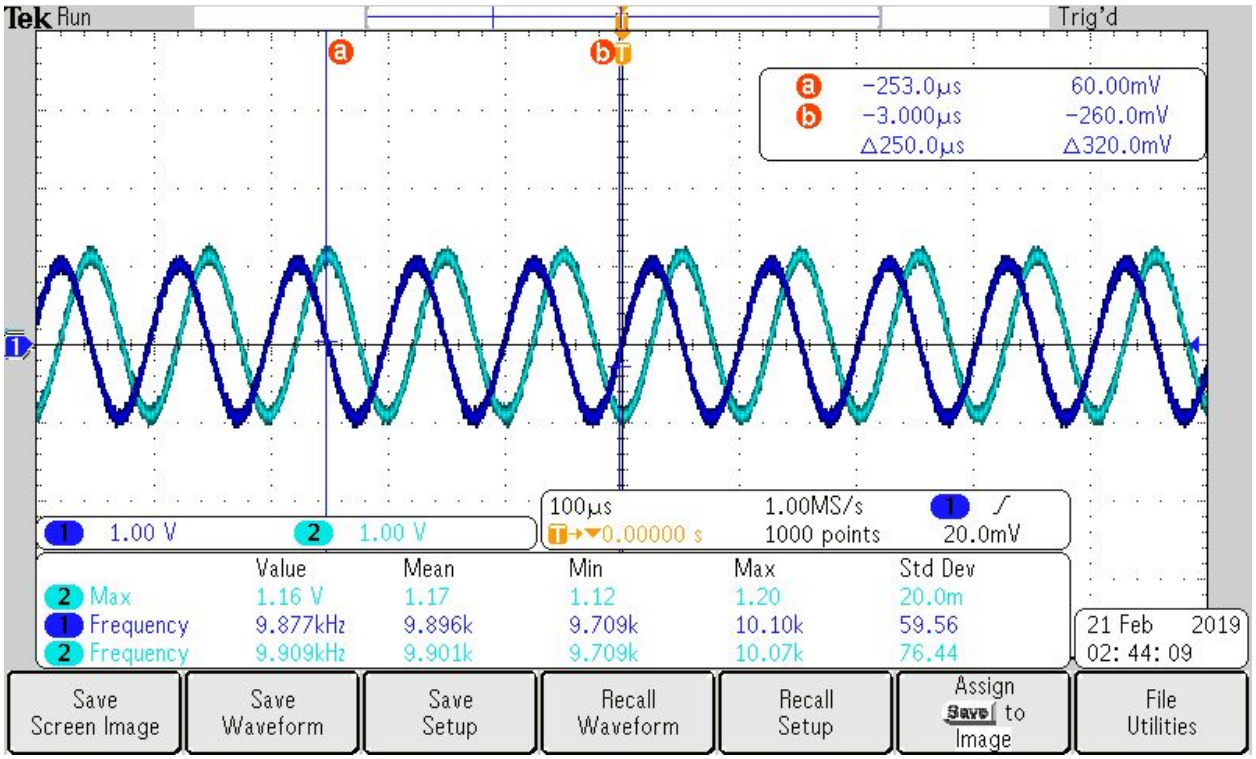


Figure 9. Oscilloscope quadratic oscillator outputs

Analog Multiplier

We run the sine signal through our device under test to produce an output current 90 degree phase shifted into a cosine signal with the same amplitude. Once we have our two oscillating cosine signals, we run it through the AD633 Analog Multiplier IC to produce an output with half the amplitude and double the frequency.

Running our two cosine signals into the AD633 multiplier we expect to see to see an output with twice the frequency and half the amplitude. Our screenshot below shows our multiplier circuit follows our design and simulation.

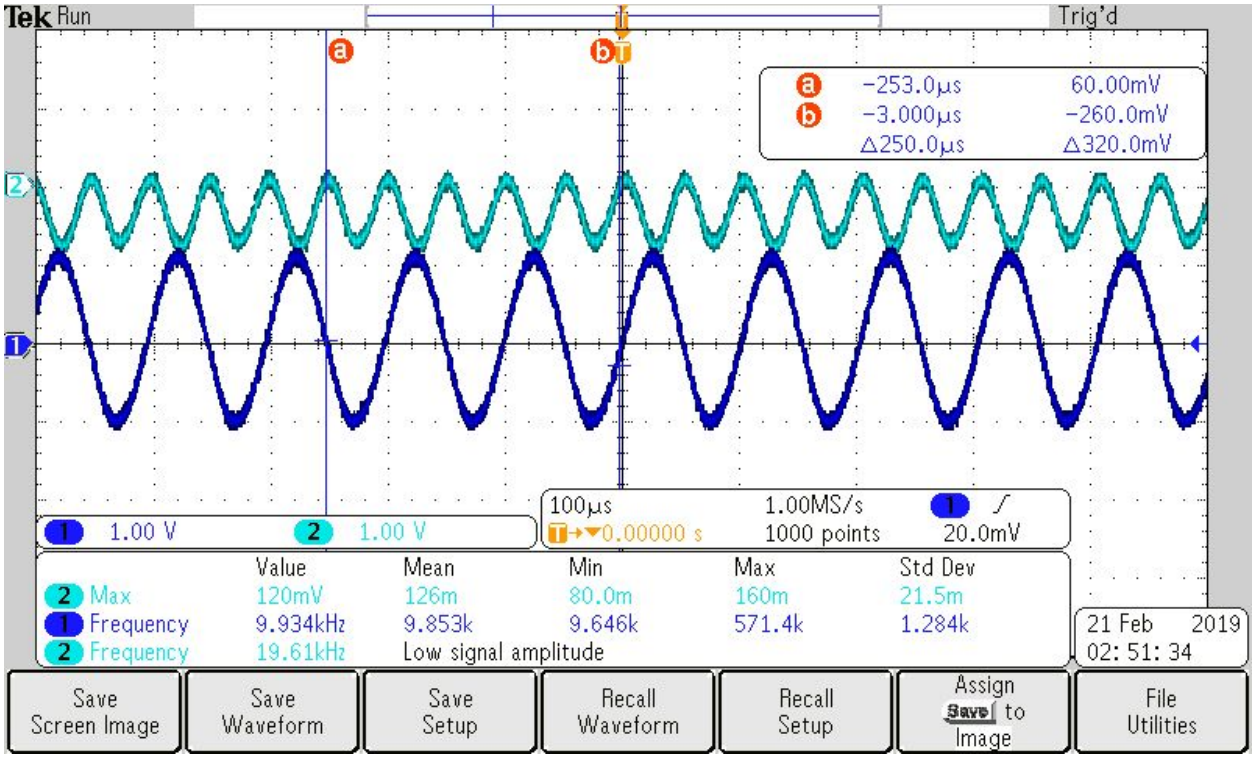


Figure 10. Oscilloscope with one input and the multiplied output

In the final stage of our circuit we use low pass filtering to create the voltage reading proportional to the capacitance of the capacitor under test. For our filter we used a gain factor of -11 with a 100k and 10k resistor. Our resulting measurements with a DMM are shown below.

Capacitor Under Test	Measured Voltage	mV / nF
1 nF	-13 mV	13
10 nF	-165 mV	16.5
100 nF	-1.43 V	14.3

Conclusion

The project challenged us to design, simulate, and build a circuit given an objective and specifications for the final product using the material we learned in class. Our final circuit was able to perform all of the requirements of the project minus the switching between ranges of the readings. The circuit also had a level of inaccuracy in the final readings from our filter that could have been improved. Due to the weather barring us from using the campus facilities, we were short on time to properly build and test our circuit. We also spent a considerable amount of time attempting to troubleshoot our multiplier chip as did the rest of the classroom before we were given a working replacement on the day of testing. We chose to present our circuit that day rather than take the 5% penalty for each day past the presentation deadline. This caused the final measurements in our presentation to be from a different edition than the one in our data.

References

AD633JNZ IC Analog Multiplier 8-DIP
NE5532 Dual Low-Noise Operational Amplifier