

# **AD246A Datasheet**

**Zhuhai Jieli Technology Co.,LTD**

**Version 1.0**

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## Revision History

Date	Revision	Description
2025.03.05	V1.0	Initial Release.

# Table of Contents

Revision History .....	1
Table of Contents .....	2
AD246A Features .....	3
1 Block Diagram .....	4
2 Pin Definition .....	5
2.1 Pin Assignment .....	5
2.2 Pin Description .....	6
3 Electrical Characteristics .....	8
3.1 Absolute Maximum Ratings .....	8
3.2 ESD Ratings .....	8
3.3 PMU Characteristics .....	8
3.4 IO Characteristics .....	9
3.5 Audio DAC Characteristics .....	10
3.6 Class-D Speaker Driver Characteristics .....	11
3.7 Audio ADC Characteristics .....	12
4 Package Information .....	14
4.1 QFN32(4mm*4mm) .....	14
5 IC Marking Information .....	15
6 Solder-Reflow Condition .....	16
7 Storage Condition .....	17
7.1 Moisture Sensitivity Level .....	17
7.2 Storage Alert .....	17

# AD246A Features

## SYSTEM

- 32bit Dual-Issue DSP 240MHz
- I-cache
- Support SDTAP/EMU
- On-chip SRAM 52kbyte(share cache ram 20k)
- NOR Flash controller
- Internal RC oscillator,PLL

## Audio

- 1 x 16bit DAC
  - ❖ SNR 96dB
  - ❖ Noise 11uVrms
  - ❖ Sampling rate 8~96kHz
- 1 x 16bit Class-D Speaker Driver
  - ❖ SNR 95dB
  - ❖ Sampling rate 8~96kHz
  - ❖ Drive speaker directly 500mW@4Ω
- 1 x 16bit ADC
  - ❖ SNR 96dB
  - ❖ Sampling rate 8~48kHz
  - ❖ Support Speaker for microphone
- I<sup>2</sup>S AUDIO Master/Slave interface

## Peripherals

- 1 x Full speed USB
- 1 x SD host controller
- 3 x Multi-function 16bit timer
- 2 x UART interface
- 1 x I<sup>2</sup>C Master/Slave interface
- 3 x SPI Master/Slave interface
- 4 x MCPWM
- 1 x GPCRC
- 1 x 10bit GPADC(16 Channels)
- 20 x GPIO Support function remapping

## PMU

- Soft off current: <3uA
- Music mode: <6mA@HSB 96M
- LVD range(3bit):1.7V~2.4V, step100mV
- HPVDD range 1.8V to 5.5V
- VPWR range 1.8V to 5.5V

- IOVDD range 2.1V to 3.6V

## Packages

- QFN32(4mm\*4mm)

## Temperature

- Operating temperature  
TC = -20℃ to +85℃(standard range)  
TC = -40℃ to +105℃(extended range)
- Storage temperature -65℃ to +150℃

## Applications

- Sound Toy
- Audio player

## 1 Block Diagram

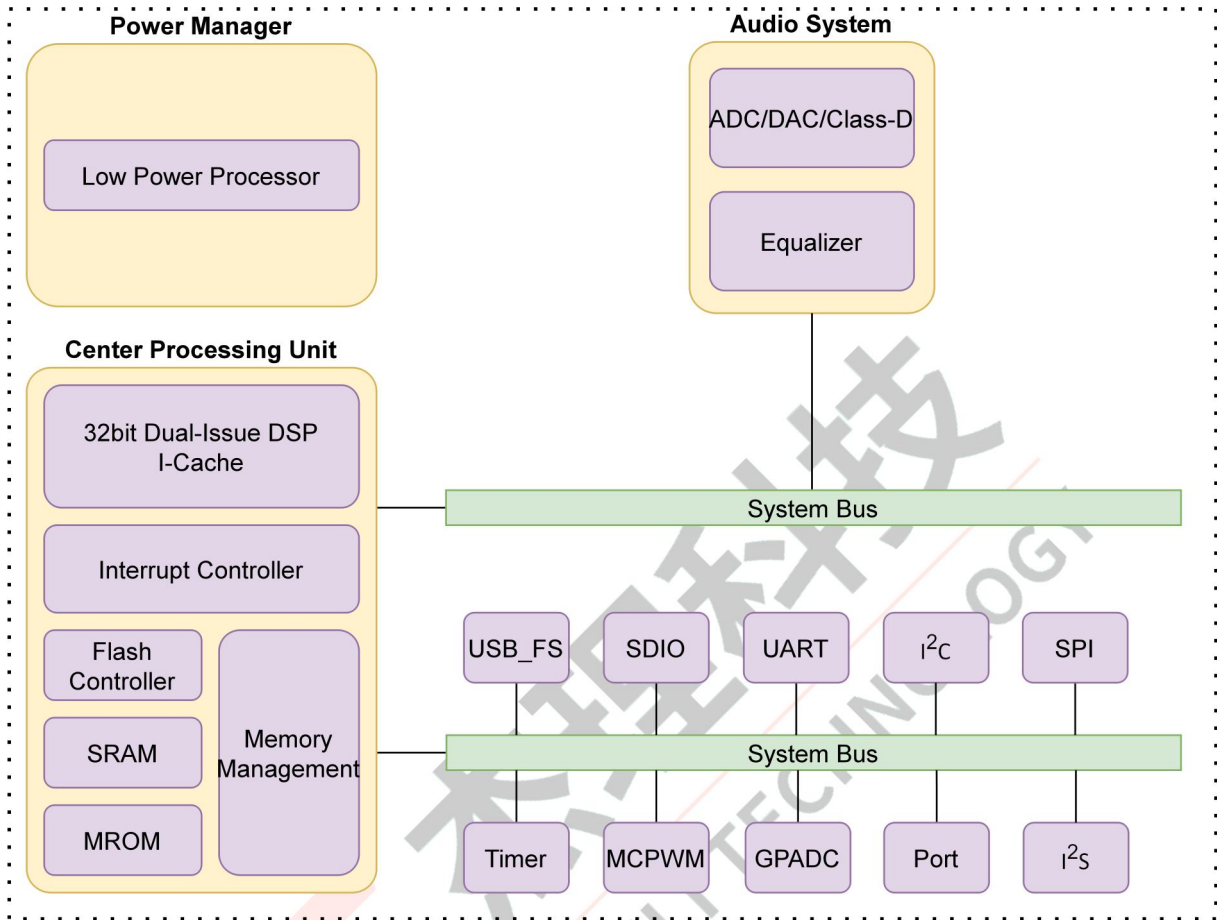


Figure 1-1 AD246A Block Diagram

## 2 Pin Definition

### 2.1 Pin Assignment

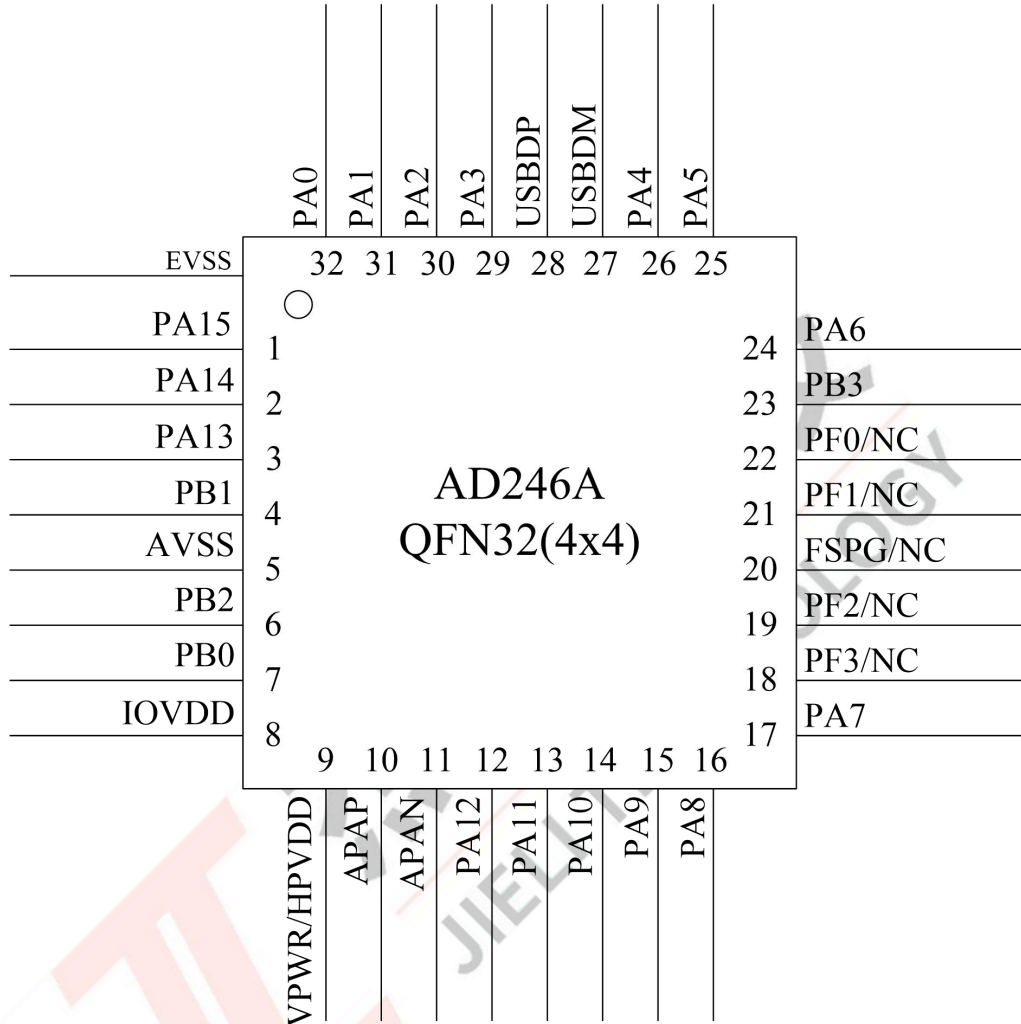


Figure 2-1 AD246A Pin Assignment

## 2.2 Pin Description

Table 2-2-1 AD246A Pin Description

Pin No.	Name		Type	IO Initial State	Description
1	PA15		I/O	Z	AIN_AN(Audio ADC negative Input) ADC14(ADC Input Channel 14)
2	PA14		I/O	Z	AIN_A2(Audio ADC Positive Input) ADC13(ADC Input Channel 13)
3	PA13		I/O	Z	AIN_A0(Audio ADC Positive Input) MICBIAS(MIC Bias Output) ADC12(ADC Input Channel 12)
4	PB1		I/O	Z	AIN_A1(Audio ADC Positive Input)
5	AVSS		G	--	Audio Ground
6	PB2		I/O	Z	--
7	PB0		I/O	Z	DAC(AUDIO DAC output) ADC15(ADC Input Channel 15) LVD(External Low Voltage Detection Input)
8	IOVDD		P	--	IO Power
9	VPWR		P	--	Chip main power supply
	HPVDD		P	--	Audio Power
10	APAP		O	--	Class-D Speaker Driver Positive Output
11	APAN		O	--	Class-D Speaker Driver Negative Output
12	PA12		I/O	Z	ADC11(ADC Input Channel 11) I <sup>2</sup> S_LRCK
13	PA11		I/O	Z	ADC10(ADC Input Channel 10) I <sup>2</sup> S_SCLK
14	PA10		I/O	Z	ADC9(ADC Input Channel 9) I <sup>2</sup> S_DATA1
15	PA9		I/O(HVT)	10kΩ Pull-down	I2S_DATA0 Firmware Download Interface
16	PA8		I/O(HVT)	10kΩ Pull-up <b>*Note1</b>	I <sup>2</sup> S_MCLK MCLR(Device Reset) <b>*Note1</b>
17	PA7		I/O	Z	NOR Flash D2A NOR Flash D3B
18	A0	PF3 <b>*Note2</b>	NIO	--	NOR Flash CSA NOR Flash D0B
	A2/4	NC			
19	A0	PF2 <b>*Note2</b>	NIO	--	NOR FlashD1A NOR Flash CLKB
	A2/4	NC			

Pin No.	Name		Type	IO Initial State	Description
20	A0	FSPG *Note2	O	--	NOR Flash Power Gate
	A2/4	NC			
21	A0	PF1 *Note2	NIO	--	NOR Flash CLKA NOR FlashD1B
	A2/4	NC			
22	A0	PF0 *Note2	NIO	--	NOR Flash D0A NOR Flash CSB
	A2/4	NC			
23	PB3		I/O	Z	NOR Flash D3A NOR Flash D2B
24	PA6		I/O	Z	ADC8(ADC Input Channel 8)
25	PA5		I/O	Z	ADC7(ADC Input Channel 7) SPI0_DATA3(C)
26	PA4		I/O	Z	ADC6(ADC Input Channel 6) SPI0_DATA2(C)
27	USBDM		I/O	15kΩ Pull-down	USB Negative Data ADC5(ADC Input Channel 5)
28	USBDP		I/O	15kΩ Pull-down	USB Positive Data ADC4(ADC Input Channel 4)
29	PA3		I/O	Z	ADC3(ADC Input Channel 3) SPI0_DATA1(C)
30	PA2		I/O	Z	ADC2(ADC Input Channel 2) SPI0_DATA0(C)
31	PA1		I/O	Z	ADC1(ADC Input Channel 1) SPI0_CLK(C)
32	PA0		I/O	10kΩ Pull-up *Note1	ADC0(ADC Input Channel 0) Hold down 0 to reset *Note1
PAD	VSS		G	--	Ground

**Note**

- 1.10kΩ Pull-up and Hold down 0 to reset function can be disable by efuse in IO Initial State.
- 2.The GPIO is uncontrollable during the initial process.
- 3.IO initial state abbreviations Z--High resistance, H--High level, L--Low level, X--May be changed during power on.
- 4.Timer, MCPWM, UART, I<sup>2</sup>C, SPI1/2 and SDIO functions can be remapped to any I/O.

**Table 2-2-2 Pin Types Description**

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
G	Ground	I	Input
NIO	NOR Flash IO	O	Output



## 3 Electrical Characteristics

### 3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T <sub>opt</sub>	Operating temperature	-20	+85	°C
T <sub>stg</sub>	Storage temperature	-65	+150	°C
VPWR	Supply Voltage	-0.3	6	V
HPVDD		-0.3	6	V
IOVDD		-0.3	3.6	V
GPIO	Input voltage of GPIO (except PA8/PA9)	-0.3	3.6	V
HVTIO	Input voltage of HVT-IO (PA8/PA9)	-0.3	5.5	V

**Note**

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

### 3.2 ESD Ratings

Table 3-2 ESD Ratings

Parameter	Typ	Test pin	Reference standard
Human Body Mode	±4kV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2kV	All pins	ANSI/ESDA/JEDEC JS-002-2022

### 3.3 PMU Characteristics

Table 3-3 PMU Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPWR	Power supply	--	1.8	5	5.5	V
<b>Operating mode</b>						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Voltage output	--	--	3	--	V
	Loading current	IOVDD=3.0V@VPWR = 5V	--	--	120	mA
<b>Low Power mode</b>						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Loading current	IOVDD=3.0V@VPWR = 5V	--	--	10	mA

**Note**

1. When powered by two dry batteries, the VPWR needs to be merged with IOVDD.

### 3.4 IO Characteristics

Table 3-5 IO Characteristics

Input Characteristics						
Symbol	Parameter	Conditions	IO	Min	Max	Unit
V <sub>IL</sub>	Low-Level Input Voltage	IOVDD = 3.0V	PA0~PA15 PB0~PB3 USBDP USBDM	-0.3	1.3	V
V <sub>IH</sub>	High-Level Input Voltage	IOVDD = 3.0V	PA0~PA7 PA10~PA15 PB0~PB3	1.7	3.3	V
		IOVDD = 3.0V	PA8~PA9 USBDP USBDM	1.7	5.5	V
Output Characteristics						
Symbol	Parameter	Conditions	IO	Typ		Unit
I <sub>OL</sub>	Output Current	IOVDD = 3.0V Voutput = 0.3V	PA0~PA7 PA10~PA15 PB0~PB3	3(HD=0) 9(HD=1) 15(HD=2) 28(HD=3)		mA
		IOVDD = 3.0V Voutput = 0.3V	PA8~PA9 USBDP USBDM	8		mA
I <sub>OH</sub>	Output Current	IOVDD = 3.0V Voutput = 2.7V	PA0~PA7 PA10~PA15 PB0~PB3	3(HD=0) 9(HD=1) 15(HD=2) 28(HD=3)		mA
		IOVDD = 3.0V Voutput = 2.7V	PA8~PA9 USBDP USBDM	8		mA
Internal Resistance Characteristics						
Symbol	Parameter	Conditions	IO	Typ		Unit
R <sub>pu</sub>	Pull-up Resistance	IOVDD = 3.0V	PA0~PA15 PB0~PB3	10k(PU=1) 100k(PU=2) 1M(PU=3)		Ω
			USBDP	1.5k		Ω
			USBDM	180k		Ω
R <sub>pd</sub>	Pull-down Resistance	IOVDD = 3.0V	PA0~PA15 PB0~PB3	10k(PD=1) 100k(PD=2) 1M(PD=3)		Ω
			USBDP USBDM	15k		Ω

**Note**

1.Internal pull-up/pull-down resistance accuracy  $\pm 20\%$

### 3.5 Audio DAC Characteristics

Table 3-5 Mono DAC Characteristics Under VCM 1.3v

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	16	--	bit
Input Sample Rate	--	8	--	96	kHz
Output Swing	Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=100kΩ	--	680	--	mVrms
Output Resistance	--	--	5	--	K Ω
SNR	Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=100kΩ	--	93	--	dB
Dynamic Range	Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=100kΩ	--	92	--	dB
THD+N	Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=100kΩ	--	-75	--	dB
Noise Floor	B/W=20Hz~20kHz A-Weighted load=100kΩ	--	15	--	uVrms

### 3.6 Class-D Speaker Driver Characteristics

Table 3-6 Class-D Speaker Driver Characteristics Under HPVDD 3.7v

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	16	--	bit
Output Sample Rate	--	8	--	96	kHz
SNR	Differential Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted load=8Ω	--	93	--	dB
Dynamic Range	Differential Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted load=8Ω	--	92	--	dB
THD+N	Differential Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted load=8Ω	--	-26	--	dB
Noise Floor	Differential Mode B/W=20Hz~20kHz A-Weighted load=8Ω	--	45	--	uVrms
Max Output Power	Differential Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted load=4Ω	--	500	--	mW

### 3.7 Audio ADC Characteristics

Table 3-7 Audio ADC Characteristics Under VCM 1.3v

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	16	--	bit
Output Sample Rate	--	8	--	48	kHz
SNR	Differential input Mode Fin=1kHz@1600mVrms Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	96	--	dB
	Single-ended input Mode Fin=1kHz@800mVrms Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	92	--	dB
	Single-ended input Mode Fin=1kHz@40mVrms Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=27dB	--	71	--	dB
Dynamic Range	Differential input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	96	--	dB
	Single-ended input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	92	--	dB
	Single-ended input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=27dB	--	72	--	dB
THD+N	Differential input Mode Fin=1kHz@1600mVrms Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	-80	--	dB
	Single-ended input Mode Fin=1kHz@800mVrms	--	-78	--	dB

Parameter	Conditions	Min	Typ	Max	Unit
	Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB				
	Single-ended input Mode Fin=1kHz@40mVrms Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=27dB	--	-72	--	dB
Analogue Gain	--	-3	--	27	dB
Max Input Level	Differential input Mode ADC gain=0dB	--	1.6	--	Vrms
	Single-ended input Mode ADC gain=0dB	--	0.8	--	Vrms

## 4 Package Information

### 4.1 QFN32(4mm\*4mm)

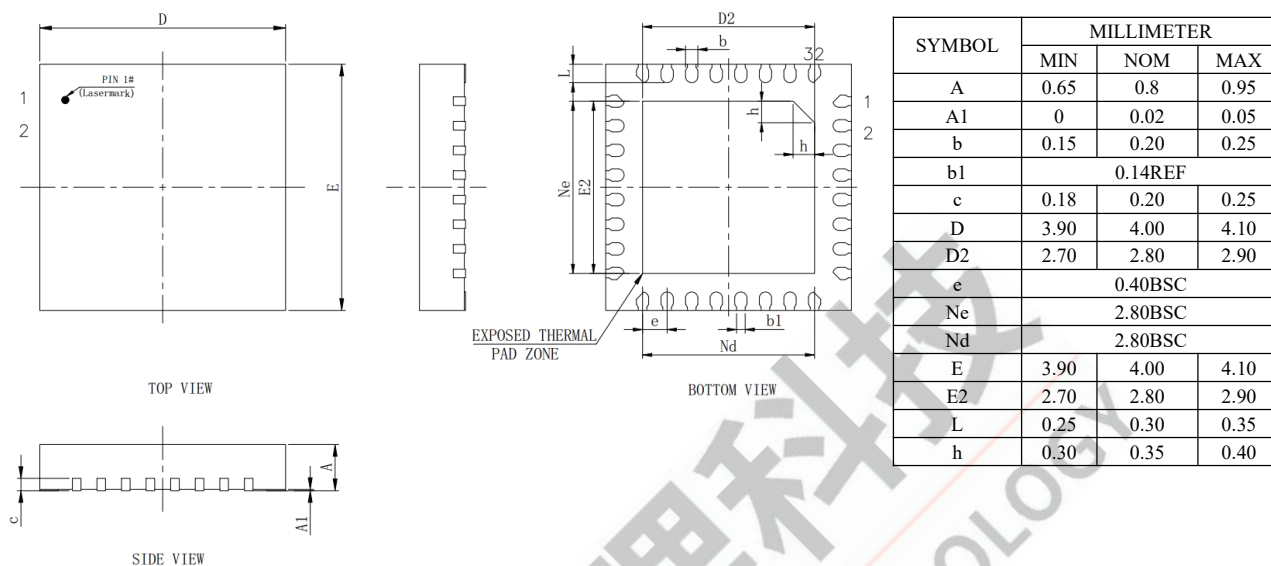


Figure 4-1 AD246A Package

## 5 IC Marking Information

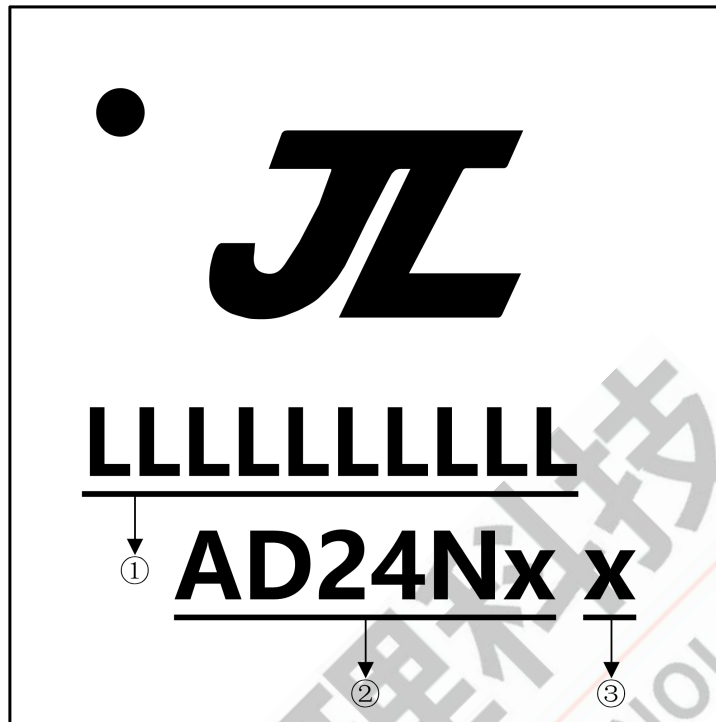


Figure 5-1 AD246A Package Outline

- ① Production Batch
- ② AD24Nx Chip Model
- ③ x: Built-in flash size
  - 0: No Flash Memory
  - 2: 2Mbit Flash
  - 4: 4Mbit Flash
  - 8: 8Mbit Flash
  - 6: 16Mbit Flash
  - 3: 32Mbit Flash
  - 5: 64Mbit Flash
  - 7: 128Mbit Flash



## 6 Solder-Reflow Condition

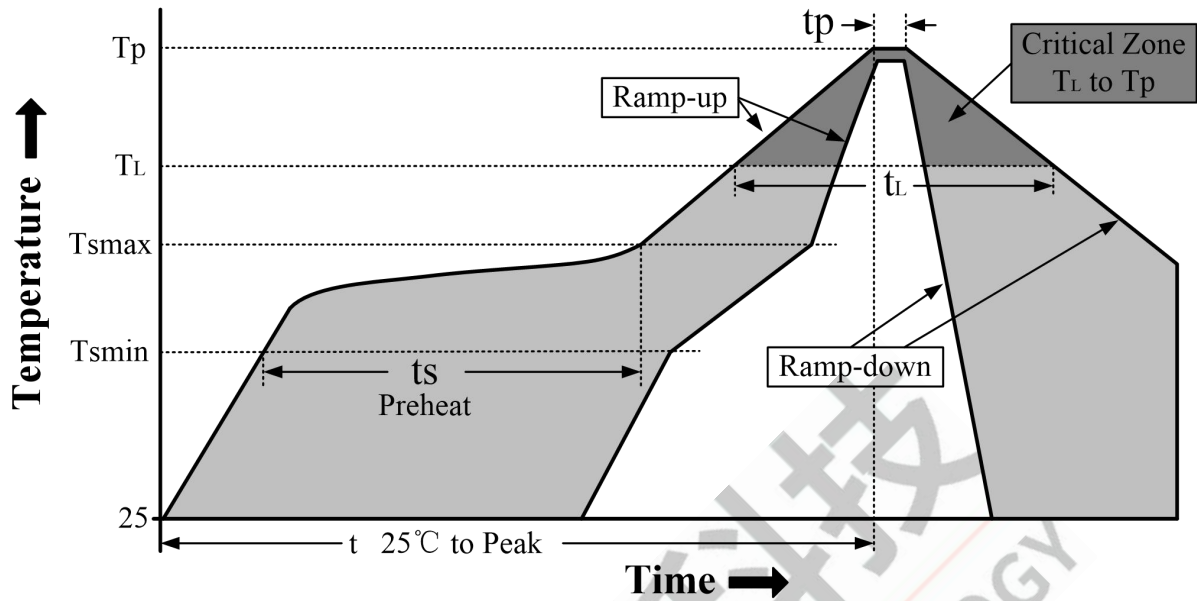


Figure 6-1 Classification Reflow Profile

Table 6-1 Classification Profiles

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak	Temperature Min ( $T_{smin}$ )	100°C	150°C
	Temperature Max ( $T_{smax}$ )	150°C	200°C
	Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )	60-120 seconds	60-180 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )		3°C/second max	3°C/second max
Liquidous temperature ( $T_L$ )		183°C	217°C
Time ( $t_L$ ) maintained above $T_L$		60-150 seconds	60-150 seconds
Peak package body temperature ( $T_p$ )		See Table 6-2	See Table 6-3
Time within 5°C of actual Peak Temperature ( $t_p$ ) <sup>2</sup>		10-30 seconds	20-40 seconds
Ramp-down rate ( $T_p$ to $T_L$ )		6°C/second max	6°C/second max
Time 25°C to peak temperature		6 minutes max	8 minutes max

**Note**

- 1.All temperatures refer to topside of the package, measured on the package body surface
- 2.Time within 5°C of actual peak temperature ( $t_p$ ) specified for the reflow profiles is a "supplier" and "user" maximum.

Table 6-2 SnPb Classification Temperature

Package Thickness	Volume mm <sup>3</sup> < 350	Volume mm <sup>3</sup> ≥ 350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

**Table 6-3 Pb-free - Classification Temperature**

Package Thickness	Volume mm <sup>3</sup> < 350	Volume mm <sup>3</sup> 350 - 2000	Volume mm <sup>3</sup> > 2000
< 1.6mm	260°C	260°C	260°C
1.6 mm - 2.5mm	260°C	250°C	245°C
> 2.5mm	250°C	245°C	245°C

**Note**

1.\*Tolerance The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C.For example 260°C+0°C)at the rated MSL level.

## 7 Storage Condition

### 7.1 Moisture Sensitivity Level

AD24N is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

### 7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at<40°C and 90% relative humidity (RH).
2. Peak package body temperature≤260°C.
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions≤30°C/60%RH or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads> 10% for level 2a-5a devices or>60% for level 2 devices when read at 23±5°C,or 3a or 3b are not met.
5. Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.