



MC34063A

LINEAR INTEGRATED CIRCUIT

DC TO DC CONVERTER CONTROLLER

■ DESCRIPTION

The UTC **MC34063A** is a monolithic regulator subsystem, intended for use as DC to DC converter. This device contains a temperature compensated band gap reference, a duty-cycle control oscillator, driver and high current output switch. It can be used for step down, step-up or inverting switching regulators as well as for series pass regulators.

该器件包含一个温度补偿的
带隙基准

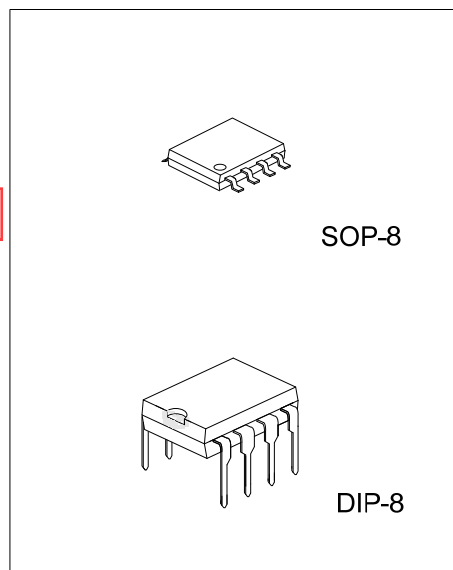
■ FEATURES

- * Operation from 3.0V to 40V.
- * Short circuit current limiting.
- * Low standby current.
- * Output switch current of 1.5A without external transistors.
- * Frequency of operation from 100Hz to 100kHz.
- * Step-up, step-down or inverting switch regulators.

■ ORDERING INFORMATION

无铅

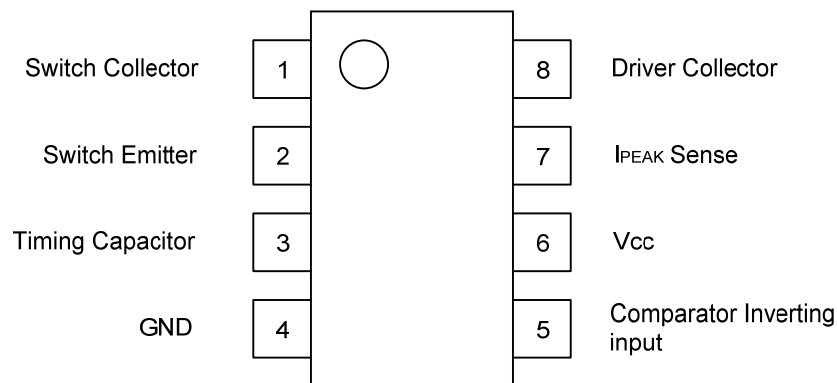
Ordering Number			Package	Packing
Normal	Lead Free	Halogen Free		
MC34063A-D08-T	MC34063AL-D08-T	MC34063AG-D08-T	DIP-8	Tube
MC34063A-S08-R	MC34063AL-S08-R	MC34063AG-S08-R	SOP-8	Tape Reel



Lead-free: MC34063AL
Halogen-free: MC34063AG

<p>MC34063AL-D08-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>		<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn</p>
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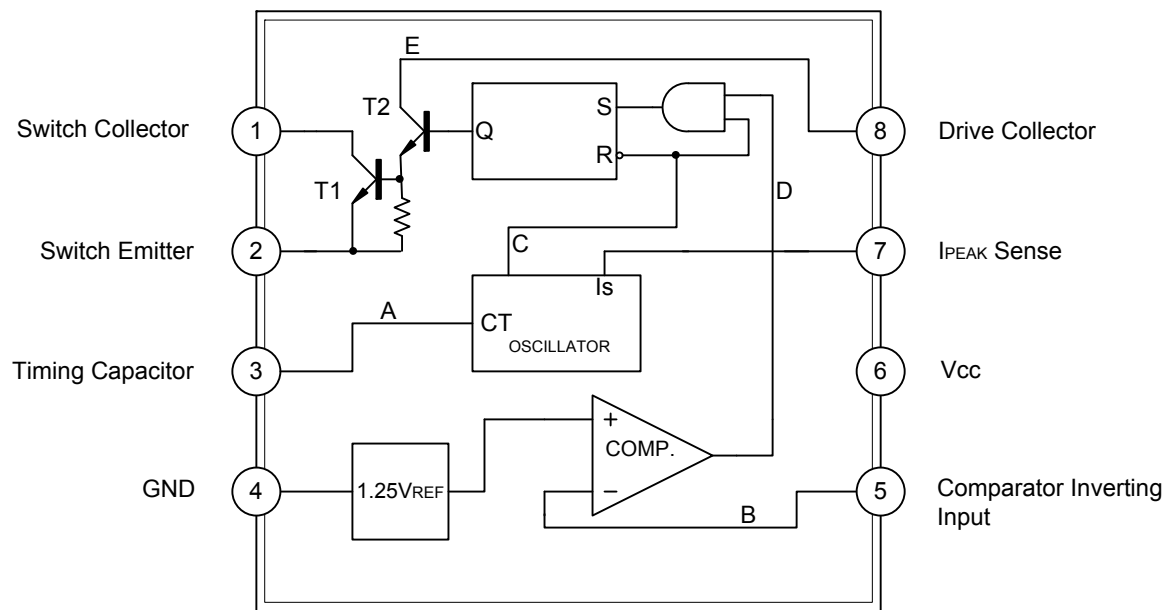
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	I/O	DESCRIPTION
1	Switch Collector	I	Internal Darlington pairs TI collector
2	Switch Emitter	O	Internal Darlington pairs TI emitter
3	Timing Capacitor		<u>The value of selected capacitor controls the internal oscillator run rate.</u>
4	GND		
5	Comparator Inverting Input	I	Inverting input of comparator which can set & initiate the Darlington pairs output switch
6	V _{CC}		
7	I _{PEAK} Sense	I	Current sense input to monitor the voltage drop across an external resistor placed in series with V _{CC}
8	Driver Collector	I	Internal Darlington pairs TI collector

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	40	V
Comparator Input Voltage Range	$V_{IN(COMP)}$	-0.3 ~ +40	V
Switch Collector Voltage	$V_{C(SW)}$	40	V
Switch Emitter Voltage	$V_{E(SW)}$	40	V
Switch Collector to Emitter Voltage	$V_{CE(SW)}$	40	V
Driver Collector Voltage	$V_{C(DR)}$	40	V
Switch Current	I_{SW}	1.5	A
Power Dissipation (Ta=25°C)	DIP-8	1250	mW
	SOP-8	625	
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	0 ~ +70	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

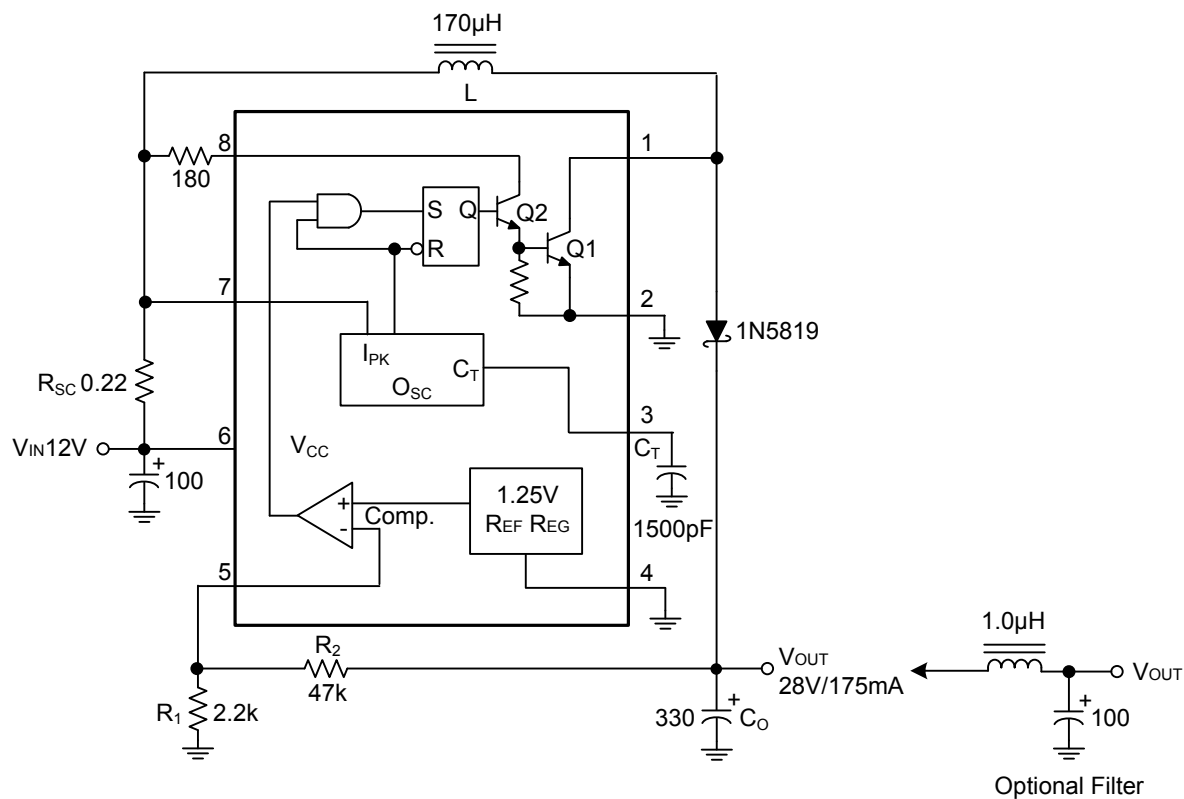
PARAMETER	SYMBOL	RATINGS	UNIT
Junction-to-Ambient	DIP-8	100	°C/W
	SOP-8	160	

■ ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0V$, $T_a=0\sim+70^\circ C$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator						
Charging Current	I_{CHG}	$V_{CC}=5$ to 40V, $T_a=25^\circ C$	22	31	42	μA
Discharging Current	I_{DISCHG}	$V_{CC}=5$ to 40V, $T_a=25^\circ C$	140	190	260	μA
Oscillator Amplitude	V_{OSC}	$T_a=25^\circ C$		0.5		V
Discharge to Charge Current Ratio	K	$V_7=V_{CC}$, $T_a=25^\circ C$	5.2	6.1	7.5	
Current limit Sense Voltage	V_{SENSE}	$I_{CHG}=I_{DISCHG}$, $T_a=25^\circ C$	250	300	350	mV
Output Switch						
Saturation Voltage 1(Note)	$V_{CE(SAT)1}$	$I_{SW}=1.0A$, $V_{C(DRIVER)}=V_{C(SW)}$		0.95	1.3	V
Saturation Voltage 2(Note)	$V_{CE(SAT)2}$	$I_{SW}=1.0A$, $V_{C(DRIVER)}=50mA$		0.45	0.7	V
DC Current Gain(Note)	$G_{I(DC)}$	$I_{SW}=1.0A$, $V_{CE}=5.0V$, $T_a=25^\circ C$	50	180		
Collector Off State Current(Note)	$I_{C(OFF)}$	$V_{CE}=40.0V$, $T_a=25^\circ C$		0.01	100	μA
Comparator						
Threshold Voltage	V_{THD}		1.21	1.24	1.29	V
Threshold Voltage Line Regulation	V_{THD}	$V_{CC}=3 \sim 40V$		2.0	5.0	mV
Input Bias Current	$I_{I(BIAS)}$	$V_{IN}=0V$		50	400	nA
Total Device						
Supply Current	I_{CC}	$V_{CC}=5\sim40V$, $C_T=0.001$ $V_7=V_{CC}$, $V_C>V_{THD}$, $Pin2=GND$		2.7	4.0	mA

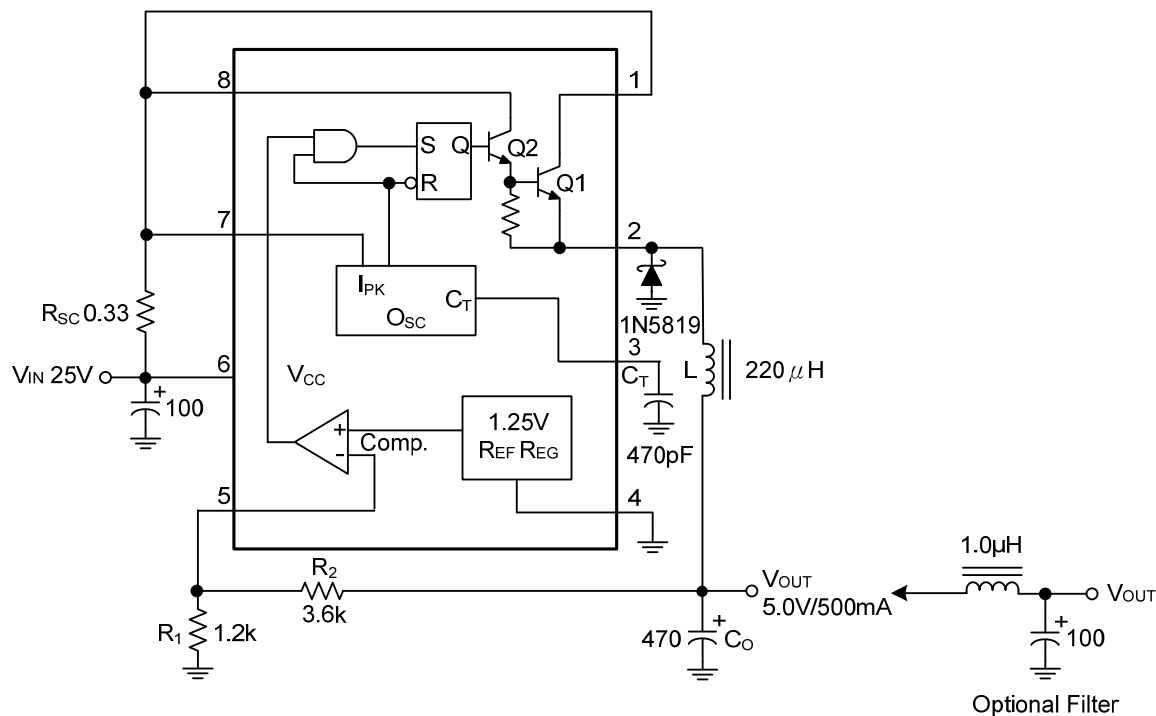
Note: Output switch tests are performed under pulsed conditions to minimize power dissipation.

■ STEP-UP CONVERTER



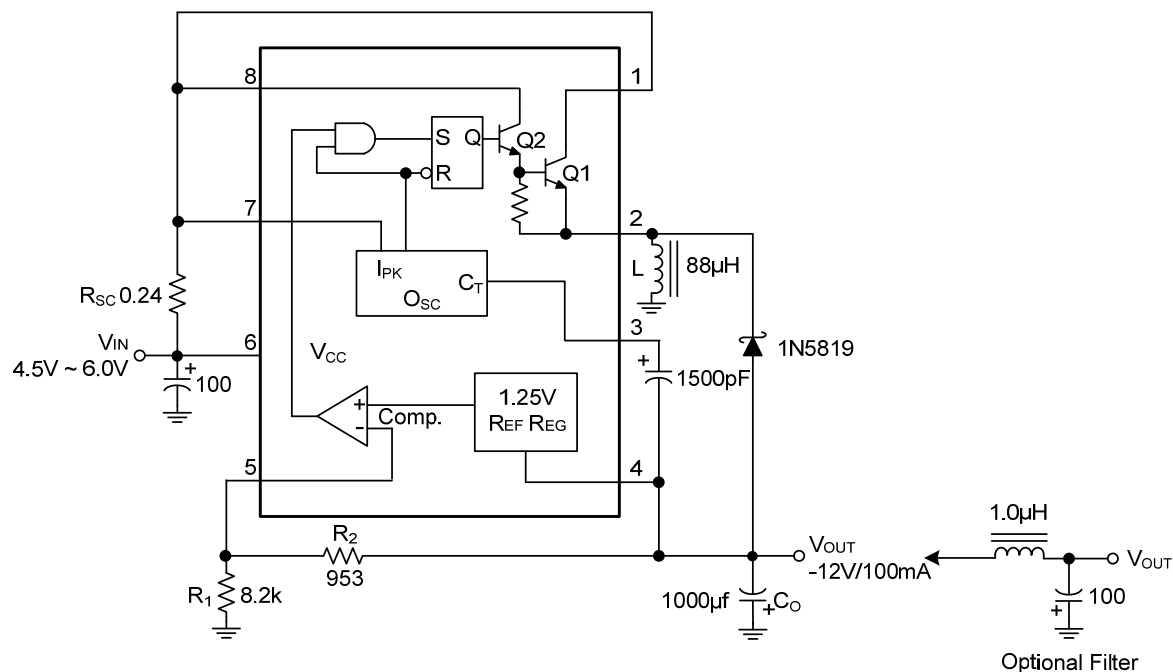
Test	Conditions	Results
Line Regulation	$V_{IN} = 8.0V \sim 16V, I_{OUT} = 175mA$	$30mV = \pm 0.05\%$
Load Regulation	$V_{IN} = 12V, I_{OUT} = 75mA \sim 175mA$	$10mV = \pm 0.017\%$
Output Ripple	$V_{IN} = 12V, I_{OUT} = 175mA$	$400mVp-p$
Efficiency	$V_{IN} = 12V, I_{OUT} = 175mA$	87.7%
Output Ripple With Optional Filter	$V_{IN} = 12V, I_{OUT} = 175mA$	$40mVp-p$

■ STEP-DOWN CONVERTER(Cont.)



Test	Conditions	Results
Line Regulation	$V_{IN} = 15V \sim 25V, I_{OUT} = 500mA$	$12mV = \pm 0.12\%$
Load Regulation	$V_{IN} = 25V, I_{OUT} = 50mA \sim 500mA$	$3.0mV = \pm 0.03\%$
Output Ripple	$V_{IN} = 25V, I_{OUT} = 500mA$	$120mV_{p-p}$
Short Circuit Current	$V_{IN} = 25V, R_L = 0.1\Omega$	$1.1A$
Efficiency	$V_{IN} = 25V, I_{OUT} = 500mA$	83.7%
Output Ripple With Optional Filter	$V_{IN} = 25V, I_{OUT} = 500mA$	$40mV_{p-p}$

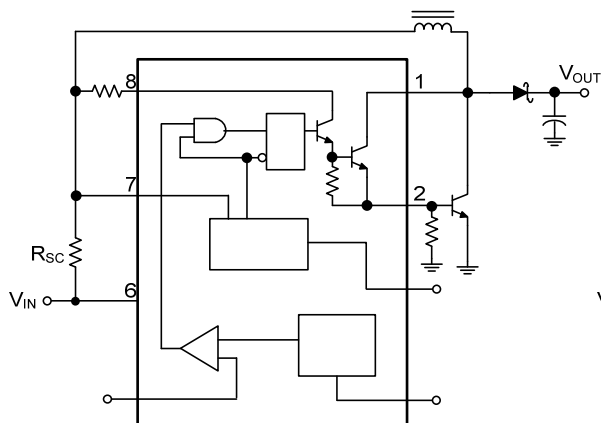
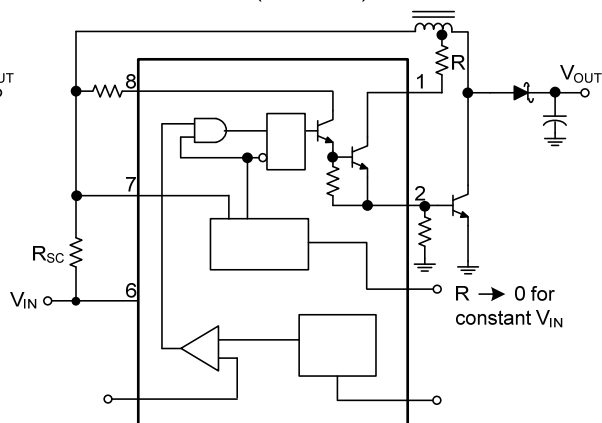
■ VOLTAGE INVERTING CONVERTER



Test	Conditions	Results
Line Regulation	$V_{IN} = 4.5V \sim 6.0V, I_{OUT} = 100mA$	$3.0mV = \pm 0.012\%$
Load Regulation	$V_{IN} = 5.0V, I_{OUT} = 10mA \sim 100mA$	$0.022V = \pm 0.09\%$
Output Ripple	$V_{IN} = 5.0V, I_{OUT} = 100mA$	$500mVp-p$
Short Circuit Current	$V_{IN} = 5.0V, R_L = 0.1\Omega$	$910mA$
Efficiency	$V_{IN} = 5.0V, I_{OUT} = 100mA$	62.2%
Output Ripple With Optional Filter	$V_{IN} = 5.0V, I_{OUT} = 100mA$	$70mVp-p$

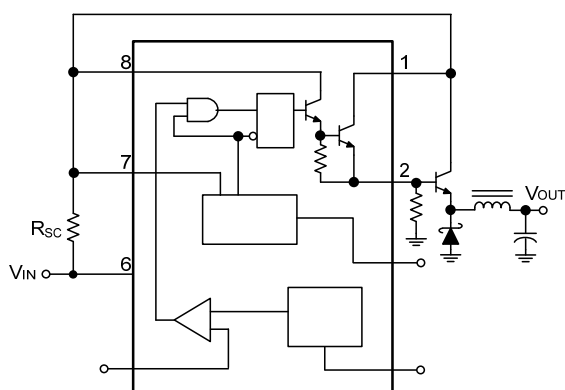
■ EXTERNAL CURRENT BOOST CONNECTIONS FOR IC PEAK GREATER THAN 1.5A

1a. External NPN Switch

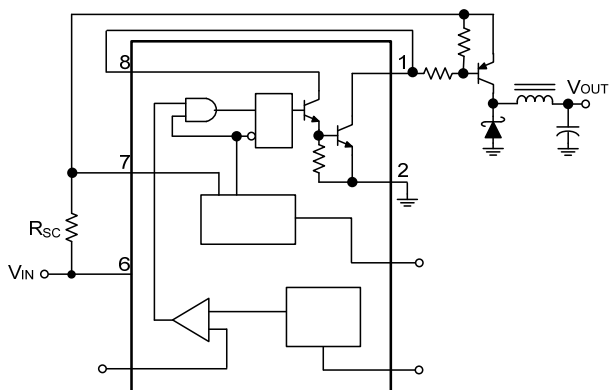
1b. External NPN Saturated Switch
(See Note 4)

Note: 4. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300\text{mA}$) and high driver currents ($\leq 30\text{mA}$), it may take up to $2.0\mu\text{s}$ to come out of saturation. This condition will shorten the off time at frequencies $\geq 30\text{kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.

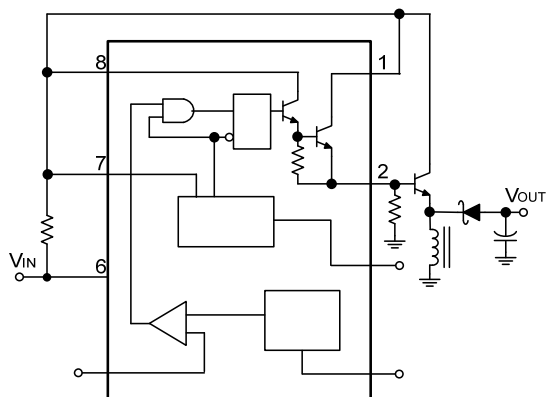
2a. External NPN Switch



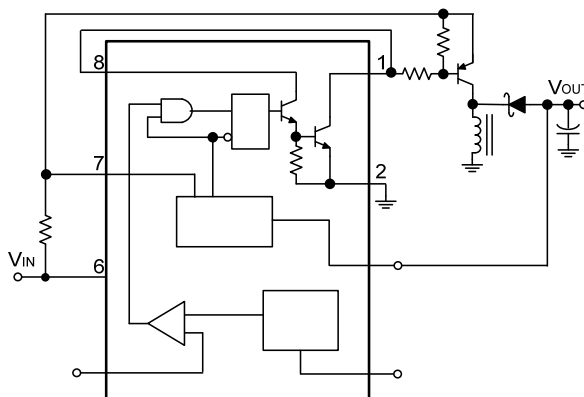
2b. External PNP Saturated Switch



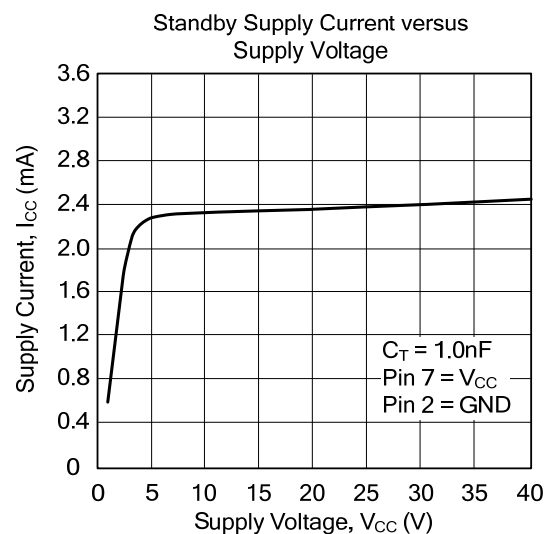
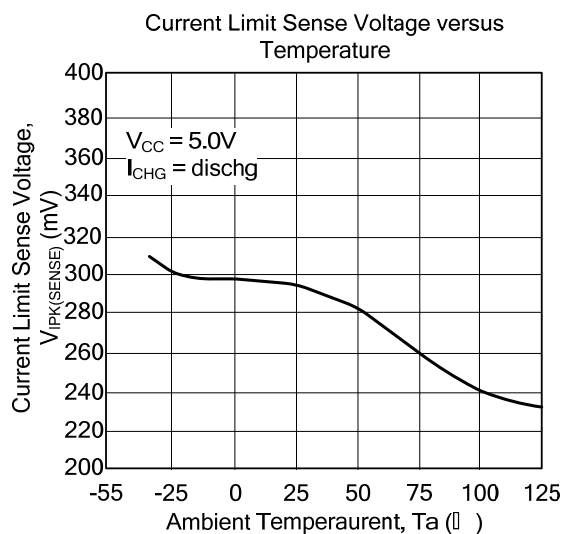
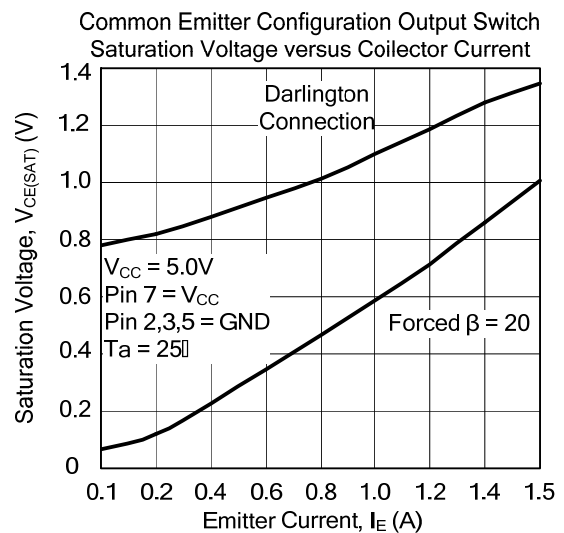
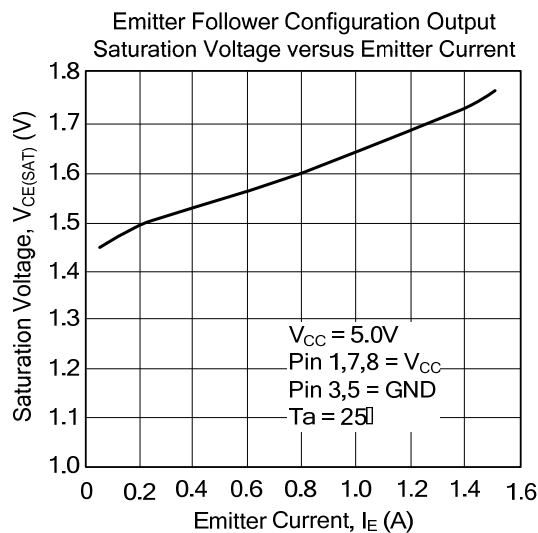
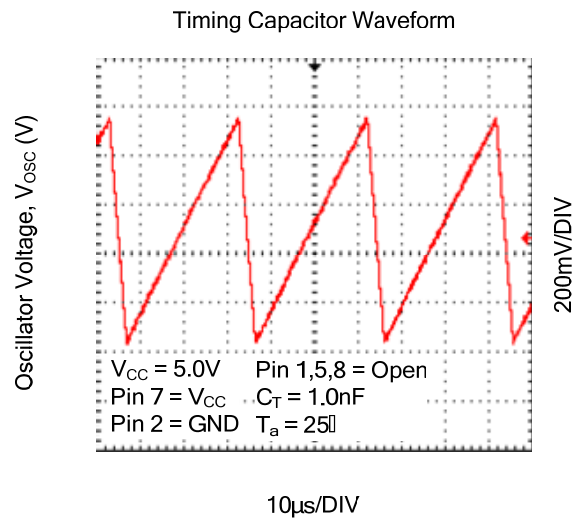
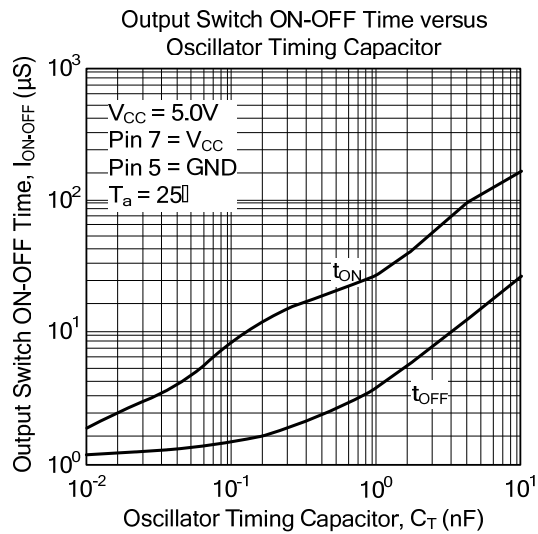
3a. External NPN Switch



3b. External PNP Saturated Switch



TYPICAL CHARACTERISTICS



■ DESIGN FORMULA TABLE

CALCULATION	STEP-DOWN	STEP-UP	VOLTAGE-INVERTING
$\frac{t_{ON}}{t_{OFF}}$	$\frac{V_{OUT} + V_F}{V_{IN(MIN)} - V_{CE(SAT)} - V_{OUT}}$	$\frac{V_{OUT} + V_F - V_{IN(MIN)}}{V_{IN(MIN)} - V_{CE(SAT)}}$	$\frac{ V_{OUT} + V_F}{V_{IN} - V_{CE(SAT)}}$
$(t_{ON} + t_{OFF})_{MAX}$	$\frac{1}{F_{MIN}}$	$\frac{1}{F_{MIN}}$	$\frac{1}{F_{MIN}}$
C_T	$4 \times 10^{-5} t_{ON}$	$4 \times 10^{-5} t_{ON}$	$4 \times 10^{-5} t_{ON}$
I_{SW}	$2I_{OUT(MAX)}$	$2I_{OUT(MAX)} \frac{t_{ON} + t_{OFF}}{t_{OFF}}$	$2I_{OUT(MAX)} \frac{t_{ON} + t_{OFF}}{t_{OFF}}$
<u>R_S</u>	<u>$0.3/I_{SW}$</u>	<u>$0.3/I_{SW}$</u>	<u>$0.3/I_{SW}$</u>
$L_{(MIN)}$	$(\frac{V_{IN(MIN)} - V_{CE(SAT)} - V_{OUT}}{I_{SW}}) t_{ON(MAX)}$	$(\frac{V_{IN(MIN)} - V_{CE(SAT)}}{I_{SW}}) t_{ON(MAX)}$	$(\frac{V_{IN(MIN)} - V_{CE(SAT)}}{I_{SW}}) t_{ON(MAX)}$
C_O	$\frac{I_{SW}(t_{ON} + t_{OFF})}{8V_{RIPPLE(P-P)}}$	$\frac{I_{OUT} t_{ON}}{V_{RIPPLE(P-P)}}$	$\frac{I_{OUT} t_{ON}}{V_{RIPPLE(P-P)}}$

$V_{CE(SAT)}$ - Saturation voltage of the output switch.

V_F - Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

V_{IN} - Nominal input voltage.

V_{OUT} - Desired output voltage, $|V_{OUT}| = 1.25(1 + R_2/R_1)$ if voltage inverts then $V_{out} = 1.25(1 + R_1/R_2)$

I_{OUT} - Desired output current.

F_{MIN} - Minimum desired output switching frequency at the selected values for V_{IN} and I_{OUT} .

$V_{RIPPLE(P-P)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

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