Atari 2600 - Television Interface Adapter (TIA)

JiggleSoft’s Standard Video Generation Timing Template

As per STDX includes as included in release: atari-2600-asm-common-2.0.0-beta-0

Timing Diagram

				Cycle																																																																									
NTSC / PAL60	PAL / SECAM	PALX / SECAMX	Display	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	##	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	Notes
1	1	1	VSYNC	STA VSYNC			STA VBLANK			LDA #$XX		STA WTIM64EI				*FREE (TO END OF LINE)*																																																					STA WSYNC			
2	2	2	VSYNC	*FREE (FULL LINE)*																																																																									STA WSYNC			
3	3	3	VSYNC	*FREE (FROM START OF LINE)*																																																																								LDA #$00		STA WSYNC			
4	4	4	VBLANK	STA VSYNC			*FREE (TO END OF LINE)*																																																																										
5	5	5	VBLANK	*FREE (FULL LINE)*																																																																											
6 to 38	6 to 46	6 to 38	VBLANK	*FREE (FULL LINES)*																																																																												
39	47	39	VBLANK	*FREE (FROM START OF LINE)*																																																															BIT RTIMEINT			BPL -4				STA CXCLR		STA WSYNC			
40	48	40	VBLANK	FREE (FROM START OF LINE) + SOFTWARE DELAY TO END OF LINE																																																																							LDA #$42		STA VBLANK			
41	49	41	KERNEL	*FREE (FULL LINE)*																																																																									STA WSYNC			
42	50	42	KERNEL	*FREE (FULL LINE)*																																																																									STA WSYNC			
43 to 230	51 to 274	43 to 280	KERNEL	*FREE (FULL LINES)*																																																																									STA WSYNC			
231	275	281	KERNEL	*FREE (FULL LINE)*																																																																									STA WSYNC			
232	276	282	KERNEL	*FREE (FULL LINE)*																																																																									STA WSYNC			
233	277	283	OVERSCAN	LDA #$42		STA VBLANK			LDA #$XX		STA WTIM64EI				*[READ CONTROLLERS +] [CLEAR LATCHES +]FREE (TO END OF LINE)*																																																						
234	278	284	OVERSCAN	*FREE (FULL LINE)*																																																																											
235 to 260	279 to 310	285 to 310	OVERSCAN	*FREE (FULL LINES)*																																																																												
261	311	311	OVERSCAN	*FREE (FULL LINE)*																																																																											
262	312	312	OVERSCAN	*FREE (FROM START OF LINE)*																																																															BIT RTIMEINT			BPL -4				LDA #$C2		STA WSYNC			

NOTE: The last line cycle 72 is the start of the display loop.
Before entering the display loop it is expected that the input latches are cleared along with the collision latches (LDA #$02, STA VBLANK, STA CXCLR).
Any other display initialisation can then be performeed e.g. resetting colours, playfield, sprite data, missile/ball enablement, etc.
The branch in the code that checks the timer interrupt (BIT+BPL) will take 2, 3, 4 cycles depending on branch taken and page boundary crossed.
Collision latches are cleared just before the KERNEL so that following the KERNEL (start of OVERSCAN) the rendered collision latches are valid throughout the OVERSCAN and the next VSYNC/VBLANK.
The reading of controllers and the clearing of the input latches is done on the first line of OVERSCAN (cycle 11).
The timer wait (BIT+BPL) may come anytime between the VBLANK and OVERSCAN when processing is complete but MUST NOT overrun.
There will be some time on the last line of VBLANK and OVERSCAN before the timer is triggered and this spare time is detailed below.
There will be some time after the timer is triggered and the end of the scan line (STA WSYNC) and this spare time is detailed below.

Wait For Timer Clock Region

Timer Regions

START TIMER | APPLICATION SPECIFIC PROCESSING | WAIT FOR TIMER (SOMEWHERE ON LAST LINE) | LAST LINE PROCESSING | FREE (TO END OF LINE) | WAIT END OF LINE (WSYNC)

Minimum / Maximum Bounds

			Cycle																																																																											
TV Standard	Lines	Display	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	##	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	Notes
NTSC/PAL60	3 – 40	VBLANK																																																																														
NTSC/PAL60		OVERSCAN																																																																														
PAL / SECAM	3 – 40	VBLANK									***TODO: DO THIS CHART !!***																																																															
PAL / SECAM		OVERSCAN																																																																														
PALX / SECAMX		VBLANK																																																																														
PALX / SECAMX		OVERSCAN																																																																														

Standard Extra TIA Video Macros

VID_INIT

display_loop:

- VID_VSYNC
  - VID_OVERSCAN_END
  - VID_VSYNC_1_BEGIN
  - VID_VSYNC_1_END
  - VID_VSYNC_2_BEGIN
  - VID_VSYNC_2_END
  - VID_VSYNC_3_BEGIN
  - VID_VSYNC_3_END
- VID_VBLANK
  - VID_VBLANK_BEGIN
  - *VID_VBLANK_PENULTIMATE*
  - VID_VBLANK_END
- VID_VDISPLAY
- VID_OVERSCAN
  - VID_OVERSCAN_BEGIN
  - VID_OVERSCAN_ENDING
- JMP display_loop