Ask a Question

Consider the following set of processes, with the length of the CPU burst given in milliseconds: ...

Question:

Consider the following set of processes, with the length of the CPU burst given in milliseconds:

Process	Burst Time	Priority
P1	2	2
P2	1	1
P3	8	4
P4	4	2
P5	5	3

The processes are assumed to have arrived in the order P1, P2, P3, P4, P5, all at time 0.

a. Draw four Gantt charts that illustrate the execution of these processes using the following scheduling algorithms: FCFS, SJF, nonpreemptive priority (a larger priority number implies a higher priority), and RR (quantum = 2)

b. What is the turnaround time of each process for each of the scheduling algorithms in part a?

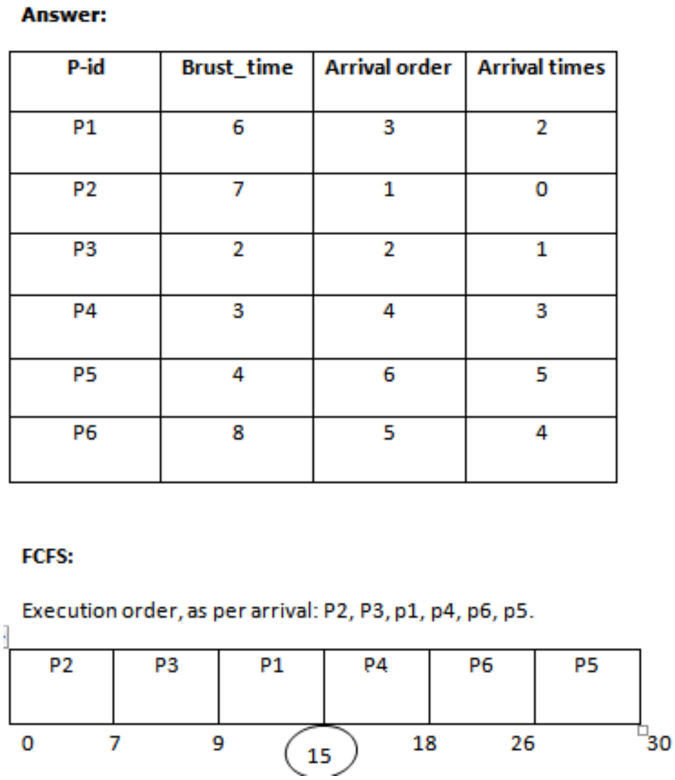
c. What is the waiting time of each process for each of these scheduling algorithms?

d. Which of the algorithms results in the minimum average waiting time (over all processes)?

CPU burst definition

In computer terminology, the CPU burst is the duration or time for which a process takes or gets the control of the CPU.

Answer and Explanation:



Answer:

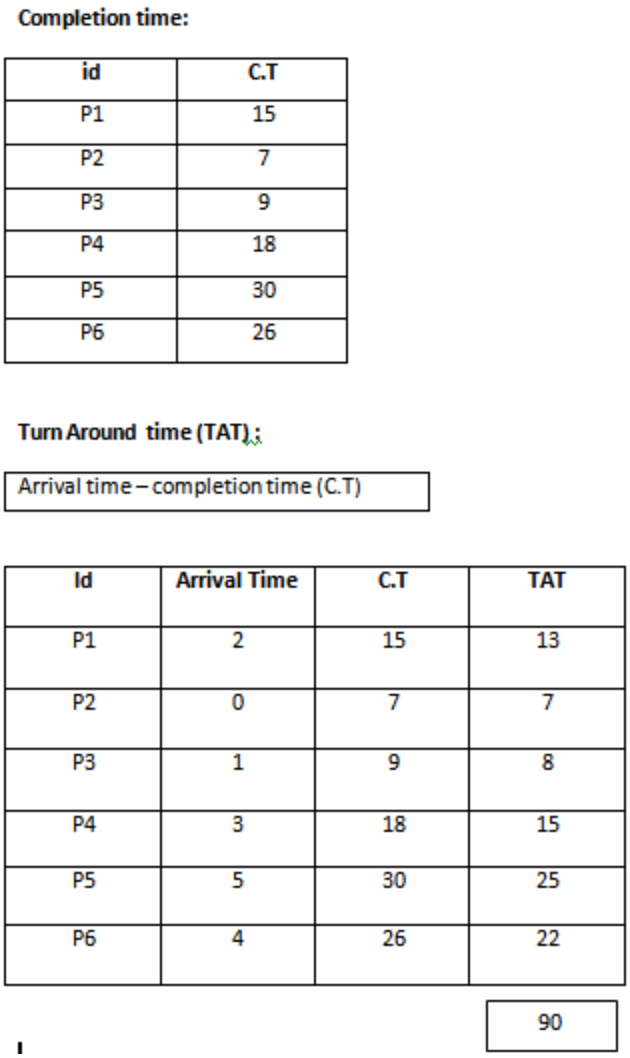
P-id	Brust_time	Arrival order	Arrival times
P1	6	3	2
P2	7	1	0
P3	2	2	1
P4	3	4	3
P5	4	6	5
P6	8	5	4

FCFS:

Execution order, as per arrival: P2, P3, p1, p4, p6, p5.

P2	P3	P1	P4	P6	P5

0 7 9 15 18 26 30



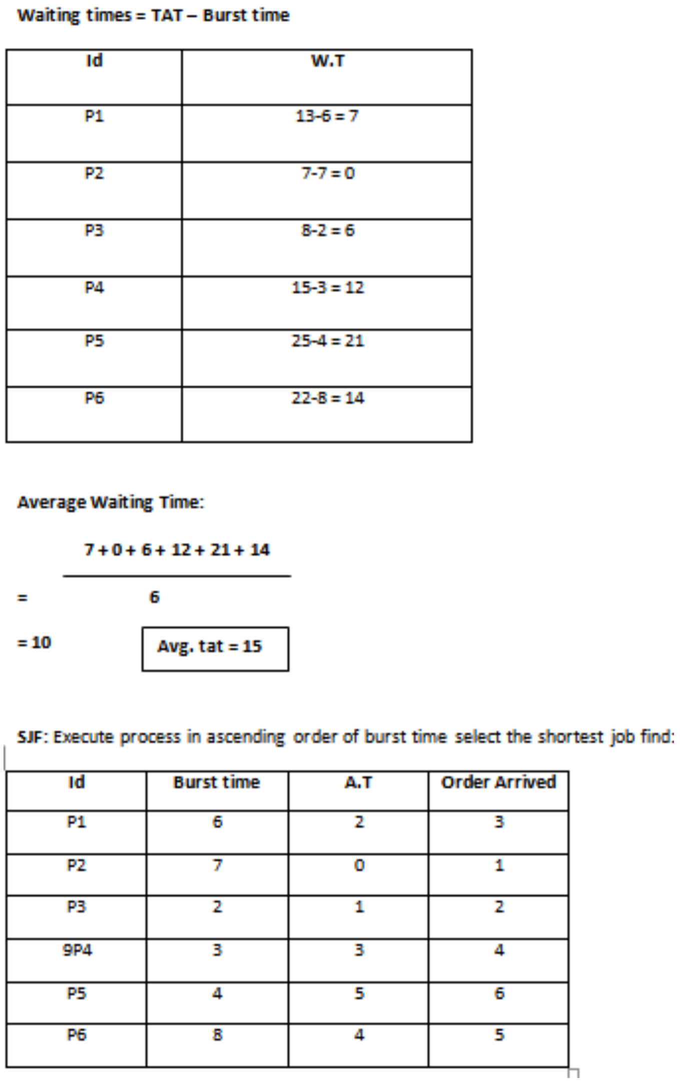
Completion time:

id	C.T
P1	15
P2	7
P3	9
P4	18
P5	30
P6	26

Turn Around time (TAT) :

Arrival time – completion time (C.T)

Id	Arrival Time	C.T	TAT
P1	2	15	13
P2	0	7	7
P3	1	9	8
P4	3	18	15
P5	5	30	25
P6	4	26	22
			90



Waiting times = TAT – Burst time

Id	W.T
P1	13-6 = 7
P2	7-7 = 0
P3	8-2 = 6
P4	15-3 = 12
P5	25-4 = 21
P6	22-8 = 14

Average Waiting Time:

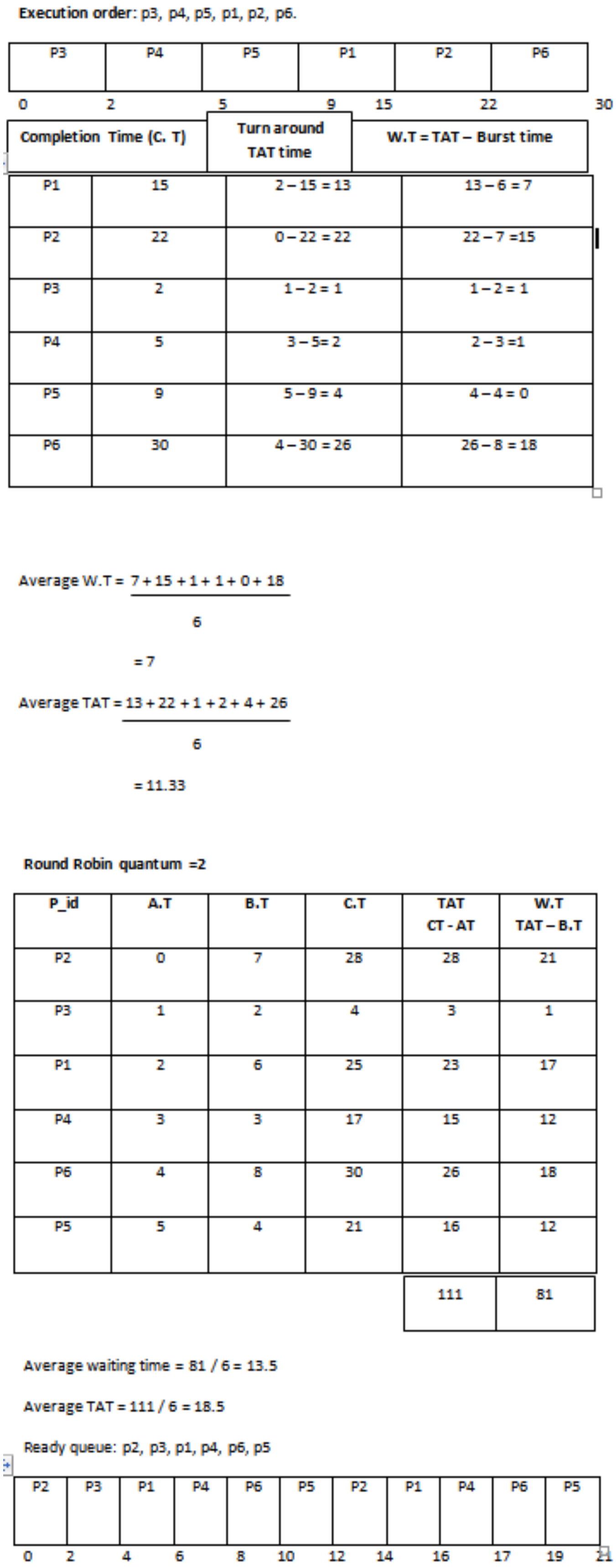
$$= \frac{7 + 0 + 6 + 12 + 21 + 14}{6}$$

= 10

Avg. tat = 15

SJF: Execute process in ascending order of burst time select the shortest job find:

Id	Burst time	A.T	Order Arrived
P1	6	2	3
P2	7	0	1
P3	2	1	2
9P4	3	3	4
P5	4	5	6
P6	8	4	5



Execution order: p3, p4, p5, p1, p2, p6.

P3	P4	P5	P1	P2	P6

0 2 5 9 15 22 30

Completion Time (C. T)		Turn around TAT time	W.T = TAT – Burst time
P1	15	2 – 15 = 13	13 – 6 = 7
P2	22	0 – 22 = 22	22 – 7 =15
P3	2	1 – 2 = 1	1 – 2 = 1
P4	5	3 – 5= 2	2 – 3 =1
P5	9	5 – 9 = 4	4 – 4 = 0
P6	30	4 – 30 = 26	26 – 8 = 18

$$\text{Average W.T} = \frac{7 + 15 + 1 + 1 + 0 + 18}{6}$$

= 7

$$\text{Average TAT} = \frac{13 + 22 + 1 + 2 + 4 + 26}{6}$$

= 11.33

Round Robin quantum =2

P_id	A.T	B.T	C.T	TAT CT - AT	W.T TAT – B.T
P2	0	7	28	28	21
P3	1	2	4	3	1
P1	2	6	25	23	17
P4	3	3	17	15	12
P6	4	8	30	26	18
P5	5	4	21	16	12
				111	81

Average waiting time = 81 / 6 = 13.5

Average TAT = 111 / 6 = 18.5

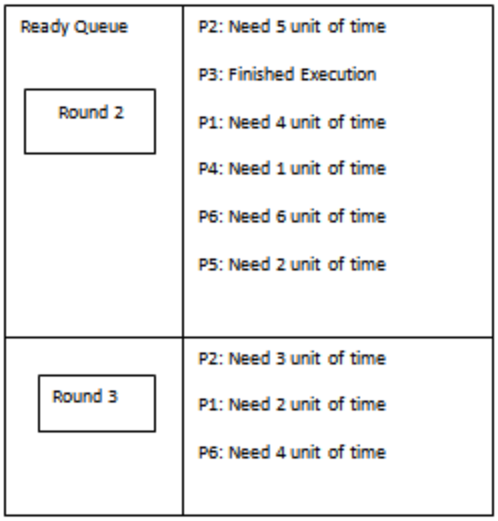
Ready queue: p2, p3, p1, p4, p6, p5

P2	P3	P1	P4	P6	P5	P2	P1	P4	P6	P5

0 2 4 6 8 10 12 14 16 17 19 21

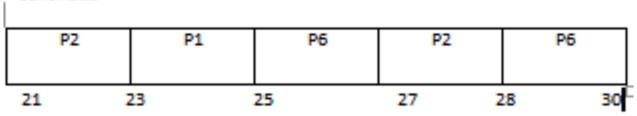
Ask a Question

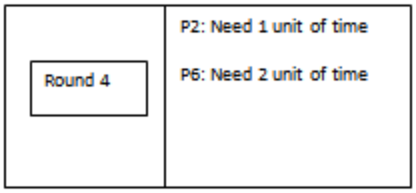
Finished process: p3 finished its execution



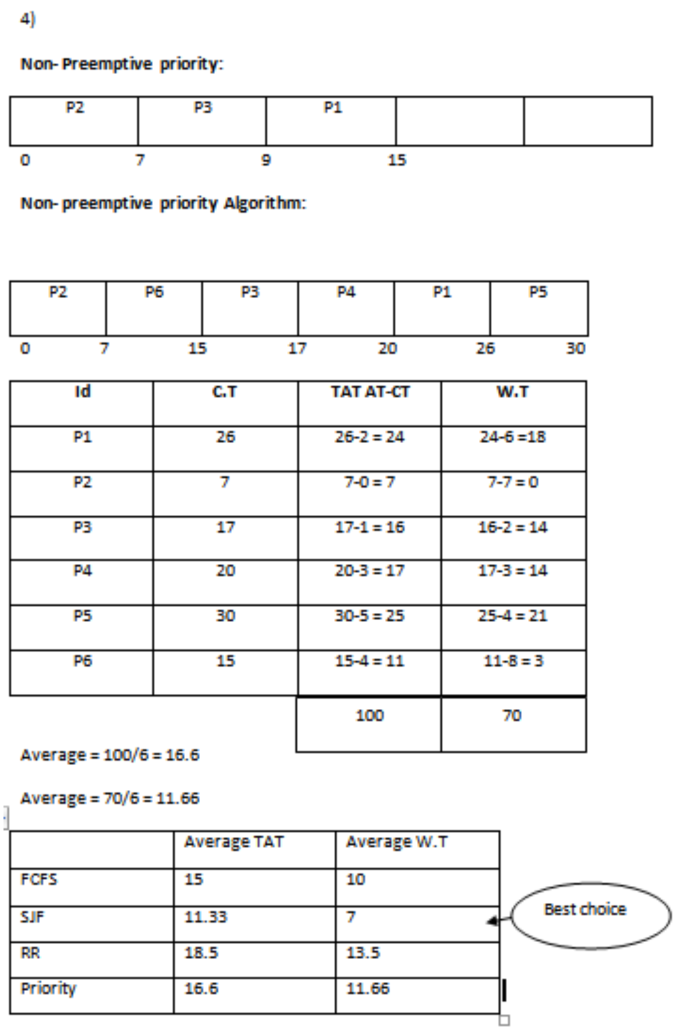
Ready Queue	
Round 2	P2: Need 5 unit of time P3: Finished Execution P1: Need 4 unit of time P4: Need 1 unit of time P6: Need 6 unit of time P5: Need 2 unit of time
Round 3	P2: Need 3 unit of time P1: Need 2 unit of time P6: Need 4 unit of time

Continued





Round 4	P2: Need 1 unit of time P6: Need 2 unit of time



4)

Non- Preemptive priority:

P2	P3	P1		
0	7	9	15	

Non- preemptive priority Algorithm:

P2	P6	P3	P4	P1	P5	
0	7	15	17	20	26	30

Id	C.T	TAT AT-CT	W.T
P1	26	26-2 = 24	24-6 =18
P2	7	7-0 = 7	7-7 = 0
P3	17	17-1 = 16	16-2 = 14
P4	20	20-3 = 17	17-3 = 14
P5	30	30-5 = 25	25-4 = 21
P6	15	15-4 = 11	11-8 = 3
		100	70

Average = 100/6 = 16.6

Average = 70/6 = 11.66

	Average TAT	Average W.T
FCFS	15	10
SJF	11.33	7
RR	18.5	13.5
Priority	16.6	11.66

Best choice

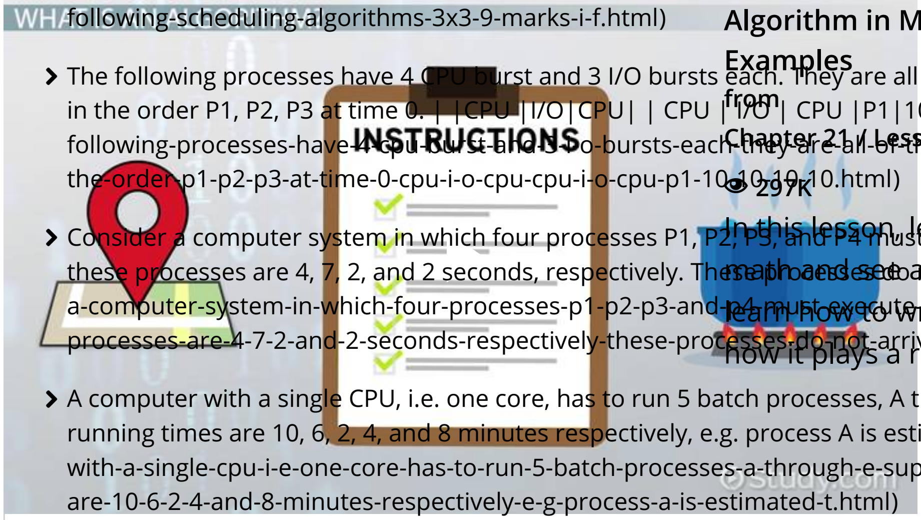
See full answer below.

Ask a Question

Learn more about this topic:

Related to this Question

- Consider the following set of processes, with the length of the CPU burst given in milliseconds: Process Burst Time Priority P1 10 3 P2 1 1 P3 2 3 P4 1 8 P5 5 2 a) Draw a timeline for each of the following scheduling algorithms (3X3 = 9 Marks) i) F (/explanation/consider-the-following-set-of-processes-with-the-length-of-the-cpu-burst-given-in-milliseconds-process-burst-time-priority-p1-10-3-p2-1-1-p3-2-3-p4-1-8-p5-5-2-a-draw-a-timeline-for-each-of-the-following-scheduling-algorithms-3x3-9-marks-i-f.html)



Algorithm in Mathematics | Definition & Examples

from

Chapter 21 / Lesson 9

👁 297K

In this lesson, learn what an algorithm is in math and see algorithm examples. Moreover, learn how to write an algorithm, and explore how it plays a role in real life.

- The following processes have 4 CPU burst and 3 I/O bursts each. They are all of the same priority and they arrive in the order P1, P2, P3 at time 0. | |CPU |I/O|CPU| | CPU |I/O| CPU |P1|10|10|10|10| (/explanation/the-following-processes-have-4-cpu-burst-and-3-i-o-bursts-each-they-are-all-of-the-same-priority-and-they-arrive-in-the-order-p1-p2-p3-at-time-0-cpu-i-o-cpu-cpu-i-o-cpu-p1-10-10-10-10.html)
- Consider a computer system in which four processes P1, P2, P3, and P4 must execute. The execution times for these processes are 4, 7, 2, and 2 seconds, respectively. These processes do not arrive at t (/explanation/consider-a-computer-system-in-which-four-processes-p1-p2-p3-and-p4-must-execute-the-execution-times-for-these-processes-are-4-7-2-and-2-seconds-respectively-these-processes-do-not-arrive-at-t.html)
- A computer with a single CPU, i.e. one core, has to run 5 batch processes, A through E. Suppose their estimated running times are 10, 6, 2, 4, and 8 minutes respectively, e.g. process A is estimated t (/explanation/a-computer-with-a-single-cpu-i-e-one-core-has-to-run-5-batch-processes-a-through-e-suppose-their-estimated-running-times-are-10-6-2-4-and-8-minutes-respectively-e-g-process-a-is-estimated-t.html)
- Consider the following snapshot of a system: Process Allocation Max Available A B C D A B C D A B C D P0 1 2 0 1 1 6 6 2 0 2 2 0 P1 1 0 0 1 1 1 0 1 P2 0 4 4 0 1 4 4 2 P3 0 0 0 2 0 0 2 3 P4 1 0 0 1 3 7 (/explanation/consider-the-following-snapshot-of-a-system-process-allocation-max-available-a-b-c-d-a-b-c-d-a-b-c-d-p0-1-2-0-1-1-6-6-2-0-2-2-0-p1-1-0-0-1-1-1-0-1-p2-0-4-4-0-1-4-4-2-p3-0-0-0-2-0-0-2-3-p4-1-0-0-1-3-7.html)
- What is the CPU utilization if there are 5 processes running at the same time and on average the CPU spends 30% of its time waiting on I/O completion? (/explanation/what-is-the-cpu-utilization-if-there-are-5-processes-running-at-the-same-time-and-on-average-the-cpu-spends-30-of-its-time-waiting-on-i-o-completion.html)
- Consider a pipeline with the following stage latencies 1) What is the clock-cycle time in a non-pipelined and a pipelined processor? 2) What is the total latency of a LW instruction in a non-pipeline (/explanation/consider-a-pipeline-with-the-following-stage-latencies-1-what-is-the-clock-cycle-time-in-a-non-pipelined-and-a-pipelined-processor-2-what-is-the-total-latency-of-a-lw-instruction-in-a-non-pipeline.html)
- Given the following set of events, show which routines the CPU is executing for Time 0 ns to 100 ns. Each handler routine (with its interrupt request) takes 20 ns to complete. The priority of an inter (/explanation/given-the-following-set-of-events-show-which-routines-the-cpu-is-executing-for-time-0-ns-to-100-ns-each-handler-routine-with-its-interrupt-request-takes-20-ns-to-complete-the-priority-of-an-inter.html)
- Given the following set of events, show which routines the CPU is executing for times 0 to 100 ns. Each handler routine (with its interrupt request) takes 20 ns to complete. The priority of the interr (/explanation/given-the-following-set-of-events-show-which-routines-the-cpu-is-executing-for-times-0-to-100-ns-each-handler-routine-with-its-interrupt-request-takes-20-ns-to-complete-the-priority-of-the-interr.html)
- Consider the following program: a. How many processes are created during the execution of this program? Explain. b. List all the possible outputs of the program. (/explanation/consider-the-following-program-a-how-many-processes-are-created-during-the-execution-of-this-program-explain-b-list-all-the-possible-outputs-of-the-program.html)
- A computer with a single CPU (i.e., one core) has to run five batch processes, A through E. Suppose their estimated running times are 10, 6, 2, 4, and 8 minutes, respectively. If the priority system i (/explanation/a-computer-with-a-single-cpu-i-e-one-core-has-to-run-five-batch-processes-a-through-e-suppose-their-estimated-running-times-are-10-6-2-4-and-8-minutes-respectively-if-the-priority-system-i.html)
- Using the information below, compute the turnaround time for every job for each of the following scheduling algorithms (ignore context switching overhead times). It may help to draw the timeline. | |Jo (/explanation/using-the-information-below-compute-the-turnaround-time-for-every-job-for-each-of-the-following-scheduling-algorithms-ignore-context-switching-overhead-times-it-may-help-to-draw-the-timeline-jo.html)
- The following statement(s) are true regarding a monitor where no condition variable is defined. (a) Only one process can be running inside the monitor at any time. (b) Processes can be blocked inside (/explanation/the-following-statement-s-are-true-regarding-a-monitor-where-no-condition-variable-is-defined-a-only-one-process-

Ask a Question

can-be-running-inside-the-monitor-at-any-time-b-processes-can-be-blocked-inside.html)

- Consider a single CPU system with two active processors A and B. Explain what happens i the following circumstances including any interrupts, system calls, etc. and how they are handled until a proces (/explanation /consider-a-single-cpu-system-with-two-active-processors-a-and-b-explain-what-happens-i-the-following-circumstances-including-any-interrupts-system-calls-etc-and-how-they-are-handled-until-a-proces.html)
- Assume we have an implementation of the instruction pipeline with the times for each stage given below. Answer the following 3 questions. a) What should the clock rate of the processor be if we use a (/explanation/assume-we-have-an-implementation-of-the-instruction-pipeline-with-the-times-for-each-stage-given-below-answer-the-following-3-questions-a-what-should-the-clock-rate-of-the-processor-be-if-we-use-a.html)
- Assume that the instruction is executed in a single-cycle datapath. The following instruction was fetched: 0000 0010 0001 0000 1000 0000 0010 0000 Assume the data memory is all zeros and that the proc (/explanation /assume-that-the-instruction-is-executed-in-a-single-cycle-datapath-the-following-instruction-was-fetched-0000-0010-0001-0000-1000-0000-0010-0000-assume-the-data-memory-is-all-zeros-and-that-the-proc.html)
- Consider a CPU that implements two parallel fetch-execute pipelines for superscalar processing. Show the performance improvement over scalar pipeline processing and nopipeline processing, assuming the (/explanation /consider-a-cpu-that-implements-two-parallel-fetch-execute-pipelines-for-superscalar-processing-show-the-performance-improvement-over-scalar-pipeline-processing-and-nopipeline-processing-assuming-the.html)
- Compute the clock period for the following clock frequencies. a. 50 kHz (early computers) b. 300 MHz (Sony PlayStation 2 processor) c. 3.4 GHz (Intel Pentium 4 processor d. 10 GHz (PCs of the early 20 (/explanation /compute-the-clock-period-for-the-following-clock-frequencies-a-50-khz-early-computers-b-300-mhz-sony-playstation-2-processor-c-3-4-ghz-intel-pentium-4-processor-d-10-ghz-pcs-of-the-early-20.html)
- Assume a RISC processor takes two microseconds to execute each instruction and an I/O device can wait at most 1 millisecond before its interrupt is serviced. What is the maximum number of instructions (/explanation/assume-a-risc-processor-takes-two-microseconds-to-execute-each-instruction-and-an-i-o-device-can-wait-at-most-1-millisecond-before-its-interrupt-is-serviced-what-is-the-maximum-number-of-instructions.html)
- Assume that a RISC processor takes 2 microseconds to execute each instruction and that an I/O device can wait at most 1 millisecond before its interrupt is serviced. What is the maximum number of inst (/explanation/assume-that-a-risc-processor-takes-2-microseconds-to-execute-each-instruction-and-that-an-i-o-device-can-wait-at-most-1-millisecond-before-its-interrupt-is-serviced-what-is-the-maximum-number-of-inst.html)
- Suppose that an unpipelined processor has a cycle time of 25 ns, and its datapath consists of modules with the latencies of 2, 3, 4, 7, 3, 2, and 4 ns (in that specific order). In pipelining this proc (/explanation/suppose-that-an-unpipelined-processor-has-a-cycle-time-of-25-ns-and-its-datapath-consists-of-modules-with-the-latencies-of-2-3-4-7-3-2-and-4-ns-in-that-specific-order-in-pipelining-this-proc.html)
- Show the stack for the following code: 000B 120300 LCALL DELAY 000E 80F0 SJMP BACK ;keep doing this 0010 0010 ; this is the delay subroutine 0300 ORG 300H 0300 DELAY: 0300 (/explanation/show-the-stack-for-the-following-code-000b-120300-lcall-delay-000e-80f0-sjmp-back-keep-doing-this-0010-0010-this-is-the-delay-subroutine-0300-org-300h-0300-delay-0300.html)
- The execution time of a program P on processor architecture X is denoted t_{execX(P)} in the lecture notes. It can be approximately measured by capturing the current system time just before the progra (/explanation/the-execution-time-of-a-program-p-on-processor-architecture-x-is-denoted-t-execx-p-in-the-lecture-notes-it-can-be-approximately-measured-by-capturing-the-current-system-time-just-before-the-progra.html)
- Given the following information: Job A, Arrival Time O, CPU Cycle 15 Job B, Arrival Time 2, CPU cycle 02 Job C, Arrival Time 3, CPU Cycle 14 Job D, Arrival Time 6, CPU Cycle 10 Job E, Arrival Time (/explanation/given-the-following-information-job-a-arrival-time-o-cpu-cycle-15-job-b-arrival-time-2-cpu-cycle-02-job-c-arrival-time-3-cpu-cycle-14-job-d-arrival-time-6-cpu-cycle-10-job-e-arrival-time.html)
- Consider the following solution to the mutual-exclusion problem involving two processes P0 and P1. Assume that the variable turn is initialized to 0. Process P0's code is presented below. /* Other cod (/explanation/consider-the-

Ask a Question

following-solution-to-the-mutual-exclusion-problem-involving-two-processes-p0-and-p1-assume-that-the-variable-turn-is-initialized-to-0-process-p0-s-code-is-presented-below-other-cod.html)

- Suppose a machine on average takes 10^{-10} seconds to execute a single algorithm step. When does the machine finish executing the below code when n=1000?(1000 \cong 2^{10}) sum=0; for(i=0; i <=n;i++) (/explanation/suppose-a-machine-on-average-takes-10-10-seconds-to-execute-a-single-algorithm-step-when-does-the-machine-finish-executing-the-below-code-when-n-1000-1000-cong-2-10-sum-0-for-i-0-i-n-i.html)

- Consider a virtual cylinder with the following characteristics: seek time is 4 ms/track, search time is 1.7 ms/sector, and data transfer time is 0.9 ms. Calculate the resulting seek time, search time, (/explanation/consider-a-virtual-cylinder-with-the-following-characteristics-seek-time-is-4-ms-track-search-time-is-1-7-ms-sector-and-data-transfer-time-is-0-9-ms-calculate-the-resulting-seek-time-search-time.html)

- Suppose the logic blocks in a processor have the following latencies... a) In a single cycle, non-pipelined processor, what is the minimum time between instructions for an application executing only (/explanation/suppose-the-logic-blocks-in-a-processor-have-the-following-latencies-a-in-a-single-cycle-non-pipelined-processor-what-is-the-minimum-time-between-instructions-for-an-application-executing-only.html)

- Assume that the instrctions of a processor P can be divided into four classes according to their CPI(class A, B, C and D). The processor P has a clock rate of 2.5GHz and CPIs of 4, 2, 1 and 3 for clas (/explanation/assume-that-the-instrctions-of-a-processor-p-can-be-divided-into-four-classes-according-to-their-cpi-class-a-b-c-and-d-the-processor-p-has-a-clock-rate-of-2-5ghz-and-cpis-of-4-2-1-and-3-for-clas.html)

- In this exercise we examine in detail how an instruction is executed in a single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instructi (/explanation/in-this-exercise-we-examine-in-detail-how-an-instruction-is-executed-in-a-single-cycle-datapath-problems-in-this-exercise-refer-to-a-clock-cycle-in-which-the-processor-fetches-the-following-instructi.html)

- Given the following information: || Job ||Arrival Time ||CPU Cycle |A| 0| 15 | B| 2| 2 | C| 3| 14 | D| 6| 10 | E| 9| 1 Calculate which jobs will have arrived ready for processing by the time the first (/explanation/given-the-following-information-job-arrival-time-cpu-cycle-a-0-15-b-2-2-c-3-14-d-6-10-e-9-1-calculate-which-jobs-will-have-arrived-ready-for-processing-by-the-time-the-first.html)

- The following three threads show how each would execute running alone on a standard superscalar processor without multithreading support. Show how they would execute running together with the followin (/explanation/the-following-three-threads-show-how-each-would-execute-running-alone-on-a-standard-superscalar-processor-without-multithreading-support-show-how-they-would-execute-running-together-with-the-followin.html)

- Consider the following pseudo-code program: sum : integer // a global variable procedure add(amount : integer) # sum := sum + amount procedure p(x : integer, adder : procedure) # integer sum # sum := (/explanation/consider-the-following-pseudo-code-program-sum-integer-a-global-variable-procedure-add-amount-integer-sum-sum-amount-procedure-p-x-integer-adder-procedure-integer-sum-sum.html)

- In this question, we will examine space/time optimizations for page tables. The following list provides parameters of a virtual memory system. Virtual address (bits): 43 Physical memory installed: 16G (/explanation/in-this-question-we-will-examine-space-time-optimizations-for-page-tables-the-following-list-provides-parameters-of-a-virtual-memory-system-virtual-address-bits-43-physical-memory-installed-16g.html)

- A non-pipelined system takes 100ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 20ns. a. Determine the speedup ratio of the pipeline for 100 tasks.\ (/explanation/a-non-pipelined-system-takes-100ns-to-process-a-task-the-same-task-can-be-processed-in-a-5-segment-pipeline-with-a-clock-cycle-of-20ns-determine-the-speedup-ratio-of-the-pipeline-for-100-tasks-what.html)

- Consider a computer running a program that requires 250 seconds, where 70 seconds is spent executing FP instructions, 55 seconds for INT operations, 85 seconds for load/save operations, and 40 seconds (/explanation/consider-a-computer-running-a-program-that-requires-250-seconds-where-70-seconds-is-spent-executing-fp-instructions-55-seconds-for-int-operations-85-seconds-for-load-save-operations-and-40-seconds.html)

- Assume your computer clock runs at the speed of 2.5 GHz (G=10^9). a. what is the clock cycle time of your

Ask a Question

computer? Reduce your answer to the final value in microseconds. b. what is the number of cloc (/explanation/assume-your-computer-clock-runs-at-the-speed-of-2-5-ghz-g-10-9-a-what-is-the-clock-cycle-time-of-your-computer-reduce-your-answer-to-the-final-value-in-microseconds-b-what-is-the-number-of-cloc.html)

- Consider a system with the following characteristics. The main memory size is 16 bytes, the cache size is 4 words, the block size is one word, and the word width is one byte. Assume the cache is initi (/explanation/consider-a-system-with-the-following-characteristics-the-main-memory-size-is-16-bytes-the-cache-size-is-4-words-the-block-size-is-one-word-and-the-word-width-is-one-byte-assume-the-cache-is-initi.html)
- A flip flop has 5 ns delay from the time the clock edge occurs to the time the output is complimented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is t (/explanation/a-flip-flop-has-5-ns-delay-from-the-time-the-clock-edge-occurs-to-the-time-the-output-is-complimented-what-is-the-maximum-delay-in-a-10-bit-binary-ripple-counter-that-uses-these-flip-flops-what-is-t.html)
- If a process is suspended (put into a wait state by an interrupt), will its threads also be suspended? Explain why the threads will or will not be suspended. Give an example to substantiate your answe (/explanation/if-a-process-is-suspended-put-into-a-wait-state-by-an-interrupt-will-its-threads-also-be-suspended-explain-why-the-threads-will-or-will-not-be-suspended-give-an-example-to-substantiate-your-answe.html)
- A. Discuss the different scheduling algorithms with respect to (a) waiting time, (b) starvation, (c) turnaround time, and (d) variance in turnaround time. B. Which scheduling algorithm was noted as (/explanation/a-discuss-the-different-scheduling-algorithms-with-respect-to-a-waiting-time-b-starvation-c-turnaround-time-and-d-variance-in-turnaround-time-b-which-scheduling-algorithm-was-noted-as.html)
- We wish to compare the performance of two different computers: M1 and M2. The following measurements have been made on these computers: Program Time on M1 Time on M2 1 2.0 sec 1.5 sec 2 5.0sec 10.0sec (/explanation/we-wish-to-compare-the-performance-of-two-different-computers-m1-and-m2-the-following-measurements-have-been-made-on-these-computers-program-time-on-m1-time-on-m2-1-2-0-sec-1-5-sec-2-5-0sec-10-0sec.html)
- Assume that main memory is composed of three page frames for public use and that a program requests pages in the following order: c c a b d c a b c a Using either the LRU or FIFO page removal algorith (/explanation/assume-that-main-memory-is-composed-of-three-page-frames-for-public-use-and-that-a-program-requests-pages-in-the-following-order-c-c-a-b-d-c-a-b-c-a-using-either-the-lru-or-fifo-page-removal-algorith.html)
- Interrupt latency is : (a) The time it takes to respond to an interrupt and begin executing an interrupt service routine. (b) The time it takes to respond to an interrupt and complete execution of an interrupt service routine. (c) The time it takes for a (/explanation/interrupt-latency-is-a-the-time-it-takes-to-respond-to-an-interrupt-and-begin-executing-an-interrupt-service-routine-b-the-time-it-takes-to-respond-to-an-interrupt-and-complete-execution-of-an-interrupt-service-routine-c-the-time-it-takes-for-a.html)
- Consider an algorithm that contains loops of this form: for (i = 1 through n) for (j = 1 through i) for (k = 1 through 10) Task T If task T requires t time units, (/explanation/consider-an-algorithm-that-contains-loops-of-this-form-for-i-1-through-n-for-j-1-through-i-for-k-1-through-10-task-t-if-task-t-requires-t-time-units.html)
- Which of the following statement regarding concurrency is incorrect? (A) In a single-processor multiprogramming system, processes are interleaved in time to yield the appearance of simultaneous execut (/explanation/which-of-the-following-statement-regarding-concurrency-is-incorrect-a-in-a-single-processor-multiprogramming-system-processes-are-interleaved-in-time-to-yield-the-appearance-of-simultaneous-execut.html)
- Consider the following method definition that has been properly defined in the class Time. void shiftBy(int dh, int dm) { hour += dh; minute += dm; } public static void main (/explanation/consider-the-following-method-definition-that-has-been-properly-defined-in-the-class-time-void-shiftby-int-dh-int-dm-hour-dh-minute-dm-public-static-void-main-string-args-int-x-2-in.html)
- Discuss the different scheduling algorithms with respect to (a) waiting time, (b) starvation, (c) turnaround time, and (d) variance in turnaround time (/explanation/discuss-the-different-scheduling-algorithms-with-respect-to-a-waiting-time-b-starvation-c-turnaround-time-and-d-variance-in-turnaround-time.html)
- Consider the following schedule: T2: R(B), T2: R(C), T3: R(C), T1: R(B), T3: R(A), T2: R(A), T3: W(A), T1: R(A), T1: W(A),

Ask a Question

T3: R(A), T3: R(B) Is the schedule serializable? If so, show an equivalent se (/explanation/consider-the-following-schedule-t2-r-b-t2-r-c-t3-r-c-t1-r-b-t3-r-a-t2-r-a-t3-w-a-t1-r-a-t1-w-a-t3-r-a-t3-r-b-is-the-schedule-serializable-if-so-show-an-equivalent-se.html)

- How do you create a Perl Module that executes system commands to retrieve system metrics like CPU utilization? (/explanation/how-do-you-create-a-perl-module-that-executes-system-commands-to-retrieve-system-metrics-like-cpu-utilization.html)
- Problems in this exercise refer to the following sequence of instructions and assume that it is executed on a 5-stage pipelined datapath. add r5,r2,r1 lw r3,4(r5) lw r2,0(r2) or r3,r5,r3 sw r3,0(r5). (/explanation/problems-in-this-exercise-refer-to-the-following-sequence-of-instructions-and-assume-that-it-is-executed-on-a-5-stage-pipelined-datapath-add-r5-r2-r1-lw-r3-4-r5-lw-r2-0-r2-or-r3-r5-r3-sw-r3-0-r5.html)
- Consider the following algorithm. for i {1, 2, 3, 4, 5, 6} do beep for j {1, 2, 3, 4} do beep for k {1, 2, 3} do for l {1, 2, 3, 4, 5} do beep for m {1, 2, 3, 4} do beep How many times does a beep (/explanation/consider-the-following-algorithm-for-i-1-2-3-4-5-6-do-beep-for-j-1-2-3-4-do-beep-for-k-1-2-3-do-for-l-1-2-3-4-5-do-beep-for-m-1-2-3-4-do-beep-how-many-times-does-a-beep.html)
- Fill in the Gant chart based on these conditions: (P, V, and context switch operations are instantaneous). Process P1 starts at time 0; P2 at time 3; P3 at time 6; P4 at time 8; and P5 at time 10. Ini (/explanation/fill-in-the-gant-chart-based-on-these-conditions-p-v-and-context-switch-operations-are-instantaneous-process-p1-starts-at-time-0-p2-at-time-3-p3-at-time-6-p4-at-time-8-and-p5-at-time-10-ini.html)
- Assume you have a queue called Q with the following contents, and trace the following operations: (front) (back) 4 8 2 3 1 System.out.println(Q.peek()); // a) What is printed? Integer Y = Q.remove (/explanation/assume-you-have-a-queue-called-q-with-the-following-contents-and-trace-the-following-operations-front-back-4-8-2-3-1-system-out-println-q-peek-a-what-is-printed-integer-y-q-remove.html)
- Consider the following Binary maxheap: a) Show the steps involved in removing the maximum and then preserving the heap properties. b) show the steps involved in adding a new node 9 and then preservi (/explanation/consider-the-following-binary-maxheap-a-show-the-steps-involved-in-removing-the-maximum-and-then-preserving-the-heap-properties-b-show-the-steps-involved-in-adding-a-new-node-9-and-then-preservi.html)
- Consider a virtual cylinder identical to the one shown the figure below with the following characteristics: seek time is 4 ms/track, search time is 1.7 ms/sector, and data transfer time is 0.9 ms. Ca (/explanation/consider-a-virtual-cylinder-identical-to-the-one-shown-the-figure-below-with-the-following-characteristics-seek-time-is-4-ms-track-search-time-is-1-7-ms-sector-and-data-transfer-time-is-0-9-ms-ca.html)
- Draw diagrams showing a conceptual view and a view and a process view of the architectures of the following systems: (a) A ticket machine used by passengers at a railway station. (b) A computer-contro (/explanation/draw-diagrams-showing-a-conceptual-view-and-a-view-and-a-process-view-of-the-architectures-of-the-following-systems-a-a-ticket-machine-used-by-passengers-at-a-railway-station-b-a-computer-contro.html)
- Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2. ||Processo (/explanation/assume-that-main-memory-accesses-take-70-ns-and-that-memory-accesses-are-36-of-all-instructions-the-following-table-shows-data-for-l1-caches-attached-to-each-of-two-processors-p1-and-p2-processo.html)
- OS Question: There are 4 processes, executing concurrently. Process P0 is in an infinite loop, incrementing the value of the variable x (x is initialized to 0). P0 is the only process that changes the (/explanation/os-question-there-are-4-processes-executing-concurrently-process-p0-is-in-an-infinite-loop-incrementing-the-value-of-the-variable-x-x-is-initialized-to-0-p0-is-the-only-process-that-changes-the.html)
- Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 60MHz and M2 has a (/explanation/consider-two-different-implementations-m1-and-m2-of-the-same-instruction-set-there-are-three-classes-of-instructions-a-b-and-c-in-the-instruction-set-m1-has-a-clock-rate-of-60mhz-and-m2-has-a.html)
- Give a big-O characterization, in terms of n, of the running time of the following method. Show your analysis!

public void Ex(int n) int a = 1; for (int i = 0 ; i less than n*n ; i++) for (int j = 0; (/explanation/give-a-big-oh-characterization-in-terms-of-n-of-the-running-time-of-the-following-method-show-your-analysis-public-void-ex-int-n-int-a-1-for-int-i-0-i-less-than-n-n-i-for-int-j-0.html)

- Which of the following is NOT contained in the process block: A. The program counter B. The accumulator C. User name D. List of open files (/explanation/which-of-the-following-is-not-contained-in-the-process-block-a-the-program-counter-b-the-accumulator-c-user-name-d-list-of-open-files.html)
- State True or False: Interrupts with a high priority can hold the execution of a CPU right after the CPU finishes a current job. (/explanation/state-true-or-false-interrupts-with-a-high-priority-can-hold-the-execution-of-a-cpu-right-after-the-cpu-finishes-a-current-job.html)
- How do you measure a computer performance? 1. Suppose you have a program runs in 100 seconds on a computer, and the multiplication subroutine takes 40 seconds. If you want the program to run 30% faste (/explanation/how-do-you-measure-a-computer-performance-1-suppose-you-have-a-program-runs-in-100-seconds-on-a-computer-and-the-multiplication-subroutine-takes-40-seconds-if-you-want-the-program-to-run-30-faste.html)
- Assume the processing time of an algorithm of Big-Oh complexity O(f(n)) to be directly proportional to f(n). Let three such algorithms, A, B, and C, have time complexity O(n), O(n \log n), O(n^2), respectively. During a test, each algorithm spends 8 milli (/explanation/assume-the-processing-time-of-an-algorithm-of-big-oh-complexity-o-f-n-to-be-directly-proportional-to-f-n-let-three-such-algorithms-a-b-and-c-have-time-complexity-o-n-o-n-log-n-o-n-2-respectively-during-a-test-each-algorithm-spends-8-milli.html)
- C ONLY. Consider the function: f(t) = 2t+1: t is [0,T] and 0 otherwise. Carry out the following steps: Read in an integer value for T. Sample the function f(t) above, at t = 0, 1, 2 . . . T and wr (/explanation/c-only-consider-the-function-f-t-2t-1-t-is-0-t-and-0-otherwise-carry-out-the-following-steps-read-in-an-integer-value-for-t-sample-the-function-f-t-above-at-t-0-1-2-t-and-wr.html)
- The equation below relates seconds to instruction cycles. CPU = time = seconds/ program = instruction/program * ???/ Instruction * seconds/cycle What goes in the ???? space? (/explanation/the-equation-below-relates-seconds-to-instruction-cycles-cpu-time-seconds-program-instruction-program-instruction-seconds-cycle-what-goes-in-the-space.html)
- Consider the following snapshot of a system (P=Process, R=Resource): Answer the following questions using banker's algorithm: a. Calculate needs matrix: b) Is the system in a safe state? If so, show h (/explanation/consider-the-following-snapshot-of-a-system-p-process-r-resource-answer-the-following-questions-using-banker-s-algorithm-a-calculate-needs-matrix-b-is-the-system-in-a-safe-state-if-so-show-h.html)
- 1. Identify and explain the three major steps for effective file maintenance. 2. How do clock speed and word size determine the performance of a CPU? 3. Which secondary storage devices are appropriate (/explanation/1-identify-and-explain-the-three-major-steps-for-effective-file-maintenance-2-how-do-clock-speed-and-word-size-determine-the-performance-of-a-cpu-3-which-secondary-storage-devices-are-appropriate.html)
- Given the following algorithms, represent the number of times x=x+1 is executed in Big-O notations. a. i=1 x=0 while (i leq 5n) x=x+1 i=i+2 b. x=0 for i=1 to n for j=1 to n i=i+1 for k (/explanation/given-the-following-algorithms-represent-the-number-of-times-x-x-1-is-executed-in-big-o-notations-a-i-1-x-0-while-i-leq-5n-x-x-1-i-i-2-b-x-0-for-i-1-to-n-for-j-1-to-n-i-i-1-for-k.html)
- You are given the following parameters for a disk drive problem: a single-platter disk, a rotation speed of 7200 RPM, 3000 tracks on one side of platter, 600 sectors per track, and a seek time of 1 ms (/explanation/you-are-given-the-following-parameters-for-a-disk-drive-problem-a-single-platter-disk-a-rotation-speed-of-7200-rpm-3000-tracks-on-one-side-of-platter-600-sectors-per-track-and-a-seek-time-of-1-ms.html)
- Consider the problem of computing N! = 1 2 3 N. (a) If N is an n-bit number, how many bits long is N!, approximately (in () form)? (b) Give an algorithm to compute N! and analyze its running time. (/explanation/consider-the-problem-of-computing-n-1-2-3-n-a-if-n-is-an-n-bit-number-how-many-bits-long-is-n-approximately-in-form-b-give-an-algorithm-to-compute-n-and-analyze-its-running-time.html)

- Consider a system with three smoker processes and one agent process (multiple threads problem). Each smoker continuously rolls a cigarette and then smokes it. But to roll and smoke a cigarette, the sm (/explanation/consider-a-system-with-three-smoker-processes-and-one-agent-process-multiple-threads-problem-each-smoker-continuously-rolls-a-cigarette-and-then-smokes-it-but-to-roll-and-smoke-a-cigarette-the-sm.html)

- Write a C program for an HCS12 microcontroller that writes the value, 0x78 to Memory Location VAR1 and then calls a delay function. The delay function should generate a delay of 0.25 milliseconds. The (/explanation/write-a-c-program-for-an-hcs12-microcontroller-that-writes-the-value-0x78-to-memory-location-var1-and-then-calls-a-delay-function-the-delay-function-should-generate-a-delay-of-0-25-milliseconds-the.html)

- Write a C program for a HCS12 microcontroller that writes the value, 0x78, to Memory Location VAR1 and then calls a delay function. The delay function should generate a delay of 0.25 milliseconds. The (/explanation/write-a-c-program-for-a-hcs12-microcontroller-that-writes-the-value-0x78-to-memory-location-var1-and-then-calls-a-delay-function-the-delay-function-should-generate-a-delay-of-0-25-milliseconds-the.html)

- Suppose the processing load of a computing system consists of 60% CPU activity and 40% disk activity. Your customers are complaining that the system is slow. After research, you discover that you can (/explanation/suppose-the-processing-load-of-a-computing-system-consists-of-60-cpu-activity-and-40-disk-activity-your-customers-are-complaining-that-the-system-is-slow-after-research-you-discover-that-you-can.html)

- Design a 4-bit down counter (decrement by 1) and analyze for the same metrics. Assume that no enable signal is used in this case. Assume the same delay characteristic equation and hold time/setup time (/explanation/design-a-4-bit-down-counter-decrement-by-1-and-analyze-for-the-same-metrics-assume-that-no-enable-signal-is-used-in-this-case-assume-the-same-delay-characteristic-equation-and-hold-time-setup-time.html)

- Assume that main memory is composed of only three page frames for public use and that a program requests pages in the following order: a, c, b, d, a, c, e, a, c, b, d, e. a. Using the FIFO page remova (/explanation/assume-that-main-memory-is-composed-of-only-three-page-frames-for-public-use-and-that-a-program-requests-pages-in-the-following-order-a-c-b-d-a-c-e-a-c-b-d-e-a-using-the-fifo-page-remova.html)

- Consider the following database. EMPLOYEE(Name, SSN, Salary, DNO, SupervisorSSN, JobCode) DEPARTMENT(DNO, TotalSalary, ManagerSSN) STARTING_PAY(JobCode, StartPay) Note that Dept_No in EMPLOYEE table i (/explanation/consider-the-following-database-employee-name-ssn-salary-dno-supervisorssn-jobcode-department-dno-totalsalary-managerssn-starting-pay-jobcode-startpay-note-that-dept-no-in-employee-table-i.html)

- Please anazlyze the time complexity of the following functions or for-loops. For each question, use the following template to figure out the total time needed to finish the corresponding function or f (/explanation/please-anazlyze-the-time-complexity-of-the-following-functions-or-for-loops-for-each-question-use-the-following-template-to-figure-out-the-total-time-needed-to-finish-the-corresponding-function-or-f.html)

- The following table represents a small memory. Refer to this table for the following questions. ||Address||Data |0000|0001 1110 0100 0011 |0001|1111 0000 0010 0101 |0010|0110 1111 0000 0001 |0011|0000 (/explanation/the-following-table-represents-a-small-memory-refer-to-this-table-for-the-following-questions-address-data-0000-0001-1110-0100-0011-0001-1111-0000-0010-0101-0010-0110-1111-0000-0001-0011-0000.html)

- Consider a program that can execute with no stalls and a CPI of 1 if the underlying processor can service every load instruction with a 2-cycle L1 cache hit. In practice, 10% of all load instructions (/explanation/consider-a-program-that-can-execute-with-no-stalls-and-a-cpi-of-1-if-the-underlying-processor-can-service-every-load-instruction-with-a-2-cycle-l1-cache-hit-in-practice-10-of-all-load-instructions.html)

- Consider the following database. EMPLOYEE(Name, SSN, Salary, DNO, SupervisorSSN, JobCode) DEPARTMENT(DNO, TotalSalary, ManagerSSN) STARTING_PAY(JobCode, StartPay) Note that Dept_No in EMPLOYEE tab (/explanation/consider-the-following-database-employee-name-ssn-salary-dno-supervisorssn-jobcode-department-dno-totalsalary-managerssn-starting-pay-jobcode-startpay-note-that-dept-no-in-employee-tab.html)

- 1. Consider the following database. EMPLOYEE(Name, SSN, Salary, DNO, SupervisorSSN, JobCode) DEPARTMENT(DNO, TotalSalary, ManagerSSN) STARTING_PAY(JobCode, StartPay) Note that Dept_No in EMPLOYEE (/explanation/1-consider-the-following-database-employee-name-ssn-salary-dno-supervisorssn-jobcode-department-dno-totalsalary-managerssn-starting-pay-jobcode-startpay-note-that-dept-no-in-employee.html)

- Design an algorithm find?in?heap(T[1...n],x]) that looks for the value x in the heap T and returns either the index of x in the heap, if it is present, or 0 otherwise. What is the running time of your (/explanation/design-an-algorithm-find-in-heap-t-1-n-x-that-looks-for-the-value-x-in-the-heap-t-and-returns-either-the-index-of-x-in-the-heap-if-it-is-present-or-0-otherwise-what-is-the-running-time-of-your.html)
- 1. Describe the following threats to the application environment: Buffer overflow Denial of Service Time-of-check to time-of-use attacks Malformed input attacks Object reuse Garbage collection Trap do (/explanation/1-describe-the-following-threats-to-the-application-environment-buffer-overflow-denial-of-service-time-of-check-to-time-of-use-attacks-malformed-input-attacks-object-reuse-garbage-collection-trap-do.html)
- Consider the following snapshot of a system: Answer the following questions using the banker's algorithm: a. Illustrate that the system is in a safe state by demonstrating an order in which the pro (/explanation/consider-the-following-snapshot-of-a-system-answer-the-following-questions-using-the-banker-s-algorithm-a-illustrate-that-the-system-is-in-a-safe-state-by-demonstrating-an-order-in-which-the-pro.html)
- A system spends 65% of the time running in the CPU and 35% of the time waiting for service. The processor option offers a 50% faster CPU but costs $8500 and the disk option offers to be 125% faster bu (/explanation/a-system-spends-65-of-the-time-running-in-the-cpu-and-35-of-the-time-waiting-for-service-the-processor-option-offers-a-50-faster-cpu-but-costs-8500-and-the-disk-option-offers-to-be-125-faster-bu.html)
- Calculate the bandwidth x delay product for the following links. Use one-way delay. a) 100-Mbps Ethernet with a roundtrip delay of 50 ms. b) 1-Mbps link, with a one-way delay of 100 ms. (/explanation/calculate-the-bandwidth-x-delay-product-for-the-following-links-use-one-way-delay-a-100-mbps-ethernet-with-a-roundtrip-delay-of-50-ms-b-1-mbps-link-with-a-one-way-delay-of-100-ms.html)
- How long does a program take to run on a processor with a 2GHz clock if it has 10^10 instructions and a CPI of 2? (/explanation/how-long-does-a-program-take-to-run-on-a-processor-with-a-2ghz-clock-if-it-has-10-10-instructions-and-a-cpi-of-2.html)
- Which of the following is not a hardware approach to mutual exclusion? (A) Interrupt disabling (B) Compare and Swap instruction (C) Spin waiting (D) Exchange instruction (E) Semaphores (/explanation/which-of-the-following-is-not-a-hardware-approach-to-mutual-exclusion-a-interrupt-disabling-b-compare-and-swap-instruction-c-spin-waiting-d-exchange-instruction-e-semaphores.html)
- Suppose a disk drive (a rather old one) has the following characteristics: *7 surfaces *1024 tracks per surface *512 sectors per track *2048 bytes per sector *Track-to-track seek time of 8 millis (/explanation/suppose-a-disk-drive-a-rather-old-one-has-the-following-characteristics-7-surfaces-1024-tracks-per-surface-512-sectors-per-track-2048-bytes-per-sector-track-to-track-seek-time-of-8-millis.html)
- Which of the following components of program state are shared across threads in a multithreaded process. (a) Register values (b) Heap memory (c) Global variables (d) Stack memory (/explanation/which-of-the-following-components-of-program-state-are-shared-across-threads-in-a-multithreaded-process-a-register-values-b-heap-memory-c-global-variables-d-stack-memory.html)
- For the program below, give the values for I_COUNT and J_COUNT to get a loop iteration of 60,000. R0 EQU $1000 R1 EQU $1001 I_COUNT EQU ______ J_COUNT EQU ______ LDAA #I_COUNT STAA R0 L2 LDAA #J_COUN (/explanation/for-the-program-below-give-the-values-for-i-count-and-j-count-to-get-a-loop-iteration-of-60-000-r0-equ-1000-r1-equ-1001-i-count-equ-j-count-equ-ldaa-i-count-staa-r0-l2-ldaa-j-coun.html)
- Consider the following recursive function and design a DP algorithm to solve this function F. F(i, j) = min F(i-1, j-1)+l(x[i], y[j]), F(i-1, j)+1, F(i, j-1)+1 , where l(x[i], y[j]) = 0 if x[i] = (/explanation/consider-the-following-recursive-function-and-design-a-dp-algorithm-to-solve-this-function-f-f-i-j-min-f-i-1-j-1-i-x-i-y-j-f-i-1-j-1-f-i-j-1-1-where-i-x-i-y-j-0-if-x-i.html)
- 1. Order the following functions from slowest growing to fastest growing by inspecting their graphs. a. T(n)=n b. T(n)=1 c. T(n)= sqrtn d. T(n)=n^2 e. T(n)=\log n 2. Give the big O for the following (/explanation/1-order-the-following-functions-from-slowest-growing-to-fastest-growing-by-inspecting-their-graphs-a-t-n-n-b-t-n-1-c-t-

Ask a Question

n-sqrtn-d-t-n-n-2-e-t-n-log-n-2-give-the-big-o-for-the-following.html)

- Rewrite the following code to minimize performance on a pipeline datapath -- that is, reorder the instructions so that this sequence takes the most clock cycles to execute while still obtaining the sa (/explanation/rewrite-the-following-code-to-minimize-performance-on-a-pipeline-datapath-that-is-reorder-the-instructions-so-that-this-sequence-takes-the-most-clock-cycles-to-execute-while-still-obtaining-the-sa.html)
- Which of the following characterize business processes that can effectively be implemented in a CRM system? (Select all that apply.) A) The processes are clear. B) The processes are differentiated fro (/explanation/which-of-the-following-characterize-business-processes-that-can-effectively-be-implemented-in-a-crm-system-select-all-that-apply-a-the-processes-are-clear-b-the-processes-are-differentiated-fro.html)
- Assume we need to build a binary max-on-top heap from keys 10, 12, 1, 14, 6, 5, 8, 15, 3, 9, 7, 4, 11, 13, 2. a) Show the result of building this heap by inserting the above keys one at a time in the (/explanation/assume-we-need-to-build-a-binary-max-on-top-heap-from-keys-10-12-1-14-6-5-8-15-3-9-7-4-11-13-2-a-show-the-result-of-building-this-heap-by-inserting-the-above-keys-one-at-a-time-in-the.html)
- a. Suppose the following LC-3 program is loaded into memory starting at location x30FF: rl x30FF b. The following memory locations contain values as shown below; rl x3050: Now, the following three L (/explanation/a-suppose-the-following-lc-3-program-is-loaded-into-memory-starting-at-location-x30ff-rl-x30ff-b-the-following-memory-locations-contain-values-as-shown-below-rl-x3050-now-the-following-three-l.html)

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