Instructions to operations translation:

Note: Every instruction needs to do PC walk (named by myself) at first. If there is no pipeline, instruction fetch is the first work we need to do. (If there is pipeline, we could do next instruction fetch when execute the previous instruction.) It is same for all

Add instruction example:

Note: For add, PC = PC + 4 is updated by itself, the execute unit won't give value to PC. So, the PC update and instruction execute could do simultaneously.

```
Add rd, rs, rt
PC walk:
Cycle 1:
    PC -> PC_DEM -> LPC_LSadd
Cvcle 2:
    LPC_LSadd -> Address_MUX -> LLS_Address
Cycle 3:
    LLS_Address -> L/S unit -> LLoaddata
Cycle 4:
    LLoaddate -> Load_DEM -> LINS
Cycle 5:
    LINS -> Instruction decoder -> (LRD, LRS, LRT, LL, Lopcode)
Cycle 6:
    Lopcode -> Instruction Look-Op Table -> Control signal array
All these 6 cycle are same for all the instructions
Execute (control signal array begin to control the execute unit):
    Immediate -> LIM (no use in add),
    LRS -> LRS_DEM -> LRS_LRF1
    LRT -> LRT_DEM -> LRT_LRF2
Cycle 8:
    LRS_LRF1 -> LRF1_MUX -> LRF1
    LRT_LRF2 -> LRF2_MUX -> LRF2
Cycle 9:
    LRF1 -> RF -> LRFOUT1
    LRF2 -> RF -> LRFOUT2
Cycle 10:
    LRFOUT1 -> LRFOUT1_DEM -> LRFOUT1_L1
    LRFOUT2 -> LRFOUT2_DEM -> LRFOUT2_L2
Cycle 11:
    LRFOUT1_L1 -> L1_MUX -> L1
    LRFOUT2_L2 -> L2_MUX -> L2
Cycle 12:
    L1 -> L1_DEM -> LDEM1_1
```

Simultaneously, we can also update the PC's value:

PC update cycle 1:

LRF1, LRF2 -> RF

PC -> PC_DEM -> LPC_Add4

PC update cycle 2:

LPC_Add4 -> Add4 -> Ladd4_OUT

PC update cycle 3:

Ladd4_OUT -> PC_MUX -> PC

Note: As these operations are totally separated from the execute unit, we could update the PC's value anytime.

If we want to update earlier (good for pipeline, begin instruction fetch earlier), we could do that in cycle 7, 8, 9.

If we want to update later (update finished when add instruction finish), we could do that in cycle 15, 16, 17.

Any time between them all works.