Less or Equal
Number of input ports: 2 64-bit each
Number of output latches: 1 64-bit
Control signal: N/A
Function: Compare the signed value present at the first input port with the value present at the second port. Produces 0 if the first input is less or equal than the second input, 1 otherwise.
Area: 600nm^2
Power: 1W

12-bit write
Number of input ports: 2 64-bit each
Number of output latches: 1 64-bit
Control signal: N/A
Function: write the second input value's last 12 bits to the first input value's last 12 bits.
Area: 300nm^2 (As the logic has four functions and area is 600 nm^2, the 12-bit write only use and to erase the last 12 bits and then use or to write the last 12 bits, I think half area and power of the logic make sense)
Power: 0.5W

L/S unit
Number of input ports: 2 64-bit each
Number of output latches: 1 64-bit
Control signal: 0b0 for load, 0b1 for store
Function: If load model, the L/S unit get the address from the address input and output the value at that address. If store model, the L/S unit get the address from the address input and get value from the value input, then store the value in corresponding address in memory.
Area: 20000nm^2
Power: 4W

Input
Number of input ports: 1 64-bit
Number of output latches: 1 64-bit
Control signal: N/A
Function: Read the value from port pointed to by 'port' footprint and send back the value through 'value' footprint.
Area: 150nm^2
Power: 0.1W

Output
Number of input ports: 2 64-bit each
Number of output latches: 1 N/A
Control signal: N/A
Function: Read the value from 'value' footprint and writes it to the output port pointed to by the value of 'port' footprint.

Area: 150nm^2
Power: 0.1W

Instruction Look-Up Table
Number of input ports: 1 5-bit
Number of output latches: control array and the latch of immediate (1-bit)
Control signal: N/A
Function: Translate the instructions to control signal vector of each cycle. It could give multiple cycle control signal vectors (belonging to the same instruction) to the control array.
Area: 20000nm^2
Power: 4W

Instruction decoder
Number of input ports: 1 32-bit (instruction)
Number of output latches: 5. (Lopcode: latch to store opcode, LRD: latch to store rd's value in this instruction, LRS: latch to store rs's value in this instruction, LRT: latch to store rt's value in this instruction, LL: latch to store literal's value in this instruction,
Control signal: N/A
Function: Translate the instructions to control signal vector of each cycle. It could give multiple cycle control signal vectors (belonging to the same instruction) to the control array.
Area: 400nm^2
Power: 0.5W