

Chapter 5 HW

5.13

a. $0001 \mid 011 \mid 010 \mid 1 \mid 00000$
 ADD R3 R2 #0

b. $1001 \mid 011 \mid 011 \mid 111111 \rightarrow 0001 \mid 011 \mid 011 \mid 1 \mid 00001 \rightarrow 0001 \mid 001 \mid 010 \mid 011 \mid 011$
 NOT R3 R3 $1^{\text{'s}}$ Com. ADD R3 R3 #1 $2^{\text{'s}}$ Com. ADD R1 R2 R3

c. $0101 \mid 001 \mid 001 \mid 1 \mid 1111$
 AND R1 R1 #1

d. Contents of general-purpose register can never be negative or zero at the same time, so this situation is impossible.

e. $0101 \mid 010 \mid 010 \mid 0 \mid 00000$
 AND R2 R2 #0

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1) <u>1001 100 001 11111</u>	NOT, R4, R1, -1
2) <u>1001 101 010 11111</u>	NOT, R5, R2, -1
3) <u>0101 110 100 000 101</u>	AND, R6, R4, R5
4) <u>1001 011 110 11111</u>	NOT, R3, R6, -1

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Address	Data	
0011 0001 0000 0000	1110 001 000100000	LEA, R1, #32 $R1 \leftarrow 0x3121$
0011 0001 0000 0001	0010 010 000100000	LD, R2, #32 $R2 \leftarrow MEM[0x3122]$
0011 0001 0000 0010	1010 011 000100000	LDI, R3, R0, #32 $R3 \leftarrow MEM[MEM[0x3123]]$
0011 0001 0000 0011	0110 100 010 000001	LDR, R4, R2, #1 $R4 \leftarrow MEM[R2 + 0x1]$
0011 0001 0000 0100	1111 0000 0010 0101	<u>HALT</u>
:	:	
:	:	
0011 0001 0010 0010	0100 0101 0110 0110	
0011 0001 0010 0011	0100 0101 0110 0111	
:	:	
:	:	
0100 0101 0110 0111	1010 1011 1100 1101	
0100 0101 0110 1000	1111 1110 1101 0011	

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x30FF	1110 0010 0000 0001	LEA, R1, #1 ($R1 \leftarrow 0x3000+1$) $R1 \leftarrow 0x3101$
x3100	0110 0100 0100 0010	LDR, R2, R1, #2 ($R2 \leftarrow MEM[R1+2]$)
x3101	1111 0000 0010 0101	<u>HALT</u>
x3102	0001 0100 0100 0001	
x3103	0001 0100 1000 0010	

1 4 8 2

$$R_2 = 0.1482$$