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Assignment #3

Total points: 100

CDA 4101
Assignment # 3

---There are 5 questions in this assignment------------------------------------

Objectives: The goal of the assignment is to:

- familiarize you with quantitative analysis of caches

- understanding different types of cache policies

- investigate which cache is better based on cache configuration

- investigate the tradeoffs between write-through and write-back caches

Part 1. Memory analysis

Question 1 (40 pt). You are given designs of 3 caches for a 16-bit address machine:

D1:
Direct-mapped cache.
Each cache line is 1 byte.
10-bit index, 6-bit tag.
1 cycle hit time.

D2:
2-way set associative cache.
Each cache line is 1 word (4 bytes).
7-bit index, 7-bit tag.
2 cycle hit time.

D3:
fully associative cache with 256 cache lines.
Each cache line is 1 word.
14-bit tag.
5 cycle hit time.

Answer the following set of questions:

a) What is the size of each cache?

D1 = 2^{10} * 1 = 1 KB

D2 = 2^7 * 4 * 2 = 128 * 4 = 512 * 2 = 1 KB

D3 = 256 * 4 = 1 KB

b) How much space does each cache need to store tags?

D1 = 1 KB * 6 tags = 6 Kb

D2 = 256 * 7 = 1792 bits

D3 = 256 * 14 = 3584 bits

c) Which cache design has the most conflict misses? Which has the least?

The cache design with the most conflict misses would be direct mapped cache since it is directly mapped. The one with least conflict miss is fully associative cache since it can never have conflict misses.

d) The following information is given to you: hit rate for the 3 caches is 50%, 70% and 90% but did not tell you which hit rate corresponds to which cache, which cache would you guess corresponded to which hit rate? Why?

Direct Mapped – 50% since it has the most conflict misses

2-way Set Associative – 70%

Fully Associative – 90% since it has the least conflict misses (0 conflict misses)

e) Assuming the miss time for each is 20 cycles, what is the average service time for each? (Service Time = (hit rate)*(hit time) + (miss rate)*(miss time)).

D1 Service Time = (0.5 * 1) + (0.5 * 20) = 10.5 cycles

D2 Service Time = (0.7 * 2) + (0.3 * 20) = 7.4 cycles

D3 Service Time = (0.9 * 5) + (0.1 * 20) = 6.5 cycles

Question 2 (30 pt). Assume we have a computer where the CPI is 1.0 when all memory accesses (including data and instruction accesses) hit in the cache. The cache is a unified (data + instruction) cache of size 256 KB, 4-way set associative, with a block size of 64 bytes. The data accesses (loads and stores) constitute 50% of the instructions. The unified cache has a miss penalty of 25 clock cycles and a miss rate of 2%. Assume 32-bit instruction and data addresses. Now, answer the following questions:

a) What is the tag size for the cache?

Tag Size = 32 – ((log 64) + (log (256K/64*4))
Tag Size = 32 – (6 + 10) = 16 bits
b. How much faster would the computer be if all memory accesses were cache hits?

CPI = 1 + (1.5 * 0.02 * 25) = 1.75

1.75 times faster.

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Part2: Handling Cache Miss

Question 3 (30 pt). You purchased a computer with the following features:

- 95% of all memory accesses are found in the cache.

- Each cache block is two words, and the whole block is read on any miss.

- The processor sends references to its cache at the rate of 10^9 words per second.

- 25% of those references are writes.

- Assume that the memory system can support 10^9 words per second, reads or writes.

- The bus reads or writes a single word at a time (the memory system cannot read or write two words at once).

- Assume at any one time, 30% of the blocks in the cache have been modified.

- The cache uses write allocate on a write miss.

- You are considering adding a peripheral to the system, and you want to know how much of the memory system bandwidth is already used.

Calculate the percentage of memory system bandwidth used on the average in the two cases below. Be sure to state your assumptions.

Read hits = 0.75 *0.95 = 0.7125

Read misses = 0.75 * 0.05 = 0.0375

Write hits = 0.25 * 0.95 = 0.2375

Write misses = 0.25 * 0.05 = 0.0125

a. Case 1: The cache is write through.

Average words transferred = (0.7125 * 0) + (0.0375 * 2) + (0.2375 * 1) + (0.0125 * 3) = 0.35
Average bandwidth used = 0.35 * 10^9
Percentage bandwidth = 35%
b. Case 2: The cache is write back.

Average words transferred = (0.7125 * 0) + (0.0375 * ((0.7 * 2) + (0.3 * 4))) + (0.2375 * 0) + (0.0125 * ((0.7 * 2) + (0.3 * 4))) = 0.13
Average bandwidth used = 0.13 * 10^9
Percentage bandwidth = 13%

--------------------------------------**Questions END here**-------------------------------