



DLD PROJECT

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PROJECT'S NAME: THREE WAYS TRAFFIC LIGHT

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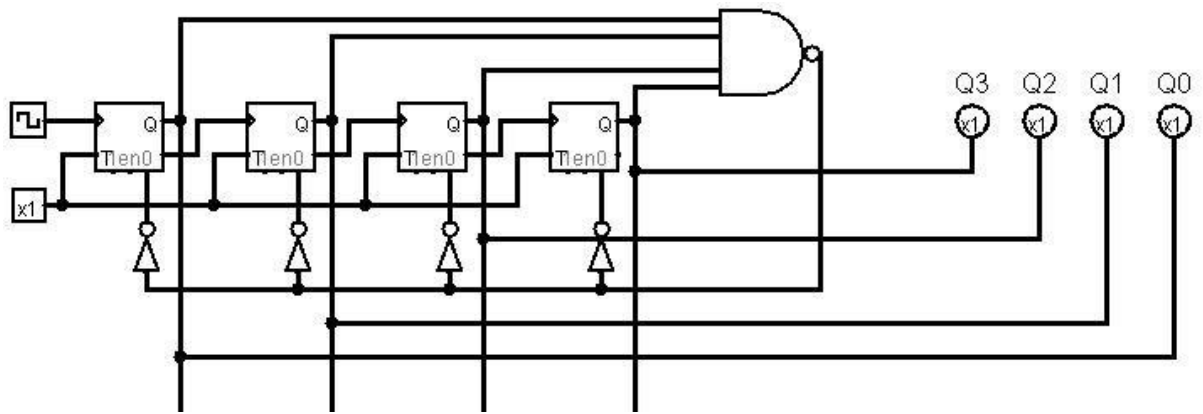
GOAL OF THE PROJECT

- To be able implemented DLD learning in the function of traffic light.
- To know how to use Logisim as a circuit software platform.
- To identify the uses of DLD component in real life machine.

DESIGN PROCESS

a) COUNTER

Asynchronous counter used in this project. There is four T flip flop is used and each of the flip flop has HIGH as the input to make sure the output work in toggle mode. The first flip flop is clocked by external clock while the other flip flop clocked by the output of previous flip flop. The modulus of the counter should be 16 due to 4 flip flop being used but this project only used 15 as the number of unique states. This is because the tempo or period for one cycle for this project only 15 second which every traffic light has 4 second to be operate as green light and 1 second as yellow light. While one of the traffic light operate, the others light up the red light to show that the way is on used for the one that being operated. To make the modulus is 15 rather than 16, the (1111) output decode with NAND gate and the output of the gate is connected to CLR bar to clear all the flip flop output to (0000). This means the output Q3,Q2,Q1 and Q0 connected to NAND gate and the gate connected to CLR bar for every flip flop. Positive edge triggered is used, so the next flip flop clock is clocked by the output of the previous flip flop which is Q bar to make the counts is count up from 0000 until 1110 (Diagram 1). The circuit of the counter can be seen below. Q3 as MSB while Q0 LSB.

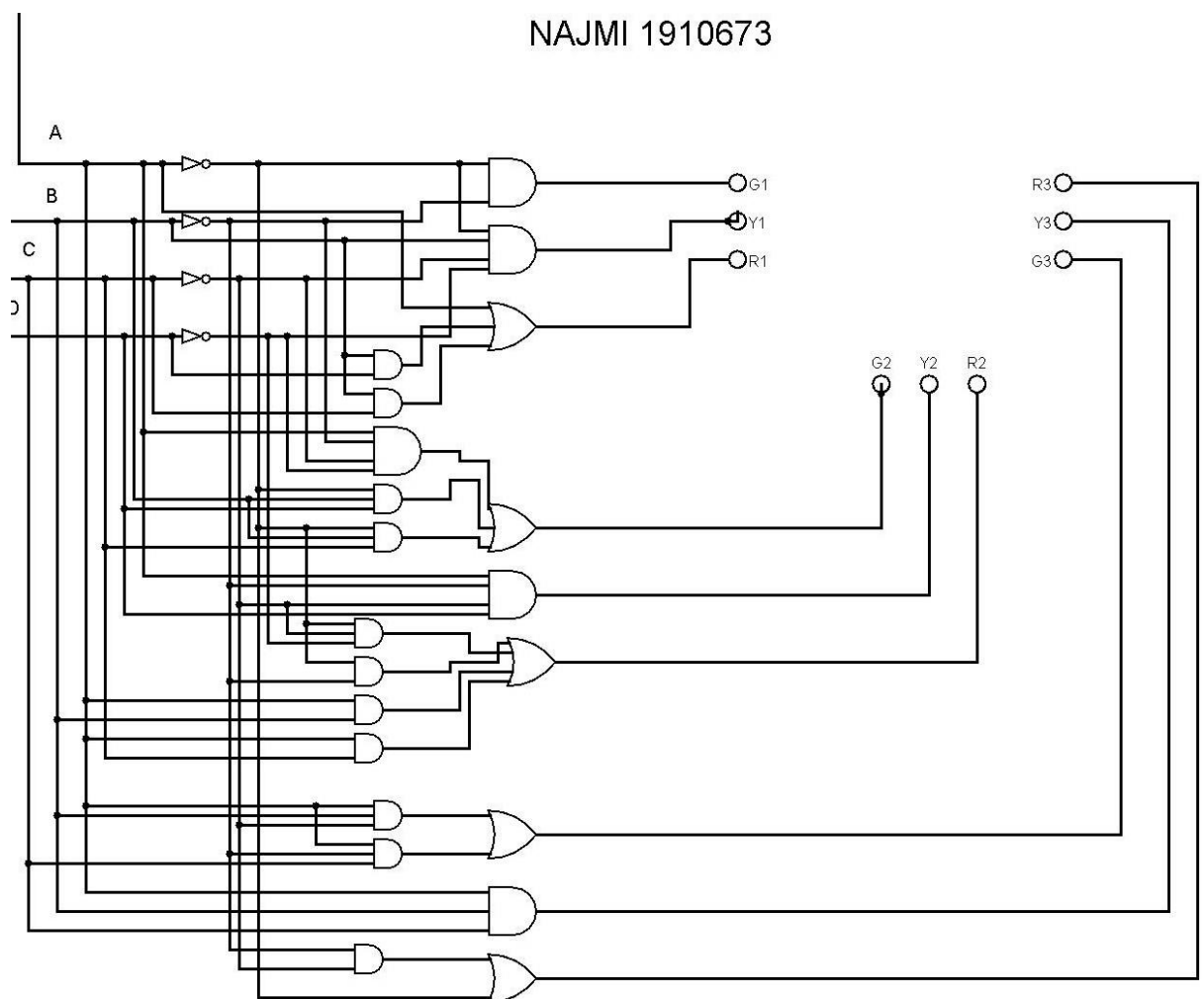


b) DECODER

The output of the counter is used as input of the decoder. The output has 4 binary digits, so the decoder should be 4 to 16 line decoder. However, we only have 15 output for the decoder makes it 4 to 15 line decoder. This is because the last output for counter (1111) not used so the number of states become 15 (in the KMAP in diagram 4, the 1111 act as don't care). The work principle of the decoder is when a unique state from counter used in the input, the output for the decoder will start to operate based on the truth table below. For example, when the input ABCD is 0000, the G1 (first green traffic light) will light on with R2(second red traffic light) and R3(third red traffic light). This indicate that the first way can go through while the other must stop and wait for their time to their green light to light up. This will keep on until 4 second end and at fifth second, the first traffic light will light up the yellow one to gave warning that it will light up the red one soon. At 6th second, the first one will turn red and second one will turn their green light(G2) to HIGH and the third one remains the same. This thing will keep going like when the first one light up the G1, the difference is this time G2 light up. After the second one turn Y2 HIGH and then R2 will turn on, the third one will operate in green light mode. This this also the same

as the cycle before but the third one will turn green until G3 turn off and Y3 turn on in 1110 states. Then its start again like when the first one G1 light up. Diagram 3 show more detail about it. We can see the decoder at the circuit below. Note that the input ABCD show how much second had passed. For examples the first second for this project is when 0000 as input.

NOTE: A=Q3, B=Q2, C=Q1, D=Q0.



DETAILED DESIGN

Counter's state diagram

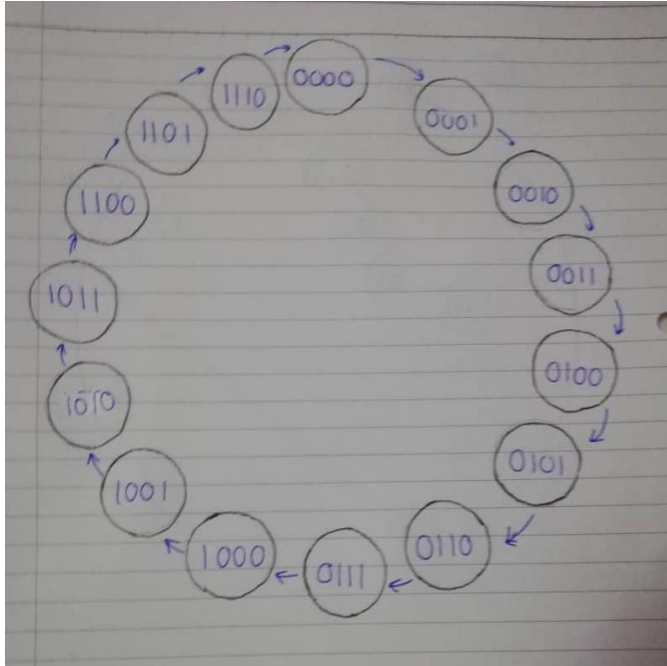


Diagram 1

Counter's timing diagram

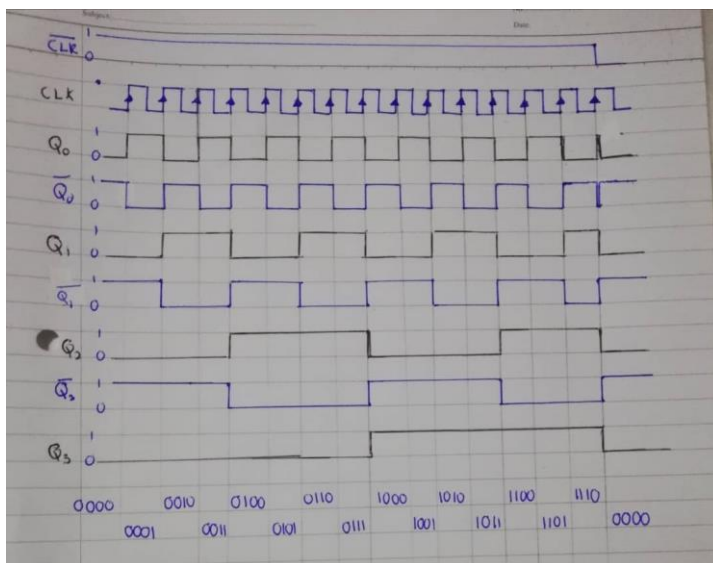


Diagram 2

DECODER'S TRUTH TABLE

Input				Output								
A	B	C	D	G1	Y1	R1	G2	Y2	R2	G3	Y3	R3
0	0	0	0	1	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	0	0	1	0	0	1
0	0	1	1	1	0	0	0	0	1	0	0	1
0	1	0	0	0	1	0	0	0	1	0	0	1
0	1	0	1	0	0	1	1	0	0	0	0	1
0	1	1	0	0	0	1	1	0	0	0	0	1
0	1	1	1	0	0	1	1	0	0	0	0	1
1	0	0	0	0	0	1	1	0	0	0	0	1
1	0	0	1	0	0	1	0	1	0	0	0	1
1	0	1	0	0	0	1	0	0	1	1	0	0
1	0	1	1	0	0	1	0	0	1	1	0	0
1	1	0	0	0	0	1	0	0	1	1	0	0
1	1	0	1	0	0	1	0	0	1	1	0	0
1	1	1	0	0	0	1	0	0	1	1	0	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	Dont care (X)								

Diagram 3

DECODER'S KMAP AND BOOLEAN FUNCTION

First traffic light

Green	Yellow	Red
$G1 = \overline{A}\overline{B}$	$Y1 = \overline{A}\overline{B}C$	$R1 = A + BD + \overline{B}C$

Second traffic light

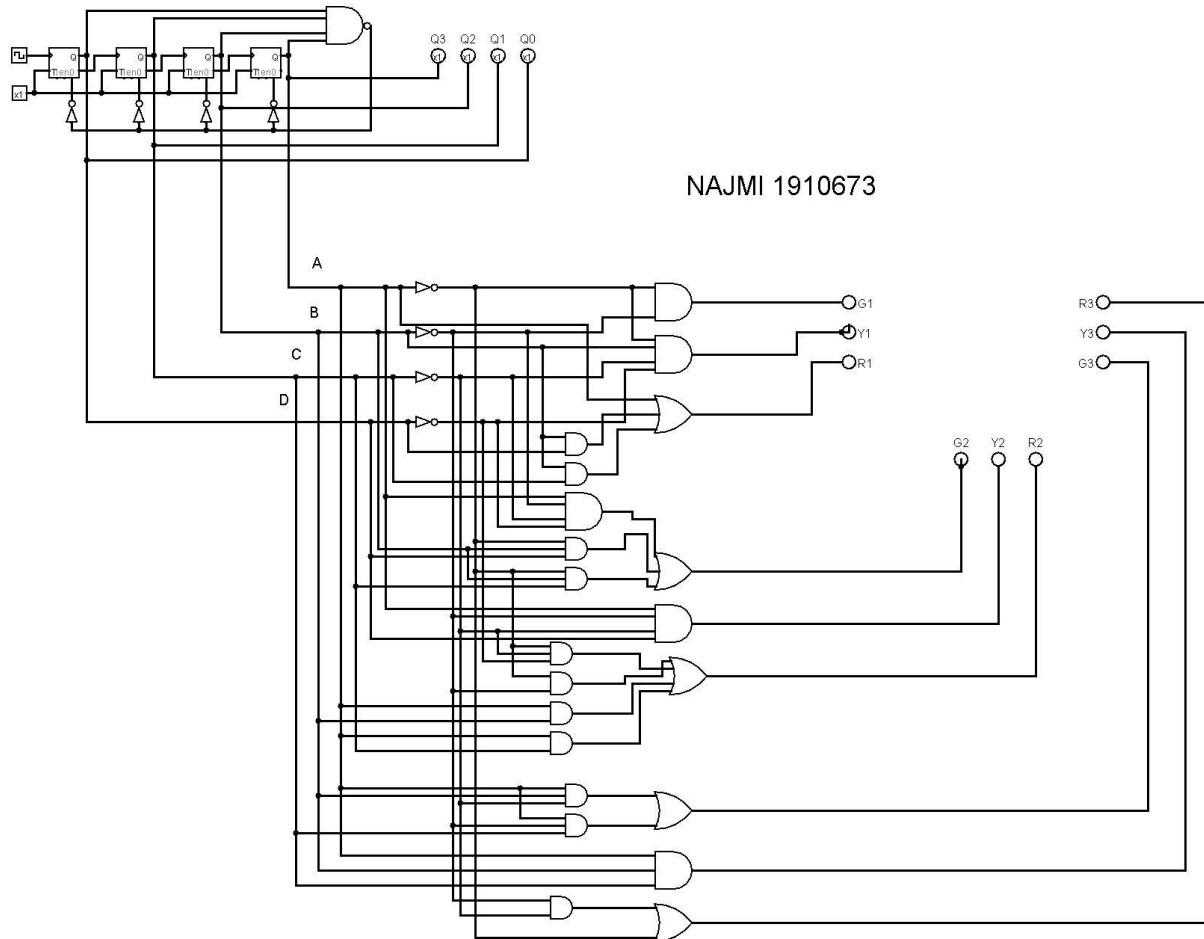
Green	Yellow	Red
$G2 = \overline{A}\overline{B}C\overline{D} + \overline{A}B\overline{D} + \overline{A}BC$	$Y2 = \overline{A}\overline{B}C\overline{D}$	$R2 = \overline{A}\overline{B} + \overline{A}C\overline{D} + AB + AC$

Third traffic light

Green	Yellow	Red
$G3 = \overline{A}\overline{B}C + \overline{A}BC$	$Y3 = \overline{A}BC$	$R3 = \overline{A} + \overline{B}C$

Diagram 4

Full circuit



CONCLUSION

In conclusion, the DLD components that being used in traffic light are basically a counter and a decoder. However, there are maybe shortage or defects compared to the real life traffic light like the period for traffic light in real life can be vary depend on situation but this traffic light project only using basic DLD and the period cycle is fixed. In real life, the component are much more than two components like in this project.

