encabu-core

Description:
The encabu-core is a single-cycle Harvard architecture processor designed for real time data analysis in sensors and robotics. It is optimized for computing trigonometric functions, square roots, and for FIR filtering of input data series, achieving up to 16 bit precision in its computations. The encabu-core's RISC instruction set is inspired from MIPS assembly. The CPU design was partially inspired by the ATtiny single cycle chips.

Features:

- Base operations for real time data analysis:
    - Finite impulse response
    - Fast CORDIC
    - Square Root

Feature Specifications:

Function	Best case (cycles)	Worst case (cycles)	Input Format	Output precision
Finite impulse response	24	48	I16Q16	16 bit
CORDIC	148	148	I1Q31	16 bit
Square root	36	60	I12Q20	12 bit

Full RISC instruction set:

- add
- sub
- mul
- div
- lw
- sw
- and
- or
- slt
- sllv
- srlv
- beq
- j
- addi