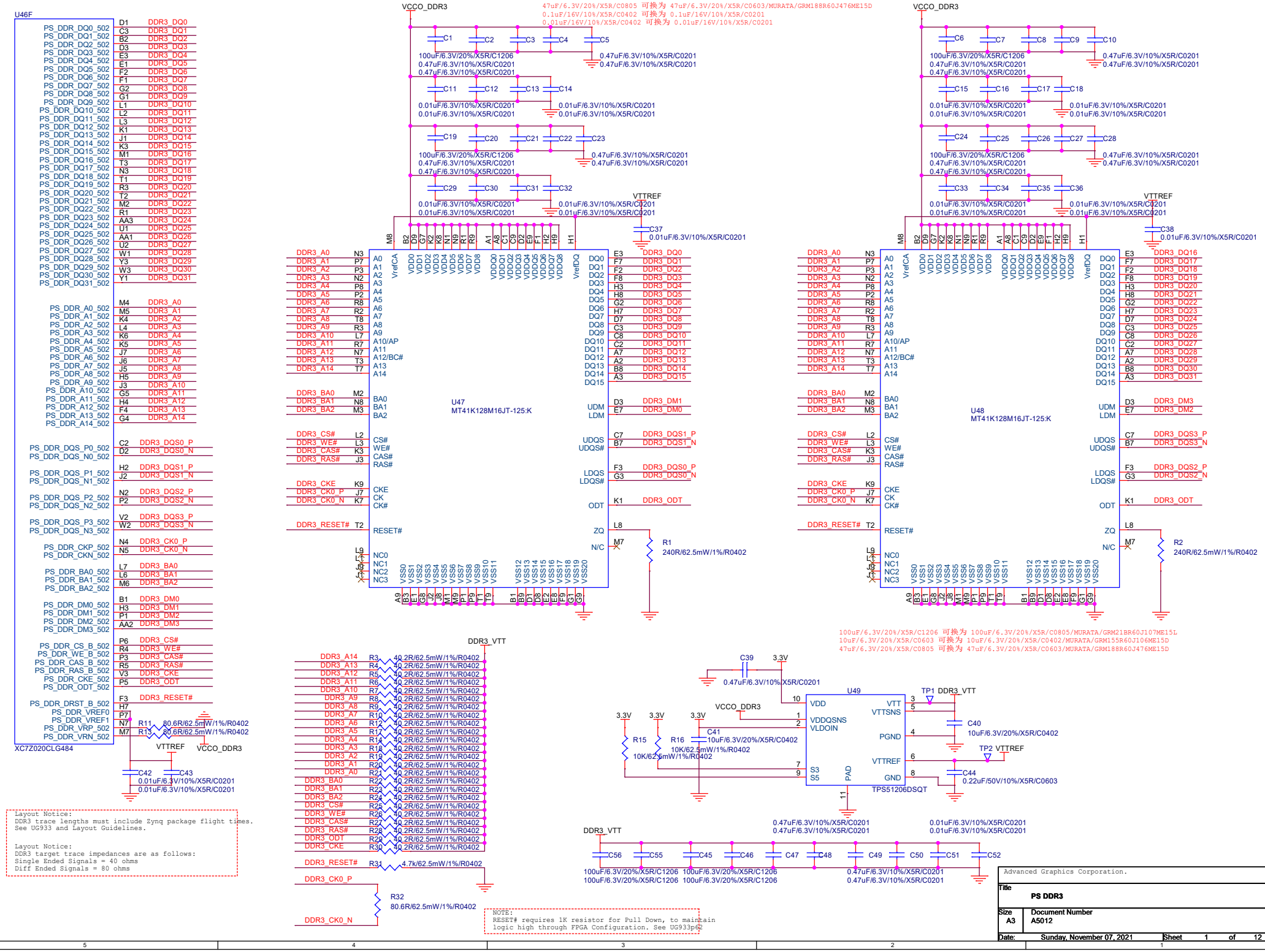
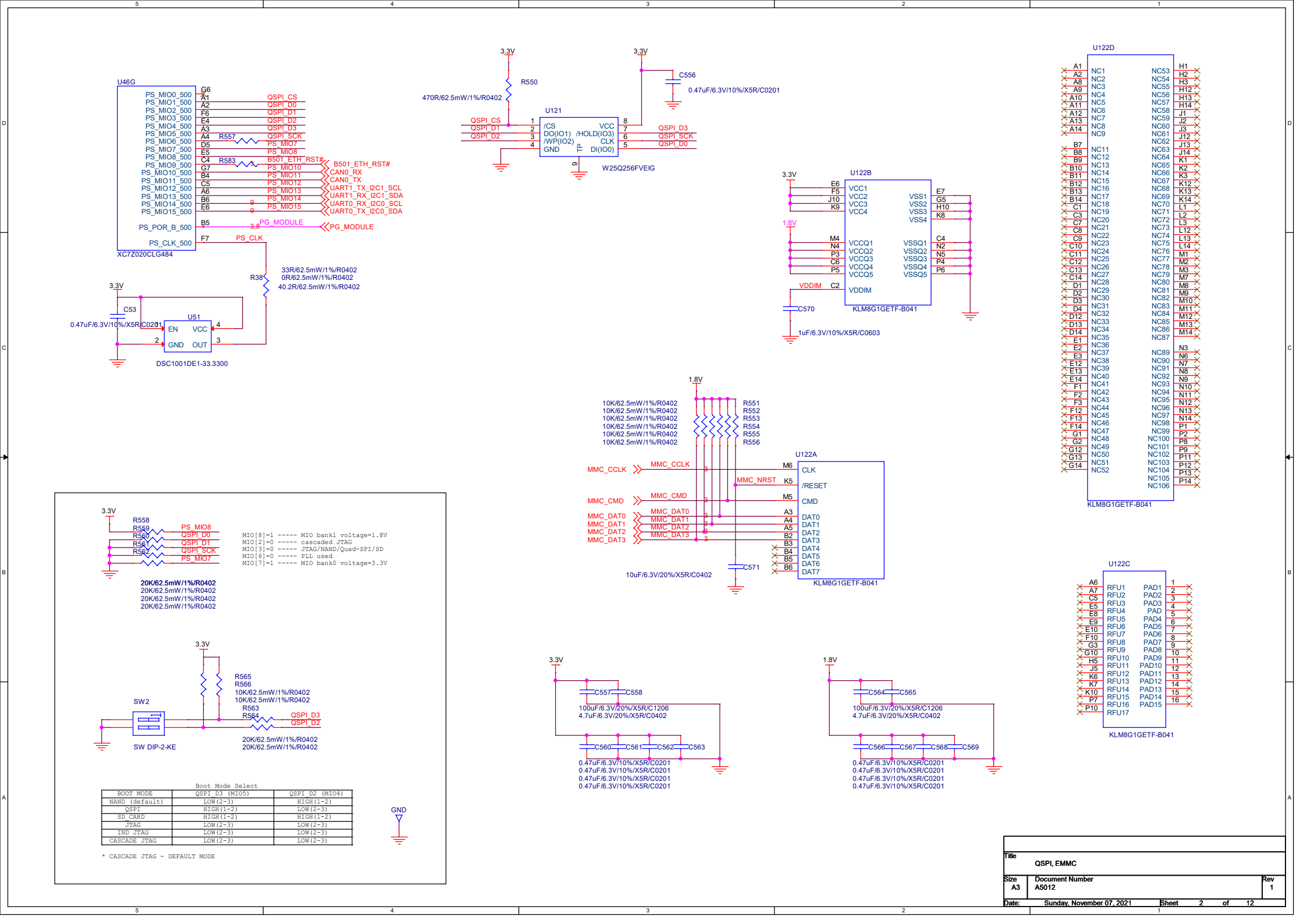
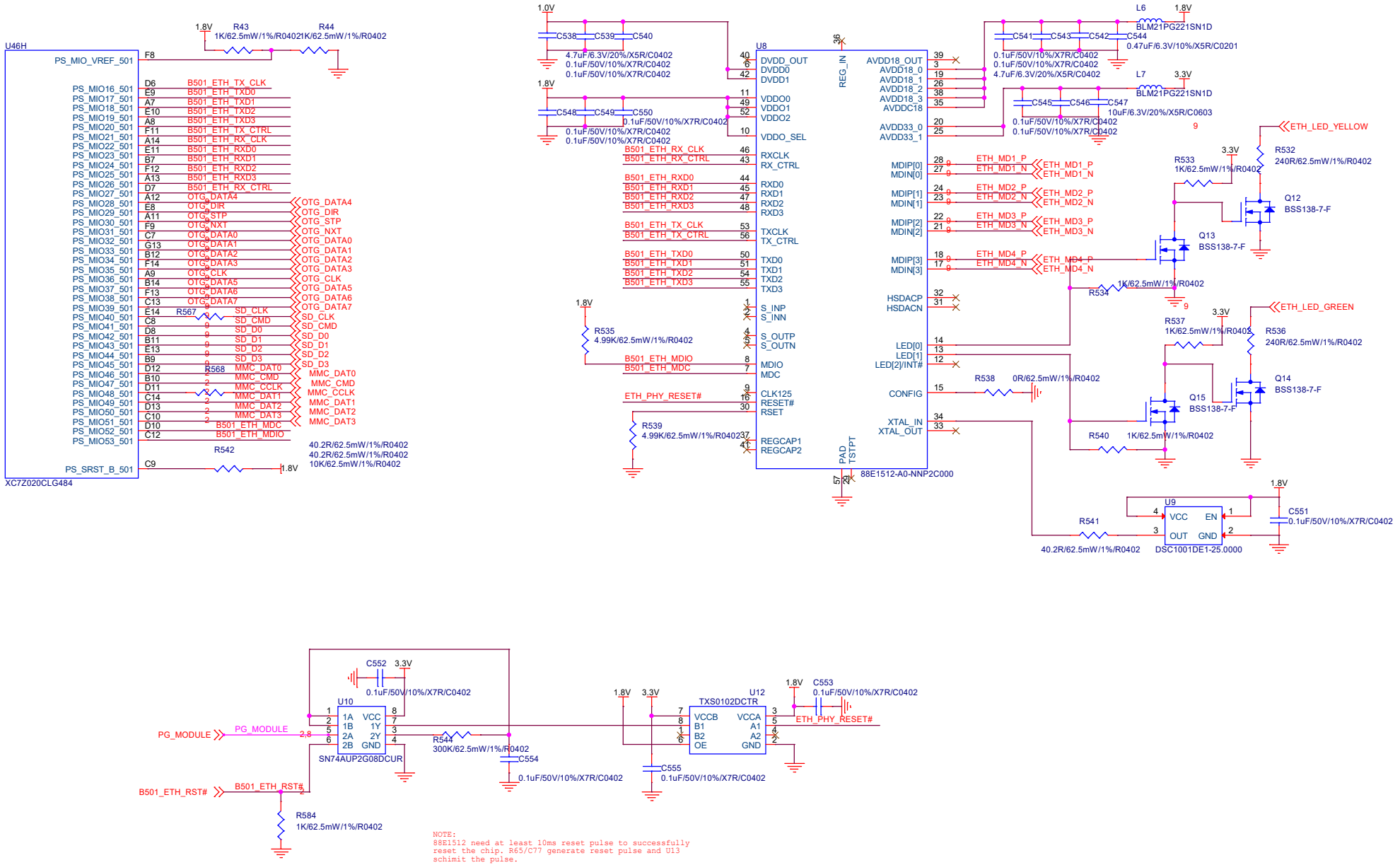
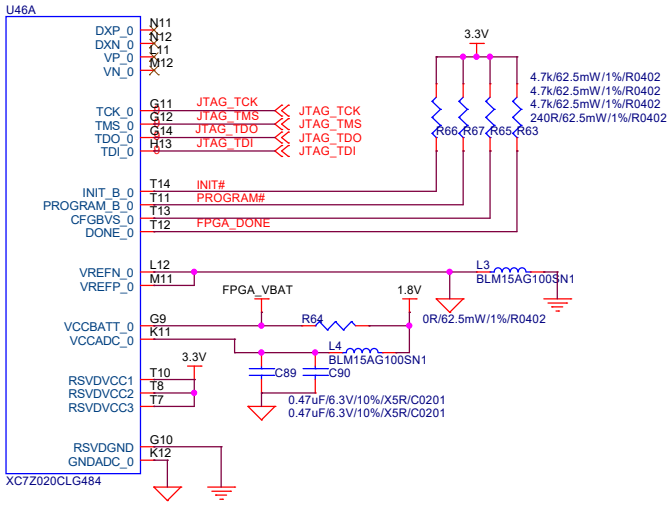
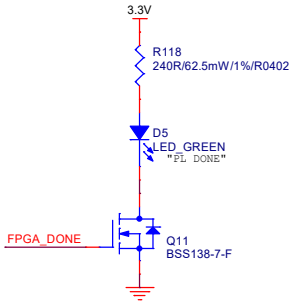

U46F
XC7Z020CLG484
PS_DDR_DQ0_502 D1 DDR3_DQ0
PS_DDR_DQ1_502 C3 DDR3_DQ1
PS_DDR_DQ2_502 B2 DDR3_DQ2
PS_DDR_DQ3_502 D3 DDR3_DQ3
PS_DDR_DQ4_502 E3 DDR3_DQ4
PS_DDR_DQ5_502 E1 DDR3_DQ5
PS_DDR_DQ6_502 F2 DDR3_DQ6
PS_DDR_DQ7_502 F1 DDR3_DQ7
PS_DDR_DQ8_502 G2 DDR3_DQ8
PS_DDR_DQ9_502 G1 DDR3_DQ9
PS_DDR_DQ10_502 L1 DDR3_DQ10
PS_DDR_DQ11_502 L2 DDR3_DQ11
PS_DDR_DQ12_502 L3 DDR3_DQ12
PS_DDR_DQ13_502 K1 DDR3_DQ13
PS_DDR_DQ14_502 J1 DDR3_DQ14
PS_DDR_DQ15_502 K3 DDR3_DQ15
PS_DDR_DQ16_502 M1 DDR3_DQ16
PS_DDR_DQ17_502 T3 DDR3_DQ17
PS_DDR_DQ18_502 N3 DDR3_DQ18
PS_DDR_DQ19_502 T1 DDR3_DQ19
PS_DDR_DQ20_502 R3 DDR3_DQ20
PS_DDR_DQ21_502 T2 DDR3_DQ21
PS_DDR_DQ22_502 M2 DDR3_DQ22
PS_DDR_DQ23_502 R1 DDR3_DQ23
PS_DDR_DQ24_502 AA3 DDR3_DQ24
PS_DDR_DQ25_502 U1 DDR3_DQ25
PS_DDR_DQ26_502 AA1 DDR3_DQ26
PS_DDR_DQ27_502 U2 DDR3_DQ27
PS_DDR_DQ28_502 W1 DDR3_DQ28
PS_DDR_DQ29_502 Y3 DDR3_DQ29
PS_DDR_DQ30_502 W3 DDR3_DQ30
PS_DDR_DQ31_502 Y1 DDR3_DQ31
PS_DDR_A0_502 M4 DDR3_A0
PS_DDR_A1_502 M5 DDR3_A1
PS_DDR_A2_502 K4 DDR3_A2
PS_DDR_A3_502 L4 DDR3_A3
PS_DDR_A4_502 K6 DDR3_A4
PS_DDR_A5_502 K5 DDR3_A5
PS_DDR_A6_502 J7 DDR3_A6
PS_DDR_A7_502 J6 DDR3_A7
PS_DDR_A8_502 H5 DDR3_A8
PS_DDR_A9_502 J5 DDR3_A9
PS_DDR_A10_502 J3 DDR3_A10
PS_DDR_A11_502 G5 DDR3_A11
PS_DDR_A12_502 H4 DDR3_A12
PS_DDR_A13_502 F4 DDR3_A13
PS_DDR_A14_502 G4 DDR3_A14
PS_DDR_DQS_P0_502 C2 DDR3_DQS0_P
PS_DDR_DQS_N0_502 D2 DDR3_DQS0_N
PS_DDR_DQS_P1_502 H2 DDR3_DQS1_P
PS_DDR_DQS_N1_502 J2 DDR3_DQS1_N
PS_DDR_DQS_P2_502 N2 DDR3_DQS2_P
PS_DDR_DQS_N2_502 P2 DDR3_DQS2_N
PS_DDR_DQS_P3_502 V2 DDR3_DQS3_P
PS_DDR_DQS_N3_502 W2 DDR3_DQS3_N
PS_DDR_CKP_502 N4 DDR3_CK0_P
PS_DDR_CKN_502 N5 DDR3_CK0_N
PS_DDR_BA0_502 L7 DDR3_BA0
PS_DDR_BA1_502 L6 DDR3_BA1
PS_DDR_BA2_502 M6 DDR3_BA2
PS_DDR_DM0_502 B1 DDR3_DM0
PS_DDR_DM1_502 H3 DDR3_DM1
PS_DDR_DM2_502 P1 DDR3_DM2
PS_DDR_DM3_502 AA2 DDR3_DM3
PS_DDR_CS_B_502 P6 DDR3_CS#
PS_DDR_WE_B_502 R4 DDR3_WE#
PS_DDR_CAS_B_502 P3 DDR3_CAS#
PS_DDR_RAS_B_502 R5 DDR3_RAS#
PS_DDR_CKE_502 V3 DDR3_CKE
PS_DDR_ODT_502 P5 DDR3_ODT
PS_DDR_DRST_B_502 F3 DDR3_RESET#
PS_DDR_VREF0 H7
PS_DDR_VREF1 P7
PS_DDR_VRP_502 N7 R11 80.6R/62.5mW/1%/R0402
PS_DDR_VRN_502 M7 R13 80.6R/62.5mW/1%/R0402
VTTREF
VCCO_DDR3
C42 0.01uF/6.3V/10%/X5R/C0201
C43 0.01uF/6.3V/10%/X5R/C0201
Layout Notice:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.
Layout Notice:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Diff Ended Signals = 80 ohms
VCCO_DDR3
47uF/6.3V/20%/X5R/C0805 可换为 47uF/6.3V/20%/X5R/C0603/MURATA/GRM188R60J476ME15D
0.1uF/16V/10%/X5R/C0402 可换为 0.1uF/16V/10%/X5R/C0201
0.01uF/16V/10%/X5R/C0402 可换为 0.01uF/16V/10%/X5R/C0201
C1 C2 C3 C4 C5
100uF/6.3V/20%/X5R/C1206
0.47uF/6.3V/10%/X5R/C0201
C11 C12 C13 C14
0.01uF/6.3V/10%/X5R/C0201
C19 C20 C21 C22 C23
C29 C30 C31 C32
VTTREF
C37 0.01uF/6.3V/10%/X5R/C0201
U47
MT41K128M16JT-125:K
DDR3_A0 N3
DDR3_A1 P7
DDR3_A2 P3
DDR3_A3 N2
DDR3_A4 P8
DDR3_A5 P2
DDR3_A6 R8
DDR3_A7 R2
DDR3_A8 T8
DDR3_A9 R3
DDR3_A10 L7
DDR3_A11 R7
DDR3_A12 N7
DDR3_A13 T3
DDR3_A14 T7
DDR3_BA0 M2
DDR3_BA1 N8
DDR3_BA2 M3
DDR3_CS# L2
DDR3_WE# L3
DDR3_CAS# K3
DDR3_RAS# J3
DDR3_CKE K9
DDR3_CK0_P J7
DDR3_CK0_N K7
DDR3_RESET# T2
DDR3_DQ0 E3
DDR3_DQ1 F7
DDR3_DQ2 F2
DDR3_DQ3 F8
DDR3_DQ4 H3
DDR3_DQ5 H8
DDR3_DQ6 G2
DDR3_DQ7 H7
DDR3_DQ8 D7
DDR3_DQ9 C3
DDR3_DQ10 C8
DDR3_DQ11 C2
DDR3_DQ12 A7
DDR3_DQ13 A2
DDR3_DQ14 B8
DDR3_DQ15 A3
DDR3_DM1 D3
DDR3_DM0 E7
DDR3_DQS1_P C7
DDR3_DQS1_N B7
DDR3_DQS0_P F3
DDR3_DQS0_N G3
DDR3_ODT K1
R1 240R/62.5mW/1%/R0402
U48
MT41K128M16JT-125:K
DDR3_DQ16 E3
DDR3_DQ17 F7
DDR3_DQ18 F2
DDR3_DQ19 F8
DDR3_DQ20 H3
DDR3_DQ21 H8
DDR3_DQ22 G2
DDR3_DQ23 H7
DDR3_DQ24 D7
DDR3_DQ25 C3
DDR3_DQ26 C8
DDR3_DQ27 C2
DDR3_DQ28 A7
DDR3_DQ29 A2
DDR3_DQ30 B8
DDR3_DQ31 A3
DDR3_DM3 D3
DDR3_DM2 E7
DDR3_DQS3_P C7
DDR3_DQS3_N B7
DDR3_DQS2_P F3
DDR3_DQS2_N G3
DDR3_ODT K1
R2 240R/62.5mW/1%/R0402
100uF/6.3V/20%/X5R/C1206 可换为 100uF/6.3V/20%/X5R/C0805/MURATA/GRM21BR60J107ME15L
10uF/6.3V/20%/X5R/C0603 可换为 10uF/6.3V/20%/X5R/C0402/MURATA/GRM155R60J106ME15D
47uF/6.3V/20%/X5R/C0805 可换为 47uF/6.3V/20%/X5R/C0603/MURATA/GRM188R60J476ME15D
DDR3_VTT
DDR3_A14 R3 40.2R/62.5mW/1%/R0402
DDR3_A13 R4 40.2R/62.5mW/1%/R0402
DDR3_A12 R5 40.2R/62.5mW/1%/R0402
DDR3_A11 R6 40.2R/62.5mW/1%/R0402
DDR3_A10 R7 40.2R/62.5mW/1%/R0402
DDR3_A9 R8 40.2R/62.5mW/1%/R0402
DDR3_A8 R9 40.2R/62.5mW/1%/R0402
DDR3_A7 R10 40.2R/62.5mW/1%/R0402
DDR3_A6 R12 40.2R/62.5mW/1%/R0402
DDR3_A5 R17 40.2R/62.5mW/1%/R0402
DDR3_A4 R14 40.2R/62.5mW/1%/R0402
DDR3_A3 R16 40.2R/62.5mW/1%/R0402
DDR3_A2 R15 40.2R/62.5mW/1%/R0402
DDR3_A1 R20 40.2R/62.5mW/1%/R0402
DDR3_A0 R21 40.2R/62.5mW/1%/R0402
DDR3_BA0 R22 40.2R/62.5mW/1%/R0402
DDR3_BA1 R23 40.2R/62.5mW/1%/R0402
DDR3_BA2 R24 40.2R/62.5mW/1%/R0402
DDR3_CS# R25 40.2R/62.5mW/1%/R0402
DDR3_WE# R26 40.2R/62.5mW/1%/R0402
DDR3_CAS# R27 40.2R/62.5mW/1%/R0402
DDR3_RAS# R28 40.2R/62.5mW/1%/R0402
DDR3_ODT R29 40.2R/62.5mW/1%/R0402
DDR3_CKE R30 40.2R/62.5mW/1%/R0402
DDR3_RESET# R31 4.7k/62.5mW/1%/R0402
DDR3_CK0_P
R32 80.6R/62.5mW/1%/R0402
DDR3_CK0_N
NOTE:
RESET# requires 1K resistor for Pull Down, to maintain
logic high through FPGA Configuration. See UG933p62
C39 3.3V
0.47uF/6.3V/10%/X5R/C0201
U49
TPS51206DSQT
VDD
VDDQSNS
VLDOIN
S3
S5
PAD
VTT
VTTSNS
PGND
VTTREF
GND
TP1 DDR3_VTT
TP2 VTTREF
C40 10uF/6.3V/20%/X5R/C0402
C41 10uF/6.3V/20%/X5R/C0402
C44 0.22uF/50V/10%/X5R/C0603
R15 10K/62.5mW/1%/R0402
R16 10K/62.5mW/1%/R0402
3.3V
VCCO_DDR3
DDR3_VTT
C56 C55 C45 C46 C47 C48 C49 C50 C51 C52
100uF/6.3V/20%/X5R/C1206
0.47uF/6.3V/10%/X5R/C0201
0.01uF/6.3V/10%/X5R/C0201
Advanced Graphics Corporation.
Title
PS DDR3
Size A3
Document Number A5012
Rev 1
Date: Sunday, November 07, 2021
Sheet 1 of 12


U46G
XC7Z020CLG484
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
PS_POR_B_500
PS_CLK_500
QSPI_CS
QSPI_D0
QSPI_D1
QSPI_D2
QSPI_D3
QSPI_SCK
PS_MIO7
PS_MIO8
B501_ETH_RST#
CAN0_RX
CAN0_TX
UART1_TX_I2C1_SCL
UART1_RX_I2C1_SDA
UART0_RX_I2C0_SCL
UART0_TX_I2C0_SDA
PG_MODULE
PS_CLK
R557
R583
R38
33R/62.5mW/1%/R0402
0R/62.5mW/1%/R0402
40.2R/62.5mW/1%/R0402
3.3V
C53
0.47uF/6.3V/10%/X5R/C0201
U51
EN
VCC
GND
OUT
DSC1001DE1-33.3300
R550
470R/62.5mW/1%/R0402
U121
/CS
DO(IO1)
/WP(IO2)
GND
VCC
/HOLD(IO3)
CLK
DI(IO0)
W25Q256FVEIG
C556
0.47uF/6.3V/10%/X5R/C0201
U122B
VCC1
VCC2
VCC3
VCC4
VCCQ1
VCCQ2
VCCQ3
VCCQ4
VCCQ5
VDDIM
VSS1
VSS2
VSS3
VSS4
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
1.8V
C570
1uF/6.3V/10%/X5R/C0603
KLM8G1GETF-B041
U122D
KLM8G1GETF-B041
U122A
MMC_CCLK
MMC_NRST
MMC_CMD
MMC_DAT0
MMC_DAT1
MMC_DAT2
MMC_DAT3
CLK
/RESET
CMD
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
R551
R552
R553
R554
R555
R556
10K/62.5mW/1%/R0402
C571
10uF/6.3V/20%/X5R/C0402
KLM8G1GETF-B041
U122C
KLM8G1GETF-B041
R558
R559
R560
R561
R562
20K/62.5mW/1%/R0402
MIO[8]=1 ----- MIO bank1 voltage=1.8V
MIO[2]=0 ----- cascaded JTAG
MIO[3]=0 ----- JTAG/NAND/Quad-SPI/SD
MIO[6]=0 ----- PLL used
MIO[7]=1 ----- MIO bank0 voltage=3.3V
SW2
SW DIP-2-KE
R565
R566
R563
R564
10K/62.5mW/1%/R0402
C557
C558
C560
C561
C562
C563
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
0.47uF/6.3V/10%/X5R/C0201
C564
C565
C566
C567
C568
C569
Boot Mode Select
BOOT MODE
QSPI_D3 (MIO5)
QSPI_D2 (MIO4)
NAND (default)
QSPI
SD_CARD
JTAG
IND_JTAG
CASCADE_JTAG
LOW(2-3)
HIGH(1-2)
* CASCADE JTAG - DEFAULT MODE
GND
Title
QSPI, EMMC
Size
A3
Document Number
A5012
Rev
1
Date:
Sunday, November 07, 2021
Sheet
2
of
12



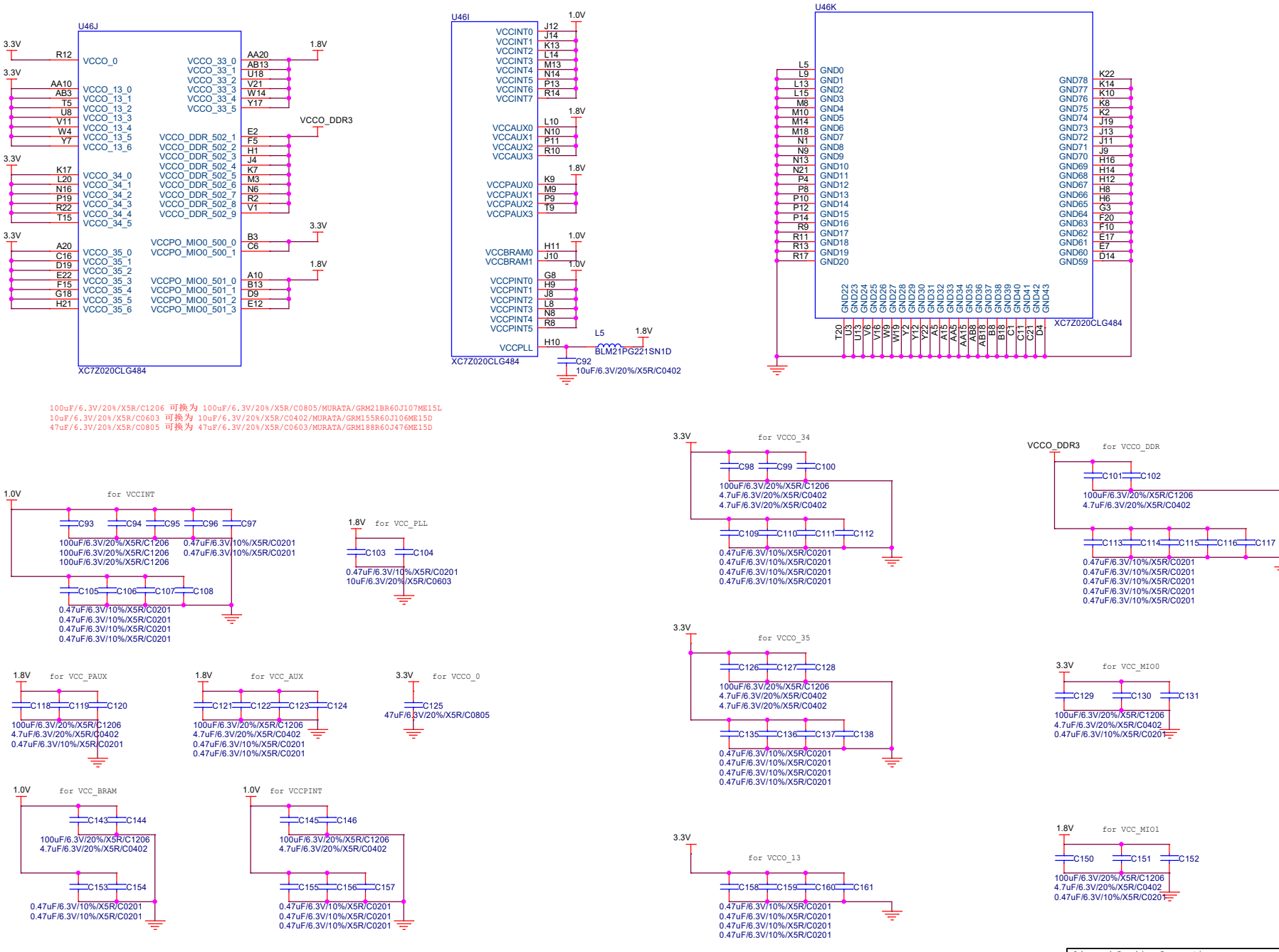
Title	ETH, UART	
Size A3	Document Number A5012	Rev 1
Date: Sunday, November 07, 2021	Sheet 3 of 15	





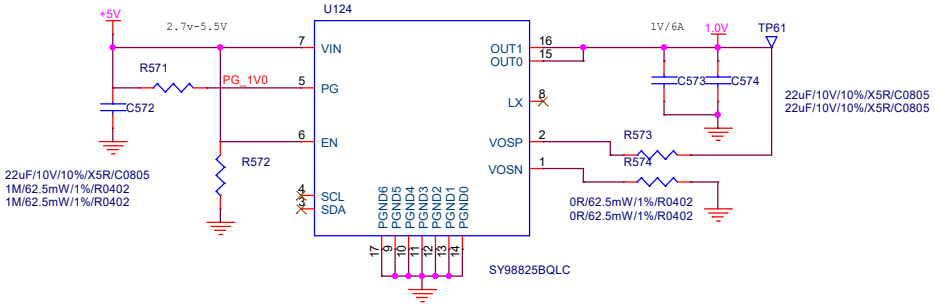
Advanced Graphics Corporation.

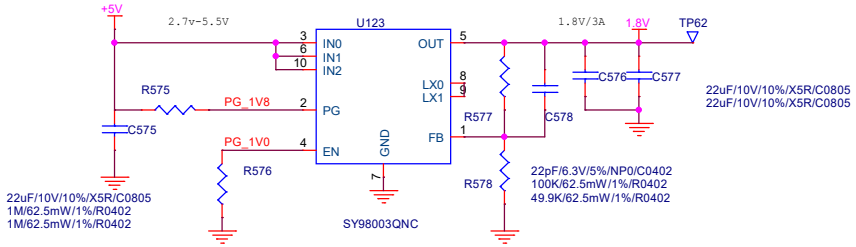
Title	RTC, JTAG	
Size A3	Document Number A5012	Rev 1
Date: Sunday, November 07, 2021	Sheet 4 of 12	

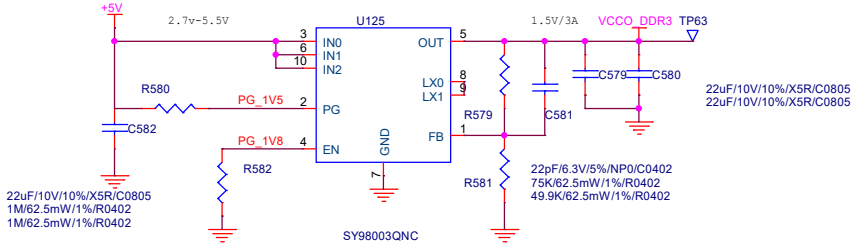

U46J
3.3V
R12
VCCO_0
3.3V
AA10
AB3
T5
U8
V11
W4
Y7
VCCO_13_0
VCCO_13_1
VCCO_13_2
VCCO_13_3
VCCO_13_4
VCCO_13_5
VCCO_13_6
3.3V
K17
L20
N16
P19
R22
T15
VCCO_34_0
VCCO_34_1
VCCO_34_2
VCCO_34_3
VCCO_34_4
VCCO_34_5
3.3V
A20
C16
D19
E22
F15
G18
H21
VCCO_35_0
VCCO_35_1
VCCO_35_2
VCCO_35_3
VCCO_35_4
VCCO_35_5
VCCO_35_6
VCCO_33_0
VCCO_33_1
VCCO_33_2
VCCO_33_3
VCCO_33_4
VCCO_33_5
1.8V
AA20
AB13
U18
V21
W14
Y17
VCCO_DDR3
VCCO_DDR_502_1
VCCO_DDR_502_2
VCCO_DDR_502_3
VCCO_DDR_502_4
VCCO_DDR_502_5
VCCO_DDR_502_6
VCCO_DDR_502_7
VCCO_DDR_502_8
VCCO_DDR_502_9
E2
F5
H1
J4
K7
M3
N6
R2
V1
3.3V
VCCPO_MIO0_500_0
VCCPO_MIO0_500_1
B3
C6
1.8V
VCCPO_MIO0_501_0
VCCPO_MIO0_501_1
VCCPO_MIO0_501_2
VCCPO_MIO0_501_3
A10
B13
D9
E12
XC7Z020CLG484
U46I
1.0V
VCCINT0
VCCINT1
VCCINT2
VCCINT3
VCCINT4
VCCINT5
VCCINT6
VCCINT7
J12
J14
K13
L14
M13
N14
P13
R14
1.8V
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
L10
N10
P11
R10
1.8V
VCCPAUX0
VCCPAUX1
VCCPAUX2
VCCPAUX3
K9
M9
P9
T9
1.0V
VCCBRAM0
VCCBRAM1
H11
J10
1.0V
VCCPINT0
VCCPINT1
VCCPINT2
VCCPINT3
VCCPINT4
VCCPINT5
G8
H9
J8
L8
N8
R8
VCCPLL
H10
L5
1.8V
BLM21PG221SN1D
C92
10uF/6.3V/20%/X5R/C0402
XC7Z020CLG484
U46K
L5
L9
L13
L15
M8
M10
M14
M18
N1
N9
N13
N21
P4
P8
P10
P12
P14
R9
R11
R13
R17
GND0
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
GND18
GND19
GND20
GND78
GND77
GND76
GND75
GND74
GND73
GND72
GND71
GND70
GND69
GND68
GND67
GND66
GND65
GND64
GND63
GND62
GND61
GND60
GND59
K22
K14
K10
K8
K2
J19
J13
J11
J9
H16
H14
H12
H8
H6
G3
F20
F10
E17
E7
D14
GND22
GND23
GND24
GND25
GND26
GND27
GND28
GND29
GND30
GND31
GND32
GND33
GND34
GND35
GND36
GND37
GND38
GND39
GND40
GND41
GND42
GND43
T20
U3
U13
V6
V16
W9
W19
Y12
Y22
A5
A15
AA5
AA15
AB8
AB18
B8
B18
C1
C11
C21
D4
XC7Z020CLG484
100uF/6.3V/20%/X5R/C1206 可换为 100uF/6.3V/20%/X5R/C0805/MURATA/GRM21BR60J107ME15L
10uF/6.3V/20%/X5R/C0603 可换为 10uF/6.3V/20%/X5R/C0402/MURATA/GRM155R60J106ME15D
47uF/6.3V/20%/X5R/C0805 可换为 47uF/6.3V/20%/X5R/C0603/MURATA/GRM188R60J476ME15D
1.0V
for VCCINT
C93
C94
C95
C96
C97
100uF/6.3V/20%/X5R/C1206
100uF/6.3V/20%/X5R/C1206
100uF/6.3V/20%/X5R/C1206
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
C105
C106
C107
C108
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
1.8V
for VCC_PLL
C103
C104
0.47uF/6.3V/10%/X5R/C0201
10uF/6.3V/20%/X5R/C0603
3.3V
for VCCO_34
C98
C99
C100
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
4.7uF/6.3V/20%/X5R/C0402
C109
C110
C111
C112
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
VCCO_DDR3
for VCCO_DDR
C101
C102
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
C113
C114
C115
C116
C117
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
1.8V
for VCC_PAUX
C118
C119
C120
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
0.47uF/6.3V/10%/X5R/C0201
1.8V
for VCC_AUX
C121
C122
C123
C124
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
3.3V
for VCCO_0
C125
47uF/6.3V/20%/X5R/C0805
3.3V
for VCCO_35
C126
C127
C128
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
4.7uF/6.3V/20%/X5R/C0402
C135
C136
C137
C138
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
3.3V
for VCC_MIO0
C129
C130
C131
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
0.47uF/6.3V/10%/X5R/C0201
1.0V
for VCC_BRAM
C143
C144
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
C153
C154
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
1.0V
for VCCPINT
C145
C146
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
C155
C156
C157
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
3.3V
for VCCO_13
C158
C159
C160
C161
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
0.47uF/6.3V/10%/X5R/C0201
1.8V
for VCC_MIO1
C150
C151
C152
100uF/6.3V/20%/X5R/C1206
4.7uF/6.3V/20%/X5R/C0402
0.47uF/6.3V/10%/X5R/C0201
Advanced Graphics Corporation.
Title
CPU VCC
Size
A3
Document Number
A5012
Rev
1
Date:
Sunday, November 07, 2021
Sheet
5
of
12

PL IO: 1

POWER UP SEQUENCE: 5V -> 1.0V -> 1.8V -> 1.5V (DDR) -> 3.3V -> PG_MODULE

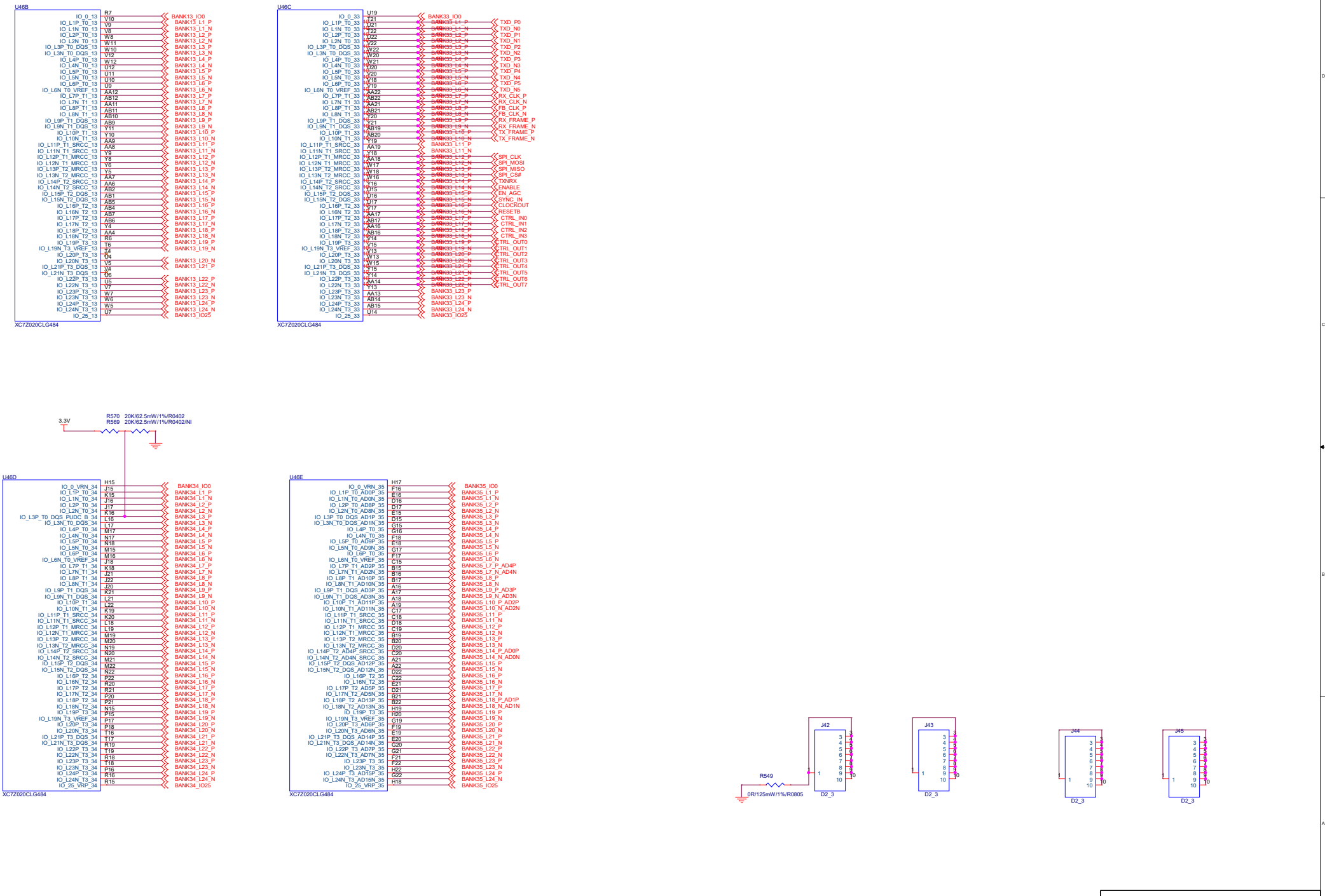


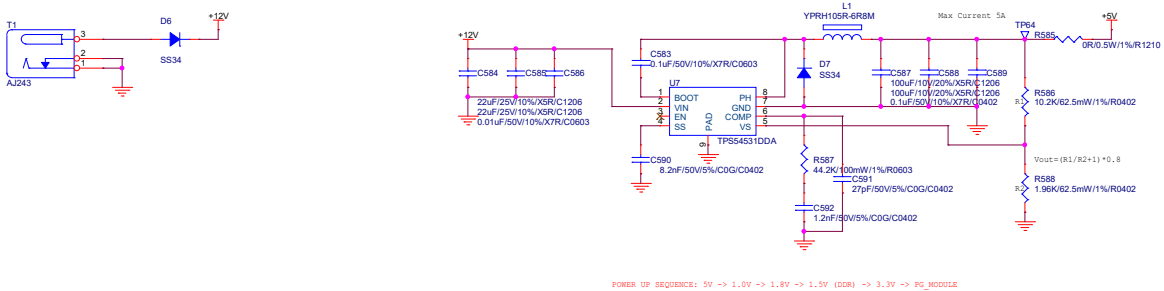




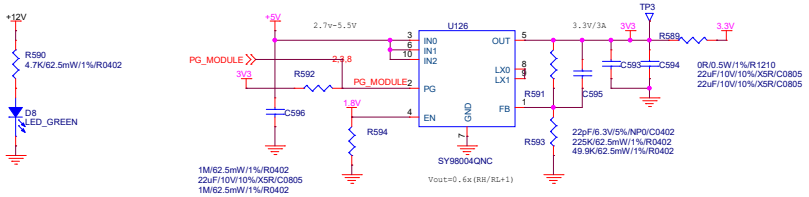
Vout=0.6x(RH/RL+1)

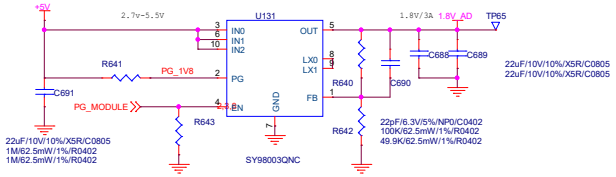
Advanced Graphics Corporation.			
Title: CPU_PWR			
Size: A3	Document Number: CB		Rev: 1
Date: Sunday, November 07, 2021	Sheet 6 of 12		


U46B
IO_0_13 R7
IO_L1P_T0_13 V10 BANK13_L1_P
IO_L1N_T0_13 V9 BANK13_L1_N
IO_L2P_T0_13 V8 BANK13_L2_P
IO_L2N_T0_13 W8 BANK13_L2_N
IO_L3P_T0_DQS_13 W11 BANK13_L3_P
IO_L3N_T0_DQS_13 W10 BANK13_L3_N
IO_L4P_T0_13 V12 BANK13_L4_P
IO_L4N_T0_13 W12 BANK13_L4_N
IO_L5P_T0_13 U12 BANK13_L5_P
IO_L5N_T0_13 U11 BANK13_L5_N
IO_L6P_T0_13 U10 BANK13_L6_P
IO_L6N_T0_VREF_13 U9 BANK13_L6_N
IO_L7P_T1_13 AA12 BANK13_L7_P
IO_L7N_T1_13 AB12 BANK13_L7_N
IO_L8P_T1_13 AA11 BANK13_L8_P
IO_L8N_T1_13 AB11 BANK13_L8_N
IO_L9P_T1_DQS_13 AB10 BANK13_L9_P
IO_L9N_T1_DQS_13 AB9 BANK13_L9_N
IO_L10P_T1_13 Y11 BANK13_L10_P
IO_L10N_T1_13 Y10 BANK13_L10_N
IO_L11P_T1_SRCC_13 AA9 BANK13_L11_P
IO_L11N_T1_SRCC_13 AA8 BANK13_L11_N
IO_L12P_T1_MRCC_13 Y9 BANK13_L12_P
IO_L12N_T1_MRCC_13 Y8 BANK13_L12_N
IO_L13P_T2_MRCC_13 Y6 BANK13_L13_P
IO_L13N_T2_MRCC_13 Y5 BANK13_L13_N
IO_L14P_T2_SRCC_13 AA7 BANK13_L14_P
IO_L14N_T2_SRCC_13 AA6 BANK13_L14_N
IO_L15P_T2_DQS_13 AB2 BANK13_L15_P
IO_L15N_T2_DQS_13 AB1 BANK13_L15_N
IO_L16P_T2_13 AB5 BANK13_L16_P
IO_L16N_T2_13 AB4 BANK13_L16_N
IO_L17P_T2_13 AB7 BANK13_L17_P
IO_L17N_T2_13 AB6 BANK13_L17_N
IO_L18P_T2_13 Y4 BANK13_L18_P
IO_L18N_T2_13 AA4 BANK13_L18_N
IO_L19P_T3_13 R6 BANK13_L19_P
IO_L19N_T3_VREF_13 T6 BANK13_L19_N
IO_L20P_T3_13 J4
IO_L20N_T3_13 O4 BANK13_L20_N
IO_L21P_T3_DQS_13 V5 BANK13_L21_P
IO_L21N_T3_DQS_13 V4
IO_L22P_T3_13 O6 BANK13_L22_P
IO_L22N_T3_13 U5 BANK13_L22_N
IO_L23P_T3_13 V7 BANK13_L23_P
IO_L23N_T3_13 W7 BANK13_L23_N
IO_L24P_T3_13 W6 BANK13_L24_P
IO_L24N_T3_13 W5 BANK13_L24_N
IO_25_13 U7 BANK13_IO25
XC7Z020CLG484
U46C
IO_0_33 U19
IO_L1P_T0_33 T21 BANK33_L1_P TXD_P0
IO_L1N_T0_33 U21 BANK33_L1_N TXD_N0
IO_L2P_T0_33 T22 BANK33_L2_P TXD_P1
IO_L2N_T0_33 U22 BANK33_L2_N TXD_N1
IO_L3P_T0_DQS_33 V22 BANK33_L3_P TXD_P2
IO_L3N_T0_DQS_33 W22 BANK33_L3_N TXD_N2
IO_L4P_T0_33 W21 BANK33_L4_P TXD_P3
IO_L4N_T0_33 Y21 BANK33_L4_N TXD_N3
IO_L5P_T0_33 V20 BANK33_L5_P TXD_P4
IO_L5N_T0_33 W20 BANK33_L5_N TXD_N4
IO_L6P_T0_33 Y19 BANK33_L6_P TXD_P5
IO_L6N_T0_VREF_33 Y20 BANK33_L6_N TXD_N5
IO_L7P_T1_33 AA22 BANK33_L7_P RX_CLK_P
IO_L7N_T1_33 AB22 BANK33_L7_N RX_CLK_N
IO_L8P_T1_33 AA21 BANK33_L8_P FB_CLK_P
IO_L8N_T1_33 AB21 BANK33_L8_N FB_CLK_N
IO_L9P_T1_DQS_33 V20 BANK33_L9_P RX_FRAME_P
IO_L9N_T1_DQS_33 V21 BANK33_L9_N RX_FRAME_N
IO_L10P_T1_33 AB19 BANK33_L10_P TX_FRAME_P
IO_L10N_T1_33 AB20 BANK33_L10_N TX_FRAME_N
IO_L11P_T1_SRCC_33 Y19 BANK33_L11_P
IO_L11N_T1_SRCC_33 AA19 BANK33_L11_N
IO_L12P_T1_MRCC_33 Y18 BANK33_L12_P SPI_CLK
IO_L12N_T1_MRCC_33 AA18 BANK33_L12_N SPI_MOSI
IO_L13P_T2_MRCC_33 W17 BANK33_L13_P SPI_MISO
IO_L13N_T2_MRCC_33 W18 BANK33_L13_N SPI_CS#
IO_L14P_T2_SRCC_33 W16 BANK33_L14_P TXNRX
IO_L14N_T2_SRCC_33 Y16 BANK33_L14_N ENABLE
IO_L15P_T2_DQS_33 U15 BANK33_L15_P EN_AGC
IO_L15N_T2_DQS_33 U16 BANK33_L15_N SYNC_IN
IO_L16P_T2_33 U17 BANK33_L16_P CLOCKOUT
IO_L16N_T2_33 V17 BANK33_L16_N RESETB
IO_L17P_T2_33 AA17 BANK33_L17_P CTRL_IN0
IO_L17N_T2_33 AB17 BANK33_L17_N CTRL_IN1
IO_L18P_T2_33 AA16 BANK33_L18_P CTRL_IN2
IO_L18N_T2_33 AB16 BANK33_L18_N CTRL_IN3
IO_L19P_T3_33 Y14 BANK33_L19_P CTRL_OUT0
IO_L19N_T3_VREF_33 Y15 BANK33_L19_N CTRL_OUT1
IO_L20P_T3_33 V13 BANK33_L20_P CTRL_OUT2
IO_L20N_T3_33 W13 BANK33_L20_N CTRL_OUT3
IO_L21P_T3_DQS_33 W15 BANK33_L21_P CTRL_OUT4
IO_L21N_T3_DQS_33 Y13 BANK33_L21_N CTRL_OUT5
IO_L22P_T3_33 Y14 BANK33_L22_P CTRL_OUT6
IO_L22N_T3_33 AA14 BANK33_L22_N CTRL_OUT7
IO_L23P_T3_33 Y13
IO_L23N_T3_33 AA13 BANK33_L23_P
IO_L24P_T3_33 AB14 BANK33_L23_N
IO_L24N_T3_33 AB15 BANK33_L24_P
IO_25_33 U14 BANK33_L24_N
BANK33_IO25
XC7Z020CLG484
3.3V
R570 20K/62.5mW/1%/R0402
R569 20K/62.5mW/1%/R0402/NI
U46D
IO_0_VRN_34 H15
IO_L1P_T0_34 J15 BANK34_L1_P
IO_L1N_T0_34 K15 BANK34_L1_N
IO_L2P_T0_34 J16 BANK34_L2_P
IO_L2N_T0_34 J17 BANK34_L2_N
IO_L3P_T0_DQS_PUDC_B_34 K16 BANK34_L3_P
IO_L3N_T0_DQS_34 L16 BANK34_L3_N
IO_L4P_T0_34 L17 BANK34_L4_P
IO_L4N_T0_34 M17 BANK34_L4_N
IO_L5P_T0_34 N17 BANK34_L5_P
IO_L5N_T0_34 N18 BANK34_L5_N
IO_L6P_T0_34 M15 BANK34_L6_P
IO_L6N_T0_VREF_34 M16 BANK34_L6_N
IO_L7P_T1_34 J18 BANK34_L7_P
IO_L7N_T1_34 K18 BANK34_L7_N
IO_L8P_T1_34 J21 BANK34_L8_P
IO_L8N_T1_34 J22 BANK34_L8_N
IO_L9P_T1_DQS_34 J20 BANK34_L9_P
IO_L9N_T1_DQS_34 K21 BANK34_L9_N
IO_L10P_T1_34 L21 BANK34_L10_P
IO_L10N_T1_34 L22 BANK34_L10_N
IO_L11P_T1_SRCC_34 K19 BANK34_L11_P
IO_L11N_T1_SRCC_34 K20 BANK34_L11_N
IO_L12P_T1_MRCC_34 L18 BANK34_L12_P
IO_L12N_T1_MRCC_34 L19 BANK34_L12_N
IO_L13P_T2_MRCC_34 M19 BANK34_L13_P
IO_L13N_T2_MRCC_34 M20 BANK34_L13_N
IO_L14P_T2_SRCC_34 N19 BANK34_L14_P
IO_L14N_T2_SRCC_34 N20 BANK34_L14_N
IO_L15P_T2_DQS_34 M21 BANK34_L15_P
IO_L15N_T2_DQS_34 M22 BANK34_L15_N
IO_L16P_T2_34 N22 BANK34_L16_P
IO_L16N_T2_34 P22 BANK34_L16_N
IO_L17P_T2_34 R20 BANK34_L17_P
IO_L17N_T2_34 R21 BANK34_L17_N
IO_L18P_T2_34 P20 BANK34_L18_P
IO_L18N_T2_34 P21 BANK34_L18_N
IO_L19P_T3_34 N15 BANK34_L19_P
IO_L19N_T3_VREF_34 P15 BANK34_L19_N
IO_L20P_T3_34 P17 BANK34_L20_P
IO_L20N_T3_34 P18 BANK34_L20_N
IO_L21P_T3_DQS_34 T16 BANK34_L21_P
IO_L21N_T3_DQS_34 T17 BANK34_L21_N
IO_L22P_T3_34 R19 BANK34_L22_P
IO_L22N_T3_34 T19 BANK34_L22_N
IO_L23P_T3_34 R18 BANK34_L23_P
IO_L23N_T3_34 T18 BANK34_L23_N
IO_L24P_T3_34 P16 BANK34_L24_P
IO_L24N_T3_34 R16 BANK34_L24_N
IO_25_VRP_34 R15 BANK34_IO25
XC7Z020CLG484
U46E
IO_0_VRN_35 H17
IO_L1P_T0_AD0P_35 F16 BANK35_L1_P
IO_L1N_T0_AD0N_35 E16 BANK35_L1_N
IO_L2P_T0_AD8P_35 D16 BANK35_L2_P
IO_L2N_T0_AD8N_35 D17 BANK35_L2_N
IO_L3P_T0_DQS_AD1P_35 E15 BANK35_L3_P
IO_L3N_T0_DQS_AD1N_35 D15 BANK35_L3_N
IO_L4P_T0_35 G15 BANK35_L4_P
IO_L4N_T0_35 G16 BANK35_L4_N
IO_L5P_T0_AD9P_35 F18 BANK35_L5_P
IO_L5N_T0_AD9N_35 E18 BANK35_L5_N
IO_L6P_T0_35 G17 BANK35_L6_P
IO_L6N_T0_VREF_35 F17 BANK35_L6_N
IO_L7P_T1_AD2P_35 C15 BANK35_L7_P_AD4P
IO_L7N_T1_AD2N_35 B15 BANK35_L7_N_AD4N
IO_L8P_T1_AD10P_35 B16 BANK35_L8_P
IO_L8N_T1_AD10N_35 B17 BANK35_L8_N
IO_L9P_T1_DQS_AD3P_35 A16 BANK35_L9_P_AD3P
IO_L9N_T1_DQS_AD3N_35 A17 BANK35_L9_N_AD3N
IO_L10P_T1_AD11P_35 A18 BANK35_L10_P_AD2P
IO_L10N_T1_AD11N_35 A19 BANK35_L10_N_AD2N
IO_L11P_T1_SRCC_35 C17 BANK35_L11_P
IO_L11N_T1_SRCC_35 C18 BANK35_L11_N
IO_L12P_T1_MRCC_35 D18 BANK35_L12_P
IO_L12N_T1_MRCC_35 C19 BANK35_L12_N
IO_L13P_T2_MRCC_35 B19 BANK35_L13_P
IO_L13N_T2_MRCC_35 B20 BANK35_L13_N
IO_L14P_T2_AD4P_SRCC_35 D20 BANK35_L14_P_AD0P
IO_L14N_T2_AD4N_SRCC_35 C20 BANK35_L14_N_AD0N
IO_L15P_T2_DQS_AD12P_35 A21 BANK35_L15_P
IO_L15N_T2_DQS_AD12N_35 A22 BANK35_L15_N
IO_L16P_T2_35 D22 BANK35_L16_P
IO_L16N_T2_35 C22 BANK35_L16_N
IO_L17P_T2_AD5P_35 E21 BANK35_L17_P
IO_L17N_T2_AD5N_35 D21 BANK35_L17_N
IO_L18P_T2_AD13P_35 B21 BANK35_L18_P_AD1P
IO_L18N_T2_AD13N_35 B22 BANK35_L18_N_AD1N
IO_L19P_T3_35 H19 BANK35_L19_P
IO_L19N_T3_VREF_35 H20 BANK35_L19_N
IO_L20P_T3_AD6P_35 G19 BANK35_L20_P
IO_L20N_T3_AD6N_35 F19 BANK35_L20_N
IO_L21P_T3_DQS_AD14P_35 E19 BANK35_L21_P
IO_L21N_T3_DQS_AD14N_35 E20 BANK35_L21_N
IO_L22P_T3_AD7P_35 G20 BANK35_L22_P
IO_L22N_T3_AD7N_35 G21 BANK35_L22_N
IO_L23P_T3_35 F21 BANK35_L23_P
IO_L23N_T3_35 F22 BANK35_L23_N
IO_L24P_T3_AD15P_35 H22 BANK35_L24_P
IO_L24N_T3_AD15N_35 G22 BANK35_L24_N
IO_25_VRP_35 H18 BANK35_IO25
XC7Z020CLG484
R549
0R/125mW/1%/R0805
J42
D2_3
J43
D2_3
J44
D2_3
J45
D2_3
Title
PL BANK
Size A2
Document Number A5012
Rev 1
Date: Sunday, November 07, 2021
Sheet 7 of 12

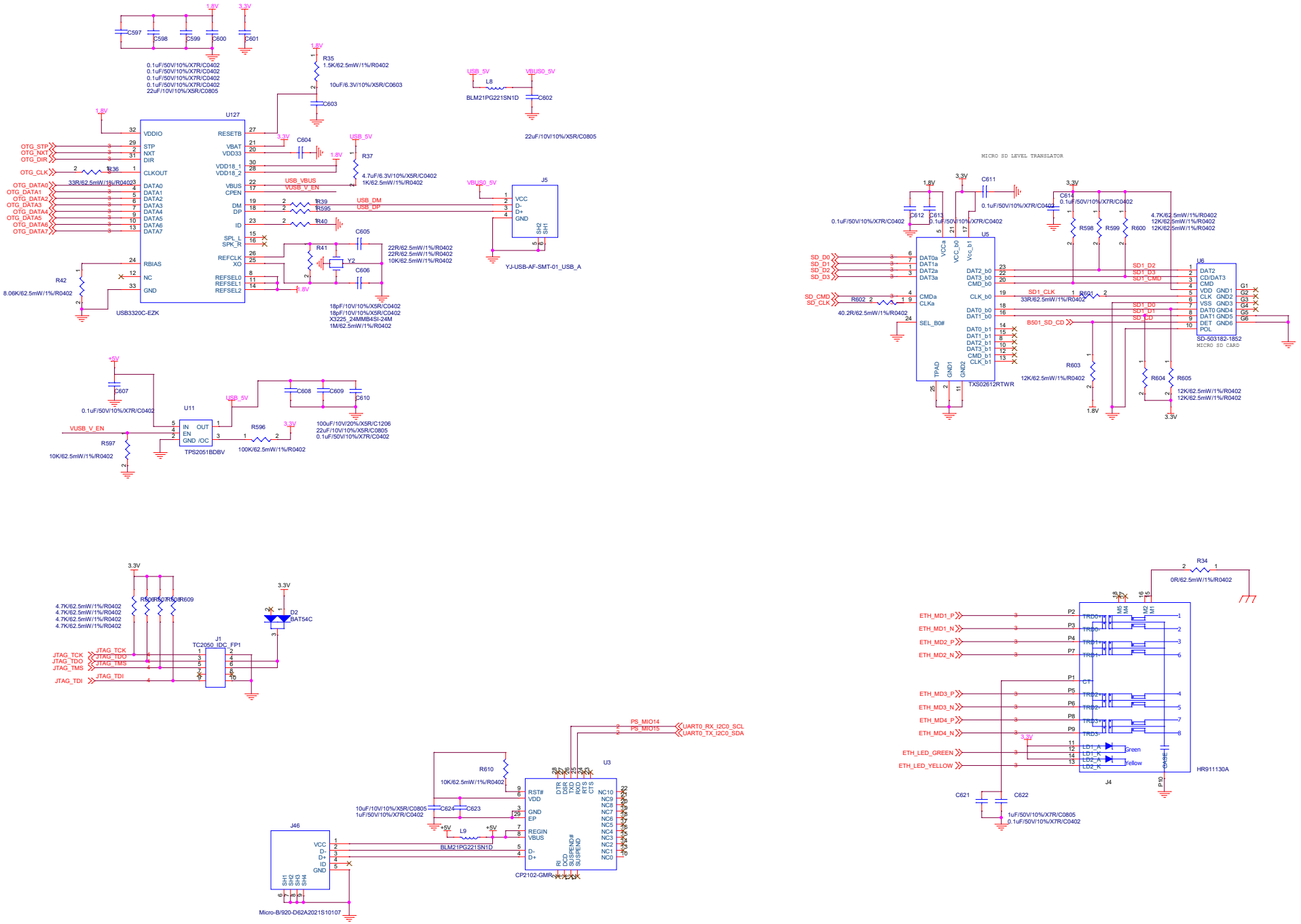


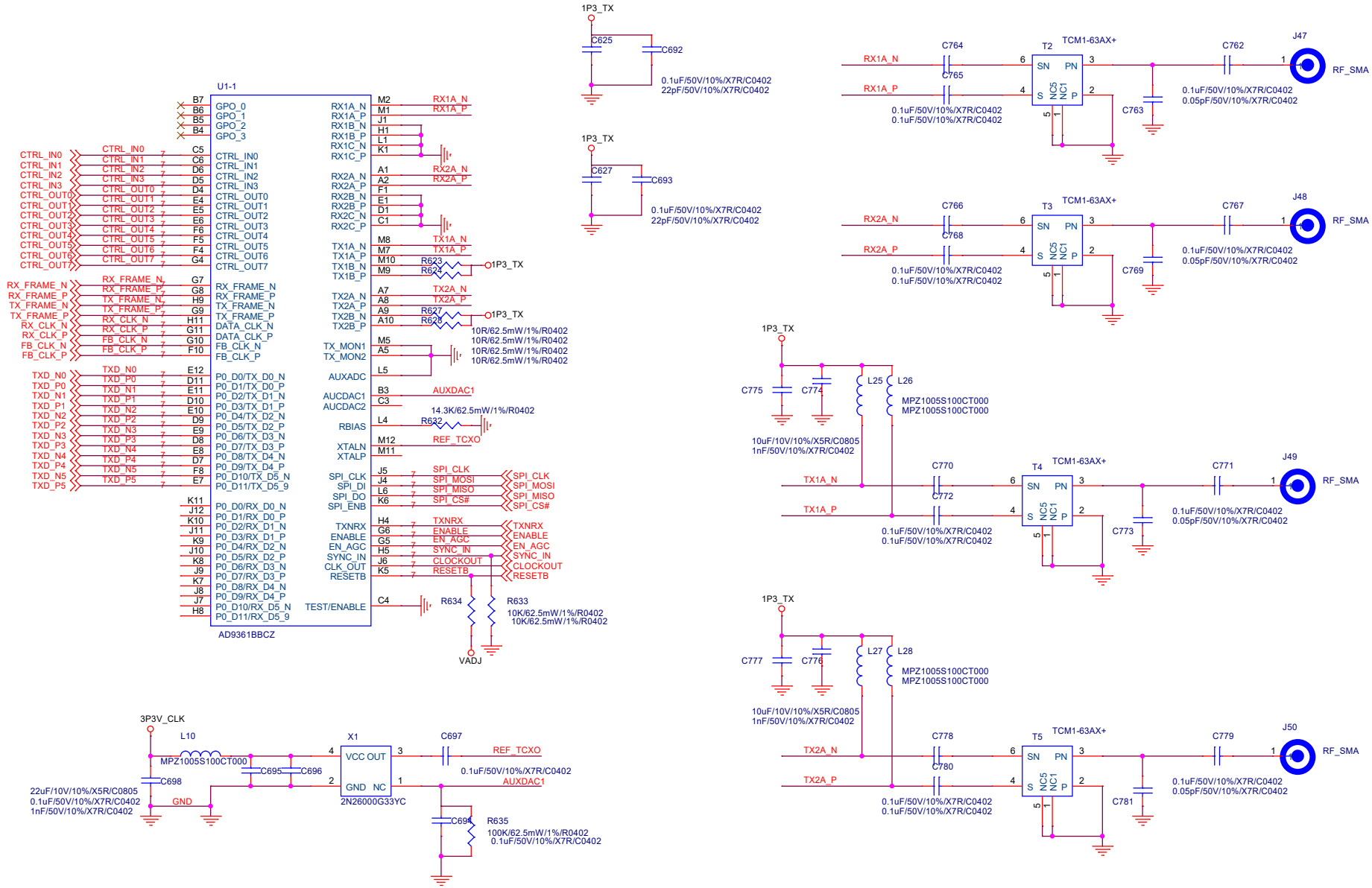
POWER UP SEQUENCE: 5V -> 1.0V -> 1.8V -> 1.5V (DDR) -> 3.3V -> PG_MODULE



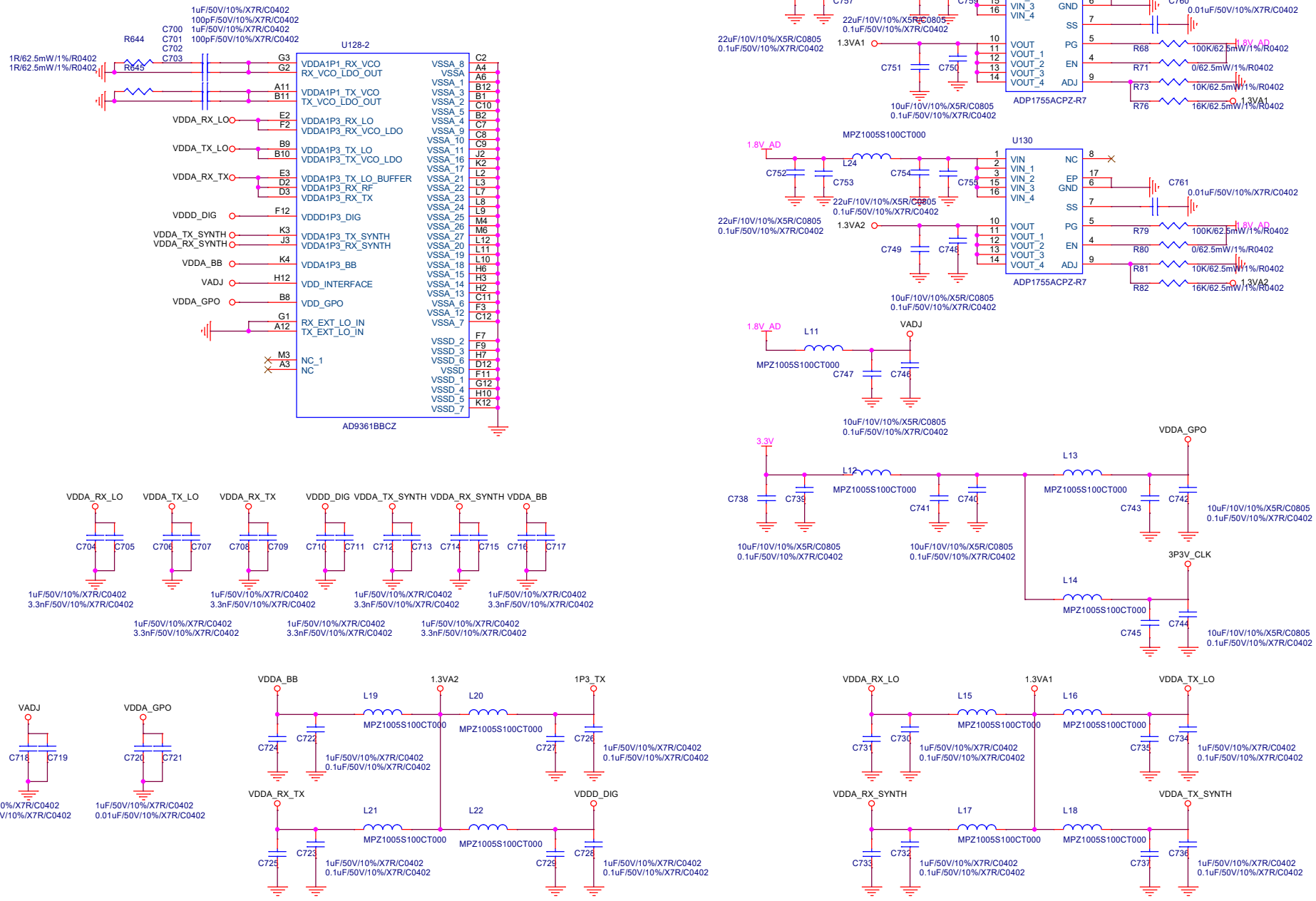


Title	<Title>	
Size A2	Document Number <Doc>	Rev <RevCo
Date: Sunday, November 07, 2021	Sheet 8 of 12	


MICRO SD LEVEL TRANSLATOR
USB3320C-EZK
TPS2051BDBV
TXS02612RTWR
CP2102-GMR
SD-503182-1852
MICRO SD CARD
HR911130A
YJ-USB-AF-SMT-01_USB_A
Micro-B/920-D62A2021S10107
BLM21PG221SN1D
0.1uF/50V/10%/X7R/C0402
22uF/10V/10%/X5R/C0805
10uF/6.3V/10%/X5R/C0603
0R/62.5mW/1%/R0402
Title
<Title>
Size A2
Document Number <Doc>
Rev <RevCo
Date: Sunday, November 07, 2021
Sheet 9 of 12



Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Sunday, November 07, 2021	Sheet 10 of 12	



Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Sunday, November 07, 2021	Sheet 11 of 12		