+

|11|

		OLNENA	L (%) ELECT	піб	2	224::695A.	3
REV Q X 2 224:	X695AA		COORDINATION TRUCTION	· KD	CONT ON SHEE	- 2	sн NO. 1
CONT ON SHEET	2 sh NO. 1	FIRST MADE FOR	193x2 <b>5 [A</b>	<b>4</b> c01 &	ABG01		
1.0 SCO	PE .			, 9.9.1	7.5001		REVI
are in S	covered in Eng Section 3.0.	overs the test p n Card, 193X251A ineering Specifi	AGUI, Its pecation 224x34	erforman 48AA. T			
2.0 <u>INST</u>	RUCTIONS SEC	Section 3.	O Frist				
2.01	tabs 21 or deviate by m	ut. Short tabs 22 should be +1. ore than <u>+</u> 22 vol	10 and 17 to 83 volts (±.1 ts. Tabs 23 8	common. 117).The	other tab : uld null be:	should no	
2.02	Tab 22 should than 5 volts	th tab 10 still s d null between 0 witha 1.82K load tabs 21 and 24 th	shorted, appl and8V and	+.50 v	volts to tak should be g	o 17.	/3
2.03	Gain Linearit should be 10 at tab 22 sho	Ey. Apply +8 volvolts (+10%). Nould be within .3	lts to tab 1 <b>7</b> low apply -8 I volts of th	, the ou volts to e value	tput at tab tab 17, th that was on	ne output n tab 21.	03 11/17
2.04 2.05	applied to tate to go to more This time a + null and the Remode Fig. 2. The Teedback Inputo to tab 18 and volts to tab 18 and nulled.	t & Bias. With ated and the for both lockouts s 20 instead of ta	A signal be the tab 23 repeat with signal will o go to more +10 volts on ward lockout hould be null b 18. Again	etween - lockout -8 volt cause t than 5 tab 17 fulled, led. Rep both loc	to null and to null and son tab 17 he tab 24 legal volts.  and the reveal apply -8.2 peat applying the chouts should be revealed applying the chouts should be revealed applying the chouts should be revealed applying the revealed applying the revealed applying the revealed be revealed by the revealed be revealed by the revealed by th	0 volts d tab 24ockout t erse 5 volts ng -8.25 ld be	3 of 8 2.01 & 2.
2.06		With +3 volts or go to more than	II VOITS.			( )	2
2.07	Armature Isola volts + 14volt should be between	ation. Apply +2 ts. Apply +10 voveen +.24 volt.	volts to tab olts to both	28, tab tabs 27	> 29 should and 28, tab	. ( -	11.
2.08	FET Gate Suppl Apply +10 volt	<u>ly</u> . Tab 5 should s to tab 6 & tab	l be between 5 should go	-19 and	-20 volts. Gen 0 and -		1000
2.09	$\underline{\text{DFP}}$ . Apply +2	0 volts to tab 1 .3 and 1 second	1 tah 8 ch	ould go	to more tha	m 17.5	5D (B)
2.10	rate of betwee	bserve tab 12. high and between n 9.8K and 11.2K p on the oscilla	Hz And 15 is	sec. wid	e with a re	petition	1 ) K ! K:
					ı		5QC <b>(2</b> B
							PRINTS
	The same of the sa	APPROVALS					
I/G.Tracy/	2-24-72	<b>X</b> 1	D_VARIATOR	DIV OR	224)	X695AA	

2/ 2

GENERAL & ELECTRIC

2247,695A.4

REV 1 TITLE CONT ON SHEET TO SHOOL 2

224X695AA TIST INSTRUCTION

CONT ON SHEET FL SH NO. 2 FIRST MADE FOR 193 251AAG01 & ABG01

REVISIONS

## 3.0 TEST CONDITIONS

3.01 Room Temperature

3.02 +20V (+.2 volt) to ab 31 Com TAB 15

CD ... 71113

3.03 -20V (+.2 volt) to tab 2

## 4.0 REQUALIFICATION

+

This card should be requalified by Quality Control every 18 months or 200 production cards, whichever comes first.

5D (BW)
5E (BW)
5L (BW)
5QC (2BW)
5R (BW)

PRINTS TO

J.G. Tracy/ 2-24-72

APPROVALS

\_SPEED\_VARIATOR

DIV OR

224x695AA

ERIE, PA.

LOCATION CONT ON SHEET

FL SHING. 2

FF-803-WA (1-70) PRINTED IN U.S.A.