9.1.0 SCOPE

This Printed Circuit card is a HIGH VOLTAGE PULSE AMPLIFIER TRANSFORMER CARD and is identified as:

DS3oOOHPTF

The HPTG mates by connection to a companion printed circuit card and by connections to the Thyristor Power Conversion Module. This Specification will check the following to insure minimum operation requirements:

Section 9.6.2 High Voltage Attenuator Test

SECTION 9.6.3 Leakage current Test
Section 9.6.5 Gate Driver Test
Section 9.6.6 Dielectric Test

9.1.1 The HPTF circuitry is analog with a mixture of both high and low voltage designs. With test safety in mind, all test voltage levels will be < 50 volts except for dielectric tests.

9.2.0 TEST EQUIPMENT

9.2.1 Standard Equipment Required:

Test equipment shall be provided which meets the requirements and accuracies prescribed in this specification. All test equipment is defined by Quality Control standard______except as noted in Section 9.2.2.

9.2.2 Special Equipment Required:

9.2.2.1 Pulse Generator:

Signal level +28V nominal Current level A maximum peak Rise and fall time $< 0.5 \mu sec$ A power transistor or darlington of like characteristics may be interfaced to complete gate driver tests in SECN-ON 9.6.5.

REV. 1	AEV. 4	AEV. 7	DL109 PRI	J.W.A	SENERAL ELECTRIC		cification TAGE PUISI
REV. 2	AEV. S	1000ED /2/	7/79		l DSD	-	
REV. 3	REV. 6	MADE SY J.Hyiten	#9092 8		SALEM, VA. U.S.A.		0 0 H P T 9BA SH.NO. 92

9.3.0 POWER SUPPLY REQUIREMENTS AND PIN CONNECTIONS

NOMINAL VOLTAGE	MAXIMUM CURRENT ²	% REG.	MAXIMUM VOLTAGE ³	PIN (S)
2 8 V	2 A	<u>+</u> 5%	32V	_ JAl
сом		į		J A2

Notes: 1. -5% voltage will be used unless otherwise specified in Section 9.6.4.

- 2. Average current is considerably lower.
- 3. Voltage above maximum volts may impair associated component performance.

9.4.0 SETUP AND INITIAL LOADING

- 9.4.1 Connect Pin GND to DCOM.
- 9.4.2 Connect a 10 Ohm, 2w, CARBON LOAD RESISTOR FROM JB1 TO JB2 and another from JC1 to JC2.

9.5.0 SIGNAL LEVELS

9.5.1 Digital input, Section 9.6.4

"0" Level = .8V

"1" Level = 28 Volt nominal

See Section 9.6.4.3 for pulse duration and pulse rate.

9.6.0 TEST PROCEDURE

9.6.1 The PWB shall be inspected prior to application of power to verify that it has been assembled according to assembly instructions.

REV. 1	REV. 4	BEIO9 P	engineer PWH	BENERAL ELECTRIC	Test Specifications HIGE VOLTAGE PULSE
REV. 2	REV. S	12/7/79		DSD	AMPLIFIER TRANSFORM D S 3 8 0 0 H F T F
REV. 3	REV. 6	J.Hylton 790928		SALEM, VA. U.S.A.	CONT. CHEM. 9CA MLMO. 9BA

9.6.0 TEST PROCEDURE (Continued)

9.6.2 High Voltage Attenuator Test:

To verify attenuator resistance continuity, perform the following resistance measurement.

From JA8 to JE value 1.992 MEGR \pm .1 0/0

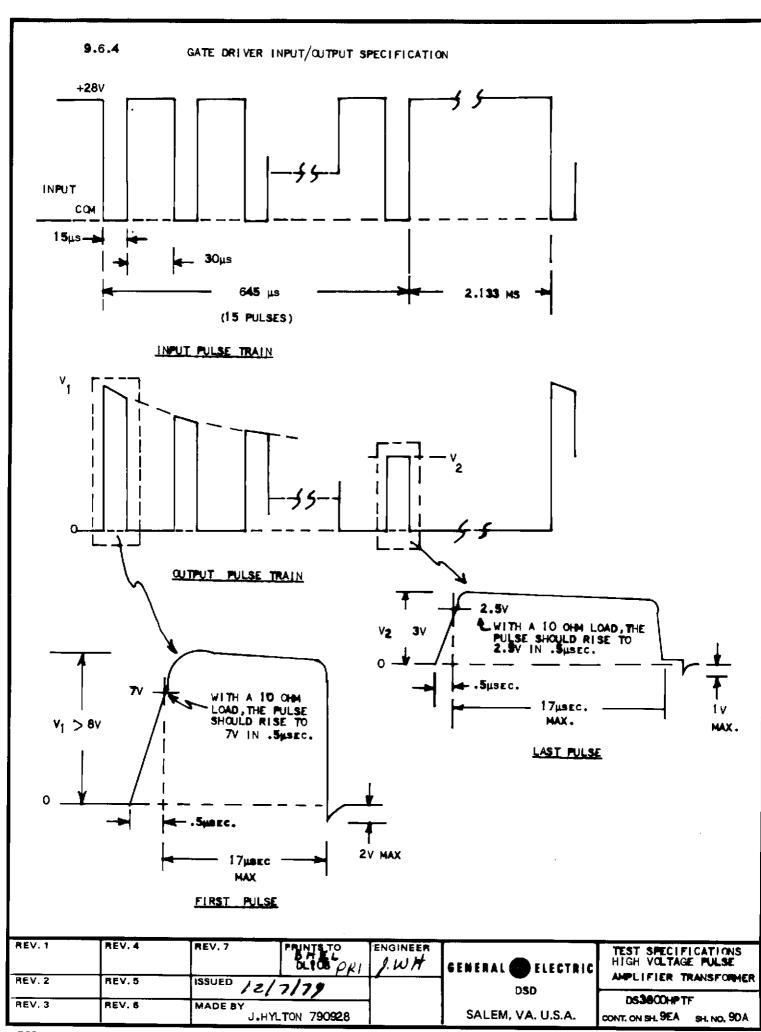
9.6.3 Leakage Current Test:

Individually apply +25 through a series 1K resistor between each of the following points and DCOM, and verify that the voltage across the 1K resistor does not exceed 1 MV.

JE4
JB1 JD1
JB2 JA8
JC1
JC3

Repeat the above test with -25 volts and again verify that each voltage measurement does not exceed 1 MV.

REV. 1	REV. 4	R€ V. 7	pling PRI	J.WH	SENERAL ELECTRIC	Test Specifications HIGH VOLTAGE PULSE AMPLIFIER TRANSFORMER
REV. 2	REV. S	12/ OBUBB	7/79		DSD	DS 3 8 0 OHPTF
REV. 3	REV. 6	J.HyIton	790928		SALEM, VA. U.S.A.	CONTECNIBLE SDA SERE SCA



9.6.5 Gate Driver Test:

- 9.6.5.1 Apply Bus Power:
 +28 VOLTS TO JA1
 (COM) TO JA2, JA3, JA5, JA6 AND JA7).
- 9.6.5.2 Apply input source between SIG1 (JA4) and COM and observe the output from THG1 (JB2)TO THC1

 JB1). REFER TO 9.6.4 SPECIFICATION.

 VERIFY THAT LED CR15 IS LUMINOUS.
- 9.6.5.3 REPEAT STEP 9.6.5.2 AND OBSERVE THE OUTPUT FROM THG2 (JC3,4) TO THC2 (JC1,2). REFER TO 9.6.4 SPECIFICATIONS.

MEV. 1	REV. 4	REV. 7	DL109 PRI	ENGINEER		Test Specifications
REV, 2	REV. 5	188UED /2	12/20	7.00	SEMENAL ELECTRIC	HIGH VOLTAGE PULSE AMPLIFIER TRANSFORM
REV. 3	REV. 6	MADE BY	<u> </u>	_	DSD	D S 3 8 0 0 H P T F
		J.Hylto	n 790928		SALEM, VA. U.S.A.	CONT. ON SH. SH. NO. 9EA

9.6.6. DIELECTRIC TEST (Hipot):

- 9.6.6.1 APPLY 3800 VRMS TO JB1 AND JC1 SIMULTANEOUSLY WITH JA2-AND GNO CONNECTED together and to Hipot common. JB1 AND JC1 MUST WITHSTAND THIS potential for 1 minute without breakdown.
- 9.6.6.2 APPLY 3800 VRMS TO JA2 AND GND WITH JB1 AND JC1 CONNECTED TOGETHER AND TO HIPOT COMMON. JA2 AND GND MUST WITHSTAND THIS POTENTIAL FOR 1 MINUTE WITHOUT BREAKDOWN.
- 9.6.7 Repeat Steps 9.6.0 to 9.6.5.

REV. 1	REV. 4	REV. 7	DL109 PRI	I.W.H	SEMERAL		HIGH	Specifications VOLTAGE PULSE
REV, 2	REV. B	100UED /2/	7/79		DSD	•	AMP.	TRANSFORMER
REV. 3	REV. 6	MAGE SHylto	n 790919	ļ	SALEM, V	A. U.S.A.	D S C	3 8 0 0 H P T FA