ENGINEERING MANUFACTURING INSTRUCTIONS — No. 5764

SUBJECT

DRIVE SYSTEMS CARD TEST

SECTION— 200
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CONT'D on PG.— 2

ROUTE

1. PURPOSE

Testing of: 1Ø NRP Control Card ML621L200G1 & G2.

2. ELEMENTARY

S&C Data Bk 1190 Sect. 200 Dwg 252A9017G1
266A2581G2

3. EQUIPMENT

a) 3Ø 115/20 Transformer assembly TL# 239053
b) 10V DC Variable Power Supply
c) Isolation transformer 115/115
d) Oscilloscope Tek 551 with type G plug-in or equiv.
e) VTVM John Fluke or equiv.
f) Reversing switch
g) Two TB's Jones 540 - 22 point Jones 541 - 18 point
h) Resistors
500 ohm 2W
100 ohm 1W
1 Kohm
10 Kohm
47 Kohm
2-10 ohm

Group 1 test per par. 5
Group 2 test per par. 6

Revision Notation	Prepared By	Section and Unit	Type Names	Signatures
	H. Keyzers	IC 910	Prod. Engineering JT Strong	AC Stevenson
	Date Issued: 14 October 77	Supersedes Issue Dated: 27 August 73	Manuf. Eng. J Legros	S. Legros 77/10/11
	SIGNATURES REQUIRED AS SHOWN →		Quality Control CA Finnamore	
			Eng'g. Lab.	

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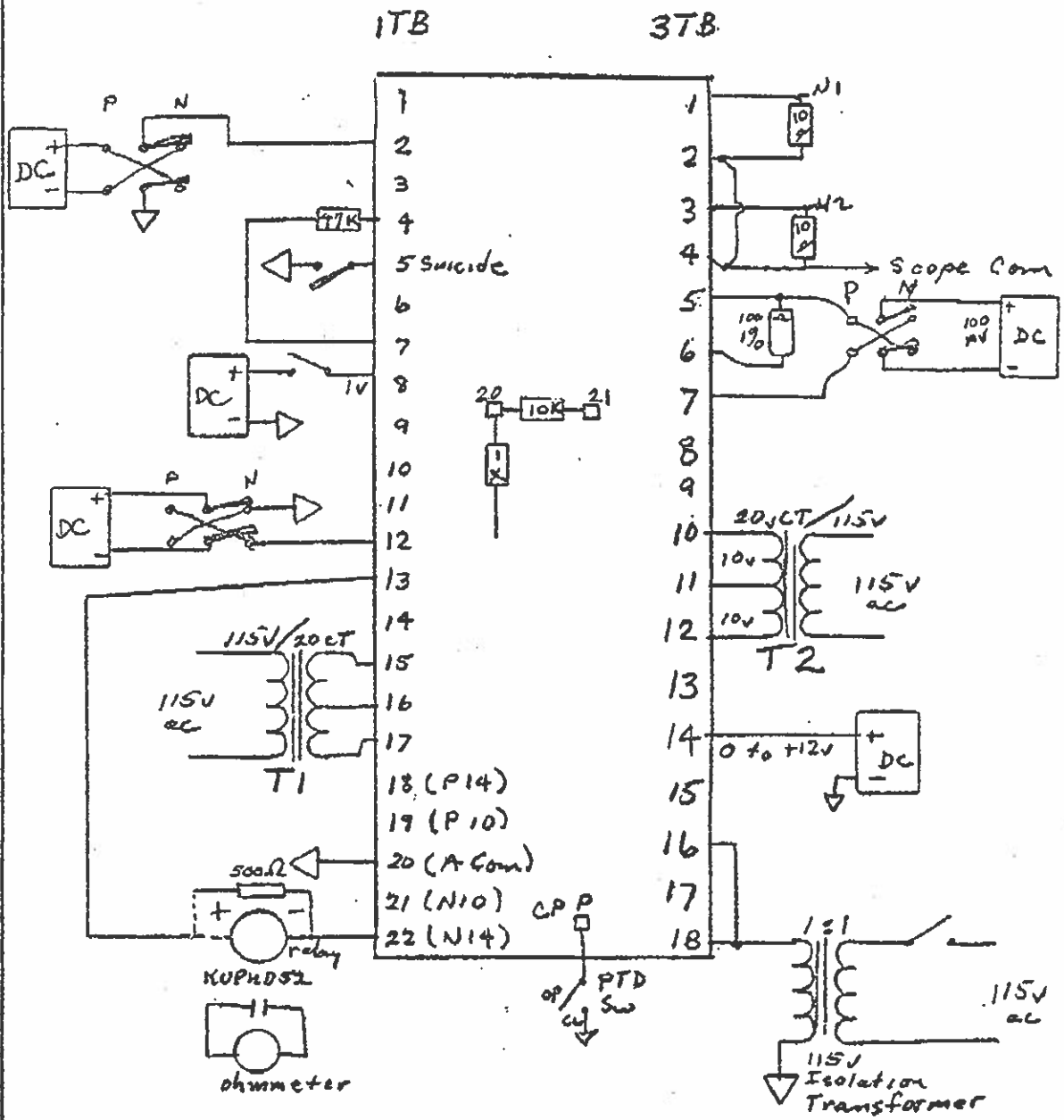
4. SET UP



ROUTE

Prepared By	Section and Unit	Type Names	Signatures
H. Keyzers	IC 910	Prod. Engineering JSTROTTER	BCStevenson 4Sept
Date Issued	Supp. Index Issue Dated	Manuf. Eng. CAFINNAMORE	
15 June 1977	27 August 1973	Quality Control CAFINNAMORE	
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5. TESTS

a) Bus Voltages (elem page 9)
   1TB18+ to 20 = P14V ± 2v
   1TB19+ to 20 = P10V ± 1V
   1TB21+ to 20 = N10V ± 1V
   1TB22+ to 20 = N14V ± 2V
   } use a DVM or AVO

b) CEMF Regulator (elem page 2)
   1) Turn R1-CCW Jumper: CP 6 to 7
      R8-CW " 3 " 4
      R9-CW Connect a ~~47K~~ between ~~1TB4~~ & 7
   2) Apply +10V to 1TB2. Check 1TB6 to be ≤ 50mv
   3) Apply +1 to 1TB2
   4) Connect 1TB5 to A COM (1TB20)
   5) Check that 1TB6 = -1v.
   6) Turn R1 CW and 1TB6 = -10v ± 1v.
   7) Turn R8 CCW and 1TB6 = -0.5v ± .1v.
   8) Apply -1v to 1TB2 and check that 1TB6 = +10v ± 1v.
   9) Turn R9 CCW and 1TB6 = +0.5v ± .1v

c) Field Current Regulator (elem page 3)
   1) Jumper CP8 to CP11
   2) Turn : R4 CCW
      R5 CCW
   3) Apply +1v to 1TB8 and check that 1TB12 = -0.7v ± 200 MV
   4) Adjust R4 CW until 1TB12 = -10v - 7.5 ± 500MV
   5) Reverse the polarity at 1TB8 and 1TB12 = +10v 7.5 ± 500 MV

d) Aux. Pots & Op Amp (elem page 3)
   1) Resistance checks
      a) 1TB10 to 1TB9 = 10K
      b) " " CP10 = 100K
      c) With R7 CCW CP16 to CP17 = 10K
      d) " " CW " " " = 0Ω
      e) " R6 CCW CP14 to CP15 = 10K
      f) " " CW " " " = 0Ω

ROUTE

Prepared By: F.J. Olson	Section and Unit: DS 934	Type Name:	Signatures
Date Issued: 27 Aug 1973	Supersedes Issue Dated: New	Prod. Engineering: JSTROTTER	ACStevenson 4Sept73
SIGNATURES REQUIRED AS SHOWN →		Manuf. Eng.: CAFINNAMORE	
		Quality Control: CAFINNAMORE	5Sept73
		Eng'g. Lab.	

Z Revision Edition

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SUBJECT: DRIVE SYSTEMS CARD TEST

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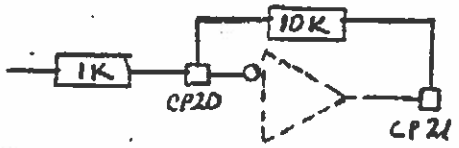
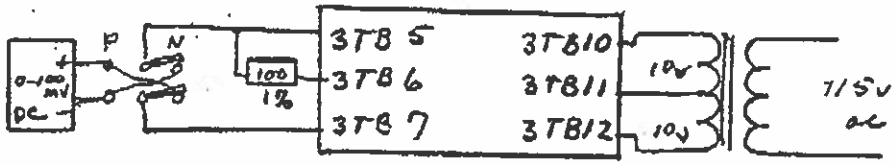
5. d) g) Connect the following;



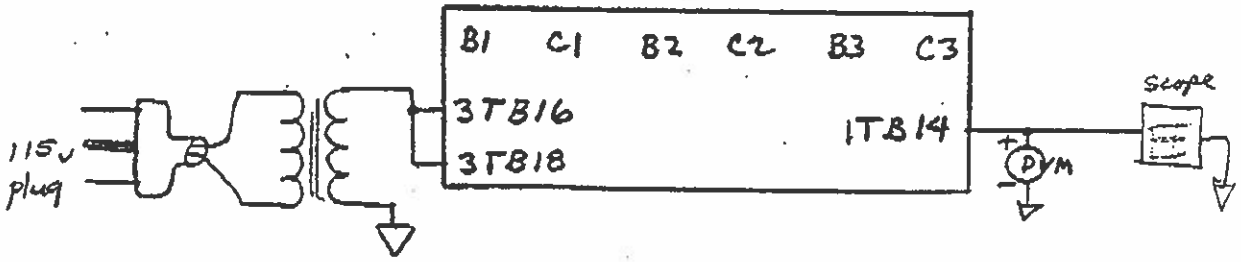
Apply +1v to 1K and CP21 = -10v
" -1v " " " " = +10v

e) Isolated Current Feedback Amp. (elem page 4)
1) Connect the following;



2) Connect 3TB5 to 3TB7. Adjust R110 until 3TB8+ to 3TB9 = Ov ± 20mv. SEAL POT.
3) Apply ~~100~~ +10v mv between 3TB5+ & 3TB7 and 3TB8- to 3TB9 = +10v ± 1v
4) Reverse input polarity and output should be = -10v ± 1v

f) Voltage Feedback (elem page 5)
1) Connect the following;



2) Turn R11 CCW
3) With 115V PLUG disconnected, adjust R88 until 1TB14 is Ov ± 10mv. SEAL POT
4) Plug in 115v PLUG and adjust R87 to give a sine wave at 1TB14 and note the amplitude.
5) Turn R11 CW and the sine wave should become 3 times the P-P value of the previous step.

ROUTE

Z — Revision
ZZ — Addition

Prepared By	Section and Unit	Type Names	Signatures
F.J. Olson	DS 934	Prod. Engineering JSTROTTER	BC Stevenson 4 Sept 73
Date Issued: 27 Aug 1973	Supersedes Issue Dated: New	Manuf. Eng. CAFINNAMORE	
SIGNATURES REQUIRED AS SHOWN →		Quality Control CAFINNAMORE	5 Sep 73
		Eng'g. Lab.	

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5. f) 6) Now adjust R87 until the sine wave is a minimum amplitude. SEAL POT.

7) Verify that the following resistors are correct & soldered in

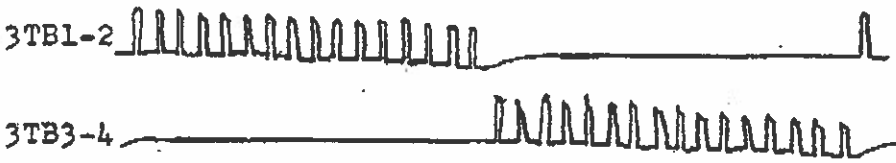
R100 = 10K } 4.99K for 62
R102 = 10K }
R105 = 10K

g) Level Detector (elem page 6)

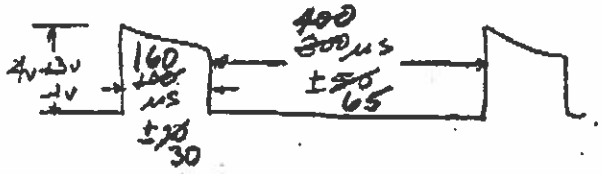
1) Connect KUP11D52 relay across 1TB13 - 1TB22
2) Jumper; CP31 to CP32
CP47 " CP48
3) Turn R10 CCW
4) Apply Ov to 3TB14 and relay should be dropped out.
" +1v " " " " pick up.
Turn R10 CW " " " drop out.
Apply +12v to 3TB14 " " " pick up.

h) Gate Pulse Generators (elem pages 7, 8)

1) Connect 10Ω loads between; 3TB1 & 3TB2
3TB3 & 3TB4
2) Set R2 fully CCW
3) Pull jumper from CP13
4) Apply +10v to 1TB12 and observe pulses on 3TB1-2 and 3TB3-4



5) The first pulse of each pulse train should be;



6) Reduce voltage at 1TB12 to zero and pulses should disappear

ROUTE

Prepared By	Section and Unit	Type Names	Signatures
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		Eng'g. Lab.	

Z —Revision
ZZ —Addition

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5. h) 7) Turn R2 fully CW and pulses re-appear.

3TB1-2 

3TB3-4 

There should be 5 pulses ± 2 in each train.

8) Reduce 1TB12 volts to -15V and pulses should remain unaffected.

i) 1) Connect CP"P" to ACOM and pulses should disappear
2) Remove ACOM from CP"P" and pulses should re-appear after 1/2 sec approx.

ROUTE

Z — Revision Edition

Prepared By	Section and Unit	Type Names	Signatures
F.J. Olson	DS 934	Prod. Engineering JSTROTTER	AC Stevenson 4 Sept 73
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SIGNATURES REQUIRED AS SHOWN →		Quality Control CAFINNAMORE	Sept 73
		Eng'g. Lab.	

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6. End of Test Routine

1) Ensure the following pots are sealed.
R87, R89, R110

2) After test pot settings

R1	- CCW	(Gain - CEMF)
R8	- CW	(Neg. Lim)
R9	- CW	(Pos. Lim)
R5	- midposition	(Ref. Adj)
R4	- CCW	(Gain - Fld)
R2	- ~~cw~~ MID. POS.	(Ret Lim Adj)
R7	- CCW	(Aux pot)
R6	- CCW	(Aux pot)
R11	- CCW	(Gain - Vfbk)
R87	- don't touch	(Vfbk trim)
R89	- don't touch	(Vfbk C. Mode trim)
R110	- don't touch	(I fbk trim)
R10	- CCW	(Level Det. Ref.)

3) Ensure that jumpers are on the following CP's;

3-4	18-19	
6-7	31-32	B3-C3
10-11	26-28	B1-C1
12-13	46-48	B2-C2

ROUTE

Z — Revision
7C — Edition

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Prepared By	Section and Unit	Type Names	Signatures
F.J. Olson	DS 934	Prod. Engineering JSTROTTER	AC Stevenson 4Sept73
Date Issued: 27 Aug 1973	Supersedes Issue Dated: New	Manuf. Eng. CAFINNAMORE	
SIGNATURES REQUIRED AS SHOWN →		Quality Control CAFINNAMORE	
		Eng'g. Lab.	

6. TESTS for G2

a) AC Input Power
1) Apply 1 phase AC power
2) With oscilloscope observe inputs per FIG 2.

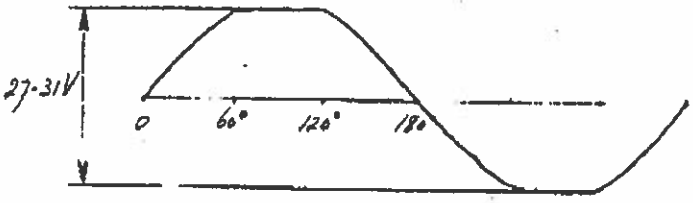

FIG 2

b) DC Power

1)	+15VDC ± 1.5V between 1TB18(+) & 1TB20(-)	<300mV
	-15VDC ± 1.5V between 1TB22(-) & 1TB20(+)	<300mV
Adjust	+10VDC ± 0.1V between 1TB19(+) & 1TB20(-)	< 30mV
Adjust	-10VDC ± 0.1V between 1TB21(-) & 1TB20(+)	< 30mV

c) GPG Phasing Supply
1) Sync oscilloscope on "line" and display on channel 1 1TB15(+) & 1TB16(-) per FIG 2.
2) With channel 2 observe the following:

Testpoint	Amplitude	Shift
0°	27-31V P/P	0°
90°	13.4-23.4V P/P	81°-84.5°
180°	27-31V P/P	180°
270°	13.4-23.4V P/P	261°-264.5°

3) Gate Pulse Generator
a) Measure Retard Limit Adj. CP40 to be between +5.7VDC and 6.3VDC.
b) With CP12-13 off and CP41-42 on apply +4.5VDC to 1TB42. Lights L30 of GPG of circuit A&B should illuminate.
Pulse trains should appear on CP 35 per FIG 3.

ROUTE

Prepared By	Section and Unit	Type Names	Signatures
H. Keyzers	IC 910	Prod. Engineering JT Strong	RC Stevenson
Date Issued: 7 November 77	Supersedes Issue Dated: New	Manuf. Eng. J Legros	S.L. Legros 7/11/11
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		Eng'g. Lab.	

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DRIVE SYSTEM CARD TESTING

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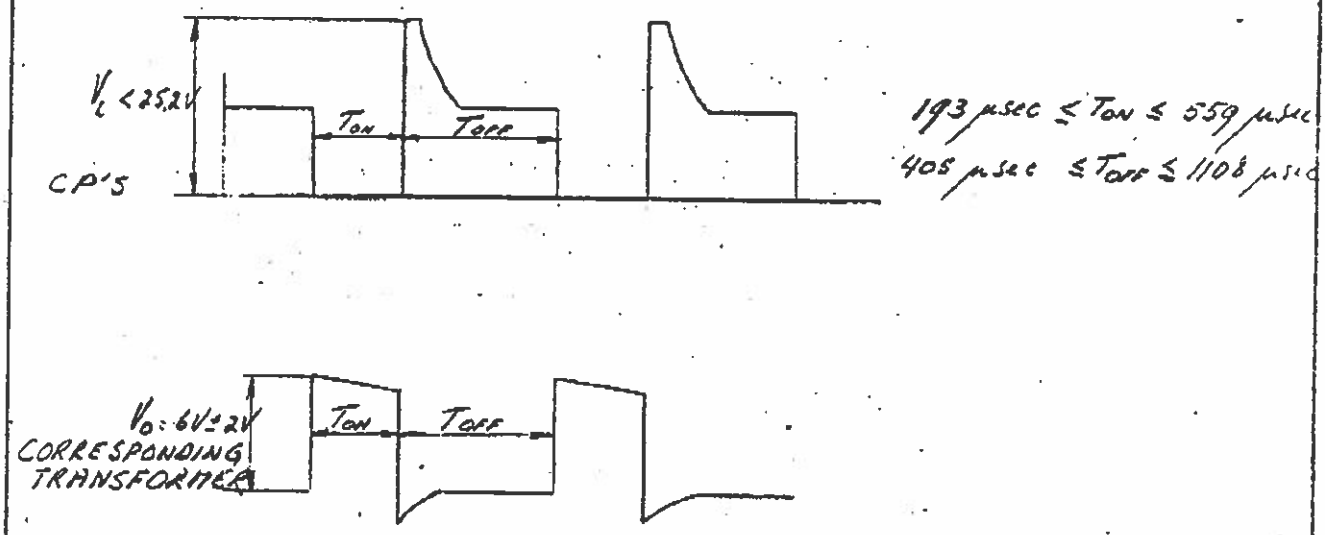

FIG 3.

Ensure that the first pulse of each train of circuit A is 8.33 msec ± .5 ms away from the first pulse of each train of circuit B.

c) Apply +10VDC to 1TB-2. L30 of circuit A&B should illuminate.
The start of the pulse train for circuit A should appear at 0° w.r.t. 1TB15(+) and pulse train should be approx. 8 msec long.

d) Apply OVDC to 1TB2
The start of the pulse train of circuit B should appear at approx. 162° w.r.t. 1TB15(+).
The start of the pulse train of circuit A should appear at approx. 342° w.r.t. 1TB15(+).

e) Apply VDC to 1TB2 and observe pulse train
Momentarily remove CP41-42 and note that pulses disappear on both circuits.
Reconnect CP41-42.

ROUTE

Prepared By	Section and Unit	Type Names	Signatures
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Date Issued	Supersedes Issue Dated	Manuf. Eng. J Legros	S.R. Legros 22/11/11
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ENGINEERING MANUFACTURING INSTRUCTIONS — No. 5764

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f) Apply OVDC to 1TB2 and observe pulse train
Momentarily connect CP-P to ACOM and note that pulses disappear on both circuits.
Remove CP-P from ACOM. Pulses should re-appear after 0.63 sec. to 1.01 sec.
Voltage on CP-P should return to +6.49VDC to 7.11VDC.

4) For remainder of tests test per par 5 b) to g).

ROUTE

Prepared By	Section and Unit	Type Names	Signatures
H. Keyzers	IC 910	Prod. Engineering JT Strong	
Date Issued: 7 November 77	Supersedes Issue Dated: New	Manuf. Eng. J. Legros	
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