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P3K-AL-0309-A01
CONT ON SHEET 13 SH NO. 12

TITLE

TEST INSTRUCTIONS FOR SPEED MATCHER 60 HZ

FIRST MADE FOR EHC MARK II

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TEST SETUP

EQUIPMENT REQUIRED (or Equivalent)

1. Frequency Source — HP Model 200 AB or HP Model 3310B
2. Frequency Counter — HP Model 5223L or 5D Model 6150
3. Digital Voltmeter — Fluke Model 8120A or HP Model 3478A
4. Oscilloscope — Tektronix Model 7514 or 7633 Equipped with Two Dual Trace Amplifiers Type 7A18 or 7A26
5. Precision Power Supply — HP Model 6114A

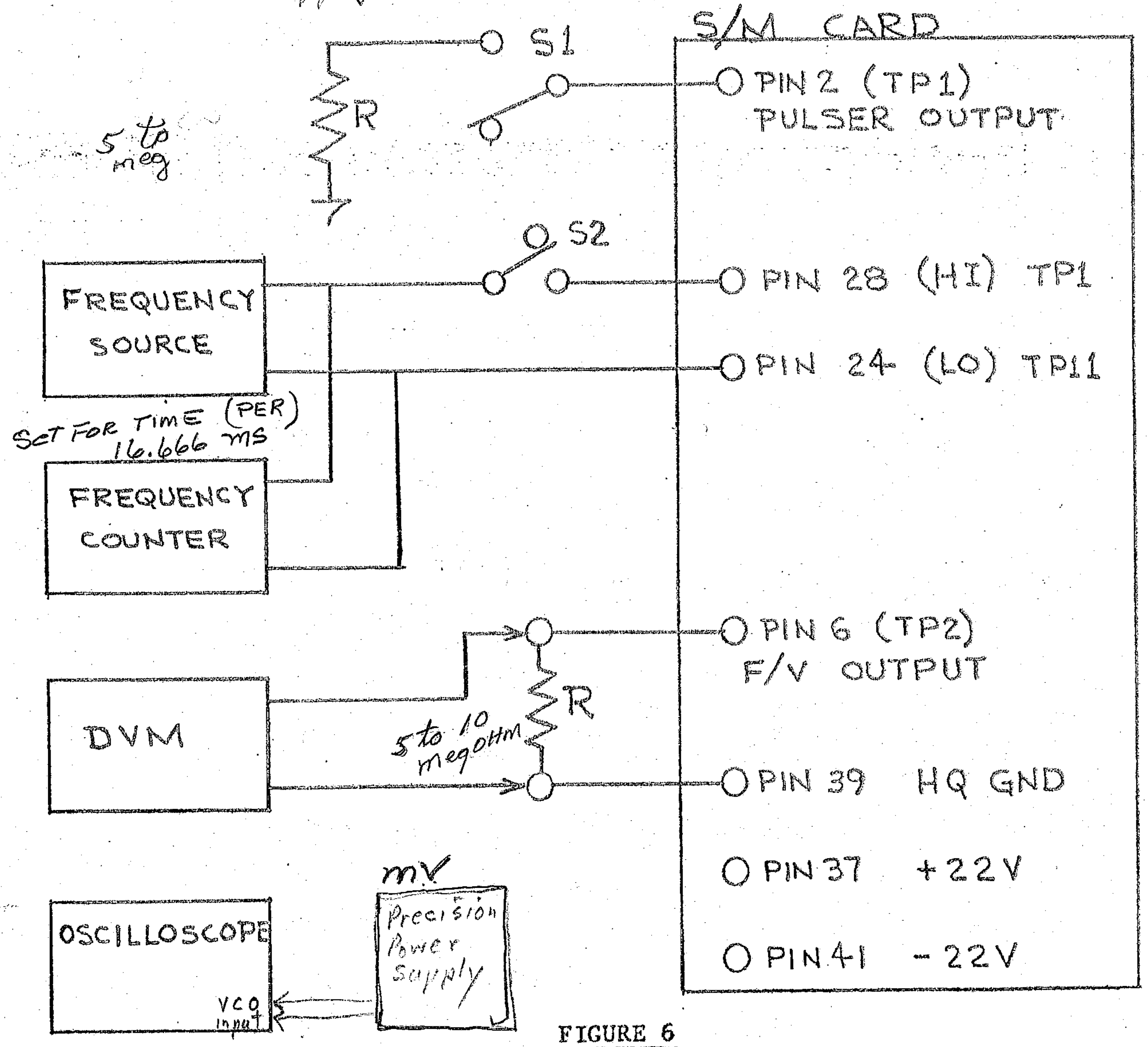

FIGURE 6

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TITLE
TEST INSTRUCTIONS FOR SPEED MATCHER 60 HZ

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IV. TEST INSTRUCTIONS (FOR SPEED MATCHER 60 HZ FREQUENCY TO VOLTAGE CONVERTER)

* All notes are intended for information purposes and for trouble shooting aids**

* NOTE: Positive logic is used thru out entire digital design.

1. CONNECT S/M circuit board per test set-up shown in Fig. 6.
2. CHECK ZENER VOLTAGES on the card per circuit specification sheets.
3. NULLING ACTIVE FILTER AMPLIFIER (IC3)

   ° Apply dc power to the S/M card but keep the input signal from the sine wave oscillator turned off. SW2 open (Important)

   \#1

   ° Adjust trimpot VR51 for zero volts output (± .001 V) at TP55.

4. NULLING VOLTAGE FOLLOWER AMPLIFIER (IC5)

   ° Adjust trimpot VR52 for zero volts output (± .001 V) from the voltage follower amplifier at TP2 when the input to IC5 is zero.

   \#2

   TP55 GN

5. SETTING INPUT LEVEL TO BE DETECTED

   ° Set the oscillator frequency at 60 HZ and the amplitude of the input sine wave to approximately 2V p to p.

   ° Reduce the 2V signal down to 100mV p to p by using a 10 turn pot as shown below:

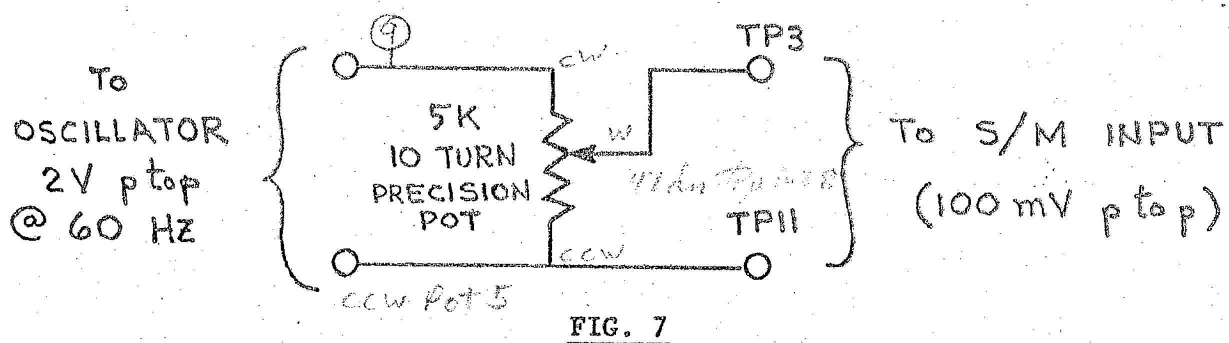

FIG. 7

° Apply the 100mV signal to the S/M input.

° Observe the output of IC1 at TP4 on the scope and slowly adjust trimpot VR50 either CW or CCW until a stable square wave can be obtained as shown below.

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IV. TEST INSTRUCTIONS (FOR SPEED MATCHER 60 HZ FREQUENCY TO VOLTAGE CONVERTER) (continued).

5. SETTING INPUT LEVEL TO BE DETECTED (continued)

*NOTE: A stable dc output voltage from the S/M card will result when the pot is properly adjusted.

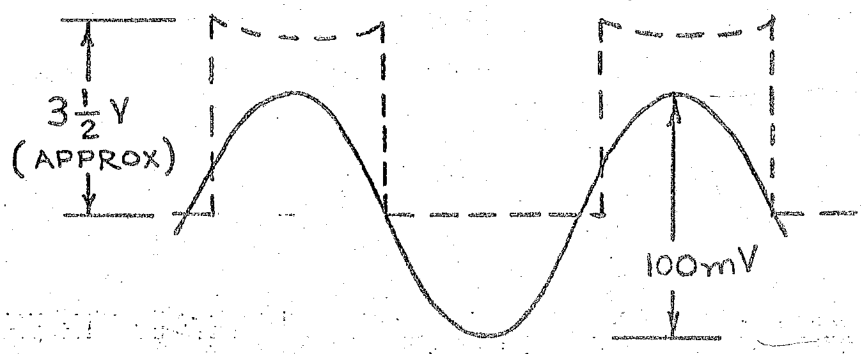

FIG. 8 ADJUSTING TRIMPOT VR50 TO OBTAIN SQUARE WAVE OUTPUT FROM IC1 @ TP4

*NOTE: The primary purpose of trimpot VR50 is to adjust the detection level of comparator IC1 so that low amplitude input signal (approx. 100 mV) can produce a stable square wave output. As soon as the input level is much $\gg$ 100mV, this adjustment is insignificant. After VR50 is adjusted, note that signals $\leqslant$ 100 mV p to p will go undetected and the S/M will not produce any dc output.

6. CHECKING & RECORDING CRITICAL VALUES

° Remove the 5K (10 turn) pot from the oscillator input. Remove TP55 Gnd.

*NOTE: This pot should be removed because it may produce noise problems in the test setup.

° Measure and record the voltage at CR4 (zener voltage must be +9.0V $\pm$ 1%). $\pm$ .090 mV

9.039

° Set the oscillator amplitude at approx. 2V p to p and the frequency at exactly 60.0 $\pm$ 0.1 Hz.

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IV. TEST INSTRUCTIONS (FOR SPEED MATCHER 60 HZ FREQUENCY TO VOLTAGE CONVERTER) (continued)

6. CHECK & RECORDING CRITICAL VALUES (continued)

° Adjust VR1 full CW and record the dc output voltage at TP2 (voltage must be ≥ -10.200 volts). For example, an output voltage of -10.400 V is acceptable but an output of -10.100 V is unacceptable.

° Adjust VR1 full CCW and record the dc output voltage at TP~~1~~ 2 (voltage must be ≤ -9.800 volts). For example, an output voltage of -9.600 V is acceptable but an output of -9.900 is unacceptable.

*NOTE: The output voltage will vary approximately 0.8 V when VR1 is adjusted from end to end. Trimpot VR1 adjusts the unijunction time from approximately 12.2 to 13.0 msec.

The unijunction time controls the width of the pulses to IC3. This time can be measured on the scope at TP5 as shown below:

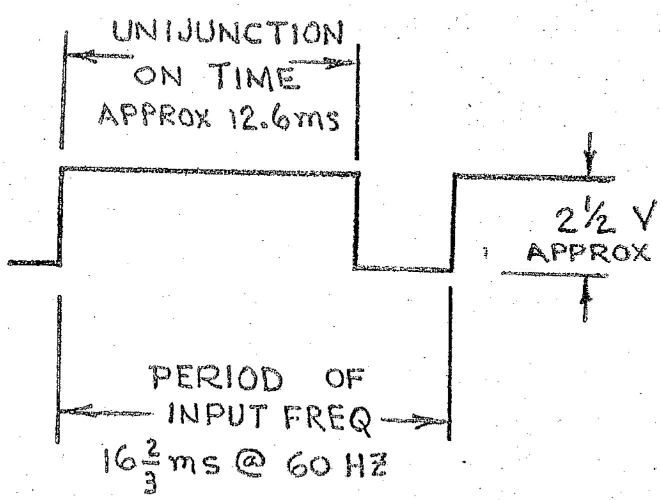

FIG. 9 WAVEFORM @ TP5 (FREQ = 60HZ)

*NOTE: The same pulse shape as shown above can also be observed at the input to the output amplifier IC3 except that the amplitude will be approximately 4 1/2 volts (measured at collector of Q2).
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IV. TEST INSTRUCTIONS (FOR SPEED MATCHER 60 HZ FREQUENCY TO VOLTAGE CONVERTER) (continued)

6. CHECK & RECORDING CRITICAL VALUES (continued)

Typical Values Associated With Adjusting VR1

VR1	OUTPUT VOLTAGE dc (TP 2)	UNIJUNCTION TIME (TP5)
Full CCW	-9.600	12.2 msec
Center of Pot	-10.000	≈ 12.6 msec
Full CW	-10.400	13.0 msec

7. CALIBRATING S/M OUTPUT VOLTAGE

- Set the oscillator frequency at exactly 60.0 ± 0.1 Hz and amplitude at approximately 2V p to p.
- Adjust trimpot VR1 until output at TP2 equals -10.000 ± .001 volts.
- Increase and decrease the oscillator amplitude from 2V p to p to 20V p to p. Note that the dc output should not be sensitive to changes in input amplitude, but only to changes in frequency.
- Check the output voltage at several additional frequency points shown below:

INPUT FREQUENCY (HZ) ±.1	Period (μs)	DC OUTPUT VOLTAGE
72	13,889	-12.000 ± .002 V
60	16,667	-10.000 ± .001 V
30	33,333	- 5.000 ± .002 V
15	66,667	- 2.500 ± .002 V

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IV. TEST INSTRUCTIONS (FOR SPEED MATCHER 60 HZ FREQUENCY TO VOLTAGE CONVERTER) (continued)

7. CALIBRATING S/M OUTPUT VOLTAGE (continued)

*NOTE: When the input frequency = 60 Hz, the output voltage will be -10.000 V, and the duty factor will be approximately 75%.

Freq. (Hz)	Period (μs)	Vout ±.002 VDC
60	16,667.	-10.000
62	16,129.	-10.333
64	15,625.	-10.666
66	15,152.	-10.999
68	14,706.	-11.332
70	14,286	-11.665
72	13,889	-11.998

- Increase the input frequency slowly from 60 Hz to 72 Hz (Note that the output must increase linearly from -10.000 to -12.00 volts).
  Note: 1.7 μs = 1 mV
- Observe that the output voltage does not decrease or fall off before reaching 72 Hz.
- After checking the linearity, increase the input frequency until the output voltage falls off to approximately -6.6 V. Observe that the input frequency is > 72Hz when this condition occurs.

*NOTE: When the S/M is operating in the linear region, the output voltage can be calculated as follows:

$$V_o = (VCR4)\left(\frac{\text{Period of unijunction}}{\text{Period of input frequency}}\right) \quad (-\text{Gain IC3})$$

WHERE:

VCR4 = Input zener voltage to output amplifier IC3.

$\frac{\text{Period of unijunction}}{\text{Period of input frequency}}$ = Ratio of the zener voltage CR4 ON time to the total time.

GAIN IC3 = GAIN of output amplifier IC3.

$= [-R20/(R17 + R18)]$

$$V_o \text{ @ 60 Hz} = (9V)\left(\frac{12.6 \text{ msec}}{16.7 \text{ msec}}\right)\left(-\frac{88.7K}{30.1K + 30.1K}\right)$$

Vo @ Rated Line Frequency = -10.00 volts.

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IV. TEST INSTRUCTIONS (FOR SPEED MATCHER 60 HZ FREQUENCY TO VOLTAGE CONVERTER) (continued)

7. CALIBRATING S/M OUTPUT VOLTAGE (continued)

As the period of the input frequency approaches the period of the unijunction, (100% duty factor) the maximum output voltage which can be obtained from the circuit is as follows:

$$\text{Vo @ 79 HZ} = (9V)\left(\frac{12.6\ \text{msec}}{12.6\ \text{msec}}\right)\left(\frac{88.7K}{30.1K + 30.1K}\right)$$

$$= -13.2\ \text{volts}$$

Therefore the upper frequency limit of the linear region is also a function of the unijunction time. Note that when the period of the input frequency becomes less than or equal to the period of the unijunction timer, the flip flop will start missing input pulses. As a result, the output voltage will drop to approximately 1/2 of the original value (approximately -6.6V).

8. OBSERVING OUTPUT FOR OSCILLATIONS & CHECKING RIPPLE AT TP2

° Vary oscillator frequency from 15 Hz to 75 Hz and observe the output on the scope. The dc ripple or noise riding on the DC output should not exceed 10 MV p to p and output must be free from oscillations.

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8A. RETESTING UNIJUNCTION TEMPERATURE COMPENSATION

- Return the oscillator frequency to exactly 60 HZ, and observe that output at TP6 equals -10.000 volts.
  Pin 6
- Set the heat probe at 55°C and apply the probe to the unijunction for 30 sec. Remove the probe and observe that the output voltage must return to within ± 3mV of the original -10.000V setting. (The unijunction heat test is repeated in order to insure that the correct temperature compensation resistor has been previously selected). Use Timer (designed for temp. compensating test) to measure 30 sec. interval that heat probe is applied.

CRITERIA S/M output must return to within ± 3mV of the original -10.000V setting when heat probe test is repeated.

Procedure to Correct Temperature Compensation to be within ± 3mV Criteria

If Production S/M output (matched parts installed) fails to meet ± 3mV change in output when unijunction is retested with heat probe, use the following procedure to reduce the change to be within the ± 3mV criteria:

1. Replace R11 (temp. compensation resistor)

   If S/M output increases more than 3 mV (-10.000V increases to more than -10.003V) when heat probe test is performed, reduce R11.

   If S/M output decreases more than 3 mV (-10.000V decreases to less than -9.997V) when heat probe is performed, increase R11.

   Note that S/M output changes 3 mV for every change in resistor step (1%).
   If After changing R11, V out at TP2 will have to be re checked per IV. 6 If values not correct R9 will have to be changed

2. If value of resistor R11 cannot be increased because it's already at a maximum, replace +11.7V zener CR5. Note that 1% change in zener voltage CR5 will cause approximately 2 mV change in S/M output.

   use 1M Res in Series

   If S/M output increases more than 3 mV (-10.000V increases to more than -10.003V) when heat probe test is performed, select a new CR5 which has lower zener voltage than original value.

   If S/M output decreases more than 3 mV (-10.000V decreases to less than -9.997V) when heat probe test is performed, select a new CR5 which has a higher zener voltage than original value.

3. If value of zener CR5 cannot be increased or decreased to temperature compensate the unijunction transistor to within 3 mV, replace all matched components and start over.

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9. CHECK ACTIVE FILTER FREQUENCY COMPENSATION NETWORK BY OBSERVING THE TIME RESPONSE TO A STEP INPUT.

- Switch the Input Frequency at TP3 from 0 HZ to 60 HZ, and observe the change in output voltage @ TP55. (Use a storage scope to capture the transient time response on the screen).
- Fig.10 shows the waveshape, % overshoot, time to peak, and tolerances which must be observed.

*NOTE:

The above time response test is used to check the active filter characteristics (Damping Ratio = .482 & Undamped Natural Frequency = 11.6 RAD/SEC) when transistor Q2 is OFF and CR4 applies 9V to the input of the active filter amplifier IC3.

- Switch the input frequency at TP3 from 60 HZ to 0 HZ, and observe the change in output voltage @ TP55 (Use a storage scope to capture the transient time response on the screen).
- Fig. 11 shows the waveshape, % Overshoot, Time to Peak, and Tolerances which must be observed.

*NOTE:

The above time response test is used to check the active filter characteristics (Damping Ratio = .625 and Undamped Natural Frequency = 11.6 RAD/SEC) when zero volts is applied to the input of the active filter amplifier IC3.

10. CHECK S/M OVERALL FREQUENCY RESPONSE BY OBSERVING THE TIME RESPONSE TO A STEP INPUT

- Switch the input frequency at TP3 from 0 HZ to 60 HZ, and observe the change in S/M output voltage at TP2. (Use a storage scope to capture the transient response on the screen).
- Fig. 12 shows the waveshape, time constant and tolerances which must be observed.

NOTE:

The above test is used to check the passive filter when the output from the active filter is applied to the input of the passive filter. This test also checks the S/M overall frequency response when a step change of input frequency is applied to the S/M.

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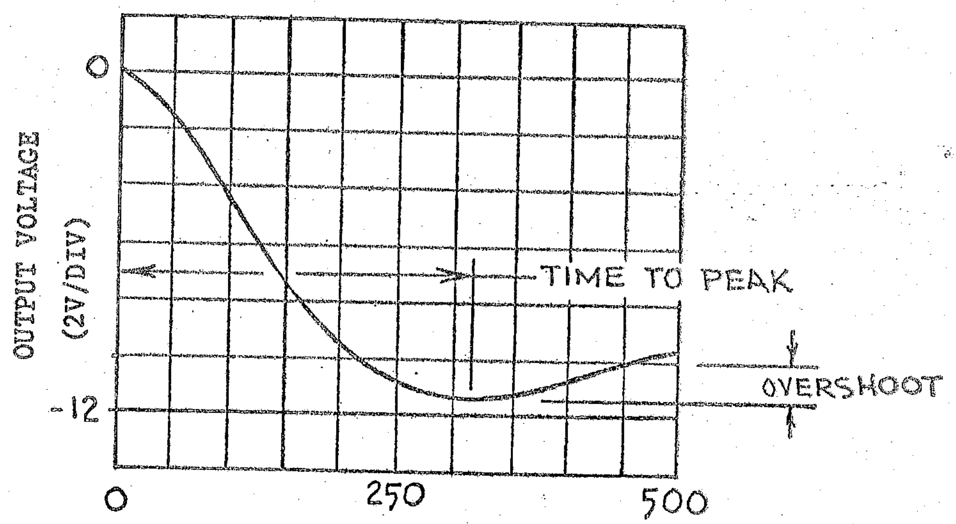
FIG. 10 S/M ACTIVE FILTER OUTPUT VOLTAGE (TP55) TRANSIENT RESPONSE

FOR STEP CHANGE OF INPUT FREQUENCY
FROM 0 HZ TO 60 HZ



NOTE:

UNDAMPED NATURAL FREQUENCY (ω_o) = 11.6 RAD/SEC

DAMPING RATIO (ζ) = .482

MAX OVERSHOOT %=17.7 ± 2.3

MAX OUTPUT VOLTAGE = 11.70 ± 0.23 VDC @ 309 ± 9 msec

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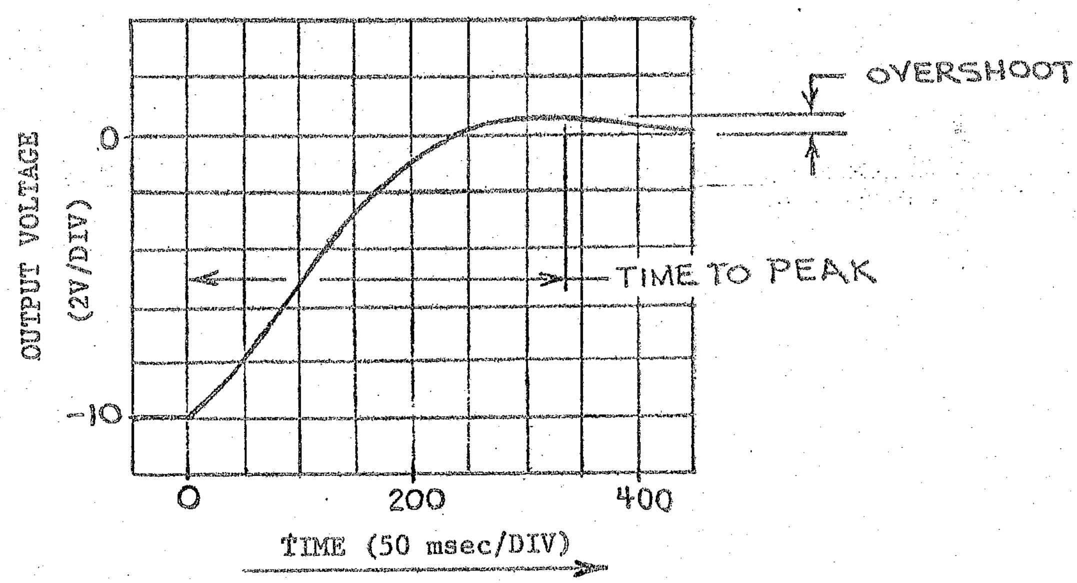
FIG. 11 S/M ACTIVE FILTER OUTPUT VOLTAGE (TP55) TRANSIENT RESPONSE

FOR STEP CHANGE OF INPUT FREQUENCY FROM 60 HZ to 0 HZ



NOTE:

UNDAMPED NATURAL FREQUENCY (ω_0) = 11.6 RAD/SEC

DAMPING RATIO (ζ) = .625

MAX OVERSHOOT %=8.0 $\pm$ 2.0

MAX OUTPUT VOLTAGE = +0.80 $\pm$ 0.20 VDC @ 347 $\pm$ 18 msec

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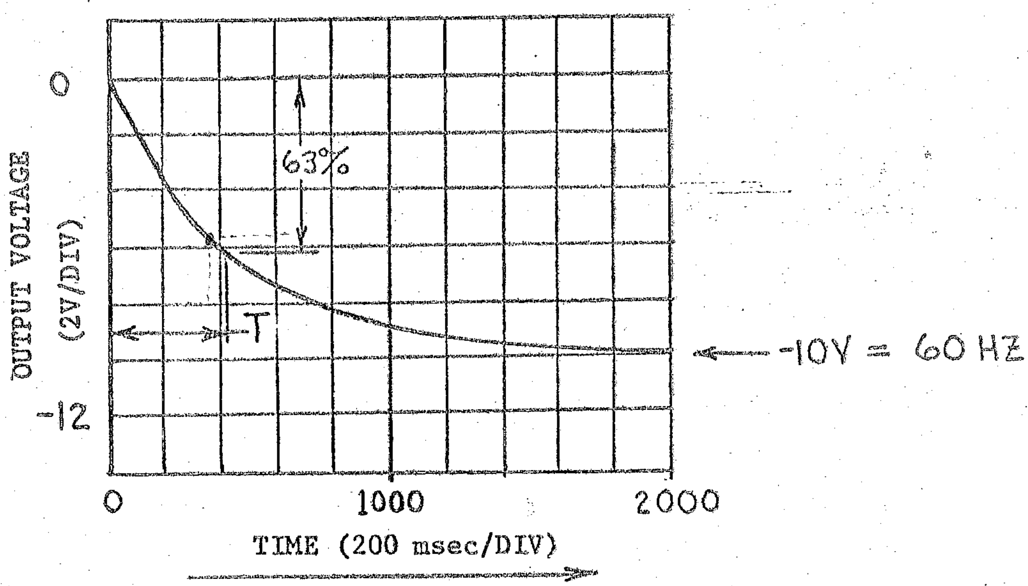
FIG. ___ SPEED MATCHER (60 HZ) OUTPUT VOLTAGE TRANSIENT RESPONSE @ TP2

FOR STEP CHANGE OF INPUT FREQUENCY FROM 0 HZ TO 60 HZ



Note that output @ TP2 changes 63% in 375 ± 45 msec. when Input Frequency is switched from 0 to 60 HZ.

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11. CHECK FREQUENCY COMPENSATION NETWORK

- Check IC1's input noise suppression lag filter specified in section III. A storage scope will be adequate for this check. Note that the output of the filter must be within 63% of the final value in one time constant (1.30 ± .08 usec)

12. CHECK PULSER

- Check Pulse Generator Output Waveform @ TP1 (use a scope to check the square wave ON time and OFF time). The PULSER output waveform must fall within the limits specified in Section III, Part G.

NOTE: Since the pulse ON time is much shorter than the OFF time, it will be necessary to magnify the ON pulse time scale, in order to verify that the waveform is within specification.

2 Stamp bd. before coat.
Test bd. per spec after bd. is coated.
A 48 hr burn in is reqd. Check for output drift.

END OF TEST

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IV. TEST INSTRUCTIONS

Test Instructions prepared by the EHC Test Engineer and approved by EHC Control Engineering.

APPROVED BY [signature] DATE 12/26/72

EHC TEST ENGINEER

PREPARED BY [signature] DATE 12/21/72

EHC CONTROL ENGINEER

APPROVED BY R C Callan DATE 12-27-72

EHC CONTROL ENGINEERING - MANAGER

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