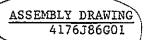
310J79G01 ?/OV SP/SP #2 Bd. 10j79g1 GE20

MARK III PC BOARD TEST

. SHEET 1 of 4



PC BOARD DRAWING

SCHEMATIC DRAWING

TEST KIT PROGRAMMABLE.4176J85 RAMP GENERATOR

1.0	INSPECTION		
	.1 IDENTIFICATION	.3 SOLDER/WIRE	.5 KEY SLOT 7 &
	.2 COMP./ CONN.	.4 TEMP CYCLE	.6
			.7
REN	MARKS: CHANGES PER A.N. 85EC10 R36 WAS 20K	008, J.A.W. 2/26/85 REV. A	
2.0	TEST SET UP		
2.1	Connect +15, -15, +5 VDC :	and common to programmable t	est kit.
2.2	Connect +15, -15 VDC and	common to ramp generator tes	
2.3	Connect up cable #4136J55	to programmable test kit.	
2.4	Connect the TTL output of jack.	a wavetek model 171 freq ge	merator to the SG1
2.5		freq generator to power sup	ply common.
2.6	Connect the ramp generator wavetek.	r BNC cable to the "VCG IN"	terminal of the
2.7	Turn all switches off.		
2.8	Set R15 CW, R35 CCW.		
2.9	Plug board into test kit.		
2.10	Ramp switch to out position	on.	
3.0	INPUT CHECKS		
3.1	Apply +4 VDC to pin 9.		
3.2	TP2 must be approximately	+14.5 VDC.	
3.3	Decrease voltage at pin 9 approximately -13.5 VDC between +1.5 to +1.9 VD	when input voltage is	
3.4	Remove voltage at pin 9.		
J • 4			
4.0	FREQ ADJ		
	FREQ ADJ	IACTIVE FOR 6	

MC DATE 3-30-9

	·
tp1310j79gl G	E20
4.1 Ac	ljust R5 for 0.00 at TP7. Pro 52 15: L1 should be on. L2, L3 should be off. Pin II should be01 to +.01 VDC.
	djust oscillator for 4000 HZ. Turn on S1. djust R8 for +10.000 VDC at TP7.
RIS CW -> L	djust Ri2 for -10.000 VDC at TP3. 1, L2 and L3 must be on. The state of the should be -15 VDC.
Ac Se	et oscillator to 3960 HZ. djust RI5 CCW until Ll just goes out. 41 10 4 et oscillator to 3950 HZ. urn Sl off, then on. Ll must be on. 41 LCW
aj	ncrease oscillator, L1 should go out at pproximately 3960 HZ. ith L1 off, pin 2 should read approximately12 VDC
TI TI	et oscillator to 3970 HZ. P9 will read approximately #14.5 VDC. P9 will switch immediately to approximately -13 VDC fter turning S1 off.
Ti L: Ti Ti	et the oscillator to 2 HZ. urn Sl on. 1, L2 and L3 must be on, (wait several seconds for 2 and L3 to go on). P8 should read approximately +9.4 VDC (unsteady). urn Sl off. L2, and L3 must go out within 1 second. urn Sl on.
Tr	et oscillator to 3564 HZ. urn S2 on, L1 must remain on. in 1 will read -7.06 TO -7.89 VDC ?-9.6 7,54 djust R35 CW until L1 just turns off.
	et oscillator to 4000 HZ.

4.8 Turn Off S2.

Connect -15 VDC to pin Il. TP4 should be +.4 to +.7 VDC. Remove -15 VDC from pin Il.

AC ripple at pin 11 must be less than .02V p-p.

tp1310j79g1 GE20

OVER-SPEED TEST SET-UP 5.0

- Connect up a dual trace scope as follows: 5.1
 - a) Channel I to output I of ramp generator.
 - b) Channel 2 to output 2 of ramp generator.
- Set scope as follows: 5.2
 - Channel 1 --- 5V/DIV, DC mode
 - b) Channel 2 --- 2V/DIV, DC mode
 - c) Chop mode
 - d) Trigger on Channel I
 - e) .1 Sec/DIV
 - f) Scope and level at "+"
 - g) Single sweep
 - h) Store mode
- Switch the wavetek to the dial position, 5.3

RAMP GENERATOR SET-UP 6.0

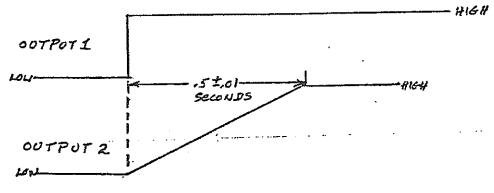
- Ramp switch to out. 6.l
- Adjust Pl for approximately 0 VDC at output 1. 6.2
- Adjust the wavetek for approximately 3600 HZ, 6.3
- Re-adjust Pl for 3600±1 HZ at the wavetek output. 6.4
- 5.5 Ramp switch to in.
- Adjust P2 for 3970±1,HZ. 6.6
- 6.7 Ramp switch to out.
- Erase the scope screen. 6.8
- Set the ramp switch to in. 6.9

Adjust P3 so that output 2 of the ramp generator

goes from low to high in .5 \pm .01 seconds.

Repeat steps 6.7 thru 6.9 until a .5 ± .01 second

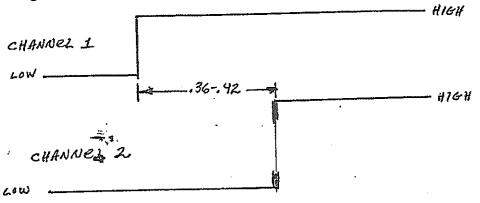
ramp time is obtained. (See Figure 1).



6.10 Set ramp switch to out. 7.0 OVERSPEED TEST

- 7.1 Disconnect channel 2 from output 2.
- 7.2 Connect channel 2 to pin 41.
- 7.3 Erase scope screen. Set scope to 50 millisec/DIV.
- 7.4 Set ramp switch to in.

 The time delay from when channel 1 goes high and channel
 2 goes high must be to .36 to .42 seconds. (See Figure 2).



- 7.5 Disconnect the ramp generator BNC cable from the "VCG IN" terminal.
- 7.6 TEST COMPLETE

2