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| P3K-AL-0559-A01 | TEST INSTRUCTIONS FOR CONTROL VALVE TEST BIAS Circuit ILI-U001 ASSY Drawing 137D6155G1 |
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REVISIONS

## I SCOPE

This instruction outlines the test specifications for circuit board 1L1-U001 (Ref. Drwg 137D6155). System Schematic 137D6131.

## II Circuit Description

The purpose of the CV test Bias circuit is to combine the speed error, load reference, and stage pressure signals and continuously compute a test bias signal which is applied to the CVA to provide a zero transfer error when switching in stage pressure feedback for control valve testing. This test bias signal will cause the CV flow reference signal, $E_L$, to be the same before and after stage pressure feedback is switched in. Subsequent changes in the stage pressure signal due to the tested valve being closed will cause $E_L$ to change and open the appropriate control valves during valve test. The bias signal is removed from the input of the CVA simultaneously with the removal of SPFDBK upon completion of a control valve test (after dropout of 15 secTDDOrelay). The logic circuitry will inhibit the application of the CV Test bias signal when the SPF transfer circuit is in "MANUAL" or Auto mode.

The summing operations are accomplished with an operational amplifier referred to as IC1. The output of IC1 is the input to the sample/hold amplifier IC3. The switching of IC3 from sample to hold is provided by IC2. When pin 17 is grounded IC3 will be in the sample mode. Removing pin 17 from ground will switch IC3 from sample to hold mode.

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273-12
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273-221
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## III. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

1. Power Supply 1: +22.000±0.002 VDC (Pin 37) at 275 MA (Approx.)

2. Power Supply 2: -22.000±0.002 VDC (Pin 41)

B. Operating Signal Levels

1. Input 1 (Speed Error Signal): ±10.000 VDC (Pin 9 & 10) (0 volts at speed, 1 volt % speed error)

2. Input 2: (stage pressure signal): 0 to +10.000 VDC (Pin 12) 0 volts at 0 pressure +10 volts at rated pressure

3. Input 3 (Load Reference Signal): 0 to -10 VDC (Pin 11) (0 volts at no load, -10 volts at full load)

C. Output Loads

1. Load 1: 133K Ohm±1% (Max. load) (Pin 34)

2. Load 2: 500K±1% VC (Std) (Pin 32)

3. Load 3: 500K±1% VC(Std) (Pin 33)

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D. Offset Adjustment Procedure for IC3

1. Zero ICI by grounding all inputs. Adjust VR51 for zero at TP8.
   Jumper 10, 11, 12 to ground.
2. The offset adjust pot VR50 should be adjusted with zero at TP8. During the adjustment, the sample/hold should be switching continously between the sample and hold mode. This can be accomplished by switching pin 17 to pin 16 (open & closed). The error at TP9 should then be adjusted to zero with pin 17 open and IC3 in the hold mode. In this way, charge offset as well as amplifier offset will be adjusted.

E. Voltage divider network for Speed Error signal TP4
(VR3, VR2, ~~R7~~, VR1 Max CW), ~~R5~~, ~~R6~~). Voltage at Pin 9 set to +10.000 VDC
Remove Pins 10, 11, 12 From Ground. RW

| VR3 Position | VR2 Position | Voltage at TP5 |
|---|---|---|
| CCW | CW | 10.000 VDC |
| CW | CW | ~~4.228 ± 0.235 VDC~~ 2.941 ± .125 VDC |
| CW | CCW | ~~2.941 ± 0.125 VDC~~ 4.228 ± .235 VDC |

Remove 10 vdc from Pin 9.!

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III. CIRCUIT SPECIFICATIONS (continued)

F. Individual Stage Performance Specifications

1. Power Supply (CR1, 2, 3 & 4)
   a. TP1: +15.7 ± 1.0 VDC
   b. TP2: -15.7 ± 1.0 VDC

2. Amplifier (IC1)
   a. Acceptable Offset at TP8 (zero input): ±1.0 mv DC
   b. Transfer Function for Speed Error (VR1, R5, C6, R6, R15, TP8, TP5)

$$\frac{\text{output} \rightarrow \text{TP8}}{\text{input} \rightarrow \text{TP5}} = \frac{-G1}{1 + T_1 \cdot S}$$

VR1 Full CW

Where: Gain ($G_1$) = -4.616 ± 0.092 volts/volt
Noise Suppression Lag Time Constant (T1) = 1.40 ± 0.15 msec.
Noise Suppression Breakpoint (F1) = 115.3 ± 12.7 HZ

VR1 full CCW

Where: Gain ($G_1$) -3.337 ± 0.150 volts/volt
Noise Suppression lag time constant ($T_1$) = 1.93 ± 0.25 msec
Noise Suppression breakpoint ($F_1$) = 83.8 ± 10.7HZ

VRI Mid-position (normal gain)

Set Where: Gain ($G_1$) -4.0008 ± 0.080 volts/volt
Noise Suppression lag time constant ($T_1$) = 1.65 ± .18 msec
Noise Suppression breakpoint ($F_1$) = 97.6 ± 10.7 HZ

III. CIRCUIT SPECIFICATIONS

F. Individual Stage Performance Specifications (continued)

c. Transfer Function for Load Reference Signal (VR4, R3, C5, R4, R15, TP6, TP8)

$$\frac{\text{output } TP\ 8}{\text{input } TP\ 6} = \frac{-G2}{1 + T_2 \cdot S}$$

VR4 Full CW

Where: Gain ($G_2$) = -1.081 ± 0.022 Volts/Volt
Noise Suppression Lag Time Constant ($T_2$) = 0.99 ± 0.11 msec
Noise Suppression Breakpoint ($F_2$) = 162.4 ± 17.8 HZ

VR4 Full CCW

Where: Gain (G2) -0.917 ± 0.031 Volts/Volt
Noise suppression lag time constant ($T_2$) = 2.38 ± 0.37 msec
Noise suppression breakpoint ($F_2$) = 68.6 ± 10.5 HZ

VR4 Mid-position (Nominal Gain)

set

Where: Gain ($G_2$) = -1.002 ± 0.020 Volts/Volt
Noise Suppression lag time constant ($T_2$) = 1.67 ± 0.18 msec
Noise Suppression breakpoint ($F_2$) = 96.6 ± 10.6 HZ

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III. CIRCUIT SPECIFICATIONS

F. Individual Stage Performance Specifications (continued)

2. (Continued)

d. Transfer Function for Stage Pressure Feedback Signal (VR5, R8, C7, R9, R15, TP7, TP8)

RW output input

$$\frac{TP8}{TP7} = \frac{-G3}{1 + T3 \cdot S}$$

VR5 Full CW

Where: Gain ($G_3$) = -1.081 ± 0.022 Volts/Volt
Noise Suppression Lag Time Constant ($T_3$) = 0.99 ± 0.11 msec
Noise Suppression Breakpoint ($F_3$) = 162.4 ± 17.8 HZ

VR5 Full CCW

Where: Gain (G3) = 0.917 ± 0.031 Volts/Volt
Noise suppression lag time constant ($T_3$) = 2.38 ± 0.37 msec
Noise suppression breakpoint ($F_3$) = 68.6 ± 10.5 HZ

VR5 Mid-position (normal gain)

vet

Where: Gain (G3) = -1.002 ± 0.020 volts/volt
Noise Suppression lag time constant (T3) = 1.67 ± 0.18 msec
Noise Suppression breakpoint (F3) = 96.6 ± 10.6 HZ

Saturation limits (TP8)
13 VDC Minimum

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## IV. SET POINTS

Adjustments of the following potentiometers should be done as outlined below. This procedure is mandatory for all customer spares or R&R circuit boards. Note that zero input signals should be set with a low output impedance power supply or operational amplifier. Input signals connected to signal ground is also acceptable. All other inputs should be zero, except where noted below. Ground Pin 17 NB

### A. Adjustment of VR1, VR2 and VR3 (10 turn Dial) and VR4

These potentiometers are used to establish the CV regulation limits for the speed error signal. CV Regulation design range is 2.5% to 7.5% inclusive. The IEEE spec. range is 2.5% - 7%.

#### A.1 7.5% CV Regulation

Gnd Pin 17

1. Set VR3 full CW and apply $V_1$ (P1) = +7.50 VDC to Pin 9 (TP4). (TP4) .759 ✓
2. Adjust VR2 for +2.50 volts at TP5. Adjust VR1 for -10.000 VDC at TP9.
3. Apply a -10.000 VDC (P52) to pin 11 (TP6) and trim VR4 for zero volts at TP9.
4. Record VR3 dial setting and voltage at TP5.
5. Adjust voltage at pin 11 to zero (TP6 at 0V remove TP6 input). Voltage at TP9 should read - 10.000 VDC

#### A.2 2.5% Regulation

Gnd Pin 17. Remove -10V from Pin 11.

1. Set VR3 full CCW and apply a $V_1$ = +2.50 VDC to Pin 9 (TP4).
2. Check that voltage at TP5 = +2.50 VDC. If not adjust input voltage at pin 9 for +2.50VDC at TP5. TP9 should read -10.000 VDC. Voltage at pin 9 should be within ± 0.100 VDC of TP5 voltage.
3. Apply -10.000 VDC to pin 11 (TP6). TP9 should = 0.00 VDC
4. Record VR3 dial setting and voltage at TP5.
5. Adjust voltage at pin 11 to zero. Voltage at TP9 should read -10.000VDC

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IV. SET POINTS (continued)

A.3 5% Regulation (Final setting all boards)

1. Apply +5.00 VDC to pin 10 (TP4). Adjust VR3 for +2.50 VDC at TP5. TP9 should read -10.000 VDC.
2. Apply a -10.000 VDC to pin 11 (TP6). Voltage at TP9 should = 0.00 VDC.
3. Record VR3 dial setting and voltage at TP5.
4. Set speed error signal at pin 10 (TP4) to zero.

Adjustment of VR5

This potentiometer sets the SPF gain and is adjusted as follows:

1. From above, apply -10.000 VDC to pin 11 (TP6).
2. Apply a +10.000 VDC to pin 12 (SPF signal). TP7
3. Adjust VR5 for zero volts at TP9.

B. Check Operation of IC3 (sample Mode)

1. Set -10.000 VDC at pin 11 (TP6) and +10.000 VDC at pin 12 (TP7).
2. Decrease voltage at pin 12 to zero (in steps of 1.0 VDC) and note that voltage at TP9 increases from 0 to +10.000 VDC.
3. Reset voltage at pin 12 to +10.000 VDC
4. Decrease voltage at pin 11 to zero (in steps of 1.0 VDC) and note that voltage at TP9 decreases from 0 to -10.000 VDC.
5. Reset voltage at pin 11 to -10.000 VDC. TP9 should = 0.00 VDC.

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B.1 Check Operation of IC3 (Hold Mode) -10.0 at Pin 11 TP6

1. Set voltage at pin 12 (TP7) to +8.00 VDC. Output at TP9 =+2.00 VDC.
2. Remove ground from pin 17 (HOLD). Note that voltage at TP9 = +2.00 VDC
3. Decrease voltage at pin 12 (TP7) toward zero and note that TP9 voltage remains at +2.00 VDC (HOLD)
4. Decrease voltage at pin 11 (TP6) toward zero and note that TP9 voltage remains at +2.00 VDC (HOLD)
   Remove TP6 voltage
5. Ground pin 17. (SAMPLE)
6. Note that output at TP9 is zero volts.

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TEST INSTRUCTIONS FOR CONTROL VALVE TEST BIAS CIRCUIT 1L1-U001 Assembly Dwg. 137D6155 G1

FIRST MADE FOR EHC Mark II LCU X781/X623

REVISIONS

PREPARED BY: J. Dombrosky DATE 5-19-77

J. Dombrosky
EHC DESIGN ENGINEERING

APPROVED BY: PC Callan DATE 5-24-77

PC Callan
EHC DESIGN ENGINEERING

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