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HMP K up use B Memory
HMP J Down use A Memory

1. Turn on the PRO 350 (on-off sw. in upper left corner, on=i, off=o)
   The computer should be left 'ON' at all times.
   The PRO 350 does a hardware check, then loads operating system,
   this takes approx. 1 minute.
   The MAIN menu is now displayed, move the cursor to DMC COMMUNICATOR 1
   and hit RETURN or DO. The HELP menu is now displayed and a message
   "DMCTASK RUNNING" and the TIME.
   Push PF1 key to set baud rate to 1200.
   Push F12 key to clear screen.

2. Set berg jumpers per elementary.
   Connect power to unit under test.
   Connect CRT to PLC/DMC card RS-232 Conn.(a null modem is required
   between ribbon cable and processor board.)

3. Apply power -- Check Power up routine (TEST SOFTWARE NOT LOADED YET)

PLC_	DMC_
DMC SELF TEST	DMC SELF TEST
PROM CSUM -- OK	PROM CSUM -- OK
BASE RAM -- OK	BASE RAM -- OK
<INITIALIZED>	<INITIALIZED>
SYSTEM RAM - OK	SYSTEM RAM - OK
APP CSUM - NEW	APP CSUM - NEW
SELF TEST DONE	SELF TEST DONE

4. Hit RETURN until the following is displayed:
   DMC MONITOR
   Rev. 3.16 4/07/87 (Rev. and/or date may differ)
   Sys ID = Default
   *>
   Enter password (P) GE2
   If PLC/DMC bottom LED (TEST) is on, turn controller off, as follows:
   For PLC, type (O) then (C) then (Y) then (Q).
   For DMC, type (O) then (C) then (OFF) then (Q).

5. Check Memory map (B) then (T) then RETURN
   Refer to Local Controller memory map master & elementary
   to determine & verify memory map.
   example:
   00000 = RAM
   02000 = NONE
   04000 = RAM (RAMA)
   0C000 = NONE
   20000 = EEPROM (EEPA)
   28000 = NONE
   8E000 = RAM (HRMB)
   90000 = NONE
   F8000 = PROM (PLC/DMC)
   COMMAND COMPLETE

   00000 = Ram
   02000 = NONE
   20000 = EEPROM
   28000 = NONE
   F0000 = Prom
   8E000 = RAM
   90000 = NONE

   Type Q to exit the B mode or any of the other modes.

   Notes: RAMA, EEPA, & PLC/DMC are on 'L' bus.
   HRMB is mapped into the memory using 'E' bus.
   This requires a ribbon cable between PLC/DMC AND HRMB.
   This cable sometimes gives us problems.
   If the HRMB does not map check that pin 37 is tied to common.

6. To load users program from PRO 350 HARD DISK
Push F17 key to clear screen.
Push HELP key.
Push PF4 key to set baud rate to 9600.
Push F17 key to clear screen.
Push HELP key.
Reset the processor board (temporarily jumper TP1 to TP2)
Push F19 key to start loading procedure.
When "Transmit File To DMC" menu comes up, type DMC, PLC or CSF (whichever is wanted) after FILENAME then push RETURN.
After a few seconds observe the counter on screen counting up, after load is complete, counter will stop and FILE CLOSED, LAST WRITE QSTAT ()=1 1, VAX NO ERRORS, SYSTEM RESTART, and another SELF TEST will be displayed.
Hit RETURN until prompt *> is displayed.
NOTE:
To determine if memory board is loaded with software for a DMCA or PLC_ hitting the RETURN key after self test will display one of the following messages on CRT preceeding the *>. (REV. NUMBER AND DATE MAY CHANGE)

DMCA
DMC Monitor
Rev. 3.4 4/21/85
Sys ID = Version_0

PLC_
DMC Monitor
Rev. 2.7 4/20/85
Sys ID = Version_0

If Sys ID = Default, the test program was not loaded, need to re-load.
Enter new password (P) PS2
Turn controller on, as follows:
For PLC, type (O) then (C) then (Y) then (Q).
For DMC, type (O) then (C) then (ON) then (Q).
If job has PCLA turn I/O channels 2 and 3 on.
If job has HXCA turn I/O channel 16 on.
To turn channels on or off, type O then ONLINE STAT O> will be displayed, type 1 then channel ? will be displayed, type the channel number desired, then RETURN then chan. status is given then MODIFY ? will be displayed, answer Y to change or N not to change.

NOTE: If loading procedure is aborted, push EXIT key, power down UUT, select DMC COMMUNICATOR 1, then F17, then HELP, then power up UUT, then F19 to go through loading procedure again. If system locks up, do a CONTROL C to get back to MAIN menu and start over again.

Example to Display Channel I/O status

```
>enter (O) return
O> enter (O) return
CONTROLLER = ON
OUTPUT     = ON
INITIAL    = ON
MMHA       = ON
BEP_SEG    = ON
CO_PRO     = ON
HXCA       = ON
MONITOR    = ON
CHANNEL 02 = ON
CHANNEL 03 = ON
CHANNEL 0F = ON
CHANNEL 16 = ON
O>
```

14. Test of 8087/80287 co-processor on PLC_/DMC_ daughter board.
Call user program and select CO_P test. Controller must be on.
This routine will exercise the co-processor to perform some arithmetic functions.

15. Test of PCLA (HMHA base board) (Control Party Line (CPL) master)
Perform test only if UUT contains PCLA
Put J15 and J16 in 'OUT' position.
Call user program and select PCLA.
Conn. Chan A of PCLA to PAAA(HSHA) slot 1A of MEM Local Controller I/O test module and Chan B of PCLA to PAAA slot 1D of MEM Local Controller I/O test module.
Controller must be on as well as channel 2 & 3.
The test is go/no go type.
NOTE: Set the WAIT times for DMCA to 20 and DMCC to 40 as follows:
Type M for 'MODIFY' mode, then another M for modify?, then type WAIT, the present WAIT time will be displayed, then value, type in the desired value.
It is best to set CPL scan time to 0 ms when doing the PCLA test from the user monitor. (Call S then M then CPL then 0)

16. Test of PXCA (HXCA base board) (C bus master)
Perform test only if UUT contains HXCA

NOTE : HXCA MUST BE STRAPPED FOR ADDRESS 6000 TO PERFORM TEST . AFTER TESTING HXCA , RE-ADDRESS PER ELEMENTARY .

J2	J3	J4	J5	J6	
.	.	.	.	.	T
.	|	|	.	.	
|	.	.	|	|	F
F	E	D	C	B	

Call user program and select HXCA
Conn. ribbon cable from HXCA JA UUT to HXRA JA in SEM Local Controller 'C' bus test module.
The test is go/no go type.

NOTE : CHANNEL 16 MUST BE ON . CHECK THAT PIN 4 ON THE HXCA GOES TO PIN 4 OF THE PROCESSOR CARD .

HTM setup to output to DMC

	Outut data switches															
Select STA-5, Page-off	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
group-desired group per chart	1	1	1	1	1	0	1	0	1	1	0	0	1	1	1	0
HEX EQUALS		F				A				C				E		

Input/output mode-simulate, test control mode-repeat, select-output page-off.

When ready to input to DMC, push test on the HTM to input a single input to DMC. Each time test is pushed (if in 'single' mode) the bottom red LED on the HLSC card in the slave module should blink. If in the 'repeat' mode the input will cycle from the HTM automatically over and over and the bottom LED on the HLSC card will follow this cycle.

At the terminal:	
> Enter B for breakpoint	CRT responds B>
Enter B for base	CRT responds base?
Enter 8E00 RETURN	CRT responds >
Enter D for display	CRT responds offset?
Enter the offset from chart, RETURN	CRT responds length?
Enter 256, RETURN	CRT responds format (W,A,B)?
Enter W for word	CRT displays no. bytes selected

When you answer length?, the first group shown should read FACE, the value input to DMC from HTM. Any lines of memory locations containing all zeros will be replaced by an * on the CRT.

HTM setup to input to HTM

Input/output mode-simulate, test control-repeat, select-input, page-off group-desired group per chart.

At the terminal:	
Enter RETURN then Q	CRT responds >
Enter B for breakpoint	CRT responds B>
Enter M for modify	CRT responds offset?
Enter offset from chart	CRT responds 8E00:(offset no.)=XX
	XX = low order byte sent from HTM

Enter two digits (one byte) HEX value to be sent to HTM, when RETURN is pushed this value should be output from DMC to the HTM and XX HEX should be displayed on 'data and address display' on HTM as low order byte. Do a RETURN and enter a second entry, this will then appear as the high order byte on the HTM. Data bytes are in memory in the following order.

Low order byte	High order byte
1100 1110	1111 1010
C E	F A

LEDs on HTM

FEDC BA98 7654 3210
1111 1111 1111 1111 = FFFF HEX

10. To test DMC I/O
    Locate the proper test instructions per table of contents.

11. To test Stick I/O
    Call user program & connect Unit Under Test(UUT) connectors to MEM DMC I/O test module JHB(34 pin) & JJB(26 pin) with ribbon cables.
    HPBC on UUT must be in decode mode
    Select card type to be tested HLIA,HLOA,NDAC,& NADA
    UUT 34 Pin connector should have pins 2,4,6,8,10,12,16,18,20 & 27 tied together and to DCOM.
    UUT 26 pin connector should have pins 2,4,6,8,12,19,21,23 & 25 tied together and to DCOM.

12. To test Local I/O
    Call user program & connect UUT connectors to MEM DMC I/O test module JKA(34 pin) & JCA(26 pin) with ribbon cables.
    HPBC on UUT must be in buffer mode
    Select card type to be tested HLIA,HLOA,NDAC,& NADA
    UUT 34 pin connector should have pins 1,2,3,5,7,9,11,13,15,17,19, 21,23,25,27,29,31 & 34 tied together and to DCOM.
    UUT 26 pin connector should have pins 1,2,3,5,7,9,11,13,15,17 & tied together & to DCOM.

13. Test of HRMB/HPBC shared memory between DMC module and Control Signal Highway (CSH).
    Connect Highway Test Module (HTM) to CSH slave module (TM2 modified)
    HTM Transmit to CSH slave HXLA JT1 (4th from top)
    HTM Receive to CSH slave HXLA JT0 (top)
    Connect maintenance cable from HTM to slave.
    Connect CSH slave connectors JF & JJ to UUT HPBC/D connectors with ribbon cables.
    Connect cable from E-bus connector on processor board to connector on HRMB (This must be done to map the RAM on HRMB board)
    HPBC input lines must be terminated with NTEA card.
    Be sure enable switch on HPBC/D is enabled.
    Be sure 48 pin ribbon cable is connected between the HLSC card and HLSD card on the CSH module.
    This test will verify E bus & CSH can read and write to HRMB 256 bytes of memory. (or whatever length you enter)
    UUT 34 pin connector should have pins 1,2,3,5,7,9,11,13,15,17,19,21, 23,25,27,29,31 & 34 tied together and to DCOM.
    UUT 26 pin connector should have pins 1,2,3,5,7,9,11,13,15 & 17 tied together and to DCOM.

E BUS BASE	ADDRESS OFFSET		HTM GROUP	HPBD GROUP
8E00	0000	--	00	0-1
	0002	--	01	0-1
	0004	--	02	0-1
	0008	--	04	0-1
	0010	--	08	0-1
	0020	--	10	0-1
	0040	--	20	2-3
	0080	--	40	4-5
	00F0	--	78	6-7
	00FE	--	7F	6-7

8. Save program on EEPROM (EEPA) or (other memory board)

```
>enter (X) return
XFER SYSTEM
X> enter (S) return
SAVE EE PROM
BASE SYSTEM ? enter (Y) return      (Y=yes N=no)
--- WORKING ---
COMMAND COMPLETE
X>
```

Repeat this procedure a second time it should only take a second if the original save was good. The program only writes to EEPROM locations that do not match RAM.

9. Verify system loads from EEPA on power up
Turn power off and back on
CRT should be as follows: (TEST SOFTWARE NOW LOADED)

PLC_

```
DMC SELF TEST
PROM CSUM -- OK
BASE RAM  -- OK
<RESTORED>
SYSTEM RAM - OK
APP CSUM   - OK
SELF TEST DONE
```

DMC_

```
SELF TEST DONE
```

CSF

```
DMC SELF TEST
PROM CSUM -- OK
BASE RAM  -- OK
8087 CHECK - OK
SYSTEM RAM - OK
APP CSUM  -- OK
CSF INIT  -- OK
SELF TEST DONE
```

Hit RETURN until CRT displays this type message:
(This is a general example, REV. and date may change)

```
DMC MONITOR
REV. 2.8  7/16/86
SYS ID = VERSION_0
*>
```

7. Test all cards containing EEPROM.
Be sure controller is turned on.
>enter (U) return (select user prog. which has OC tests)
Select EEPA test from menu
The starting address must be entered(The MSB is the segment)
The CBL block multiplies the address entered by 16 to get the total address segment & base. EX: You enter 2000 which is segment 2, base 0000. The amount of memory to be tested is the second entry.
Each segment may consist of up to 64K of memory.
See HUMA/HUMB/HUMC section of test instructions for addition info. on berg settings and special memory map situations.
The following map is for a 32K EEPA card which is a HUMA using 2K x 8 EEPROM chips.

	QUAD "A"	QUAD "B"	QUAD "C"	QUAD "D"
START ADDRESS	2000	2200	2400	2600
MEM TO BE TESTED	1FFF	1FFF	1FFF	1FFF
CHIP 1 Even Add	2000 U23 0FFE	2200 U27 0FFE	2400 U31 0FFE	2600 U35 0FFE
CHIP 2 Odd Add	2000 U25 0FFF	2200 U29 0FFF	2400 U33 0FFF	2600 U37 0FFF
CHIP 3 Even Add	2100 U24 0FFE	2300 U28 0FFE	2500 U32 0FFE	2700 U36 0FFE
CHIP 4 Odd Add	2100 U26 0FFF	2300 U30 0FFF	2500 U34 0FFF	2700 U38 0FFF

The following example map is for a 64K X 8 EEPROM MMAB memory board which is a HUMA board with 8K X 8 RAM chips in quads A & B and 8K X 8 EEPROM chips in quads C & D.

	QUAD "A"	QUAD "B"	QUAD "C"	QUAD "D"
START ADDRESS			2000	2800
MEM TO BE TESTED			3FFF	3FFF
CHIP 1 Even Add	DO A MEMORY MAP ONLY FOR QUADS A, AND B		2000 U31 3FFE	2800 U35 3FFE
CHIP 2 Odd Add			2000 U33 3FFF	2800 U37 3FFF
START ADDRESS			2400	2C00
MEM TO BE TESTED			3FFF	3FFF
CHIP 3 Even Add			2400 U32 3FFE	2C00 U36 3FFE
CHIP 4 Odd Add			2400 U34 3FFF	2C00 U38 3FFF

Other starting addresses may apply, but only 16K (3FFF) should be tested at a time to speed up the isolation of a bad chip. Other boards may have EEPROM in different quads, but same procedure should be used.

17. Test of HXMA (Local Controller/Series 6 shared memory 32 bytes)
HXMA contains 2-- 32 x 8 memories
The memory is accessed by L bus I/O from the Local Controller and F bus from the HXRA/DXRA (series 6 interface).
L bus Inputs & F bus outputs access one 32 x 8 memory and
L bus outputs & F bus inputs access the other 32 x 8 memory.

Connect twisted ribbon cable between HXRA(JA) & DS3815PXCA(HXCA & prom)
If UUT is a DMC,a PXCA can be borrowed and temporarily inserted in any 'L' bus slot.(Pin 4 of PXCA slot must be wired to PLC_ pin 4 to allow PXCA to work correctly(a temporary jumper may be added).
NOTE: Channel 16 & controller must be on for this test.
C_BUS scan set to 100ms
Switch on HXRA must be in the active position.
HXMA F-BUS starting address must be F-F for proper operation of the communication. (FAB-5=F FAB-6=F)
Bottom light on HXRA must be blinking to indicate proper C_bus communication.
Enter (U) on keyboard & Select HL0A test from menu.
Enter adderess 8000 .
Select display test (D).
Enter 1010101010101010 , Return .
Enter (N) return to exit without clearing data .
Enter EX, return(to exit user monitor program)
Select Display 'D' mode. CRT responds 'DISPLAY?'
Enter IX01,return CRT should read HLIA =-21846.
Enter (M) for modify , CRT reads 'MODIFY ?'
Enter OX01 , CRT reads VALUE ? Enter 21845 , Return .
CRT reads D > , Enter (Q) to exit .
Enter (U) to select users program .
Select HL0A test , address 8000 .
Select display test (D). Enter (0),return (An output is done prior to an input to freeze the data for the input(read) function.
Select HLIA test , address 8000 .
Data should read 0101010101010101 .
Exit program , select HL0A test
and repeat above procedure for the following addresses .

NOTE : Address 8000 thur 803C are examples only , if HXMA is addressed for 8000 , the address's are valid . Refer to elementary for correct address .

	(D) DISPLAY	(M) MODIFY
8000	IX01	0X01
8004	IX02	0X02
8008	IX03	0X03
800C	IX04	0X04
8010	IX05	0X05
8014	IX06	0X06
8018	IX07	0X07
801C	IX08	0X08
8020	IX09	0X09
8024	IX10	0X10
8028	IX11	0X11
802C	IX12	0X12
8030	IX13	0X13
8034	IX14	0X14
8038	IX15	0X15
803C	IX16	0X16

C. NDAC--NADA
Connect special test harness from NDAC to NADA. Select USER MONITOR (U). Select NDAC test and set the four outputs for a voltage. (+/- 10 volts) When exiting use N RETURN, this saves the NDAC outputs. A normal exit would reset them to 0 volts. Select and run NADA test and check that voltages read compare with those output from NDAC.

D. Special 'F' bus test for HDRA, HEXA, LOOP:
HDRA test can be used to test any input/output addresses. If two cards in question can be connected together this is a very useful test. Ripple or display test can be used.

HEXA test is an output test where the output is entered in HEX format rather than binary. This test is useful in testing display driver cards.

LOOP test is used primarily by final test to input a signal on one channel and display that value on an output channel. Useful when testing in panels.

38. HAFA test
The HAFA card contains 16 digital inputs(backplane) & 16 digital inputs(JB CONN),and 8 digital outputs on the backplane.It also has 16 analog inputs connected to a mux which typically is controlled by HAIA/C card types.

DIGITAL INPUTS:
Refer to elementary for address of HAFA and use desired suffix from chart below.

	MSB							LSB
Base address	PA29	PA28	PA27	PA25	PA24	PA23	PA22	PA21
Base + 2H	PA49	PA48	PA47	PA46	PA41	PA39	PA32	PA30
Base + 4H	JB8	JB6	JB4	JB3	JB5	JB7	JB10	JB9
Base + 6H	JB15	JB17	JB19	JB20	JB18	JB16	JB13	JB14
Base + 8H	PA53	PA55	PA57	PA59	PA62	PA69	PA71	PA80

Note JB2=Com.

Use HLIA test from User Monitor and base address of HAFA + 4H,the 16 bits displayed represent JB15(MSB) thru JB9(LSB).To test the Digital section ,walk a "0" thru the 16 bits by jumpering Dcom (JB2) to each input pin on JB as shown on chart,observe appropiate bit goes low after jumper is installed and keyboard RETURN is done.

DIGITAL OUTPUTS:
Use 'L'Bus user monitor test and base address + 8H

OUTPUT CODE	BASE ADD. PLUS 8H

Ex. 0;X X C D , X X X X
Type in desired output value;low byte of output code=digital output value.

B. If card is not directly on 'F' bus ie: connected to DMC via 'C' bus or 'CPL' link the following technique can be used. The output can be controlled using the modify 'M' command to the address of the output to be monitored.
.06000B or .06000C for output #1
.06002B or .06002C for output #2
.06004B or .06004C for output #3
.06006B or .06006C for output #4

The following applies to NDAC and to NDAD when J1A and J1B are set to the bipolar position on NDAD. The B format will modify the returned word in HEX and the C format will modify it as a number. The format of the output word is as follows:

```
                    F|E D C  B A 9 8  7 6 5 4 |3 2 1 0
                    X|X X X  X X X X  X X X X |X X X X
          Sign bit|                            |  Bits 0-3
                  |                            |  not used
```

Each bit is equal to 4.885 mv
To set the desired output modify the 'C' or 'B' format as follows:

Output voltage desired	'C' value to be output	'B' value to be output
0	0	0000
1	3278	0CD0
-1	-3278	F330
2.5	8196	2000
-2.5	-8196	E000
5.0	16392	4000
-5.0	-16392	C000
7.5	24590	6000
-7.5	-25590	A000
9.9951	32764	7FF0
-10	-32768	8000

The format of the output word for NDAD for circuit #1 in unipolar mode is as follows:

```
                  F E D C  B A 9 8  7 6 5 4 |3 2 1 0
                  X X X X  X X X X  X X X X |X X X X
                                            |  Bits 0 - 3
                                            |  not used
```

Each bit is equal to 2.44 mv
To set the desired output modify the 'C' or 'B' format as follows:

Output voltage desired	'C' value to be output	'B' value to be output
0	0	0000
1	6570	19B0
2.5	16400	4010
5.0	32800	8020
7.5	49200	C020
9.9	65535	FFF0

35. LCFBUS TESTABLE OUTPUT CARDS

HLOA--5VDC 16 bit non-isolated
HLOB--5VDC 8 bit non-isolated
HLOC--5VDC 16 bit non-isolated
HRRB--8 bit normally open reed relay isolated
HSDD--8 bit fused solenoid driver isolated
NDAC/D--digital to analog, 4 channels +/- 10 volts

HLOA, HLOB, HLOC, HRRB, HSDD HLOC ouput's Inverted
ENSURE IF NOT RUNNING HSDD THAT HSDD SWITCH IS IN OPEN POSS.

A. Select USER MONITOR (U). Use HLOA for any 16 bit card. Use HRRB for 8 bit card. Run ripple test or display test and check that LEDs correspond to data being input.

B. If two 8 bit cards are addressed to a word (16 bit), one low byte and one high byte, use the HLOA test.

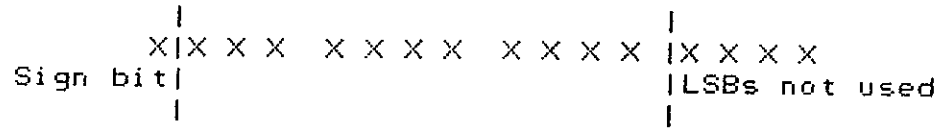
C. If the module being tested has an HLOA (output) and an HLIA (input) connect the test harness between HLIA JA and HLOA JA. Select USER MONITOR HDRA test. Enter HLOA address for output address and HLIA address for input address. Ripple or display test can be used to test both cards simultaneously.

D. If the card is not directly on the 'F' bus ie: connected to DMC via 'C' or 'CPL' link the following technique can be used. The output can be controlled using the modify 'M' command to the address of the output to be monitored.
Example: Modify HLOA output addressed at 6000 on 'C' bus.
Do modify .06000B (B calls for HEX format)
Input desired output A261 (1010 0010 0110 0001)

36. HSDD test----------
Use HRRB test. NOTE: ~~Pin 18 on the HSDD should be tied to pin 56 on the processor board.~~ CHANGE HSDD SWITCH ON TOP OF UNIT TO CLOSE POS.

37. NDAC/D----------
A. Select USER MONITOR (U) Select NDAC test. Connect voltmeter to first circuit and output voltage (Range +/- 10 volts) Voltmeter should read the output voltage. Repeat at different voltages and for all 4 circuits.
TP1--COM--JA4
TP2--CKT#1--JA3
TP3--CKT#2--JA5-(JA8 COM)
TP4--CKT#3--JA7-(JA8 COM)
TP5--CKT#4--JA9-(JA10 COM)
When using the NDAD in the unipolar mode, (J1A and J1B = +) only the operation of circuit #1 is affected. Using the NDAC test, when you ask for X number of volts out you will get one half of that value on circuit #1. Circuits #2-4 still produce a 1 to 1 ratio.

C. If card is not directly on 'F' bus ie: connected to DMC via 'C' bus or 'CPL' link, the following technique can be used. The output can be displayed using the display 'D' command. The format of the output is as follows:



Using the C (counts) mode for display, the conversion to volts can be made as follows:

$$\text{Input volts} = \frac{\text{Counts displayed}}{16} * .00488 \text{ volts} * \frac{1}{.8}$$

The division by 16 is to account for the 4 LSBs not being used in the returned word format. The .8 factor is to account for the gain of .8 from input to A/D converter on the card.

Example: NADA card on 'C' bus with starting address at 6000.
Use display 'D' of .I6000C and get 16393 (0100 0000 1001 0000)
Convert to volts as follows:

$$\text{Input volts} = \frac{16393}{16} * .00488 * \frac{1}{.8} = 1024.5 * .00488 * 1.25 = 6.249V$$

If card is NADB the above information applies to the +/- 12.5 volts jumper setting. If the jumper is set for +/- 10 volts operation, the .00488 number changes to .0039.

34. HDRA/C ----------

A. R-bus test: Connect a ribbon cable from HDRA JA to HDRA JB
Select USER MONITOR (U) and HDRA test. Enter HDRA address for input and output address. Ripple or display test can be run, then verify correct inputs and outputs.

B. Manual mode test: Place a 'TEST' HDRA card in slot 1G of 'TEST MEM' with J1 set to the 'R' position and J2 to the 'RW' position. Connect a 34 pin cable from JA of 'TEST' HDRA to JB of HDRA in UUT. Call up HLOA test from USER MONITOR at address 4010 and do the display test, set in different bit patterns to exercise the HDRA outputs.

The following table shows bit position to output pin relationship and input to output relationship.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
57	58	59	60	53	54	55	56	48	47	50	52	76	74	72	70	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 1 HDRA output
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 0 HDRA output

The output pins may be looked at with DVM or if HDRA outputs drive into logic circuits the inputs to HDRA may be changed to set up permissives for the logic circuits.

HLIA, HLIC, HSCA, HSCB, HSCC, HSCD, HSCE, HSCH

A. Select USER MONITOR (U) and HLIA test. Connect the input test box to card under test. Apply the appropriate signal for the card under test to the test box. (Refer to card backsheets and module wiring to provide proper test signal inputs to card) Open and close switches on test box and verify CRT readout tracks the changes. For 8 bit cards use the LSBs on the HLIA display. The MSBs should be '0' if no other card is connected to that address.

B. If UUT has HLIA and HLOA, connect the special test harness between HLIA-JA and HLOA-JA. Select USER MONITOR (U) and HDRA test. Enter HLOA address for output address and HLIA address for input address. Use ripple or display to test both cards at the same time.

C. If card is not directly on 'F' bus ie: connected to DMC via 'C' bus or 'CPL' link the following technique can be used. The input can be displayed by using the display 'D' command.
Example: Assume an HLIA card on 'C' bus addressed at 6002, use display .I6002B (B for HEX format)
If the displayed value were CF72 (1100 1111 0111 0010) would be the binary pattern that should also be present on that card.

31. HSCA, HSCB and HSCE test (8 circuits, inputs on JA2,4,6,8,10,12,14,16) Apply appropriate input voltage to appropriate pins on card under test per list at beginning of step 30. connect COM to pin 17 of front edge connector and to DCOM on module. Check for correct output and proper LED is on.

32. HSCC, HSCD and HSCH test (16 circuits, inputs on JA1 through JA16 Apply appropriate input voltage to appropriate pins on card under test per list at beginning of step 30. connect COM to pin 17 of front edge connector and to DCOM on module. Check for correct output and proper LED is on.

33. NADA/B----------

A. Select USER MONITOR (U) and NADA test. Connect power supply to NADA JA (see * below) input voltages (+/- 12.5 volts) to the 8 channels and check for the same voltages being read when the NADA test is run.

*NADA channel:	0N-JA1	channel	1N-JA3	channel	2N-JA5	channel	3N-JA7
	0P-JA2		1P-JA4		2P-JA6		3P-JA8
	4N-JA9		5N-JA11		6N-JA13		7N-JA15
	4P-JA10		5P-JA12		6P-JA14		7P-JA16

B. NDAC to NADA, See special note in output section to test UUT which contains NDAC and NADA cards.

28. HCMA test----------

The HCMA is tested utilizing a special loop back cable and PTCA, PTCB or PTCC software on the card. Any other configuration is not testable. The loop back cable must be connected between JA & JB. The test is go/nogo type. Enter the 'L' bus address of card and the test will run.

Printer or other output device may be verified by utilizing above test,but remove loop back cable from JA to JB on HCMA and connect device to be tested to JA.
use "Modify" utility to set HCMA baud rate("Baud1") to match baud rate of device under test.
When test is performed printer should print "ABCDEF123",and monitor will indicate test failure(due to open loop).
After test is complete reset"Baud1" to 4800 and verify by modify/ display utility.

29. NRTA/NPSL test----------

The NRTA/B card is tested using the HAIA Analog user monitor test and DMC test box 1.Test box switches resistors across each of the 8 circuits on the board as follows. * IT TAKES 20 MINUTES FOR CARD TO WARM UP -

```
JA21--|----{  R  }----JA20
JA19--|
```

To perform test,set appropiate switch on test box and type in control word.Control word will echo on monitor and 7.5volt output will be displayed.Repeat for each circuit.

NOTE: Z in the control word should reflect the jumper on NRTA,if it is low,Z should be "0",if it is high,Z should be "1".If two NRTA outputs are tied together,the high/low jumpers must be set different on each card to avoid confliction.

CKT#		HAIA CONTROL WORD CHAN CKT
0	JA21,JA19-------JA20	XXXX Z000
1	JA22,JA23-------JA24	XXXX Z001
2	JA18,JA16-------JA17	XXXX Z010
3	JA14,JA13-------JA15	XXXX Z011
4	JA12,JA10-------JA11	XXXX Z100
5	JA7,JA9---------JA8	XXXX Z101
6	JA5,JA6---------JA4	XXXX Z110
7	JA2,JA3---------JA1	XXXX Z111

EXAMPLE: channel 12, circuit 1, with NTRA jumper high-----1100 1001

30. LCFBUS TESTABLE INPUT CARDS

HLIA	5VDC 16 bit non-isolated
HLIC	5VDC 8 bit isolated
HDRA	JA 16 bit output (5V), JB 16 bit input
HSCA	115VAC/105VDC 8 bit isolated
HSCB	125VDC 8 bit isolated
HSCC	28VDC 16 bit non-isolated
HSCD	105VDC 16 bit non-isolated (JA17 must be tied to DCOM)
HSCE	105VDC/28VDC 8 bit non-isolated
HSCH	28 VDC non-isolated
NADA/B	Analog to digital 8 channels +/- 12.5 volts

SLOT 2F ADDL 8200

LOOK IN FOLDER SLEEVE FOR ADDL

* Cable is Marke HXPC JA + JB

24. HAIA/HAIC TEST----------

Call HAIA test from User Monitor and input address.
Connect* cable between JA & JB and run digital I/O check.
Use special test to control or display back plane pins.
Use analog section to control mux(internal & external) and perform A/D conversion and display results. Type in the 8 bits of the control word. Ex: 0100 0011 would select chan. 4 and input #3 (PA21)
Control word format:

MSB LSB
XXXX XXXX

MSB control selects Chan 0-15(PA16,19,18,21-24, 2,4,13,15,8,17,10,12) to be A/D converted

LSB control determines the state of 1PA0-1PA3 (PA39,41,49,47) which are used by multiplexer cards such as NAIA or NTCF.

25. NAIA, NAIB, NAIE TEST ----------

NAIA/NAIE TEST (4-20ma = 2 to 10 volts out)
Use special NAIX/NTCF test fixture
Input 1.5v to box and connect ribbon cable between box & NAI_
Use HAIA test for mux control & A/D converting
Expect 7.5 volts to be displayed by HAIA test
Exercise all 16 inputs by switches on test box & HAIA control
Repeat with -1.5 volts in and -7.5 volts out

NAIB TEST (+/-10 volts in = +/-10volts out)
Input + & - 7.5 volts and expect + & - 7.5 volts to be displayed with HAIA test.

26. NTCA,NTCB,NTCC,NTCD,NTCF TEST

Use special NAIA/NTCF test fixture with user monitor HAIA test.
Input proper voltage per table below to test box.
(Input voltage times stated gain should = 7.5V read with HAIA test)
Select input to be tested via switches on test box
Exercise all 16 inputs by switches on test box & HAIA control

BOARD	GAIN	INPUT VOLTAGE
NTCA	361.4	20.8 MV
NTCB	304.1	24.7 MV
NTCC	271.1	27.7 MV
NTCD	199.9	37.6 MV
NTCF	216.3	34.7 MV

27. NVAA TEST----------

4 Current driver circuits
Typically driven by NDAC
0-10 volts in = 4-20 ma out
Load all 4 output circuits with 500 ohms(IMOK led should be on)
Measure voltage across each load resistor
Value measured should be within 1% of the following computed values
Volts across resistor = .004*RL + .0016*Vin*RL where:
RL=load resistor value Vin=input voltage via NDAC

Example:
Load circuits with 511 ohm resistors & put +2 volts in from NDAC
Value to be measured = .004*511 + .0016*2*511
Value to be measured = 2.044 + 1.635 = 3.679

18. HSPC & HPCA
Connect test tach box to HSPC JA connector. The 3 jumpers on the HSPC must be set to 'SIN' position for the test tach. Reset to elementary position upon completion of this test. Turn knob on test box CW check that count up led is on & ST-0 thru ST-3 Leds are on. Turn knob on test box CCW. Check that count down Led is on & ST-0 thru ST-3 Leds are on. Put switch on HPCA to test position(up) check that Leds are counting. Put switch to normal position on HPCA. Check Leds g,d,e,f on HPCA count up & down as knob on tach box is turned. Use the DISPLAY of the I/O address of the HPCA and verify 4 LED's agree with the most signifigant byte of the word displayed.

19. HXPC/D test ----------
Digital I/O is checked utilizing a wrap around cable and test is called from the USER MONITOR. If test fails HLOA,HLIA, or HDRA test may be used to further isolate faults. Card address to use is Base-address + 6H (card is mapped at 9000H use 9006 for input & output address. Interupts and counters are not checked.

20. HIOD TEST----------
Connect special test harness to JA,JB & JC connectors. Select USER MONITOR HIOD test. Select loop test (GO/NO GO) for module level test. For final test or diagnostics use the discrete input & output options available.

21. NCVA TEST----------
Card has 8 identical circuits,inputs at JA connector and outputs connected to NADA.Test as NADA(refer to NADA test),Input current to appropiate JA conn.pins,read output volts from NADA.Inputs of 4 to 20 mil-amps will output 2 to 10 volts,test at mid-range .

22. HPRB/HPRC TEST----------
Call HPRC test from User Monitor and input I/O address. Input test frequency of approx. 1khz at 10vrms to JA connector,verify with counter.The value measured by counter should match that displayed by test program.More than 1 input can be exercised at a time if signal generator being used is capable.Make sure terminal is running at 9600.

CKT	JA CONNECTIONS	
	INPUT	COM
1	JA-1	JA-2
2	JA-3	JA-4
3	JA-5	JA-6
4	JA-7	JA-8

23. HRTA TEST---------- (ONLY WORKS WITH DMCA AT PRESENT)
Call HRTA test from User Monitor and input address. Select frequency and channel to be output and verify output with counter. For base clock frequency pin 4 must be tied to pin 8.

ANALOG INPUTS:
Use HAIA user monitor Analog test (refer to HAIA card test located elsewhere in this documentation)and address of HAIA/C from elementary.Use Special test box(#1),connect ribbon cable from test box to JA on HAFA card.Connect external power supply to box for various input test voltages and use appropiate test switches to apply test voltages to each line.
NOTE! DO NOT TRY TO INPUT TO CIRCUITS 12 OR 13 WITH SWITCHES OR EXTERNAL SUPPLY,THESE INPUTS ARE FIXED AND SHOULD BE TESTED WITH THE FIXED LEVEL ONLY.

CKT#	+	-	Gain to mux input	Gain of mux output depends on G3, it can be 1 or 5 (ckts. 0-6)
0	JA1	JA2	1	1 OR 5
1	JA3	JA4	1	1 or 5
2	JA5	JA6	1	1 or 5
3	JA7	JA8	1	1 or 5
4	JA9	JA10	1	1 or 5
5	JA11	JA12	1	1 or 5
6	JA13	JA14	1	1 or 5
7	JA15	JA16	1	1 OR 5
~~7~~	~~JA15~~	~~JA16~~	~~1~~	Fixed gain ~~1~~
8	JA17	JA18	1	1
9	JA19	JA20	1	1
10	JA21	JA22	1	1
11	JA23	JA24	1	1
12	+5 VOLTS(FIXED)		1	1
13	DCOM(FIXED)		1	1

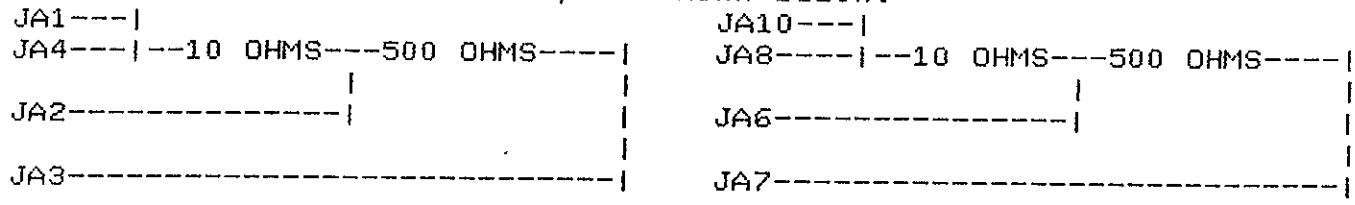
			Select input gain with G1A and G1B			
14	JA29	JA30	G1A	G1B	GAIN	
			1	1	1	1
			2	2	2	1
			4	4	4	1

			Select input gain with G2A and G2B			
15	JA31	JA32	G2A	G2B	GAIN	
			1	1	1	1
			2	2	2	1
			4	4	4	1

EX. With circuits 14 and 15 set to a gain of 4, 1 volt into the test box produces 4 volts out.

39. HCVA test

The HCVA card contains 2 D/A's(0-10v .61039mv/bit),2 4-20ma current outputs and an 8 channel multiplexer to monitor its own signals.
J1A,J1B,J2A & J2B set to I, J4 & J5 set to S, J3 set to RUN.
NOTE:THESE ARE TEST SETTINGS AND SHOULD BE RESET TO ELEMENTARY.
Connect test load card & 10 pin ribbon cable to JA of HCVA.
Test Load card is set up as shown below:



D/A output #1 requires 1 full word of 'L' bus I/O to Base address of HCVA
D/A output #2 requires 1 full word of 'L' bus I/O to base address +2H

TEST 1, Circuit 1: Select User Monitor and LBUS test, follow the screen instructions as follows:

FOR D/A #1 Output, type O; then 'L'Bus output code (ABCD) which sets the output value, then enter base address of HCVA XXXX,
Example : To call for 10 ma to flow to test circuit #1. Do the following:
Set D/A #1 to 5 volts (Use LBUS test, output code of 4000 at base address of XXXX and 10ma. should flow. (Ex:O;4000;A400)
Measure voltage drop across 10 ohm resistor (on test load card) connected between JA4 & JA2. (10 ohms * .010amps = 100 mv) Exercise as follows:

DESIRED OUTPUTS CURRENT	MV AT TEST CARD	OUTPUT CODE A B C D	BASE ADDRESS X X X X
5 MA	50 MV	2 0 0 0	EX. A 2 0 0
10 MA	100 MV	4 0 0 0	X X X X
20 MA	200 MV	7 F F E	X X X X

Set output code to 4000 before test #2.
TEST 2 Circuit 1: Select User Monitor then HAIA and AN test to monitor the following signals:

	HCVA value	Mux gain	HAIC value	HAIC HVCA chan control word
VREF1	-5v	1	-5	xxxx 0000
FBK1	-5v	1	-5	xxxx 0001
OUT1	5.5v	.5	2.75	xxxx 0010
CUR1	1.85v	2.5	4.62	xxxx 0011

Note: CUR circuit has a problem, it is non-linear and becomes more accurate as you approach max current(20ma). In our test case (10ma) the board value should be 2. volts but in reality is close to 1.85
Set D/A #1 to 0 volts (Ex:O;0000;A400)
Test 1 Circuit 2: Test procedure is same as used for circuit #1. Set D/A #2 to 5 volts(Use LBUS test with output code of 4000 and base address + 2H)
Measure voltage drop across 10 ohm resistor connected between JA8 & JA6.
10ohms * .010= 100mv
Test 2 Circuit 2: Select User Monitor then HAIA and AN test to monitor the following signals:

	HCVA value	Mux gain	HAIC value	HAIC HVCA chan control word
VREF2	-5v	1	-5	xxxx 0100
FBK2	-5v	1	-5	xxxx 0101
OUT2	5.5v	.5	2.75	xxxx 0110

46. ESA PRBA TEST (IN A PRODUCTION MODULE) ----------

A. For the purpose of this test the TEST MEM will be referred to as the 'MASTER' and the module under test as the 'SLAVE'.

Set-up for 'SLAVE'

Set bergs on PRBA board as follows:

JØ - J7 = Ø
J8 = INT.
J9 = 2K
J1Ø - J12 = Ø
J13 & J14 = 1
J15 & J16 = IN
J17 = IN

Replace the production HUMA with 'TEST' HUMA which has PRBA software or power up and download the PRBA test from the PRO-35Ø into a spare quad on the production HUMA that has been set up for segment 2ØØØ. (be sure to disable any other quad that is set for segment 2ØØØ) Turn on the controller if it is not already on.

Set-up for 'MASTER' MEM

Plug in a null-modem cable to PCLA board JA and run to module under test, but do not connect to anything at this point.
MASTER should have an HMPJ with DMCA software.
Power up, enter password, turn on controller, channel 2 and set CPL segment to 5ØMS.

B. TEST
With communications cable connected to 'MASTER' do a 'modify' of .O46ØØB and enter some HEX value. (remember this value)
Now do a 'display' of .I46ØØB and a HEX value will be displayed, now plug in the null-modem cable to the PRBA in the 'SLAVE' and observe that the value being displayed changed to the one you just set with the 'modify' routine.
Do several 'modify' and 'displayed' routines, setting in different values to be sure the value being displayed changes to the new value of the 'modify' routine.

C. TEST COMPLETE

Disconnect the communications cable from 'MASTER'
Remove null-modem cable and remove 'TEST' HUMA from 'SLAVE' if used and replace production HUMA or reset bergs on production HUMA to enable TEST software and disable the PRBA test.
Reset bergs on PRBA to match requisition paperwork if changed.

46. ESA PRBA TEST (IN A))DUCTION MODULE) ----------

A. For the purpose of this test the TEST MEM will be referred to as the 'MASTER' and the module under test as the 'SLAVE'.

Set-up for 'SLAVE'

Set bergs on PRBA board as follows:

J0 - J7 = 0
J8 = INT.
J9 = 4K
J10 - J12 = 0
J13 & J14 = 1
J15 & J16 = IN
J17 = IN

* HUMB IF USING HMPK AS uPROCESSOR

Replace the production HUMA with 'TEST' HUMA which has PRBA software or power up and download the PRBA test from the PRO-350 into a spare quad on the production HUMA that has been set up for segment 2000. (be sure to disable any other quad that is set for segment 2000) Turn on the controller if it is not already on.

Set-up for 'MASTER' MEM

Plug in a null-modem cable to PCLA board JA and run to module under test, but do not connect to anything at this point.
MASTER should have an HMPJ with DMCA software.
Power up, enter password, turn on controller, channel 2 and set CPL segment to 50MS.

** (OR HMPK & HUMB)

B. TEST

With communications cable connected to 'MASTER' do a 'modify' of .04600B and enter some HEX value. (remember this value)
Now do a 'display' of .I4600B and a HEX value will be displayed, now plug in the null-modem cable to the PRBA in the 'SLAVE' and observe that the value being displayed changed to the one you just set with the 'modify' routine.
Do several 'modify' and 'displayed' routines, setting in different values to be sure the value being displayed changes to the new value of the 'modify' routine.

C. TEST COMPLETE

Disconnect the communications cable from 'MASTER'
Remove null-modem cable and remove 'TEST' HUMA from 'SLAVE' if used and replace production HUMA or reset bergs on production HUMA to enable TEST software and disable the PRBA test.
Reset bergs on PRBA to match requisition paperwork if changed.

*>

ENTER S
THEN M
THEN CPL, RETURN
ENTER 50MS, RETURN

Perform 'E' bus test as follows:

1. Enter return then Q
2. CRT responds > then enter B for breakpoint.
3. CRT responds BREAKPOINT B> then enter B for base.
4. CRT responds BASE ? then enter 8E00, RETURN.
5. CRT responds B> then enter M for modify.
6. CRT responds OFFSET ? then enter offset from chart,RETURN.
7. CRT responds 8E00:(offset #)= XX- (XX- = low order byte presently at that address.
8. Enter a new 2 digit value then hit return twice.
9. CRT responds B> then enter D for display.
10. CRT responds OFFSET ? then enter same offset as above,RETURN
11. CRT responds LENGTH ? then enter 1 for 1 byte, RETURN.
12. CRT responds FORMAT(W,A,B) ? then enter B for byte, RETURN.
13. CRT responds 8E00:(offset #) XX (XX = the 2 digit value you put in.
14. Go back to step 5. and repeat this test several times with a new offset value at step 6. and a new value at step 8.

END PLC_ AND DMCA BOARD TEST

G. Have user monitor program on EE prom (EEPA) after loading from PRO350 or by testing board in a module with program already on EE prom.

H. Verify system loads from EE prom on power-up.
Turn power off then back on, CRT should display the following:

```
    PLC_                          DMC_
DMC SELF TEST               SELF TEST DONE
PROM CSUM--OK
BASE RAM --OK
<RESTORED>
8087 CHECKED--OK
SYSTEM RAM--OK
APP CSUM  --OK
SELF TEST DONE
```

I. Enter password (P)---PS2
Turn controller on
To turn controller on, type (O) then (C) then (Y) for PLC_ or (ON) for DMCA then (Q).

J. Test of 8087 co-processor on CLCB daughter board.
Call user program and select CO_P test.
The co-processor 68A9193P2 should be mounted in position U13 of DMPC.
This routine will exercise the co_processor to perform some arithmetic functions.

K. Test of 'E' bus functions
Be sure the 50 pin ribbon cable is in from JE on HRMB/D to JE on CLCB.
Turn controller off and recheck memory map to be sure there is RAM at 8E000.
Turn controller on.

E bus address

BASE	OFFSET
8E00	0000
	0002
	0004
	0008
	0010
	0020
	0040
	0080
	00F0
	00FE

45. DS3815PLC_ AND DS3815DMCA BOARD TEST INSTRUCTIONS -------

A. USE DMC TEST MODULE , SLOT 2M

B. CHECK THAT PROM SET IS LATEST REVISION.

C. SET BERG JUMPERS

PLCA JUMPERS	J1=D	J2=L	J3=8K			
PLCC JUMPERS	J1=D	J2=L	J3=B	J4=B	J5=B	J6=A
PLCE JUMPERS	J1=D	J2=L	J3=B	J4=B	J5=B	J6=A
DMCA JUMPERS	J1=IN	J2=L	J3=B	J4=B	J5=B	J6=A
CLCB JUMPERS	J1=INT	J2=COM	J3=COPRO (GND IF NO COPRO)			
HRMB/D SEGMENT JUMPERS	J6=B	J7=B	J8=B	J9=A		
HRMB/D BASE ADDRESS JUMPERS	J10=A	J11=A	J12=A			

D. APPLY POWER, CHECK POWER-UP ROUTINE

PLC_	DMC_
DMC SELF TEST	SELF TEST DONE
PROM CSUM--OK	
BASE RAM --OK	
<INITIALIZED>	
SYSTEM RAM--OK	
APP CSUM - NEW	
SELF TEST DONE	

E. Enter password (P)----PS2
If PLC_ or DMCA LED (TEST) is on, turn controller off.
To turn controller off, type (O) then (C) then (Y) for PLC_ or (OFF) or DMCA then (Q).

F. Check memory map, type (B) then (T) then RETURN
refer to local controller memory map master & elementary to determine & verify memory map.

EX.
```
00000 = RAM
02000 = NONE
04000 = RAM
0C800 = NONE
20000 = EEPROM (EEPA)
28000 = NONE
8E000 = RAM     (HRMB/D)
90000 = NONE
F8000 = PROM (PLCA)          F0000 = PROM (PLCC or DMCA)
COMMAND COMPLETE
```

NOTE: RAMA,EEPA,PLC_ & DMCA are on 'L' bus.
HRMB/D is mapped into memory using 'E' bus.
This requires a ribbon cable between PLC_ or DMCA and HRMB/D.
This cable sometimes gives us a problem.
If the HRMB/D does not map, check that pin 37 is tied to com.

44. COMPUTER INTERFACE MODULES ----------

Replace the PCBA/HMPJ with a 'TEST' DMCA/HMPJ.
Set bergs: J3=B, J4=A, J5=B and J6=A on HMPJ.
Install 'TEST' HUMA in spare L bus slot, enable the CSF #2 software.
Add a test jumper from HMPJ pin 17 to PLNC/D pin 19, this enables you to have PLNC/PLND in segment #2 (2:8000) for the CSF test. Set the bergs on PLNC/PLND and HLND per CSF test instructions except make J6=F and J7=T on the PLNC/PLND in UUT.
Make sure to have a short ribbon cable between PLNC/PLND and HLND, 4 inches or less.
Set HRMD bergs per elem. except set J1=B, J2=B, J3=A, J4=A and J5=A, this will map HRMD RAM (8K) at 0:C000 in memory map.
Connect a ribbon cable between HRMD and DMCA. (E-bus)
Power up per CSF test instructions and run CSF test.
Do a memory map test and use the following as a general guide:

0:0000	RAM on DMCA
0:4000	J3=B, J4=A, J5=B, J6=A
0:4000	Base RAM on 'TEST'
0:C000	HUMA/MMAC
0:C000	RAM on HRMD
0:E000	(L-bus) 8K
2:0000	EEPROM on 'TEST' HUMA/MMAC
2:8000	CSF software for sta. #2
2:8000	DP RAM on PLNC/PLND/PLNE
2:C000	
2:C000	RAM on PLNC/PLND
3:0000	This depends on berg settings
3:0000	RAM on HRMD (E-bus) depends on berg settings
3:2000	might be at 8:E000-9:0000
F:0000	PROM
F:FFFF	

Reset all berg jumpers per elem. before T-out.

43. DMCD test ----------

Check board for proper revision, I.D. and I.P. stamp
Verify berg jumpers as follows:

HMPK	DMPK	DMPK	DMPK
J1 = NOT 1	J1 = NOT P	J9 = NOT P	J17 = 32K
J2 = NOT 2	J2 = NOT P	J10= NOT P	
J3 = NOT 4	J3 = NOT P	J11= NOT P	
J4 = NOT 8	J4 = NOT P	J12= NOT P	
J5 = NOT 10	J5 = NOT P	J13= P	
J6 = 7GND	J6 = NOT P	J14= P	
	J7 = NOT P	J15= P	
	J8 = NOT P	J16= P	

If testing a direct ship board in the 'TEST' MEM, set the bergs on JPB on the 'TEST' MEM header to accommodate an HMPK board.
Remove other boards in 'TEST' MEM or UUT that show up in a memory map.
Insert DMCD board into slot 2M of 'TEST" MEM or into designated slot of production UUT.
Connect communications cable.
Power up and do a memory map which should display the following map:
(Refer to DMCMOD test instructions, steps 3 through 5)

```
0 0000 RAM
0 C000 NONE
2 0000 EEPROM
2 8000 NONE
C 0000 PROM      * IGNORE OTHER LOCATIONS OF SEGMENT C WHICH MAY APPEAR
D 0000 NONE
F 0000 PROM
```

Load test software from PRO 350 in order to functionally test board.
(Refer to DMCMOD test instructions, steps 6 through 9)
Turn on controller, call up user monitor and do CO_P test.
Do the EEPA test next at starting address of 2000 and test a total memory of 7FFF. After successful tests do a save of test program.
Power down, remove communications cable
T stamp boards that passed test on back of board at end of DS3815 I.D. strip.

SPECIAL NOTES
MAUA and MAUD modules are tested in card test but may be checked with this setup by putting them in place of one of the 'TEST' units on CSF TEST CART and going through the above exercise.

3820MAUB modules may be tested by putting them in series with one of the twinax cables between the two MAUD modules and going through the above exercise. Change the position of S1 on MAUB and verify COUNT 1-20 are incrementing.

CSF boards may be tested on any of the DMC stations by setting up the TEST MEM as follows:
Put processor bd. in slot 2M with DMCA software (6 segment proc. bd.)
Put 'TEST HUMA' in slot 2K (enable RAM and CSF STA.#2)
Put 'TEST HUMB' in slot 2K if a 16 segment processor bd. is used in 2M.
If testing PLNE or PLNF put it in slot 2J
If testing HLNC, put it in slot 2J (requires an HLND in slot 2H)
Match the type of CSF bds. in sta.#1 to the type of CSF bds. in sta.#2.
Use CONTROL SYSTEM FREEWAY TEST instructions to test these boards with the DMC test station as CSF station #2 and TEST CART as CSF station #1.

42. DMCB test ----------

To test the DMCB board proceed through the test instructions for DMCMOD with the DMCB board in place of the DMCA board up to step 6. Go through loading procedure for DMC software per step 6 up to where CRT displays "SYSTEM RESTART". After this the CRT displays "CLEAR MEMORY" ? At this point do a reset on DMCB board (short TP1 to TP2) System will reinitialize and display the following:

```
DMC SELF TEST
PROM CSUM        OK
BASE RAM         OK
8087 CHECK       BAD
CONTINUE ?       type Y
SYSTEM RAM       OK
APP CSUM         BAD
COMTINUE ?       type Y
SELF TEST DONE
```

System should be ready to use per DMCMOD test instructions.

Connect communications cable to processor board JB in UUT.
Power up UUT, observe self test, the I'm OK LED is lit on the PLNC, PLND, PLNE or PLNF. The controller should be on, if not, turn it on.

TEST PROCEDURE
CONNECT COMMUNICATIONS CABLE TO STA.#1 DMC (ON CART)

OPERATOR COMMAND		TERMINAL RESPONSE
Hit RETURN until		Prompt *>
Type M		DISPLAY/MOD? M>
Type M		MODIFY?
Type WRITE1	RETURN	VALUE?
Type 1	RETURN	M>
Type M		MODIFY?
Type WRITE2	RETURN	VALUE?
Type 1	RETURN	M>
Type M		MODIFY?
Type WRITE4	RETURN	VALUE?
Type 1	RETURN	M>
Type R	RETURN	SCREEN?
Type 1	RETURN	A test screen is displayed

Observe that on the left, WRITE1, 2 and 4 = 1 and WRITE8, 10 and 20 = 0, COUNT1, 2 and 4 are incrementing, COUNT8, 10 and 20 = 0 and CSFOT 1-20 = 1

MOVE COMMUNICATIONS CABLE TO UUT

Hit RETURN until		Prompt *>
Type M		DISPLAY/MOD? M>
Type R	RETURN	SCREEN?
TYPE 1	RETURN	A test screen is displayed

Observe that on the left, WRITE1-20 = 0, COUNT1, 2 and 4 are incrementing, COUNT8-20 = 0 and CSFOT 1-20 = 1. Hit RETURN until you get M> then type Q.

Follow the first set of operator commands as stated above, but substitute WRITE8 for WRITE1, WRITE10 for WRITE2 and WRITE20 for WRITE4.

Observe that on the left, WRITE1, 2 and 4 = 0 and WRITE 8, 10 and 20 = 1, COUNT1-20 are incrementing and CSFOT 1-20 = 1.

MOVE COMMUNICATIONS CABLE TO STA.#1 DMC (ON CART)

Hit RETURN until		Prompt*>
Type M		DISPLAY/MOD? M>
Type R	RETURN	SCREEN?
Type 1	RETURN	A test screen is displayed

Observe that WRITE1, 2 and 4 = 1, WRITE8, 10 and 20 = 0, COUNT 1-20 are incrementing and CSFOT 1-20 = 1.

Power down and replace the production memory board in UUT, remove the 20 pin cable and communications cable. Reset berg jumpers on CSF boards per requisition paperwork.

TEST COMPLETE

41. CONTROL SYSTEM FREEWAY test ----------

THIS TEST PROCEDURE MAY BE USED TO TEST 3815PLNC, PLND, PLNE, PLNF. 3820MAUA, MAUB, MAUC AND MAUD ARE TESTED IN CARDROOM, BUT MAY BE TESTED IN THIS SYSTEM. FOR THE PURPOSE OF THIS TEST, THE EQUIPMENT ON TEST CART WILL BE STATION #1 AND UUT WILL BE STATION #2. BERG JUMPER SETTINGS SHOULD BE SET FOR STATION #1, TEMPORARILY SET BERGS ON CSF BOARDS IN UUT (STA #2) PER LIST BELOW.

6 SEG.PROC.BD. EX. HMPJ			6 & 16 SEG. PROC.BD.		16 SEG. PROC. BD. EX. HMPK		
STA.#1 AND #2	STA.#1	STA.#2	STA.#1	STA.#2	STA.#1 AND #2	STA.#1	STA.#2
PLNC/D	PLNE/F	PLNE/F	HLND	HLND	PLNC/D	PLNE/F	PLNE/F
J1--0	J4--T	J4--F	J1-T	J1-F	J1--0	J4--T	J4--F
J2--0	J5--F	J5--T	J2-F	J2-T	J2--0	J5--F	J5--T
J3--0	J6--F	J6--F	J3-F	3-F	J3--0	J6--F	J6--F
J4--0	J7--F	J7--F	J4-F	4-F	J4--0	J7--F	J7--F
J5--T	J8--F	J8--F	J5-F	5-F	J5--T	J8--F	J8--F
J6--T	J9--F	J9--F	J6-F	6-F	J6--F	J9--F	J9--F
J7--F	J10-F	J10-F	J7-F	7-F	J7--T	J10-F	J10-F
J8--F	J11-F	J11-F	J8-F	8-F	J8--F	J11-F	J11-F
J9--F	J13-F	J13-F	J9-IN	9-IN	J9--F	J13-F	J13-F
J10-0	J14-T	J14-T			J10-0	J14-T	J14-T
J11-0	J15-T	J15-T			J11-0	J15-F	J15-F
J12-0	J16-F	J16-F			J12-0	J16-T	J16-T
J13-0	J17-F	J17-F			J13-0	J17-F	J17-F
	J18-F	J18-F				J18-F	J18-F
	*J19-8/16	*J19-8/16				*J19-8/16	*J19-8/16
	*J20-INT	*J20-INT				*J20-INT	*J20-INT

* PLNF ONLY

NOTE: Certain jobs may require segment 2 to be temporarily wired from the processor board to the CSF board. The on board jumper which services the input where segment 2 comes in must be set 'T' with the other 3 segment jumpers set 'F'.

TEST SETUP (ON CSF TEST CART TO UUT)
Put PLNC or PLND module in DMC module, slot 1D. (ON CART) (IF UUT HAS A PLNC OR PLND)
Put HLND card in DMC module slot 1C. (ON CART) (IF UUT HAS HLND)
If UUT has PLNE or PLNF , put PLNE or PLNF in slot 1D (ON CART) in place of PLNC or PLND. (REMOVE HLND)
Connect a 20 pin cable from HLND JA (on UUT) to #2 MAUD JA. (ON CART)
Connect a 50 pin ribbon cable from HLND DA to PLNC or PLND JA. (ON UUT) and from HLND DA to PLNC or PLND JA (ON CART)
PLNE or PLNF requires only the 20 pin cable from JA (UUT) to #2 MAUD JA.
Connect jumper from HLND ST1 to PLNC or PLND ST1 (ON UUT) and from HLND ST1 to PLNC or PLND ST1. (ON CART)

POWERING UP
Connect communications cable to processor board JB, in #1 DMC.(ON CART)
Turn on power supply for #1 DMC and #1 & #2 MAUD and observe self test.
Observe that after self test is complete the I'm OK LED is lit on the PLNC, PLND, PLNE or PLNF. The controller should be on, if not, turn it on.
Set up the UUT as CSF station #2 by removing production memory board and plugging in a 'TEST' memory bd. with RAM and CSF station #2 enabled.
Use HUMA with 6 segment processor bd. and HUMB with 16 segment bd.

40. Miscellaneous boards in the DMC such as DOAA/NOAA where discrete components are mounted per ENG ML by factory must be checked. Normal test procedure should be to verify all component values & BERG jumpers per ELEM & indicate verification on ELEM.

Any 3810 or 3815 board module in the DMC should have the upper ear engraved with the 3810/3815 nomenclature. It should also have a label located on the back side of the card with the full 3810/3815 number on it. This label should be near the outside edge and readable without removing the card. If the card was tested during the DMC test the label on the back should have a small 'T' stamped on it.

Examples:

Original card	Lower ear	Upper ear	Label on back	Proper Rev.
HMPH	HMPH	PLCA	DS3815PLCA1A1A	
HUMA	HUMA	RAMA	DS3810RAMA1A1A	
HUMA	HUMA	EEPA	DS3810EEPA1A1A	
HMHA	HMHA	PCLA	DS3815PCLA1A1A	
HCMA	HCMA	PTCA	DS3815PTCA1A1A	
HXCA	HXCA	PXCA	DS3815PXCA1A1A	

T - STAMP JOB & SHIP

47. ESA PRBA TEST (DIRECT SHIP CARD)

A. For the purpose of this test the TEST MEM will be referred to as the 'MASTER' and the SEM in the CSF cart as the 'SLAVE'.
Check card revision against the orange book.

Set-up for 'SLAVE'

Set bergs on PRBA board as follows:

JØ - J7 = Ø
J8 = INT.
J9 = 2K
J1Ø - J12 = Ø
J13 & J14 = 1
J15 & J16 = IN
J17 = IN

Enable the PRBA quad on HUMA in slot 1E and disable the CSF quad.
Replace the PLNC/PLND in slot 1D with the PRBA to be tested, and pull HLND in slot 1C.
Power up and turn on controller if it is not already on.

Set-up for 'MASTER' MEM

Plug in null-modem cable to PCLA board JA and run to CSF cart, but do not connect to anything at this point.
MASTER should have an HMPJ with DMCA software.
Power up, enter password, turn on controller , channel 2 and set CPL segment to 5ØMS.

B. TEST

With communications cable connected to 'MASTER' do a 'modify' of .O46ØØB and enter some HEX value. (remember this value)
Now do a 'display' of .I46ØØB and a HEX value will be displayed, now plug in the null-modem cable to the PRBA in the 'SLAVE' and observe that the value being displayed changed to the one you just set with the 'modify' routine.
Do several 'modify' and 'display' routines, setting in different values to be sure the value being displayed changes to the new value of the 'modify' routine.

C. TEST COMPLETE

Disconnect the communications cable from the 'MASTER'.
Remove the null-modem cable and remove the PRBA card from 'SLAVE'
Reset bergs on HUMA in 'SLAVE' to enable the CSF test software and disable the PRBA test software.
Replace PLNC/PLND and HLND in slots 1D and 1C respectively.
T stamp I.D. strip on back of board and on the N.P. on box.

49. DS382ØDPA_ TEST (DMC/process & uPSS panel)

A. Tests for forms A & B
Use 'TEST' DMC MEM and connect a 1Ø pin ribbon cable from DPA JC to 'TEST' DMC header connector JDA.

B. Connect two 2Ø pin ribbons from DPA panel JA, JB to HXPC/D JA, JB respectively.

C. Select HLOA test from user monitor. Base address +6H (9ØØ6). Ripple test, 2 cycles at 1ØØØ msec. The LEDs should cycle ON-OFF-ON, except the 'DMC OK' LED will be OFF-ON-OFF.

BIT PATTERN:

	Ø	1	2	3	
	*	*	*	*	
	4	5	6	7	
8	*	*	*	*	
*					C
	D	E	F		*
9	*	*	*		
*					
A					
*					
B					
*					

D. Select HLIA test from user monitor, base address +6H (9ØØ6).

E. Set key sw. to 'LOCAL' Bit pattern = 1111 1111 1110 1111

F. Set key sw. to 'REMOTE' Bit pattern = 1111 1111 1101 1111

G. Depress sw. 'TEST' Bit pattern = 1111 1111 1101 1110

H. Depress sw. 'ONLINE' Bit pattern = 1111 1111 1101 1101

I. Depress sw. 'STANDBY' Bit pattern = 1111 1111 1101 1011

J. Depress sw. 'OFFLINE' Bit pattern = 1111 1111 1101 0111

K. Depress sw. 'DETAIL' Bit pattern = 1111 1110 1101 1111

L. Depress sw. '1' Bit pattern = 1101 1111 1101 1111

M. Depress sw. '2' Bit pattern = 1011 1111 1101 1111

N. Depress sw. '3' Bit pattern = 0111 1111 1101 1111

	INPUT POINT	INPUT VALUE	CHAN. CKT.	OUTPUT
14.	JA9 to TP2 AND JA11 to TP2	-10V / 10V	XXXX0111	+3.5V +/- 10%
15.	JA9 to TP2 AND JA11 to TP2	10V / 10V	XXXX0110	-2.0V +/- 10%
16.	JA9 to TP2 AND JA11 to TP2	-10V / 10V	XXXX0110	+2.0V +/- 10%
17.	JA11 to TP2 JA11 to TP2	+/-10V 14.097V	XXXX0100 XXXX0100	+7.0V +/- .1V +10.0V +/- .2V
18.	JA9 to TP2 JA9 to TP2	+/-5V 6.761V	XXXX0010 XXXX0010	+7.3V +/- .1V +10.0V +/- .2V

19. Test of PA65 (backplane pin of card under test)
(follow the sequence below)

INPUT POINT	INPUT VALUE	OUTPUT PA65
JA1 to TP2 AND JA3 to TP2	0V / -.2V	DON'T CARE
JA1 to TP2 AND JA3 to TP2	0V / *	0
JA1 to TP2 AND JA3 to TP2	-.2V / -.2V	0
JA1 to TP2 AND JA3 to TP2	-.2V / *	1
JA1 to TP2 AND JA3 to TP2	0V / -.2V	1

*NOTE: * Means to change input from -.2V to 0V then back to -.2V.

59. SSPD SEM TEST ----------(DS382ØSSPD)

This test is to be done in ESA ONLY if there are no 77MM SILCO panels on final floor which can be utilized to test this SEM.

Berg settings:

HFPB (slot c)
J1 = 4K
J2 = ROM
J3 = 4K
J4 = ROM

HFXA (slot d)
J1 = 1
J2 = L
J3 = ROM
J4 = ROM
J5 = ROM
J6 = ROM

HFXB (slot e)
BJ3 = GND (not NC)
BJ4 = NC (not PWR)
BJ5 = POSITION C AND E
BJ6 = POSITION B

Power test:
Connect power cable to JA on SEM
Connect communication cable to JB conn. on HFXB
Set terminal for 3ØØ baud rate, 7 data bits, 2 stop bits

Apply power and observe the following:
]IØ-SELFTEST COMPLETE: COMPUTER OK
]I1-SYSTEM INITIALIZED
]AØ-BRIDGE TEST FAULT: NO PLL SYNC (CHECK AC POWER)
]CC-SPARE 1 INPUT ACTIVATED
]C6-POWER SUPPLY INTERLOCK SET
]CB-TRANSFORMER OVER TEMP
]C5-HIGH AMBIENT TEMP OR FEEDBACK OPEN
]CA-FAN LOSS
]C4-PLL INTERLOCK SET
]CØ-DC BREAKER OPEN
]EI-P5 SUPPLY BUS HIGH

END OF TEST, T-STAMP MOD.

	INPUT POINT	INPUT VALUE		CHAN. CKT.	OUTPUT
14.	JA9 to TP2 AND JA11 to TP2	-10V 10V	\ /	------- XXXX0111	+3.5V +/- 10%
15.	JA9 to TP2 AND JA11 to TP2	10V 10V	\ /	------- XXXX0110	-2.0V +/- 10%
16.	JA9 to TP2 AND JA11 to TP2	-10V 10V	\ /	------- XXXX0110	+2.0V +/- 10%
17.	JA11 to TP2 JA11 to TP2	+/-10V 14.097V		------- XXXX0100 ------- XXXX0100	+7.0V +/- .1V +10.0V +/- .2V
18.	JA9 to TP2 JA9 to TP2	+/-5V 6.761V		------- XXXX0010 ------- XXXX0010	+7.3V +/- .1V +10.0V +/- .2V

19. Test of PA65 (backplane pin of card under test)
(follow the sequence below)

INPUT POINT	INPUT VALUE		OUTPUT PA65
JA1 to TP2 AND JA3 to TP2	0V -.2V	\ /	------ DON'T CARE
JA1 to TP2 AND JA3 to TP2	0V *	\ /	------ 0
JA1 to TP2 AND JA3 to TP2	-.2V -.2V	\ /	------ 0
JA1 to TP2 AND JA3 to TP2	-.2V *	\ /	------ 1
JA1 to TP2 AND JA3 to TP2	0V -.2V	\ /	------ 1

*NOTE: * Means to change input from -.2V to 0V then back to -.2V.

58. NPTA TEST ----------

Call HAIA test from user monitor and select AN test from menu. Determine input chan. being used from elem. Use DIGITEKS or equivalent to input voltages on JA pins as listed.
Set bergs as follows: J1=T, J2=H and J3=H.

	INPUT POINT	INPUT VALUE	CHAN CKT	OUTPUT
1.	JA1 to TP2 AND JA3 to TP2	10V 10V	------- XXXX0111	-3.5V +/- 10%
2.	JA1 to TP2 AND JA3 to TP2	-10V 10V	------- XXXX0111	+3.5V +/- 10%
3.	JA1 to TP2 AND JA3 to TP2	10V 10V	------- XXXX0110	-2.0V +/- 10%
4.	JA1 to TP2 AND JA3 to TP2	-10V 10V	------- XXXX0110	+2.0V +/- 10%
5.	JA3 to TP2 JA3 to TP2	+/-10V 14.097V	------- XXXX0101 ------- XXXX0101	+7.0V +/- .1V +10.0V +/- .2V
6.	JA1 to TP2 JA1 to TP2	+/-5V 6.761V	------- XXXX0001 ------- XXXX0001	+7.3V +/- .1V +10.0V +/- .2V
7.	JA5 to TP2 AND JA7 to TP2	10V 10V	------- XXXX0111	-3.5V +/- 10%
8.	JA5 to TP2 AND JA7 to TP2	-10V 10V	------- XXXX0111	+3.5V +/- 10%
9.	JA5 to TP2 AND JA7 to TP2	10V 10V	------- XXXX0110	-2.0V +/- 10%
10.	JA5 to TP2 AND JA7 to TP2	-10V 10V	------- XXXX0110	+2.0V +/- 10%
11.	JA7 to TP2 JA7 to TP2	+/-10V 14.097V	------- XXXX0011 ------- XXXX0011	+7.0V +/- .1V +10.0V +/- .2V
12.	JA5 to TP2 JA5 to TP2	+/-5V 6.761V	------- XXXX0000 ------- XXXX0000	+7.3V +/- .1V +10.0V +/- .2V
13.	JA9 to TP2 AND JA11 to TP2	10V 10V	------- XXXX0111	-3.5V +/- 10%

*PRDA/

57. PRDB/HRCA AND NRCA TEST ----------

TEST EQUIPMENT NEEDED: DUAL RESOLVER TEST MODULE FROM FINAL FLOOR
The base address is derived from the elementary on job or if you are using the test MEM to talk to the HPBD in the UUT in the buffer mode the address will be: 4200 for word 0
4204 for word 1
4208 for word 2
420C for word 3

Run test cables from the buffer receptacles on test station to header receptacles on UUT (see UUT elementary)
Connect cables from resolver module to NRCA board(s) per elemmetary.

1. Apply power
2. To initiate a software reset call user monitor and HL0A test at WORD 2 (address 4208), select display test and display 00FF.
2A —
3. To see if reset is complete call user monitor and HL1A test at WORD 3 (address 420C), observe FF00.
4. To acknowledge the reset call user monitor and HL0A test at WORD 2 (address 4208), select display test and display FF00.
4A —
5. To read run and fault status call user monitor and HL1A test at WORD 3 (address 420C) and observe 0000 which says "running and no fault".
6. To check that register counts up and down call user monitor and HL1A test at WORD 0 (address 4200), CW increments count and CCW decrements count. (Set count on or near zero for next step)
7. To check that a register count changes when WORD 0 count passes through zero call user monitor HL1A test at WORD 1 (address 4204) and observe that count being displayed changes as resolver is turned CW or CCW to make count from previous step go through zero.
8. Set a data pattern per step 6, drop and reapply power, reset per steps 2 - 5, call user monitor and HL1A at WORD 0 (address 4200) and observe the data pattern just set has not changed.
9. While still observing WORD 0 turn resolver to be sure all bits can be changed with fine and course resolver. Fine resolver changes bits 0-9 and course resolver changes bits A-F.

*Note: PRDA — Single Resolver
Step 8 - only bits 0-9 (Fine resolver) Works.

2A - RESET WORD 2 ADD TO 0000

4A - RESET WORD 2 ADD TO 0000

54. HUMC BERG SETTINGS

J1 Access time quad A (see note in step 52 for setting)
J2 Access time quad B (see note in step 52 for setting)
J3 Oscillator enable (set to 'IN')
(#) L Enables quad on L bus and selects segment 0
(#) LD Memory base address (*) set to T = MSB in address = 2, F = 0
(#) LE Memory base address (*) set to T = MSB in address = 4, F = 0
(#) LF Memory base address (*) set to T = MSB in address = 8, F = 0
(#) L10 Segment select (*) set to T = 1 for segment number, F = 0
(#) L11 Segment select (*) set to T = 2 for segment number, F = 0
(#) L12 Segment select (*) set to T = 4 for segment number, F = 0
(#) L13 Segment select (*) set to T = 8 for segment number, F = 0
(#) E Enables quad on E bus
(#) ED Memory base address (*) set to T = MSB in address = 2, F = 0
(#) EE Memory base address (*) set to T = MSB in address = 4, F = 0
(#) EF Memory base address (*) set to T = MSB in address = 8, F = 0
(#) E10 Segment select (*) set to T = 1 for segment number, F = 0
(#) E11 Segment select (*) set to T = 2 for segment number, F = 0
(#) E12 Segment select (*) set to T = 4 for segment number, F = 0
(#) E13 Segment select (*) set to T = 8 for segment number, F = 0

(#) There is one of these bergs for each quad
(*) If more than one memory address jumper and/or more than one segment select jumper is set to 'T', then add their values together to arrive at proper address and/or segment value(s).
NOTE: See table 1 in step 52 for list of daughter boards vs access times vs memory devices vs GE part numbers.

55. NSMB ---------- (Preliminary Test)
The NSMB card is tested using the HAIA test from the user monitor. Input the address of the HAIA/HAIC card, then select the AN test, then type in the eight bits of the control word. Derive the channel used by NSMB into the HAIA/HAIC from elem. as the MSB and use 0110 (6) as the LSB. See step 24 sh.10 as a guide for this test. When test is exercised you will see a value of 5 volts +/- 10% displayed. This is a set value on card and says that you have communicated with card.

56. NPRB ---------- (Preliminary Test)
The NPRB card is tested using the HAIA test from the user monitor. Input the address of the HAIA/HAIC card, then select the AN test, then type in the eight bits of the control word. Derive the channel used by NPRB into the HAIA/HAIC from elem. as the MSB and use 1101 (D) as the LSB. See step 24 sh.10 as a guide for this test. When test is exercised you will see a value of -8 volts +/- 10% displayed. This is a set value on card and says that you have communicated with card. Repeat the test using same channel as MSB but use 1110 (E) as the LSB and you will then see a value of 5 volts +/- 10% displayed.

52. HUMA BERG SETTINGS

J1 Memory base address (*) set to A = MSB in address = 2, B = 0
J2 Memory base address (*) set to A = MSB in address = 4, B = 0
J3 Memory base address (*) set to A = MSB in address = 8, B = 0
J4 Segment select (set for 0, 1, 2, D, E, or F)
J5 Oscillator enable (set for 'A')
J6 Read access time (set for 250,350 or 450 nanoseconds.
NOTE: selected setting must match or be longer than the slowest read access time of any memory device)
(*) If more than one memory base address jumper is set to 'A', then add their values together to arrive at proper address value.

TABLE 1

DAUG. BD. GROUP NO.	MEMORY DEVICE	GE DRAWING NO.	ACCESS TIME
G1	2K x 8 RAM	68A9249P1	150NS
G2	X2816A EEPROM	68A9192P1	450NS
G3	2732A EPROM	68A9182P2	200NS
G4	2764 EPROM	68A9187P1	200NS
G5	8K X 8 RAM	68A9196P1	150NS
G6	X2816A EEPROM	68A9192P1	450NS
G7	27128A EPROM	68A9255P1	250NS
G8	27256-2 EPROM	68A9261P1	200NS
G9	8K X 8 EEPROM	68A9294P1	450NS
G10	32K X 8 RAM	68A9411P1	100NS
G11	64K EPROM	68A9404P1	200NS
G12	32K X 8 EEPROM	68A9442P1	350NS

53. HUMB BERG SETTINGS

J1 Oscillator enable (set to 'IN')
(#) JS Access time (one per quad, set per devices in each quad)
(#) J Enable quad (Put J in 'DIS' for unused QUADS)
(#) JD Memory base address (*) set to T = MSB in address = 2, F = 0
(#) JE Memory base address (*) set to T = MSB in address = 4, F = 0
(#) JF Memory base address (*) set to T = MSB in address = 8, F = 0
(#) J10 Segment select (*) set to T = 1 for segment number, F = 0
(#) J11 Segment select (*) set to T = 2 for segment number, F = 0
(#) J12 Segment select (*) set to T = 4 for segment number, F = 0
(#) J13 Segment select (*) set to T = 8 for segment number, F = 0

(#) There is one of these bergs for each quad
(*) If more than one memory address jumper and/or more than one segment select jumper is set to 'T', then add their values together to arrive at proper address and/or segment value(s).

NOTES:
See table 1 in step 52 for list of daughter boards vs access times vs memory devices vs GE part numbers.

If an HUMB card has a pair of 32K X 8 RAM or EEPROM chips in any given quad with a G8, G10 or G12 daughter board then the following will apply:
If the chips are in U23 & U25 or U27 & U29 or U31 & U33 or U35 & U37 then these chips will show up in memory map per J10-J13 of each quad.
If the chips are in U24 & U26 or U28 & U30 or U32 & U34 or U36 & U38 then these chips will show up in memory map one segment higher than called for by J10-J13 of each quad.

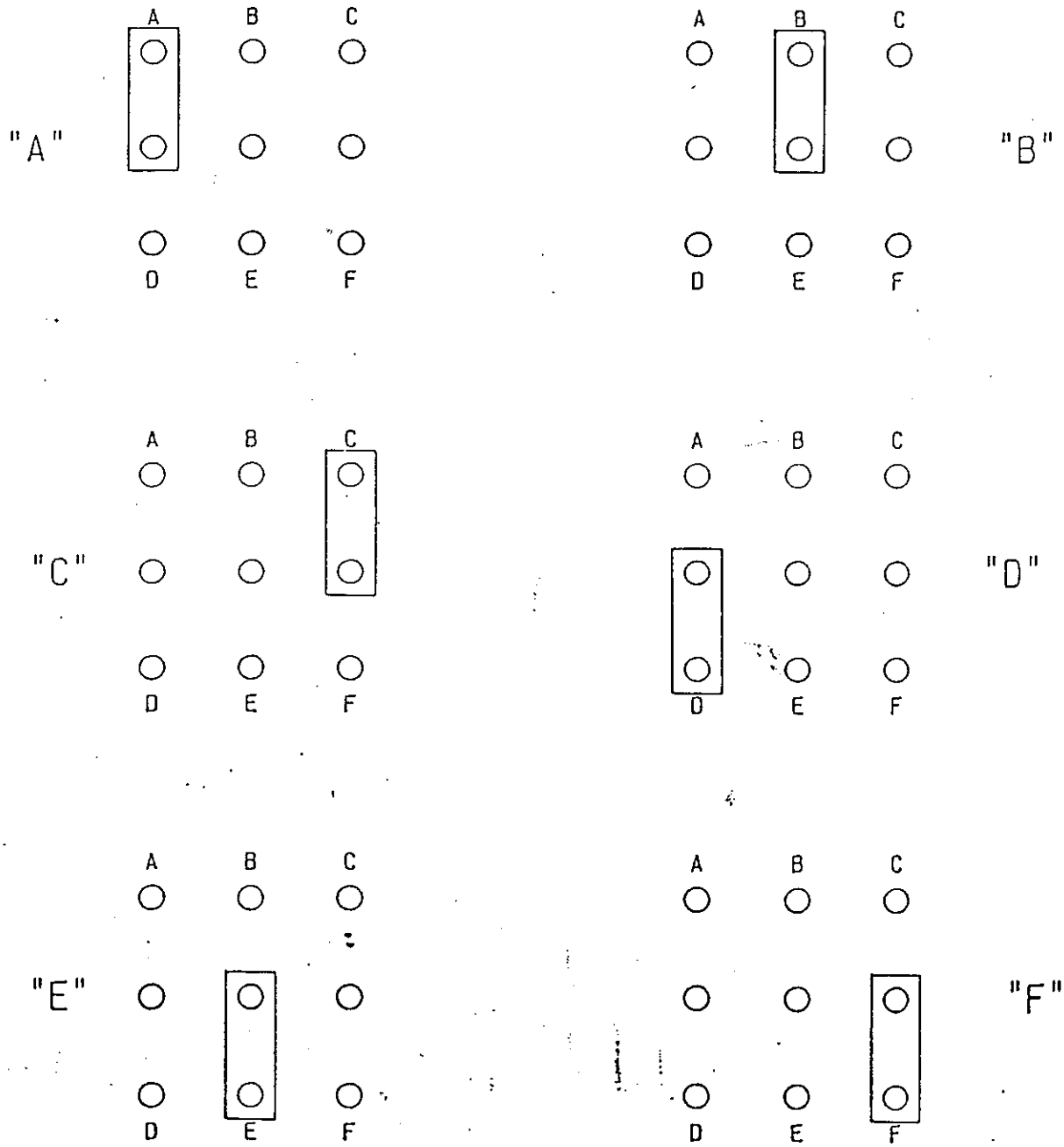
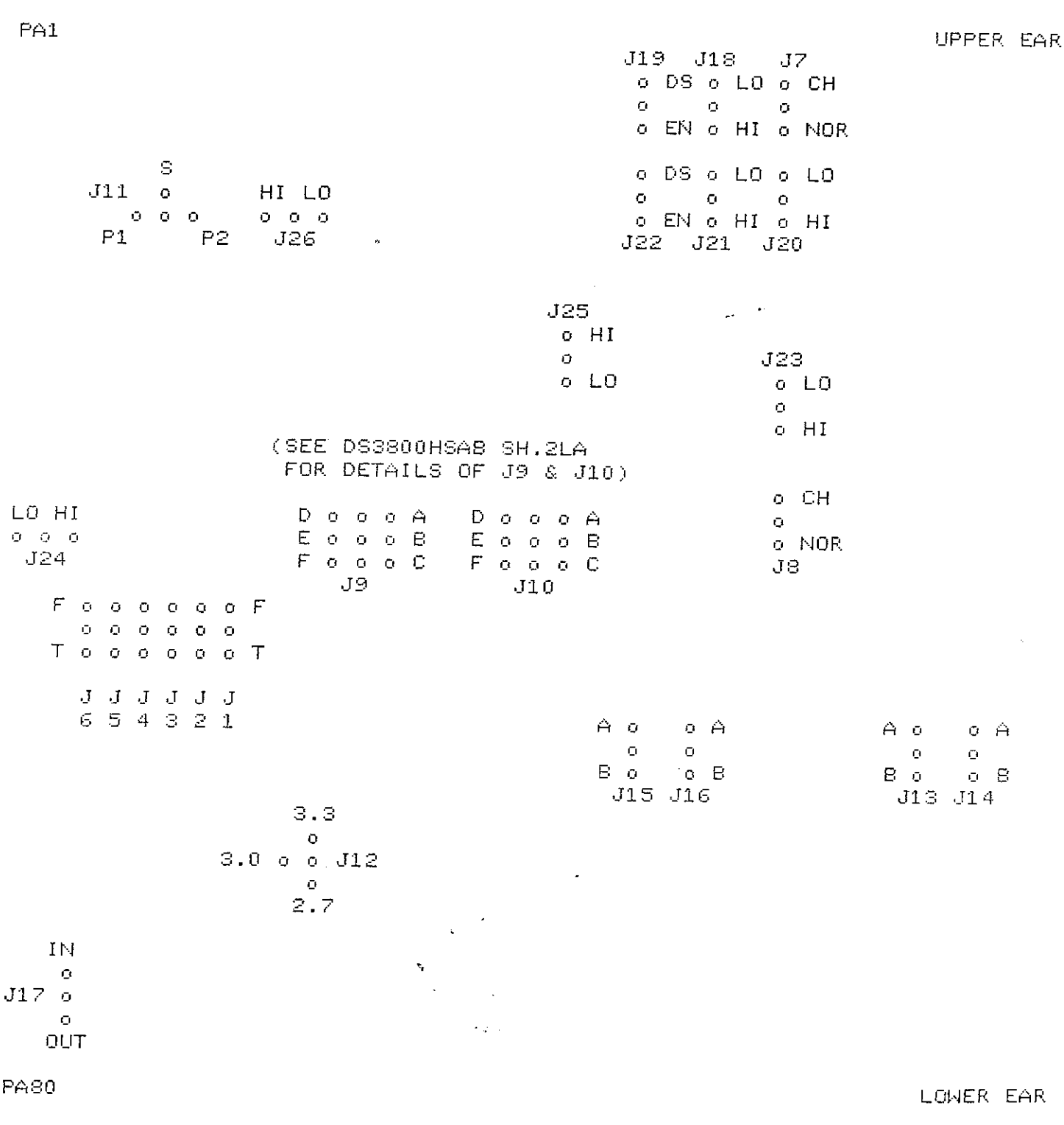


FIGURE 2 : SETTINGS FOR BERG JUMPERS J9 AND J10.

REV.1	REV.4	REV.7	PRINTS TO DL102	ENGINEER LSB	
REV.2	REV.5	ISSUED Jan 29, 1987		GENERAL ELECTRIC	APPLICATION NOTES SERVO VALVE
REV.3	REV.6				

ADDENDUM TO STEP 51, PHYSICAL LAYOUT OF HSAB BERG JUMPERS



EXP chan 0000 | output 1011 will show Ref2 on channel 0
(ENABLE BIT)

Channel 0000 - 1111
0 - 15

C. Check for REF1 and REF2 into HAIA/C by setting up the conditions in step B then go to user monitor and call HAIA test at the appropriate address then 'AN' test then appropriate channel XXXX into HAIA/C (based on which HSAB is being tested) and circuit #000 to read REF1 value on CRT. To test REF2 put in appropriate channel XXXX and circuit #011 to read REF2 value on CRT. Exercise at different voltages. Voltage read should be within 1%.

ADDR 8200

D. Check for output at CUR1 and CUR2 which are fed by REF1 and REF2. Set up REF1 and REF2 for 2.5v (1FFF) and monitor JA12 to 18 and JA 14 to 16 respectively for an output of approx. 40 ma. Change REF1 and REF2 to -2.5v (DFFF) and read approx. -40ma at JA output points. Set up REF1 and REF2 for approx. 1V (0CCC) then check for approx. 25ma. from JA12 to JA18 and JA14 to JA16 respectively. While the meter is connected call up HAIA test at appropriate address and channel and circuit #010 and #101 respectively to read approx. 1.25V at CUR1 and CUR2.

MUST close Relay By Taking PA4 To Ground

Meter Must be hooked to the Circuit Being tested to Complete Circuit

E. Check for output at POS1 and POS2 by putting a 1vdc signal on JA 7 to JA 5 and JA 9 to JA 11 and monitor TP2 to TP7 and TP5 to TP7 respectively to read approx. -1.5vdc.

7 to 5
9 to 11

F. Check for POS1 and POS2 into HAIA by setting up the conditions in step E then go to user monitor and call HAIA test at the appropriate address then 'AN' test then appropriate channel XXXX and circuit #001 to read POS1 and appropriate channel XXXX and circuit #100 to read POS2.

G. Check for fixed +5V into HAIA/C by selecting user monitor and HAIA test at appropriate address and 'AN' test at the appropriate channel XXXX and circuit #110. Should read +5V.

H. With an 88 ohm load across JA19 (ACOM) to JA20 check for 7.07VRMS +/- 1% and 3.0 KHZ +/- 5HZ.

I. Call up HAIA test with appropriate address, use AN test then channel per elem. and circuit #111. Verify -3.0V +/- 1%.

51. HSAB TEST ----------

A. Set berg jumpers as follows: (See sheet 34 for physical layout of berg jumpers.)

Slot 2G
ADDR = 8100
J1 = T
J2-J6 = F

J1 - J6 = desired address, the range is from 8000-BF00
The address word is structured as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	0	J6	J5	J4	J3	J2	J1	X	X	X	X	X	X	?	X

? > 0 = REF1 - TP1
? > 1 = REF2 - TP4

J7 - CHR/NOR = NOR
J8 - CHR/NOR = NOR
J9 - A-F = D for 6.3v/v gain
J10- A-F = D for 6.3v/v gain
J11- P1/P2/S = S
J12- 2.7/3.0/3.3 = 3.0
J13- A/B = A for 40 ma. sat. curr.
J14- A/B = A for 4 ma/v gain
J15- A/B = A for 40 ma. sat. curr.
J16- A/B = A for 4 ma/v gain
J17- IN/OUT = IN
J18- LO/HI = HI
J19- EN/DS = EN
J20- LO/HI = HI
J21- LO/HI = HI
J22- EN/DS = EN
J23- LO/HI = HI
J24- LO/HI = LO
J25- LO/HI = LO
J26- LO/HI = LO

B. If bergs J1-J6 are set for ~~8000~~ 8100, set port address to ~~8000~~ 8100 and monitor TP1 (REF1) to TP7 (ACOM) for desired voltage then set port address to ~~8000+2~~ 8102 and monitor TP4 (REF2) to TP7 (ACOM) for desired voltage. Proceed as follows to set the port address and desired voltage. Try several different voltages and be sure that voltages read are within 1%.

Push RETURN until	CRT responds >
Type I for I/O	Crt responds with I>
Type W for write	CRT responds PORT ADDR ? %
* Type ~~8000~~ 8100 or ~~8002~~ 8102 RETURN	CRT responds BYTE I/O ?
Type N for NO RETURN	CRT responds COUNT ?
Type 1 RETURN	CRT responds VALUE ? %
Type 3FFF for 5V or 7FFF for 10V or 8000 for -10V or C000 for -5V then RETURN	CRT displays COMMAND COMPLETE

* Put in the appropriate addresses based on where J1-J6 are set.

W, 810x, N, 1, Data

5Ø. DS3820DPA TEST (DMC/process & uPSS panel)

A. Tests for forms C & D
Use 'TEST' DMC MEM and connect a 1Ø pin ribbon cable from DPA JC to 'TEST' DMC header connector JDA.

B. Connect two 2Ø pin ribbons from DPA JA, JB to HXPC/D JA, JB respectively.

C. Select HLOA test from user monitor, base address +6H (9ØØ6). Ripple test, 2 cycles at 1ØØØ msec. The LEDs should cycle ON-OFF-ON.

BIT PATTERN:

Ø	1	3	2
*	*	*	*

* There will be a 12 second delay between cycles.

D. Select HLIA test from user monitor, base address +6H (9ØØ6).

E. Set key sw. to 'NORMAL' Bit pattern = 1111 1111 1110 1111

F. Set key sw. to 'TEST' Bit pattern = 1111 1111 1101 1111

G. Depress sw. 'OFFLINE' Bit pattern = 1111 1111 1101 1110

H. Depress sw. 'ONLINE' Bit pattern = 1111 1111 1101 1101

59. SSPD SEM TEST ----------(DS382ØSSPD)
This test is to be done in ESA ONLY if there are no 77MM SILCO panels on final floor which can be utilized to test this SEM.
Berg settings:

HFPB (slot c)
J1 = 4K
J2 = ROM
J3 = 4K
J4 = ROM

HFXA (slot d)
J1 = 1
J2 = L
J3 = ROM
J4 = ROM
J5 = ROM
J6 = ROM

HFXB (slot e)
BJ3 = GND (not NC)
BJ4 = NC (not PWR)
BJ5 = POSITION C AND E
BJ6 = POSITION B

Power test:
Connect power cable to JA on SEM
Connect communication cable to JB conn. on HFXB
Set terminal for 3ØØ baud rate, 7 data bits, 2 stop bits

Apply power and observe the following:
]IØ-SELFTEST COMPLETE: COMPUTER OK
]I1-SYSTEM INITIALIZED
]AØ-BRIDGE TEST FAULT: NO PLL SYNC (CHECK AC POWER)
]CC-SPARE 1 INPUT ACTIVATED
]C6-POWER SUPPLY INTERLOCK SET
]CB-TRANSFORMER OVER TEMP
]C5-HIGH AMBIENT TEMP OR FEEDBACK OPEN
]CA-FAN LOSS
]C4-PLL INTERLOCK SET
]CØ-DC BREAKER OPEN
]EI-P5 SUPPLY BUS HIGH

END OF TEST, T-STAMP MOD.