REV NO. 0

P3K-AL-0439-A01

CONT ON SHEET 2 SH NO. 1

TITLE

TEST INSTRUCTIONS FOR LOADING RATES AND LOAD SET LIMITS CIRCUIT 1L1-D002 (ASSEMBLY DRAWING 125D3615 G1)

FIRST MADE FOR EHC MARK II

125D3615 >
118D1380

REVISIONS

I. SCOPE

This instruction outlines the test specifications for circuit board 1L1-D002 (Ref. Drawing 125D3615 G1 - Schematic 118D2107).

II. CIRCUIT DESCRIPTION

The loading rates and Load Set Limits Circuit impose rate of change and load level limitations on the load set signal in order to produce the load reference signal.

This circuit is used only on those turbines which have starting and loading on the control valves.

The Loading Rates and Load Set Limits Circuit has as an input the Load Set Signal which is amplified by a variable gain operational amplifier designated the Load Set Amplifier.

A second set of inputs to the board are biases for 10, 5, 3, 1, and 0.5 percent loading rates. These bias voltages are applied to an integrator type operational amplifier designated the Loading Rate Integrator.

The two operational amplifiers are gated together in a low value gate. Operation of this gating is such that only the operational amplifier which is in control of the board's output voltage, is out of negative saturation.

The circuit board contains a power output stage to provide output current capacity to drive up to a 2.2K ohm load.

ACTIVE FOR Test

BY DC DATE 7/21/77

273-2
273-1
273-7
273-1
273-2
273-2
PRINTS

MADE J Polacek SEP 21 1977

ISSUED SEP 22 1977

APPROVALS

Steam Turbine DIV OR DEPT.

Schenectady, N.Y. LOCATION

P3K-AL-0439-A01

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REVISIONS

III. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

1. Power Supply 1: (Pin 37) +22.000 ± 0.002 VDC at 220 ma (approximately)

2. Power Supply 2: (Pin 41) -22.000 ± 0.002 VDC at 150 ma (approximately)

B. Operating Signal Levels

1. Input 1 (Load Set Signal): (Pin 35) 0 to +2.000 VDC (0 volts at No Load) (+2 volts at Full Load)

2. Input 2 through 6: +22.000 VDC for specified condition, 0 VDC otherwise.

a. Input 2 (Pin 30): Main Circuit Breaker Open

b. Input 3 (Pin 31): 10%/minute loading rate selected can be adjusted for 5%/minute if required.

c. Input 4 (Pin 32): 3%/minute loading rate selected.

d. Input 5 (Pin 33): 1%/minute loading rate selected.

e. Input 6 (Pin 34): 0.5%/minute loading rate selected.

C. Output Load

1. Load 1 (Pin 16): 2.2K Ohm ± 1% (Max. load)

2. Load 2 (Pin 38): 1 Meg Ohm ± 1%

3. Load 3 (Pin 29): 1 Meg Ohm ± 1%

D. Individual Stage Performance Specification

1. Power Supply (CR1, 2, 3, and 4) (R1 and R2)

a. TP1: +18.7 ± 1.1 VDC

b. TP2: -18.7 ± 1.1 VDC

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REV NO. 0
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TITLE
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REVISION

III. CIRCUIT SPECIFICATIONS (continued)

D. Individual Stage Performance Specification (continued)

2. Load Set Amplifier (IC2, Q1)
(IC3 saturated and not controlling TP6)

Pin 4 to (22 V) to pin 31

a. Acceptable offset at TP6
(zero input): ± 1.0 MV DC

b. Low GAIN Transfer Function for Load Set Signal (R11, R12, R14, C3, TP6, TP12) (VR2 full CCW).

not for 116D1360

$$\frac{TP6}{TP12} = \frac{-G_3}{1 + T_3 S}$$

1 V to pin 35

Where: Gain (G3) = 4.031 ± 0.081 volt/volt
Noise Suppression lag time constant (T3) = 1.65 ± 0.18 msec.
Noise Suppression lag breakpoint (F3) = 97.5 ± 10.7 HZ

c. High Gain Transfer Function for Load Set Signal R11, R12, R14, C3, TP6, TP12)
(VR2 full CW)

$$\frac{TP6}{TP12} = \frac{-G_4}{1 + T_4 S}$$

SET GAIN FOR -10.0 V/V with VR2

Where: Gain (G4) = 14.042 ± 1.181 volts/volt
Noise Suppression Lag Time constant (T4) = 1.65 ± 0.18 msec.
Noise Suppresssion lag breakpoint (F4) = 97.5 ± 10.7 HZ

d. Soft Floor Limit (R30, R31, CR15, TP5)
(TP6, and TP12 grounded for standardization)

TP5 voltage = -13.29 ± 0.27 VDC

e. Saturation Limits (TP5): +16 VDC (minimum)
-13.29 VDC (approximately)

f. Voltage drop across CR10 (TP5, TP7): 0.7 VDC (approximately)

3. Loading Rate Integrator (IC3, Q1)
(IC2 saturated and not controlling TP6)

a. Acceptable Offset at TP6
(Zero Input): ± 1.0 MV DC

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III. CIRCUIT SPECIFICATIONS (continued)

D. Individual Stage Performance Specification (continued)

3. (continued)

b. Transfer function for circuit breaker open signal (R15, R16, R36, C4, C6, C7, C8, TP6, TP9)

$$\frac{TP6}{TP9} = \frac{-G_5 \ (1+T6\ S)}{S\ (1 + T5\ S)\ (1 + T7\ S)}$$

Where: Gain (G5) = 0.0251 $\pm$ 0.0015 Volts/Volt
Noise Suppression lag time constant (T5) = 1.86 $\pm$ 0.21 msec
Noise Suppression Breakpoint (F5) = 86.4 $\pm$ 9.5 HZ
Lead Time Constant (T6) = 47 $\pm$ 3 usec
Lead Breakpoint (R6) = 3396.8 $\pm$ 203.7 HZ
Lag Time Constant (T7) = 47 $\pm$ 3 usec
Lag Breakpoint (F7) = 3397.3 $\pm$ 203.7 HZ

c. Transfer Function for loading rate bias (R22, T23, R36, C5, C6, C7, C8, TP6, TP10)

$$\frac{TP6}{TP10} = \frac{-G6\ (1 + T9\ S)}{S\ (1 + T8\ S)\ (1 + T10\ S)}$$

Where: Gain (G6) = 0.0085 $\pm$ 0.0005 Volts/Volt
Noise Suppression lag time constant (T8) = 1.77 $\pm$ 0.19 msec
Noise Suppression Lag breakpoint (F8) = 91.2 $\pm$ 10.0 HZ
Lead Time constant (T9) = 47 $\pm$ 3 usec
Lead breakpoint (F9) = 3396.8 $\pm$ 203.7 HZ
Lag breakpoint (T10) = 47 $\pm$ 3 usec.
Lag breakpoint (F10) = 3397.3 $\pm$ 203.7 HZ

d. Soft floor limit (R28, R29, CR11, TP8)
(TP6, TP10 grounded for standardization.

TP8 voltage = -13.94 $\pm$ 0.28 VDC

e. Saturation Limits (TP8): +16 VDC (minimum)
-13.94 VDC (approximately)

f. Voltage drop across CR14 (TP7, TP8): 0.7 VDC (approximately)

III. CIRCUIT SPECIFICATIONS (continued)

D. Individual Stage Performance Specification (continued)

4. 10%/Minute Loading Rate Bias
(R17, R21, R22, R23, VR3, TP10)

VR3 Full CW: 3.666 ± 0.061 VDC
VR3 Full CCW: 0.720 ± 0.104 VDC

5. 5%/Minute Loading Rate Bias
(R17, R21, R22, R23, VR3, TP10)

Can be adjusted for 5%/Minute where required.

6. 3%/Minute Loading Rate Bias
(R18, R21, R22, R23, VR4, TP10)

VR4 Full CW: 0.889 ± 0.017 VDC
VR4 Full CCW: 0.444 ± 0.029 VDC

7. 1%/Minute Loading Rate Bias
(R19, R21, R22, R23, VR5, TP10)

VR5 VR4 Full CW: 0.326 ± 0.006 VDC
VR4 Full CCW: 0.132 ± 0.010 VDC

8. 0.5%/Minute Loading Rate Bias
(R20, R21, R22, R23, VR6, TP10)

VR6 Full CW: 0.188 ± 0.004 VDC
VR6 Full CCW: 0.061 ± 0.005 VDC

9. Load Set Amplifier Divider
(R32, R33, -10.000 VDC at TP5) (1 meg ohm load)

Pin 38 = -4.951 ± 0.050 VDC

10. Loading Rate Integrator Divider
(R34, R35, -10.000 VDC at TP8) (1 meg ohm load)

Pin 29 = -4.951 ± 0.050 VDC

IV. SET POINTS

A. Adjustment of VR2

This resistor sets the gain of the load set amplifier to compensate for output variations in load set transducer and demodualtor.

VR2 should be adjusted for a DC gain, from TP12 to TP6, of -10.000 volts/volt.

B. Adjustment of VR3 - 10%/Minute Rate

Set VR3 to produce 1.961 VDC at TP10. This will set a loading rate of the Loading Rate Integrator of 10.000 $\pm$ 0.588%/Minute.

C. Adjustment of VR3 - 5%/Minute Rate (when required)

Set VR3 to produce 0.981 VDC at TP10. This will set a Loading Rate of the Load Rate Integrator of 5.00 $\pm$ 0.299%/Minute.

D. Adjustment of VR4

Set VR4 to produce 0.588 VDC at TP10. This will set a loading rate on the Loading Rate Integrator of 3.000 $\pm$ 0.177%/Minute.

E. Adjustment of VR5

Set VR5 to produce 0.196 VDC at TP10. This will set a loading rate on the Loading Rate Integrator of 1.000 $\pm$ 0.059%/Minute.

F. Adjustment of VR6

Set VR6 to produce 0.098 VDC at TP10. This will set a loading rate on the Loading Rate Integrator of 0.500 $\pm$ 0.029%/Minute.

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1L1-D002 (ASSEMBLY DRAWING 125D3615 G1)

FIRST MADE FOR EHC MARK II

REVISION

TEST INSTRUCTION
PREPARED BY J. Dombrosky DATE 4-10-75
J. Dombrosky
EHC DESIGN ENGINEERING

TEST PROCEDURE
APPROVED BY P C Callan DATE 9-12-77
P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE
REVIEWED BY R. W. Debertolis DATE 9-9-77
R. Debertolis
EHC TEST ENGINEER

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