REV NO. A

68A9443934
CONT ON SHEET 2 SH NO. 1

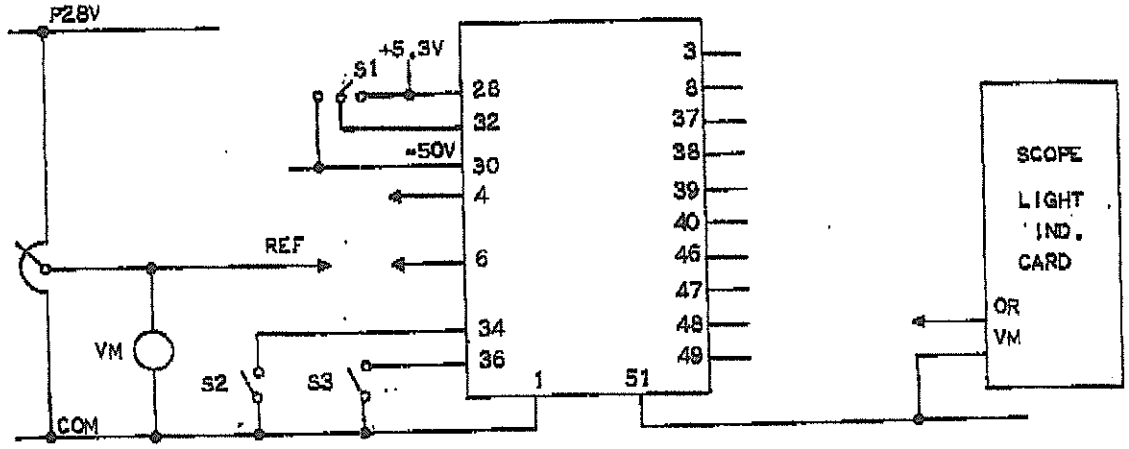
TITLE
TEST SPECIFICATIONS
REV. LOGIC AND STATIC IOC
FIRST MADE FOR IC3600TRLM1

REVISIONS

ELEMENTARY - IC3600TRLEM SH. 3.0

POWER INPUT - P5.3V TO PIN 28
COMMON TO PIN 1 AND 51
N50V TO PIN 30
P28V REF.

CONNECT CARD IN TEST CIRCUIT SHOWN BELOW.



1. TEST FOR CONFORMANCE WITH FOLLOWING TABLE

TOLERANCE ON ALL REF. VOLTAGES ± 5%
ON SWITCH S1 - X= CLOSED TO PIN 28. O= CLOSED TO -50V CIRCUIT.

X=CLOSED O=OPEN			REFERENCE INPUT		SET TRIMPOTS R1 AND R2 AS	1 INDICATES VOLTAGE AT PIN =4.5V ± 1V O INDICATES VOLTAGE AT PIN ≤1 VOLT									
S1	S2	S3	VOLTS	TO PIN	INDICATED BELOW	3	8	37	38	39	40	46	47	48	49
O	X	X	0	4&6	FULLY CW	1	1	1	0	0	1	1	0	1	0
X	X	X	0	4&6	" "	1	1	0	1	1	0	1	0	1	0
X	X	X	.15	6	" "	1	1	1	0	0	1	1	0	1	0
O	X	X	.15	4	" "	1	1	0	1	1	0	1	0	1	0
O	X	X	.15	4&6	" "	1	1	1	0	1	0	0	1	1	0
O	X	X	18	.4	ADJUST R2 TO OBTAIN O AT PIN 48	1	1	←	O	M	I	T	→	0	1
O	X	X		6	R2 SAME SETTING DETERMINE REF INPUT VOLTAGE TO PIN 6 WHICH CAUSES O SIGNAL AT PIN 48 ← (18V ± 1V)	1	1	←	O	M	I	T	→	0	1
REMOVE REFERENCE VOLTAGE															
O	X	X		4&6	SET R1 MAX CLOCKWISE POSITION AND FIND REF INPUT VOLTAGE TO CAUSE O SIGNAL AT PINS 3 AND 8. (24V ± 1V)	0	0	←	O	M	I	T	→	0	1

SEE TECH NOTES

1 MEM 10/28/72

4043
1338
2520

PRINTS TO

MADE BY GARY HARRIS
ISSUED 2-21-72
APPROVALS M.B. Jarman
INDUSTRY CONTROL DIV OR DEPT.
SALEM, VIRGINIA LOCATION
68A9443934
CONT ON SHEET 2 SH NO. 1
CODE IDENT NO

FF-802-WF (11-68)
PRINTED IN U.S.A.

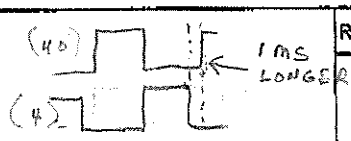
REV NO. A

68A9443 94

CONT ON SHEET FL. SH NO. 2

TITLE
TEST SPECIFICATIONS
REV. LOGIC AND STATIC IOC
FIRST MADE FOR 103600TRLM1

REVISIONS



2. CHECK TIME DELAYS

A. WITH S1 TO NEG. REF AND S2 AND S3 CLOSED, APPLY 5V PEAK TO PEAK, 60 HZ SQUARE WAVE TO PIN 4 WITH RESPECT TO PIN 51. USE DUAL CHANNEL SCOPE TO MEASURE TIME DELAY BETWEEN TRAILING EDGE OF INPUT PULSE AND RISING EDGE OF OUTPUT PULSE AT PIN 40. PULSE AT PIN 40 MUST STAY NEGATIVE FOR 1MS ± .3 MS. AFTER INPUT PULSE HAS GONE NEGATIVE.

B. CLOSE SWITCH S1 TO PIN (38) AND CONNECT WAVE TEK OUTPUT TO PIN 6. TIME DELAY BETWEEN FALLING PULSE AT PIN 6 AND RISING PULSE AT PIN 38 MUST BE 1 MS ± .3 MS.

* C. REMOVE WAVE TEK, SET DC REF. TO 20V AND MOMENTARILY APPLY REF. TO PIN 4. USE SCOPE TO DETERMINE THAT VOLTAGE AT PIN 48 REDUCES TO LESS THAN 1 VOLT WHEN REF. IS APPLIED AND STAYS LESS THAN 1 VOLT FOR AT LEAST .5 SEC., EVEN THOUGH REF. WAS ONLY MOMENTARILY APPLIED. REPEAT ABOVE TEST EXCEPT WITH INPUT REF. APPLIED TO PIN 6.

NOTE: TIME DELAY STARTS TIMING OUT AS SOON AS REF. IS APPLIED SO REF. MUST BE REMOVED IN LESS THAN .5 SEC.

NOTE: REMOVE ±67V POWER AND AC REFERENCER BEFORE INSERTING OR REMOVING CARD FROM TEST FIXTURE.

* SEE NOTES

PSA
1336
2520

PRINTS TO

MADE BY GARY HARRIS
ISSUED 2-21-72
APPROVALS
INDUSTRY CONTROL DIV OR DEPT.
SALEM, VIRGINIA LOCATION
68A9443 94
CONT ON SHEET FL. SH NO. 2
CODE IDENT NO

FF-602-WF (11-68)
PRINTED IN U.S.A.

TECH NOTES

IC 2 - MC836
IC 3 - MC836
IC 4 - MC836
IC 4 - MC846
IC 5 - MC846
IC 6 - MC846

} IC TYPES

HAVE HAD SEVERAL CARDS WITH INCORRECT LOGIC ON THE FIRST STEP OF THE CHART OF STEP #1, MAINLY INVOLVING PINS 37, 38 AND 39, 40. THESE WERE TRACED TO BAD CONNECTIONS ON THE "THRU THE BOARD" CONNECTIONS UNDER U2 - U6. RESOLDERING THE EYELETS UNDER THE ICS RESTORES THE CARD TO CORRECT OPERATION. 9-13-01 DAL

ON SOME CARDS THE REF VOLTS INPUT IN STEP 2C MUST BE 20V AT PIN 4 OR PIN 6. AN OPEN CIRCUIT SETTING OF THE 10K TEST POT TO 20V WILL DROP VOLTS TO 16 OR SO AND THE CIRCUIT WILL NOT TRIP TO LOWER PIN 48 TO ZERO.

TECHNICIAN: _____ **DATE:** _____