GENERAL ELECTRIC

277A3758

CONT ON SHEET 2 SH NO. 1

REV NO.

277A3758

CONT ON SHEET 2 SH NO. 1

TITLE Test Specifications
FREQUENCY TRANSDUCER

FIRST MADE FOR 44C331856G01

REVISIONS

STANDING INSTRUCTIONS
FOR
FREQUENCY TRANSDUCER

Printed Circuit Board
for
Power System Stabilizer

44C331856G01

Distribution:

1 QC Engineering
1 QC Test
1 Engineering

3EL1
4QA3
1RA2
4EK1

PRINTS TO

MADE BY RR Gerlitz 781011

ISSUED 10-13-78

APPROVALS RKG 10-11-78

Drive Systems SW OR DEPT.

Salem, VA. U.S.A. LOCATION

277A3758

CONT ON SHEET 2 SH NO. 1

CODE IDENT NO.

FF-603 WF (11-77)
PRINTED IN U.S.A.

REV NO.

277A3758

CONT ON SHEET 3 SH NO. 2

TITLE Test Specifications
FREQUENCY TRANSDUCER

FIRST MADE FOR 44C331856G01

REVISIONS

I. Test Equipment Required

A. Printed Circuit Board Test Setup 44C931365.

B. Adaptor Cable - Amp Mod II - 30 pin.

C. Adaptor Cable - Power Supplies.

D. Patchboard PB1.

E. Drawings

44C306562	Elementary
44B331728	Assembly
44C931365	Test Fixture

II. Connection

A. Connect the Amp Mod II 30 pin adaptor to "PL1" on the Universal Tester (U.T.).

B. Connect the power supply cable to "PL3" on the U.T. and to power supplies per lead markings.

C. Insert patchboard PB1 into carrier and close.

D. Connect a Digital DC Voltmeter to "BJ-1". Red (+) and Black (-).

E. Connect WAVETECH TO "BJ-11 ON TGE U.T.

III. Wire Check

Test Point	Pin	Resistance (Ohms)
1N(IN)	11	0
12TP	1	0
11TP	5	0
Out	15	0
3TP	17	150 ± 15
In/Out Ground	3	0

Visual Check

40R	7.5K
22R	33K
3R	220

All electrolytic capacitors for proper orientation.

3EL1
4QA3
1RA2
4EK1

PRINTS TO

MADE BY RK Gerlitz 781011
ISSUED 10-13-78

APPROVALS R Ick 10-11-78

Drive Systems DIV OR DEPT.
Salem, VA. U.S.A. LOCATION

277A3758
CONT ON SHEET 3 SH NO. 2
CODE IDENT NO.

FF-803 WF (11-77)
PRINTED IN U.S.A.

IV. Setup

A. Place all switches to OFF on the U.T. and the Universal Power Supply (UPS).

B. Turn all power supplies to zero and all variacs to zero.

C. Apply power to the Test Stand.

D. Connect jumper 1S Ter. 2 to Ter. 3.

V. Electrical Test

~~A. Close "SW-1" and depress "LPB-10". Adjust PS1 to 24 ±0.5 VDC at "BJ-1".~~ NOT USED.

~~NOTE: Should it become necessary to remove all DC power, open "SW-1".~~

B. Depress "LPB-2" and adjust PS-2 to 15 ±0.05 VDC at "BJ-1". — APPLY +15VDC to PIN 1

C. Depress "LPB-3" and adjust PS-3 to 15 ±0.05 VDC at "BJ-1". — APPLY -15VDC to PIN 5
— CONNECT 15V RETURN to PIN 3

~~D. Place "SW-9" down.~~

E. Set waveteck fir 35 +/- 1mv RMS 60HZ sine wave at 11 to 3. — CONNECT PIN 7 to PIN 1
CONNECT PIN 4 to PIN 3

verify 1TP is approxamately 9VDC

Slowly turn 1P CW until a square wave appears at 1TP

Slowly lower the waveteck voltage just to the point where the square wave at 1TP goes to a steady 9VDC

Slowly turn 1P more CW until the square wave reappears and then slowly lower the waveteck voltage until the square wave again foes to a steady 9VDC

Repeat turning 1P CW and lowering the waveteck voltage per above until the point is reached where the turning 1P CW causes the signal at 1TP to fo to a steady OV instead of a square wave.

Substitute attached step E.
ame 9/7/99

REVISIONS

3EL1
4QA3
1RA2
4EK1

PRINTS TO

1P ~~CCW~~ opposite rotation
on MC MOD ONLY ADM 911211

E. Set 1P fully ~~CCW~~ CW

56mVP-P

Set wavetek for 35 +/- 1mv RMS 60HZ sine wave at [11] to [3].

Verify 1TP is approximately ~~9VDC.~~ >=9Vdc (13.96✓

Slowly turn 1P~~C~~CW until a square wave appears at 1TP.

Slowly lower the wavetek voltage just to the point where the square wave at 1TP goes to a steady ~~9~~VDC. ~~HV~~ >=9VDC

Slowly turn 1P more~~C~~CW until the square wave reappears and then slowly lower the wavetek voltage until the square wave again goes to a steady ~~9~~VDC. ~~HV~~ >=9V

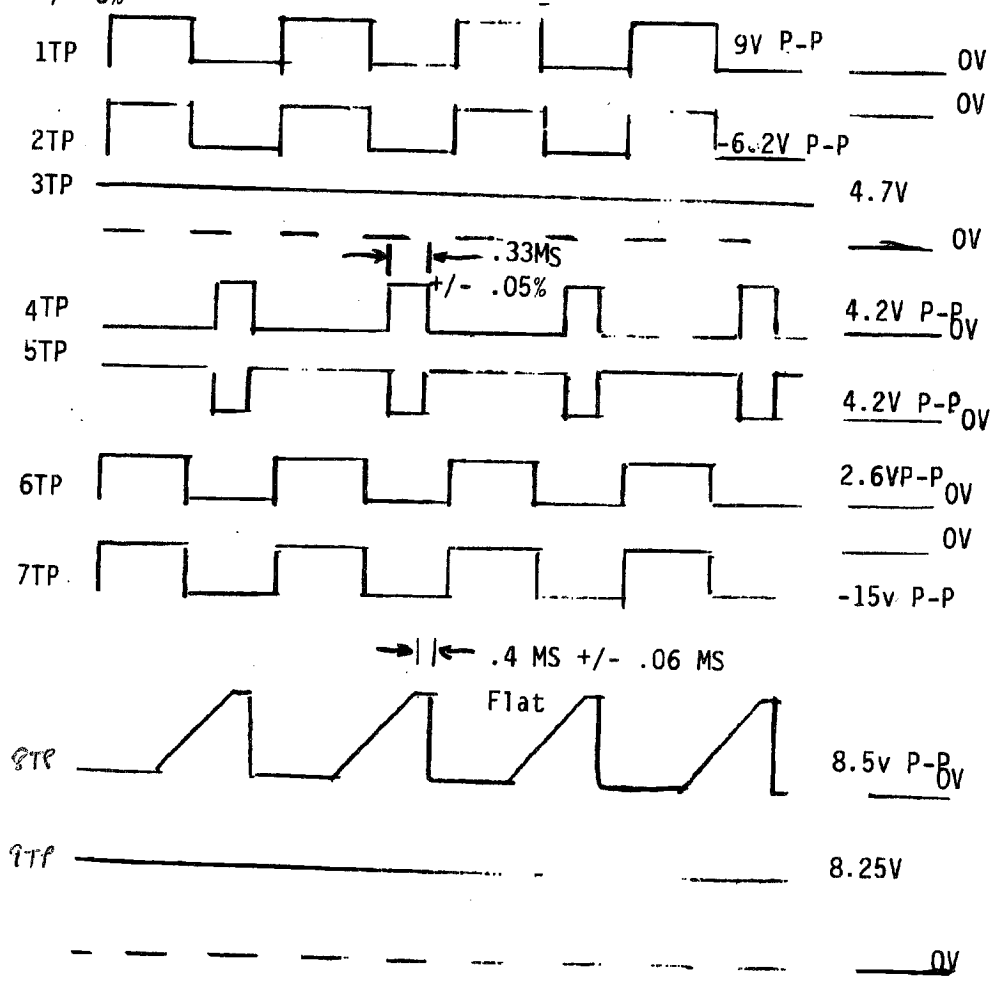
Repeat turning 1P~~C~~CW and lowering the wavetek voltage per above until the point is reached where the turning 1P~~C~~CW causes the signal at 1TP to go to a steady 0V instead of a square wave.

Adjust wavetek to 6VRMS 60HZ

Substitute new step E above for old step E on sheet 3 of 277A3758.

.086
116
202

F. Check the following waveforms with an oscilloscope. All measurements +/- 5%



REVISIONS

G. Adjust WAVETECH output to 3 ± 0.1 V peak at "BJ-10". Connect the oscilloscope to TP9. This waveform should be 8.25 ± 0.41 VDC. 7.84 ↔ 8.66 VDC

Switch the oscilloscope to AC and increase the sensitivity observing the notch created by the sample and hold circuit.

Adjust 2P for equal positive and negative amplitude of this notch above and below the nominal voltage of 8.25 volts.

H. Connect the oscilloscope to "OUT" Test Jack. Adjust WAVETECH output to 8.48 ± 0.05 V peak 60 Hz ± 0.1 at "BJ-10".

Adjust 4P for zero output at OUT Test Jack. ØVDC.

I. Increase the WAVETECH frequency to 63 ± 0.1 Hz maintaining 8.48 ± 0.01V peak at "BJ-10".

Adjust 3P for 4.8 ± 0.2 volts D.C. at Out Test Jack

J. Decrease the WAVETECH frequency to 57 ± 0.1 Hz maintaining 8.48 ± 0.01V peak. The OUT Test Jack shall be -5.2 ± 0.2 volts D.C.

K. Change is jumper from 2-3 to 1-2.

L. Increase the WAVETECH frequency to 63 ± 0.1 Hz. Adjust 5P for 0.475 ± 0.02 volts DC at OUT Test Jack.

M. Decrease the WAVETECH frequency to 57 ± 0.1 Hz. The OUT Test Jack shall read -0.53 ± 0.02 volts D.C.

N. Reset WAVETECH frequency to 60 ± 0.1 Hz.

O.

A.C. Input	Freq.		Output (Scope)	Jumper
5 ± 0.5	60.6 Hz		x volts	1-2
5 ± 0.5	-59.4 Hz		-y volts	1-2
	1.2 Hz	=	0.2 ± 0.02 VDC	
5 ± 0.5	60.6 Hz		x volts	2-3
5 ± 0.5	-59.4 Hz		+y volts	2-3
	1.2 Hz	=	2.0 ± 0.2 VDC	

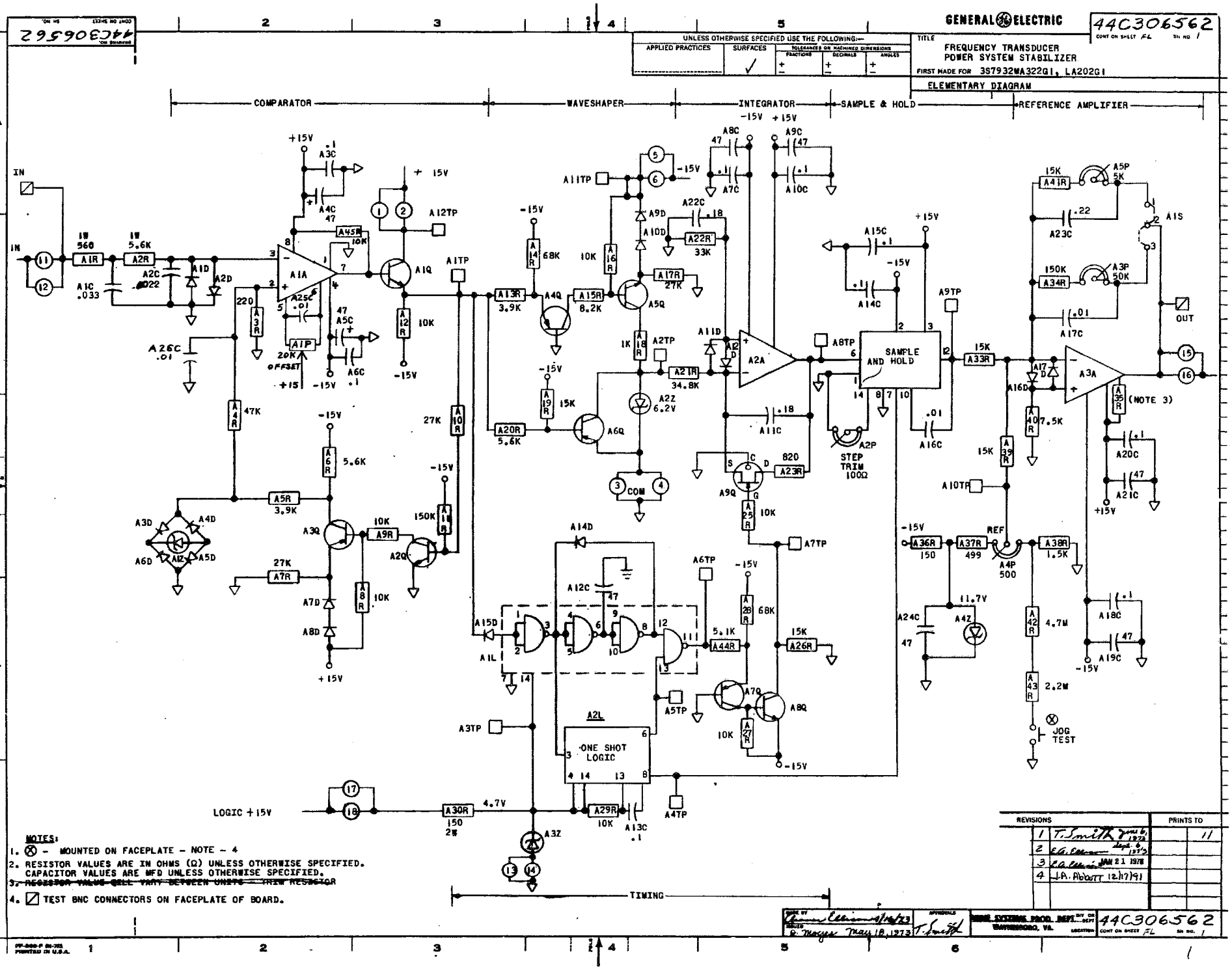
Short out 42R.

P. Connect DC voltmeter to 10TP. Depress "Jog Test" SW. Voltage at 10TP shall droop 0.001 to 0.002 VDC. Release "Jog Test" SW and voltage shall increase 0.001 to 0.002 VDC. Remove 42R jumper.

Q. Open "SW-1". Then all remaining switches. Turn all power supplies to zero.

3EL1
4QA3
1RA2
4EK1

PRINTS TO


44C306562
GENERAL ELECTRIC
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES
SURFACES
TOLERANCES ON MACHINED DIMENSIONS
FRACTIONS
DECIMALS
ANGLES
TITLE
FREQUENCY TRANSDUCER
POWER SYSTEM STABILIZER
FIRST MADE FOR 357932WA322G1, LA202G1
ELEMENTARY DIAGRAM
COMPARATOR
WAVESHAPER
INTEGRATOR
SAMPLE & HOLD
REFERENCE AMPLIFIER
SAMPLE AND HOLD
ONE SHOT LOGIC
TIMING
JOG TEST
STEP TRIM 100Ω
OFFSET
COM
LOGIC +15V
NOTES:
1. ⊗ - MOUNTED ON FACEPLATE - NOTE - 4
2. RESISTOR VALUES ARE IN OHMS (Ω) UNLESS OTHERWISE SPECIFIED. CAPACITOR VALUES ARE MFD UNLESS OTHERWISE SPECIFIED.
3. RESISTOR VALUE WILL VARY BETWEEN UNITS - TRIM RESISTOR
4. TEST BNC CONNECTORS ON FACEPLATE OF BOARD.
REVISIONS
PRINTS TO
1 T. Smith June 6, 1972
2 E.G. Clemens Sept. 6 1972
3 E.G. Clemens JAN 21 1978
4 J.A. Abbott 12/17/91
DRAWN BY R. Morgan May 18, 1973
APPROVALS T. Smith
POWER SYSTEMS PROD. DEPT. DIV. OR DEPT
WATERFORD, WI. LOCATION
44C306562
CONT ON SHEET FL SH NO. 1