Data Sheet

1/9/2012 CW

Job # 90007765			
Serial # ODB99C			Burn-in Start 6-9-12 @ 3:45 PM
Date 3-6-12			
Data Sheet for 115D3332G0001			Burn-in Stop 6-15-12 @ 9:00 AM
Test Procedure 83K-AL-0135-A02			Technician J. FRANCIS / WGC

Test Procedure Step	Nominal	Lower Limit	Pre-Burn in Results	Post Burn in Results	Upper Limit	Pot Values if applicable CW	Pot Values if applicable CCW	Pass/Fail	
2.III.D.CR3	+5.10 VDC	+4.84 VDC	+5.11VDC	+5.15	+5.35 VDC	*****	*****		
2.III.D.CR4	+9.00 VDC	+8.91 VDC	+9.01VDC	+9.03	+9.09 VDC	*****	*****		
2.III.D.CR5	+11.70 VDC	+11.11 VDC	+11.60VDC	+11.61	+12.28 VDC	*****	*****		
2.III.D.CR6	+16.00 VDC	+15.20 VDC	+15.37VDC	+15.58	+16.80 VDC	*****	*****		
2.III.D.CR7	+12.00 VDC	+11.40 VDC	+11.79VDC	+11.86	+12.60 VDC	*****	*****		
2.III.D.CR8	-16.00 VDC	-16.80 VDC	-15.44VDC	-15.53	-15.20 VDC	*****	*****		
4.B	0 V	*****	0VDC	0.000 V	*****	-73.3mVDC	+18.51 mVDC		R4
5.D	SQUARE WAVE	SQUARE WAVE	SQ. WAVE	6a wave 50mV P/P 100Hz	SQUARE WAVE	+3.0VDC	-.165VDC		R2
6.B	+9.00 VDC	+8.91 VDC	+9.03VDC	+9.03	+9.09 VDC	*****	*****		
6.D	≥ -10.2 VDC	≥ -10.2 VDC	-10.63VDC	-10,563	≥ -10.2 VDC	-10.6VDC	-9.7VDC		R1
6.E	≤ -9.8 VDC	≤ -9.8 VDC	-9.73VDC	-9.672	≤ -9.8 VDC	*****	*****		
7.B	-10.000 VDC	-10.001 VDC	-10.000VDC	-10.000V	-9.999 VDC	*****	*****		
7.C	-10.000 VDC	-10.001 VDC	-10.000VDC	-10.000V	-9.999 VDC	*****	*****		
7.D - 6000 Hz	-12.500 VDC	-12.502 VDC	-12.501VDC	-12.500 V	-12.498 VDC	*****	*****		
7.D - 4800 Hz	-10.000 VDC	-10.001 VDC	-10.000VDC	-10.000 V	-9.999 VDC	*****	*****		
7.D - 2400 Hz	-5.000 VDC	-5.002 VDC	-4.999VDC	-4.999 V	-4.998 VDC	*****	*****		
7.D - 480 Hz	-1.000 VDC	-1.002 VDC	-1.000VDC	.9998V	-0.998 VDC	*****	*****		
7.D - 48 Hz	≈-0.1 VDC	≈-0.1 VDC	-.100VDC	-.0999V	≈-0.1 VDC	*****	*****		
7.D - 4.8 Hz	≈-0.01 VDC	≈-0.01 VDC	-.010VDC	.01 V	≈-0.01 VDC	*****	*****		
7.E	-10.000 VDC	-10.001 VDC	-10.000VDC	-10.000V	-9.999 VDC	*****	*****		
7.F	-10.000 VDC	-10.003 VDC	-10.000VDC	-10,000V	-9.997 VDC	*****	*****		
8.A	-12.500 VDC	-12.502 VDC	-12.501VDC	-12.500	-12.498 VDC	*****	*****		

Data Sheet

2 of 2

1/9/2012

8.C	-13.300 VDC	-13.700 VDC	-13.289VDC	-13.286V	-12.900 VDC	-13.28VDC	-12.50VDC		R3 CW
8.D	-13.300 VDC	-13.700 VDC	-13.289VDC	-13.287V	-12.900 VDC	*****	*****		
9.A - 480 Hz TO 10 Khz	≤ 10 mVDC	≤ 10 mVDC	-.010P/P	<.010 VP/P	≤ 10 mVDC	*****	*****		
9.B - 4.8 Hz	-0.01 VDC	-0.01 VDC	-.010VDC	-.010VDC	-0.01 VDC	*****	*****		
9.B - 4.8 Hz	100 mVAC (Vpp)	100 mVAC (Vpp)	100mVAC	80mV	100 mVAC (Vpp)	*****	*****		
9B - 12 Hz	-0.025 VDC	-0.025 VDC	-.025VDC	-.024	-0.025 VDC	*****	*****		
9.B - 12 Hz	80 mVac (Vp-p)	80 mVac (Vp-p)	80mVAC	70 mV	80 mVac (Vp-p)	*****	*****		
9B - 24 Hz	-0.05 VDC	-0.05 VDC	-.050VDC	-.050V	-0.05 VDC	*****	*****		
9.B - 24 Hz	60 Mvac (Vp-p)	60 Mvac (Vp-p)	60mVAC	60 mV	60 Mvac (Vp-p)	*****	*****		
9.B - 48 Hz	-0.1 VDC	-0.1 VDC	-.10VDC	-.100 V	-0.1 VDC	*****	*****		
9.B - 48 Hz	40 mVAC (Vp-p)	40 mVAC (Vp-p)	40mVAC	35mV	40 mVAC (Vp-p)	*****	*****		
9.B - 120 Hz	-0.25 VDC	-0.25 VDC	-.25 VDC	-.250V	-0.25 VDC	*****	*****		
9.B - 120 Hz	20 mVAC (Vp-p)	20 mVAC (Vp-p)	20mVAC	18mV	20 mVAC (Vp-p)	*****	*****		
9.B - 240 Hz	-0.5 VDC	-0.5 VDC	-.5VDC	-.500V	-0.5 VDC	*****	*****		
9.B - 240 Hz	10 mVAC (Vp-p)	10 mVAC (Vp-p)	10mVAC	10mV	10 mVAC (Vp-p)	*****	*****		
9.B - 480 Hz	-1.0 VDC	-1.0 VDC	-1.00VDC	-1.000V	-1.0 VDC	*****	*****		
9.B - 480 Hz	10 mVAC (Vp-p)	10 mVAC (Vp-p)	10mVAC	<10mV	10 mVAC (Vp-p)	*****	*****		
10.D - 6000 Hz	TP5 - Off	TP5 - Off	OFF	OFF	TP5 - Off	*****	*****		

SCOPE: This test instruction outlines the specifications for the Frequency to Voltage (F/V) converter circuit board.

ACTIVE FOR C3 BY JDC DATE 2-28-95

APPLICABLE DRAWINGS

Schematic - 115D2970
Circuit Board - 115D3332 G-1

EQUIPMENT REQUIRED (Or Equivalent)

1.	Frequency Source	HP Model 200 AB
2.	Frequency Counter	HP Model 5223L
3.	Digital Voltmeter	Systron Donner Model 7000
4.	Oscilloscope	* Tektronix Model 7514 storage scope with two dual trace amplifiers Type 7A18. or equivalent *

GENERAL DESCRIPTION

The F/V converter circuit consists of a voltage comparator (IC1), 2 flip-flops (IC2 & IC4), 2 switching transistors (Q1 & Q2), a unijunction (Q3) and an output amplifier (IC7). The circuit also contains 3 additional IC's (IC3, IC5 & IC6) which are used to LOCK UP the output (hold output voltage constant) when the input frequency exceeds 6000 Hz.

The comparator (IC1) converts the input sine waves from the speed pickup on the turbine to square waves of equal frequency. IC2 is used for wave shaping and its output is differentiated to produce a spike waveform which triggers flip flop IC4 and turns Q1 on and Q2 off. When Q1 is switched on, the unijunction timer circuit is initiated, and when Q2 is switched off, a fixed voltage is applied to amplifier IC7.

When the unijunction times out and fires, it produces a reset pulse back to flip-flop IC4 which switches Q1 off and Q2 on; thus removing the fixed voltage from amplifier IC7. Note that Q1 initiates the unijunction timer and Q2 applies a fixed voltage to the output at the start of each incoming positive going pulse and that the fixed voltage is turned off when the unijunction circuit times out causing the flip flop to change state. Since this constant voltage is switched on for a precise time, a constant amplitude, fixed pulse width results (note that the amplitude is fixed by the zener voltage (+9 V), width is held constant by the unijunction circuit (~156 usec) and the pulse occurrence corresponds to the input frequency).

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GENERAL DESCRIPTION (continued)

The output amplifier (IC7) along with a 2nd order, multiple feedback, low pass active filter, converts the input pulses to a dc output which is proportional to frequency.

The characteristic frequency to voltage curve which the F/V converter circuit produces is shown below. As the input frequency increases from 0 to 6000 Hz, the output voltage increases linearly from 0 to -12.50 volts. At rated speed (4800 Hz), the output voltage = -10.000 volts.

For all frequencies greater than 6000 Hz, the LOCK UP circuit will hold the output constant at approximately -13.3 volts.

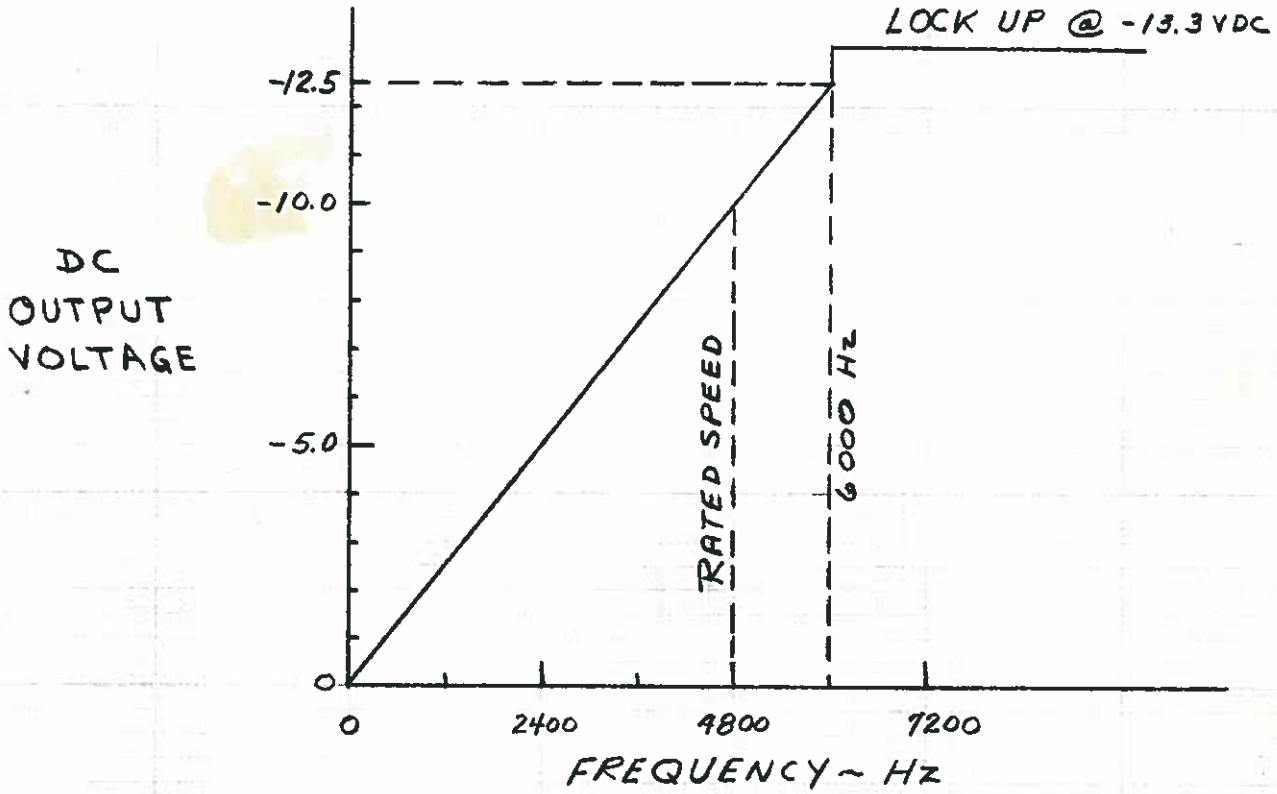

FIG. 1 FREQUENCY/VOLTAGE CHARACTERISTIC CURVE

DUTY FACTOR

The duty factor of the F/V circuit is 75% at rated speed (4800 Hz), placing the 100% duty factor at 6400 Hz. The duty factor is 93.5% at LOCK UP (6000 Hz).

LOCKUP DETECTOR

The lockup detector is a 9601 one-shot, which is retriggerable and remains set when inputs occur at a period shorter than its operating time. Inputs that occur while the one-shot is set are counted by a binary counter, so that one interferring pulse cannot actuate a lockup. When the counter is full, IC5 causes the F/V converter to LOCK UP and also inhibits the counter. When a clear cycle occures with no interference, the counter is reset when the one-shot times out, removing the lockup.

The circuit requires a minimum of 13 inputs shorter than the timing of the 9601 one shot to achieve lockup. Since lock up occurs at a frequency below that at which the unijunction begins to skip, the unijunction timer flip-flop is still running properly. The output jumps up to the locked-up level when the time period of the input frequency is equal to the one shot time. At lockup (6000 Hz) the output jumps from -12.5 V up to -13.3 V.

BINARY COUNTER

The 4-stage binary counter as shown in Figure 2 counts input triggers that occur while the one shot is on. The counter is reset to zero whenever the one shot is off, so that inputs (combination of interference and normal) must occur closer together than the one shot time in order for the count to accumulate. The counter can accommodate up to 15 inputs, although only 13 are actually used in the final system, in order to optimize the gate circuits. When the count reaches 13, NAND gate G2 enables, and its output turns off the input to the counter via NAND gate G1, thereby sustaining the counter in state 13. It also goes to NAND gate G3, which locks up the output from the main flip-flop.

The 13 count delay in applying lock-up to the output can be tolerated because it will occur in 13 cycles of the input frequency while it is between the 95% and 100% duty factor points. In this region, flip-flop 1 is still running normally. With 100% speed in the kilocycle region, only about 10 milliseconds is required to actuate the lock-up, and even manual ramping of an oscillator frequency source is not fast enough to produce any observable down-scale transient when raising the frequency past 100%.

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NOISE IMMUNITY

For interference occurring near the operating frequency, seven spurious inputs are required to actuate the lock-up circuit. Together with the 6 adjacent normal inputs, the count of 13 is achieved as shown in Figure 3. However, the frequency of the interference needs to be only slightly lower in order to cease having any effect at all on the d-c output. This is the frequency which will allow the one-shot to time out just before the lock-up count gets to 13. The limit involves the duty factor of the one shot at the frequency of the normal input. For our application where the duty factor is 75%, the result is immunity to any interferring frequency below 91.2% of the normal input. This result is not strongly dependent on the counter capacity. A count 15 would only raise it to 92.4%. A three stage counter with a capacity of 7 is still immune to interference up to 84% of the normal frequency.

The basic noise immunity of the unijunction timer also depends on its action when noise occurs in the time that its flip-flop is off. This condition will start a premature timing cycle, but will not effect the output through the filter since the result is to move the position of that cycle without affecting its duration. This is true as long as the next normal input occurs while the unijunction is still timing, which will be the case for any location of the interference as long as the duty factor of the unijunction flip-flop is 50% or greater. At lower input frequencies, interference can inject a complete extra unijunction time cycle between its normal ones, thereby raising the output. Therefore, the system design uses a normal duty factor of 75%. As typically used for speed feedback, the increase in output that interference can cause at low speeds is in the safe direction.

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P3K-AL-0135-A02

TITLE

TEST INSTRUCTIONS FOR FREQUENCY TO VOLTAGE CONVERTER

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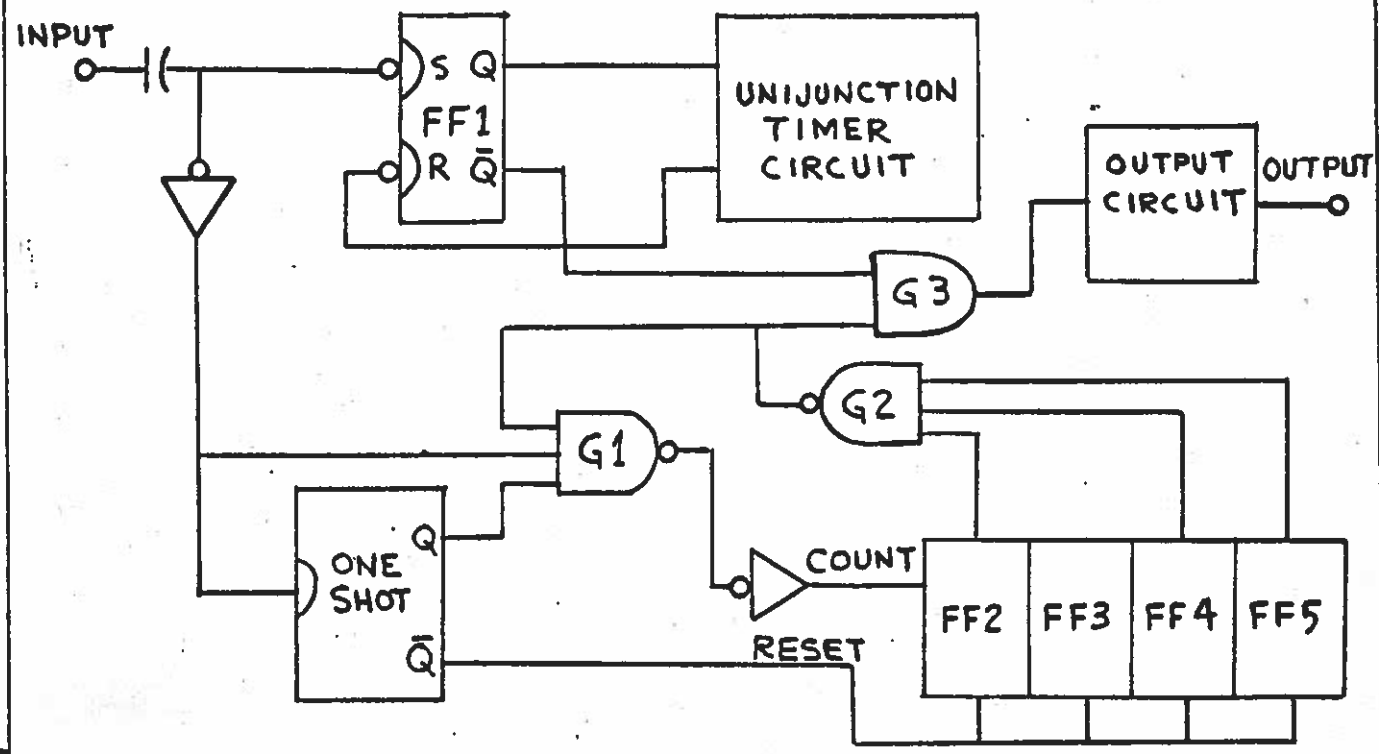
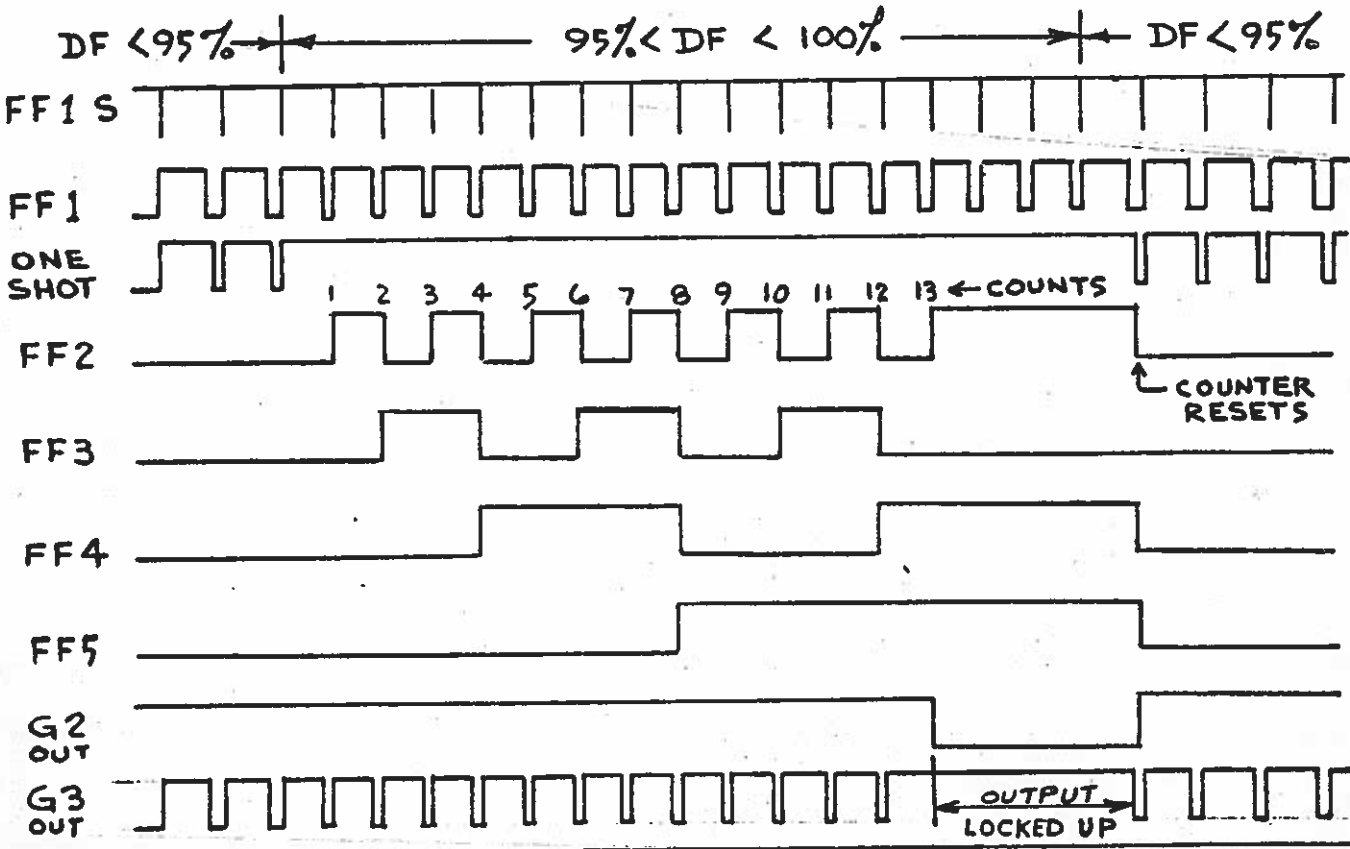
FIG 2 FREQ/VOLTAGE CONVERTER BLOCK DIAGRAM





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D.Mone June 17, 1971		Steam Turbine (DIV OR DEPT.)	P3K-AL-0135-A02
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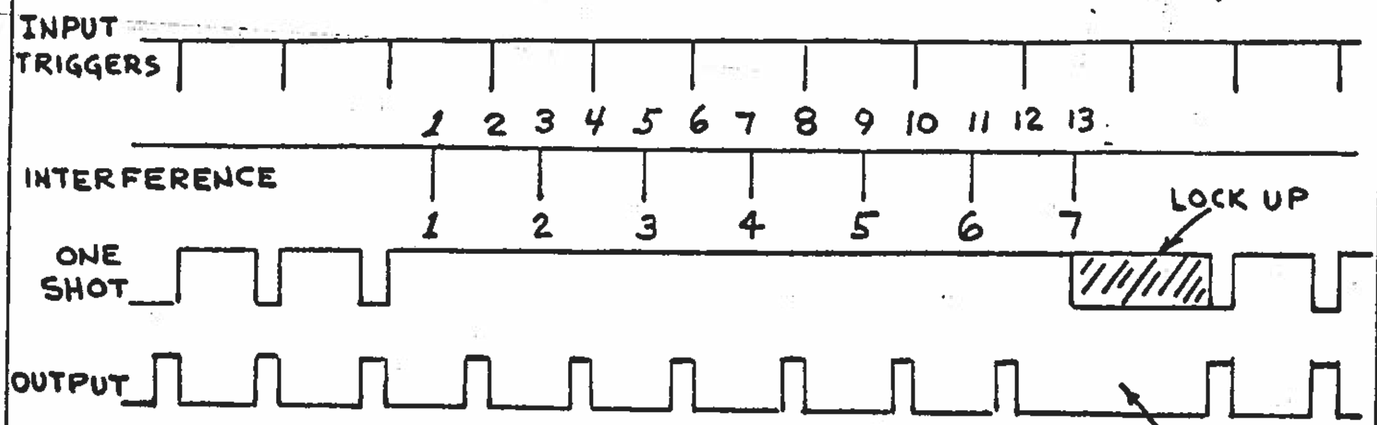
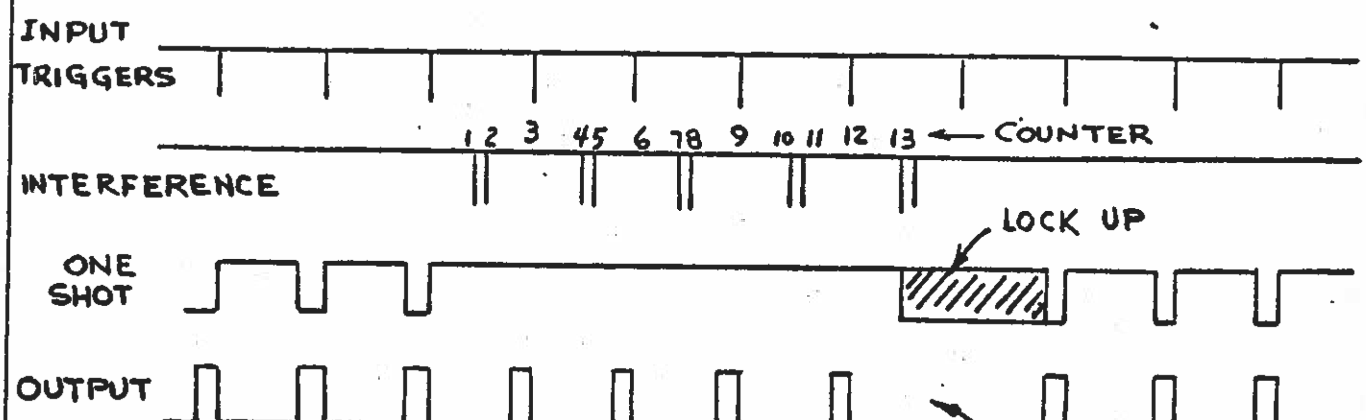


NOTE: 6 INTERFERENCE PULSES SHOULD NOT AFFECT THE OUTPUT

FIG 3a EFFECT OF INTERFERENCE (ONE PULSE PER INPUT CYCLE)



NOTE: 4 INTERFERENCE PULSE PAIRS SHOULD NOT AFFECT THE OUTPUT

FIG 3b EFFECT OF INTERFERENCE AT ONE PULSE PAIR PER INPUT CYCLE

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III. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

+ Power Supply: +30.000 ± .002 VDC
(Pin 17) (plus supply draws approx. 200ma)

- Power Supply: -22.000 ± .002 VDC
(Pin 21) (minus supply draws approx. 50ma)

B. Operating Signal Levels

(Pins 28 & 24)

Input Frequency: 4.8 Hz to 10,000 Hz.

Input Amplitude: 50 mV to 80 V p to p sinewave
Noise suppression lag at 122.5 ± 7.5 KHz.

C. Output Load

(Pin 6) Refer to test setup - Fig. 4

D. Zener Regulated Voltages

CR3 = +4.84 to +5.35 VDC
CR4 = +8.91 to +9.09 VDC
CR5 = +11.11 to +12.28 VDC
CR6 = +15.2 to +16.8 VDC
CR7 = +11.4 to +12.6 VDC
CR8 = -15.2 to -16.8 VDC

E. Output Characteristics (TP6)

Saturation Level of IC7: -14.0 ± .8V & +11.25 ± .6V.

DC OUTPUT = -10.000 ± .001 V at 4800 ± 1 Hz

DC OUTPUT: Must increase linearly with input frequency (0 to -12.5 VDC for 0 to 6000 Hz).

DC OUTPUT: Must remain constant at -13.30 ± .20 VDC for input frequencies > 6000 Hz.

DC OUTPUT: Must be adjustable above and below -10.000 V when input frequency is held constant at 4800 ± 1 Hz.

R1 full CW DC OUTPUT VOLTAGE ≧ -10.200 VDC

R1 full CCW DC OUTPUT VOLTAGE ≦ - 9.800 VDC

DC OUTPUT: Must be sensitive to changes of input frequency and insensitive to changes of input amplitude.

ACCEPTABLE OFFSET: 1 mV after nulling output.

TEMPERATURE STABILITY: DC OUTPUT must not change more than 5 mV when temperature is varied between 20 to 55°C, & frequency is held constant at 4800 Hz

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III. CIRCUIT SPECIFICATIONS (continued)

E. OUTPUT CHARACTERISTICS (TP6) (continued)

DC OUTPUT VOLTAGE TRANSFER FUNCTION (WHEN 9V APPLIED TO INPUT OF ACTIVE FILTER)

$$\frac{E_o}{E_1} = \frac{-k}{\frac{s^2}{\omega_o^2} + \frac{2\zeta}{\omega_o} s + 1}$$

$$= \frac{-k\,\omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}$$

$$= \frac{(-1.475)(76.7)^2}{s^2 + 2\,(.507)\,(76.7)\,s + (76.7)^2}$$

$$= \frac{-8677}{s^2 + 77.77s + 5883}$$ NOMINAL VALUES

WHERE:

k = GAIN = 1.475 ± .030 V/V

ζ = DAMPING RATIO = .507 ± .028

ω_o = UNDAMPED NATURAL FREQUENCY = 76.7 ± 5.0 RAD/SEC.

f_o = UNDAMPED NATURAL FREQUENCY = 12.2 ± 0.8 HZ

NOTE:

The transfer function for the F/V converter results from the multiple feedback active filter, amplifier IC7. This low pass quadratic filter is underdamped, and the characteristics k & ζ change when Q2 switches R17 in and out of the active filter network. As a result, the output voltage transfer function changes as follows:

OUTPUT VOLTAGE TRANSFER FUNCTION
(WHEN ZERO VOLTS APPLIED TO INPUT OF ACTIVE FILTER)

$$\frac{E_o}{E_1} = \frac{-k\,\omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}$$

$$= \frac{(-2.95)\,(76.7)^2}{s^2 + 2\,(.689)\,(76.7)\,s + (76.7)^2}$$

III. GIRCUIT SPECIFICATIONS (continued)

E. OUTPUT CHARACTERISTICS (TP6) (continued)

$$\frac{E_o}{E_1} = \frac{-17354}{s^2 + 105.7s + 5883}$$ { NOMINAL VALUES

WHERE:

k = GAIN = 2.950 ± .060 V/V

ζ = DAMPING RATIO = .689 ± .042

ω_o = UNDAMPED NATURAL FREQUENCY = 76.7 ± 5.0 RAD/SEC.

f_o = UNDAMPED NATURAL FREQUENCY = 12.2 ± 0.8 HZ

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TEST SETUP

EQUIPMENT REQUIRED (or Equivalent)

1. Frequency Source — HP Model 200 AB
2. Frequency Counter — HP Model 5223L
3. Digital Voltmeter — Systron Donner - Model 7000
4. Oscilloscope * — Tektronix model 7514 storage scope with two dual trace amplifiers type 7A18 or equivalent

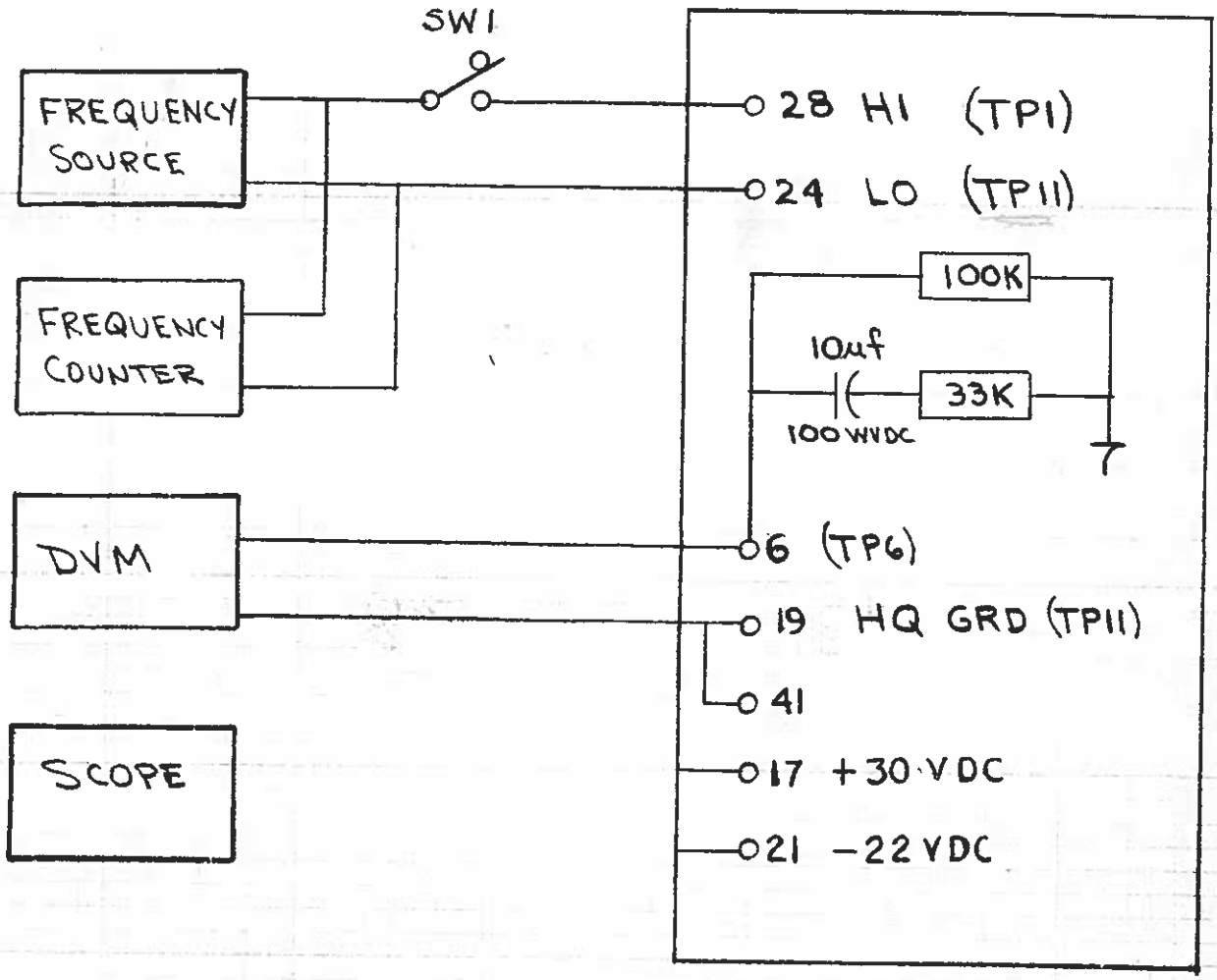

FIGURE 4

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3	DEC 1 1972	Dorothy Lyons
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IV. TEST INSTRUCTIONS

(1 3)

*All notes are intended for information purposes and for trouble shooting aids.

*NOTE: Positive logic is used throughout entire F/V digital design.

1. CONNECT F/V circuit board per test set-up shown in Fig. 4.

2. CHECK ZENER VOLTAGES on the card per circuit specifications, Section III 3D.

3. ADJUST LOCKUP CIRCUIT OUT OF LINEAR REGION:

   a) Adjust trimpot R3 full CCW.

      *NOTE: Adjusting R3 full CCW sets the reset time of the Binary Counter to approx. 140 usec. (measured on scope at IC6 pin 2). As a result, the lock up circuit will not function until the input frequency is approx. 7000 Hz, which is well above the normal linear working region of 0 to 6000 Hz.

4. NULLING OUTPUT AMPLIFIER:

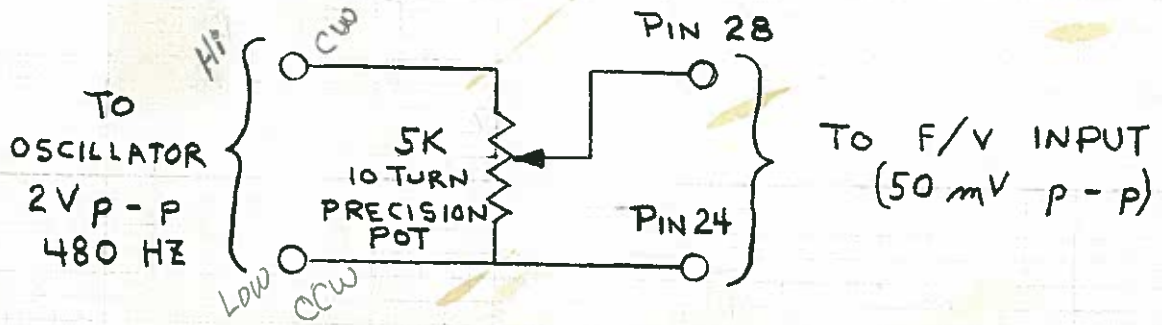
   a) Apply dc power to the F/V card but keep the input signal from the sine wave oscillator turned off.

   b) Adjust trimpot R4 for zero volts output (± .001V) at TP6.

5. SETTING INPUT LEVEL TO BE DETECTED:

   a) Set the oscillator frequency at 480 Hz and the amplitude of the input sine wave to approx. 2V p to p.

   b) Reduce the 2V signal down to 50mV p to p by using a 10 turn pot as shown below measure at TP1:



   c) Apply the 50mV signal to the F/V input.

   * d) Observe the output of IC1 at TP2 on the scope and slowly adjust trimpot R2 either CW or CCW until a stable square wave can be obtained as shown.

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5. SETTING INPUT LEVEL TO BE DETECTED (continued):

*NOTE: A stable dc output voltage from the F/V card will result when the pot is properly adjusted.

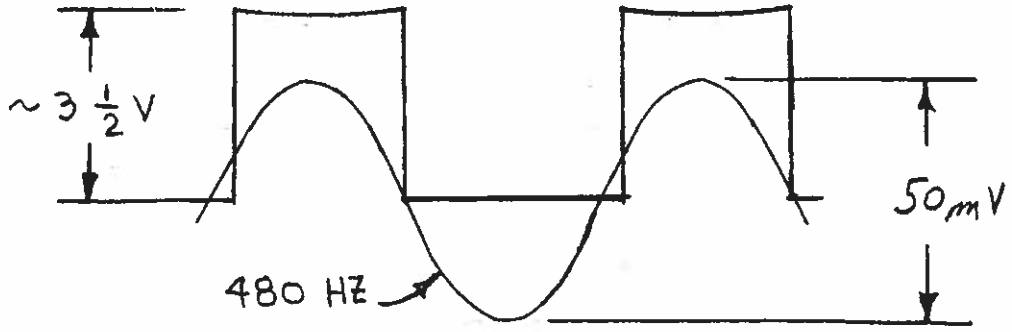

FIG. 5 ADJUSTING TRIMPOT R2 TO OBTAIN SQUARE WAVE OUTPUT FROM IC1 at TP2

*NOTE: The primary purpose of trimpot R2 is to adjust the detection level of comparator IC1 so that low amplitude input signal (approx. 50mV) can produce a stable square wave output. As soon as the input level is much >50mV, this adjustment is insignificant. After R2 is adjusted, note that signals <50MV p to p will go undetected and the F/V converter will not produce any dc output.

6. CHECKING & RECORDING CRITICAL VALUES:

a) Remove the 5K precision pot from the oscillator input.

*NOTE: This pot should be removed because it may produce noise problems in the test setup when the lock up circuit is checked out.

* b) Measure the voltage at CR4 (zener voltage must be +8.91 to +9.09 VDC.

c) Set the oscillator amplitude at approx. 2V p to p (.707 Rms) and the frequency at exactly 4800 ± 1 Hz.

d) Adjust R1 full CW and measure the dc output voltage at TP6 (voltage must be ≧ -10.200 volts). For example, an output voltage of -10.400 V is acceptable but an output of -10.100 V is unacceptable.

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6. CHECKING & RECORDING CRITICAL VALUES (continued):

e) Adjust R1 full CCW and measure the dc output voltage at TP6 (voltage must be -9.800 volts). For example, an output voltage of -9.600 V is aeceptable but an output of 9.900 is unacceptable.

*NOTE: The output voltage will vary approx. 0.8V when R1 is adjusted from end to end. Trimpot R1 adjusts the unijunction time from approx. 150 to 162 usec.

The unijunction time controls the width of the pulses to IC7. This time can be measured on the scope at TP3 as shown below:

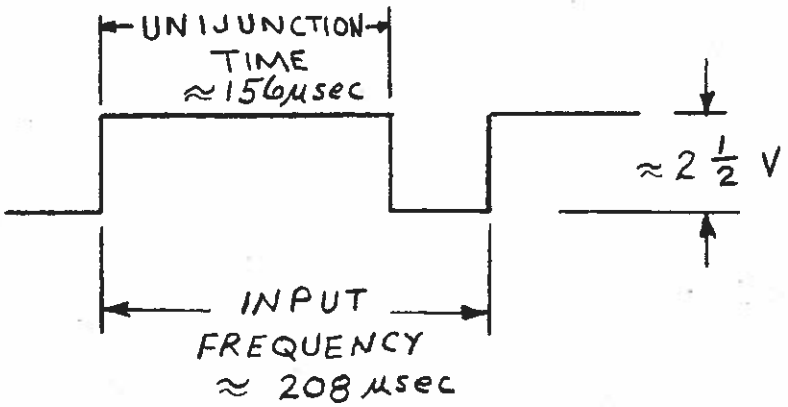

FIG. 6 WAVEFORM AT TP3
(INPUT FREQ. = 4800 HZ)

NOTE: DUTY FACTOR = 75%

*NOTE: The same pulse shape as shown above can also be observed at the input to the output amplifier IC7 except that the amplitude will be approx. 4 1/2 volts (measured at collector of Q2).

R1	TP6 OUTPUT VOLTAGE dc	UNIJUNCTION TIME
Full CCW	-9.600	150 usec
Center of Pot	-10.000	156 usec
Full CW	-10.400	162 usec

TYPICAL VALUES ASSOCIATED WITH ADJUSTING R1

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7. CALIBRATING F/V OUTPUT VOLTAGE

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a) Set the oscillator frequency at exactly 4800 ± 1 Hz and amplitude at approx. 2V p to p.

b) Adjust trimpot R1 until output at TP6 equals -10.000 ± .001 volts.

c) Increase and decrease the oscillator amplitude from 2V p to p (.707 Rms to 7.07 Rms) to 20 V p to p. Note that the dc output should not be sensitive to changes in input amplitude, but only to changes in frequency.

d) Check the output voltage at several additional frequency points shown below:

INPUT (TP1) FREQUENCY (Hz)	DC OUTPUT VOLTAGE (TP6)
6000	-12.500 ± .002 V
4800	-10.000 ± .001 V
2400	- 5.000 ± .002 V
480	- 1.000 ± .002 V
48	Approx. -0.10 V
4.8	Approx. -0.01 V

*NOTE: When the input frequency = 4800 Hz, the output voltage will be -10.000 V, and the duty factor will be 75% as shown in Fig. 6.

e) Return the oscillator frequency to exactly 4800 Hz, and observe that output at TP6 equals -10.000 volts.

f) Set the heat probe at 55°C and apply the probe to the unijunction (Q3) for 30 sec. Remove probe and observe that the output voltage must return to within ± 3mV of original -10.000V setting.

*NOTE: The unijunction heat test is repeated in order to insure that the correct temperature compensation resistor has been previously selected.

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2	D.Mone	NOV 10 1972
3	D.Mone	DEC 21 1972
4	D.Mone	SEP 18 1974

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7. CALIBRATING F/V OUTPUT VOLTAGE (Continued)

NOTE: When the F/V is operating in the linear region, the output voltage can be calculated as follows:

$$Vo = (V\ in)\ (-GAIN\ IC7)$$

$$Vo = (VCR4)\left(\frac{\text{Period of unijunction}}{\text{Period of input frequency}}\right)(-GAIN\ IC7)$$

WHERE:

VCR4 - Input zener voltage to output amplifier IC7.

$\left(\frac{\text{Period of unijunction}}{\text{Period of input frequency}}\right)$ = Ratio of the zener voltage CR4 ON time to the total time.

GAIN IC7 = GAIN of output amplifier IC7.

$= -R20/(R17 + R18)$

$$Vo\ @\ 4800\ HZ = (9V)\left(\frac{156\ usec}{208\ usec}\right)\left(-\frac{113K}{38.3K + 38.3K}\right)$$

Vo @ Rated Frequency = -10.00 volts.

As the period of the input frequency approaches the period of the unijunction, (100% duty factor), the maximum output voltage which can be obtained from the circuit is as follows:

$$Vo\ max = (9V)\left(\frac{156\ usec}{156\ usec}\right)\left(-\frac{113K}{38.3K + 38.3K}\right)$$

$$= -13.3\ volts$$

Therefore, the upper frequency limit is also a function of the unijunction time. Note that when the period of the input frequency becomes less than or equal to the period of the unijunction timer, the flip flop will start missing input pulses.

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TEST INSTRUCTIONS FOR FREQUENCY TO VOLTAGE CONVERTER

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REVISIONS
2 D.Mone NOV 10 1972 [illegible] added
3 D.Mone DEC 2 1 1972 Nocha the [illegible]
4 D.Mone SEP 18 1974 Nocha the [illegible]

8. **SETTING LOCK UP LEVEL:**

a) Increase the input frequency slowly from 4800 Hz to 6000 Hz (note that the output must increase linearly from -10.000 to -12.50 volts).

b) Observe that the output voltage does not decrease or fall off before reaching 6000 Hz.

c) Adjust R3 CW unitl the output voltage jumps from -12.50 to -13.30 ± 0.40 volts at the input frequency of 6000 HZ.

d) After setting the lockup point at 6000 Hz, increase the input frequency from 6000 Hz up to 10,000 Hz and back down. Observe that the output voltage does not change in the lockup region.

*NOTE: The result of adjusting R3 is to set the reset time (which clears the binary counter) to approx. 165 usec. This reset time can be observed on the scope at IC6, pin 2 as shown below: AT 4800 Hz

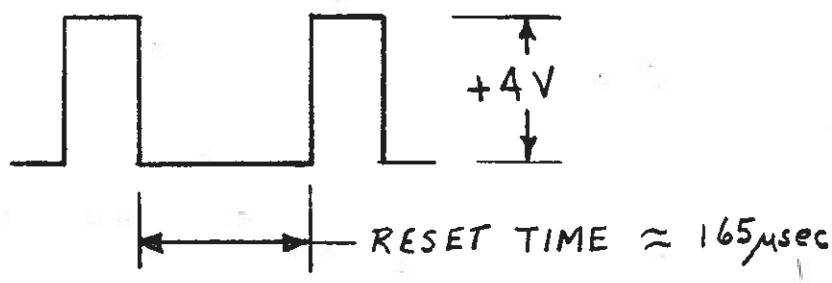

FIG. 7 RESET WAVEFORM
(FREQ. = 4800 HZ)

Adjusting R3 full CCW sets the reset time to approx. 140 usec. while adjusting R3 full CW should produce a reset time of approx. 200 usec. The reset time will normally be set at 165 usec (6000 Hz).

*NOTE: The voltage level at TP4 will change from HI to LO, as soon as the frequency reaches 6000 Hz and the binary counter registers 13 pulses as shown below:

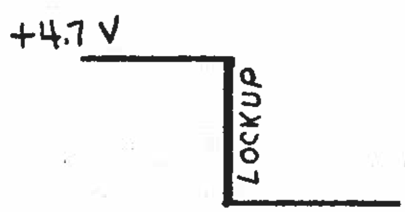

FIG. 8 TP4 WAVEFORM AT LOCKUP

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ISSUED NOV 10 1972
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8. SETTING LOCK UP LEVEL (continued):

e) When TP4 is switched from HI to LO, the output of flip-flop IC4 at TP5 is also held LO (OFF). As a result, Q2 will be held off, CR4 will be held on, and the output jumps up to -13.3 volts. This output voltage measurement can be used to check the gain of the active filter amplifier (IC7) as follows:

$$(Vin) * (GAIN_{IC7}) = V_o$$

$$(V_{CR4}) \quad \left(\frac{R20}{(R17 + R18)}\right) = V_o$$

$$(9V) \quad \left(\frac{113K}{(38.3K + 38.3K)}\right) = V_o$$

$$(9V) \quad (1.475) = 13.3V \quad \text{TYPICAL VALUES}$$

Therefore, in order to obtain the gain of IC7, divide the measured output voltage by the measured zener voltage.

$$\text{GAIN IC7} = \frac{Vout}{V_{CR4}} \quad \text{at lockup}$$

Therefore, when TP4 switches from HI to LO, the output voltage will jump up to -13.3 V, which indicates that lock up has occurred.

This lock up condition results when the frequency pulses occur faster than IC3 can reset (clear) the binary counter. Since IC3 is reinitiated on each incoming pulse, it cannot time out and reset the counter. As a result, whenever the frequency period is shorter than the reset time (≈165 usec) for at least 13 pulses, lock up occurs. The first pulse whose frequency is less than 6000 Hz (period 165 usec), allows IC3 to reset the counter; IC7 will immediately be able to respond to the incoming frequency pulses and produce a dc output which is proportional to frequency.

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9. OBSERVING OUTPUT FOR OSCILLATIONS & CHECKING RIPPLE AT TP6

a) Vary oscillator frequency from 480 Hz to 10 K Hz and observe the output on the scope. The dc ripple or noise riding on the DC output should not exceed 10 MV p to p.

b) Vary frequency from 4.8 Hz up to 480 Hz and observe on the scope that the ac ripple does not exceed the values listed below.

FREQUENCY (Hz)	DC OUTPUT VOLTAGE (volts)	AC OUTPUT VOLTAGE (V p to p)	WAVE SHAPE
4.8	- .01	100 mV	
12	- .025	80 mV	
24	- .05	60 mV	
48	- .10	40 mV	
120	- .25	20 mV	
240	- .50	10 mV	
480	- 1.0	10 mV	

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2	D.Mone NOV 10 1972	Minor changes
3	D.Mone DEC 21 1972	No change this sht.
4	D.Mone SEP 18 1974	No change this sht.

PRINTS TO

10. CHECKING OPERATION OF FLIP FLOP IC4, UNIJUNCTION TIMING CIRCUIT, AND LOCK UP TIME SETTING:

a) Return Oscillator frequency to 4800 Hz.

b) Connect TP3 to scope external trigger input.

c) Connect TP3 & TP5 to scope inputs. (Outputs of FLIP FLOP IC4)

d) Increase oscillator frequency to 6000 Hz, and observe that waveform at TP5 will disappear before waveform at TP3 begins to skip (This condition occurs at the lock up frequency). At frequencies less than lock up, the waveform at TP3 will be the inverse of the waveform at TP5.

*NOTE: When lock up occurs at 6000 Hz, TP5 will be held LO (OFF), due to TP4 being held LO. However, FLIP FLOP IC4 (Pin 1) will continue to respond to incoming frequency pulses, and the unijunction will continue to time out and produce reset pulses back to IC4. As a result, pulses can be observed on the scope at TP3 and IC4 pin 5 even though TP5 is held off when LOCK UP occurs (Output voltage jumps to -13.3 volts). Also note that at LOCK UP, a duty factor of approx. 93.5% can be observed on the scope at TP3 as shown below:

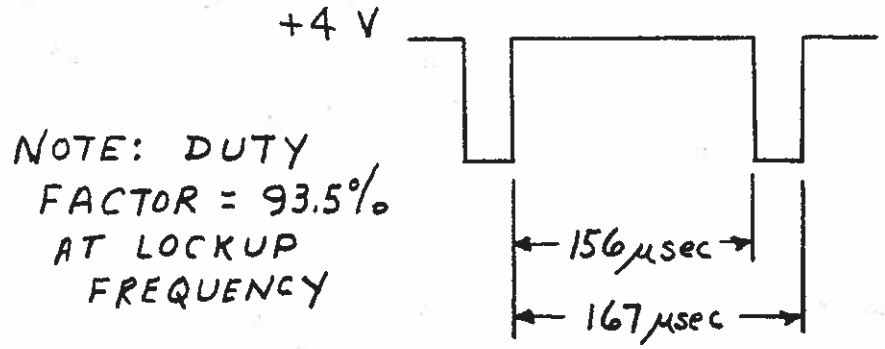

FIG. 9 WAVEFORM AT TP3
(FREQ. = 6000 HZ)

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1	D.Mone	Nov 10 1972
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NOTES

1. Both IC2 and IC3 are triggered simultaneously at the falling edge.
2. Output IC2 (Pin 8) HI until t1 is reached.
3. Output IC3 (Pin 6) LO until t2 is reached.
4. Output $\bar{Q}$ inhibits both IC1 and IC2 from retriggering until t2 is reached.
5. "On" time controlled by VR1.
6. "Inhibit" time controlled by VR2.
7. T2 must be greater than T1.
8. Adjust VR1 to increase t1.
9. Adjust VR2 to increase t2.
10. +5 VDC supply for IC1 (9946) must be separate from +5 VDC supply for IC2 and IC3 (9601).
11. Input pulses will be transmitted to output during time t1, and will be inhibited from the output during time t2-t1.

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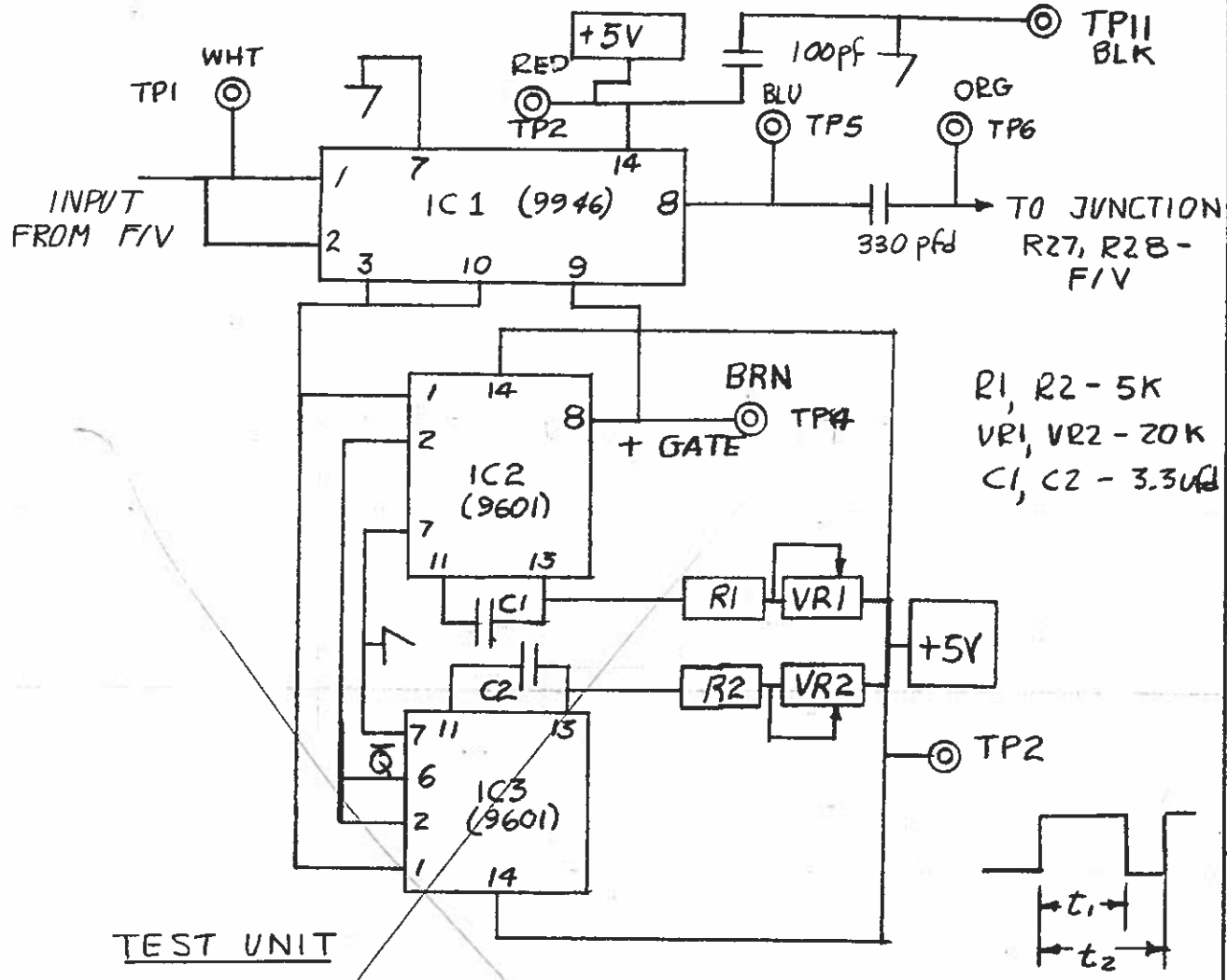

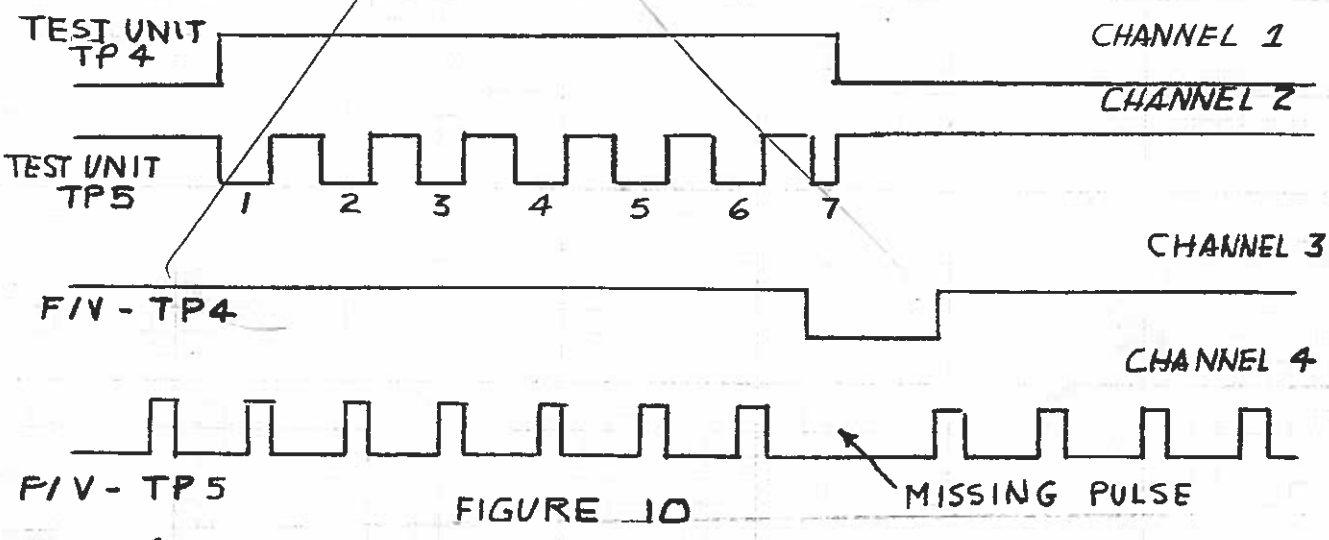

FIGURE 10

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R1, R2 - 5K
VR1, VR2 - 20K
C1, C2 - 3.3ufd

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11. CHECKING LOCK UP CIRCUIT

TEST DESCRIPTION

The test which follows uses a separate digital TEST UNIT to inject interference pulses into the F/V converter and cause lock up to occur. The entire test which follows will be observed on the scope and is intended to functionally check out the lock up circuit for the following:

1. The ability of the One Shot (IC3) to detect input frequencies > 6000 HZ.
2. The ability of the binary counter to count exactly 13 pulses (frequency = 6000 Hz) and cause the output of IC5 (TP4) to change state from HI to LO, thus inhibiting the unijunction flip-flop output at TP5.
3. The ability of IC5 to inhibit the counter once 13 pulses have been registered.
4. The ability of IC3 to reset (clear) the counter and unlock the F/V, as soon as the input frequency drops below 6000 Hz.

In order to achieve a lock up condition, a minimum of 13 consecutive input pulses whose time period is shorter than the One Shot time, are required. Therefore, in order to test this portion of the F/V, exactly 13 pulses whose period is shorter than the One Shot reset time (≈165 usec.) will be injected into the LOCK UP circuit. These pulses will be generated by summing 7 pulses from a separate TEST UNIT board along with 6 normal frequency pulses. The TEST UNIT pulses will be spaced midway between the frequency pulses (4800 Hz = 208 usec) as shown below:

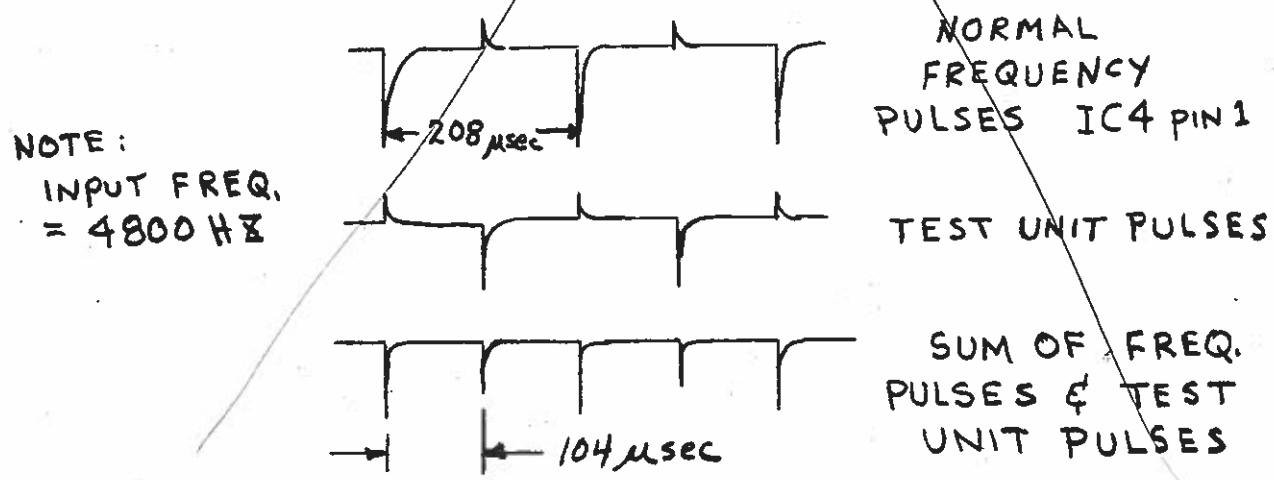

FIGURE 11 PULSE TRAIN TO LOCKUP CIRCUIT

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3 DVM DEC 2 1972

4 DVM SEP 18 1974

PRINTS TO

11. CHECKING LOCK UP CIRCUIT (continued)

TEST DESCRIPTION (continued)

The result of injecting 13 continuous pulses whose period is approx. 104 usec will prevent the One Shot from resetting the Binary Counter. Therefore the counter will count the 13 pulses and cause IC5 at TP4 to change state from HI to LO. This condition will cause the output at TP5 to also be held off. As a result, Q2 will be held off, CR4 will be held on (for a longer time than normal), and the F/V output voltage will jump up to a value greater than -10V (approx. -10.3V).

Since the next input frequency pulse (14th) will have a normal period of 208 usec, the One Shot will be able to reset (clear) the counter and unlock the F/V.

TEST UNIT

The digital TEST UNIT board also receives its input frequency pulses from the F/V voltage comparator IC1. The test unit + GATE output is used as a control unit and the number of output pulses from the TEST UNIT. The width of the scope B + GATE pulse can be varied by adjusting VR1 on the test unit. By adjusting the + GATE, the TEST UNIT can produce from 3 to 9 output pulses. When the + GATE is set to produce exactly 7 pulses, a LOCK UP condition should result for only 1 pulse period. If 8 pulses are induced, LOCK UP should occur for 2 pulse periods, etc. LOCK UP should not occur for less than 7 pulses from the TEST UNIT.

NOTE: It will be necessary to observe good grounding practices as well as minimum lead lengths in order to prevent noise from falsly triggering the LOCK UP circuit during testing. If false triggering does occur, this condition can be observed on the scope and the test set up should be corrected.

TEST SET-UP:

a) Return oscillator frequency to 4800 Hz.

b) Connect the Test Unit per Figure 10. Observe on the scope

1. Channel 1 - Test Unit - TP4
2. Channel 2 - Test Unit - TP5
3. Channel 3 - F/V board - TP4
4. Channel 4 - F/V board - TP5

c) Adjust VR1 until seven (7) pulses (TP5, Test Unit) appear on the scope).

d) At the start of pulse 7, (TP5, Test Unit,) TP4, (F/V board) shows a negative pulse.

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1 DYNAMO NOV 10 1972

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3 DYNAMO SEP 18 1974

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TEST INSTRUCTIONS FOR FREQUENCY TO VOTLAGE CONVERTER

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II. CHECKING LOCK UP CIRCUIT (continued)

TEST SET-UP: (continued)

e) TP5 (F/V board) pulse train shows a missing pulse.

f) F/V output shall increase from -10.000 VDC to -10.30 VDC.

g) Remove all Test Units, wire, and Power Supplies from the F/V board.

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12. CHECK ACTIVE FILTER FREQUENCY COMPENSATION NETWORK BY OBSERVING THE TIME RESPONSE TO A STEP INPUT.

- Switch the Input Frequency at TP1 from 0 HZ to 4800 HZ, and observe the change, in output voltage @ TP6. (Use a storage scope to capture the transient time response on the screen).
- Fig. 13 shows the waveshape, % overshoot, time to peak, and tolerances which must be observed.

*NOTE:

The above time response test is used to check the active filter characteristics (Damping Ratio = .507 & Undamped Natural Frequency = 76.7 RAD/SEC) when transistor Q2 is OFF and CR4 applies 9V to the input of the active filter amplifier IC7.

- Switch the input frequency at TP1 from 4800 HZ to 0 HZ, and observe the change in out put voltage @ TP6 (Use a storage scope to capture the transient time response on the screen).
- Fig. 14 shows the waveshape, % Overshoot, Time to Peak, and Tolerances which must be observed.

*NOTE:

The above time response test is used to check the active filter characteristics (Damping Ratio = .689 and Undamped Natural Frequency = 76.7 RAD/SEC) when zero volts is applied to the input of the active filter amplifier IC7.

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REV NO. 34

P3K-AL-0135-A02

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TEST INSTRUCTIONS FOR FREQUENCY TO VOLTAGE CONVERTER

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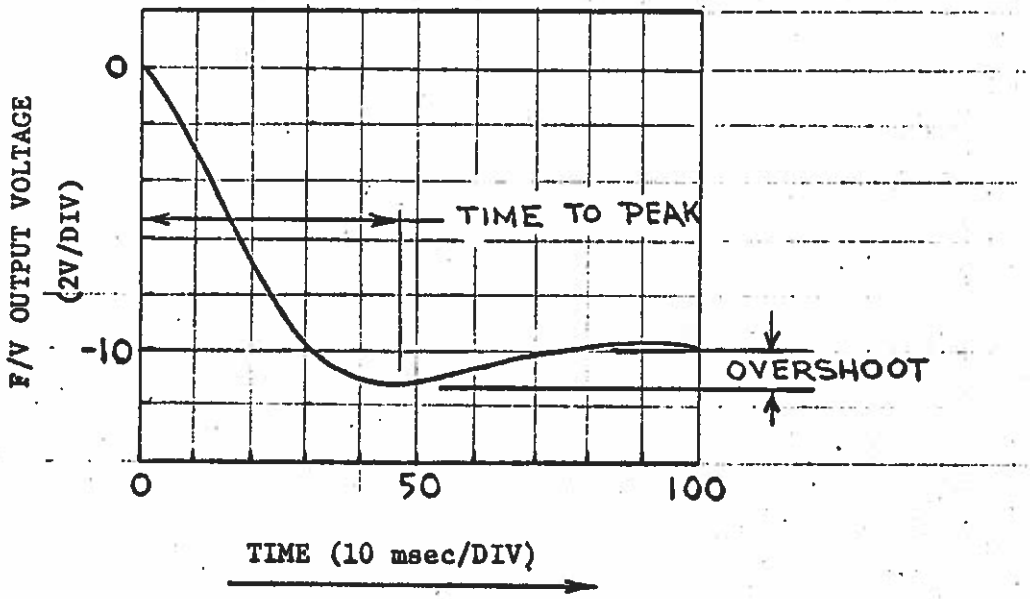
FIG. 13 F/V CONVERTER OUTPUT VOLTAGE TRANSIENT RESPONSE

FOR STEP CHANGE OF INPUT FREQUENCY FROM 0 HZ to 4800 HZ



NOTE:

UNDAMPED NATURAL FREQUENCY (ω_o) = 76.7 RAD/SEC.

DAMPING RATIO (ζ) = .507

MAX OVERSHOOT % = 15.7 ± 2.3%

MAX OUTPUT VOLTAGE = -11.57 ± 0.23 VDC @ 47.5 ± 1.5 msec

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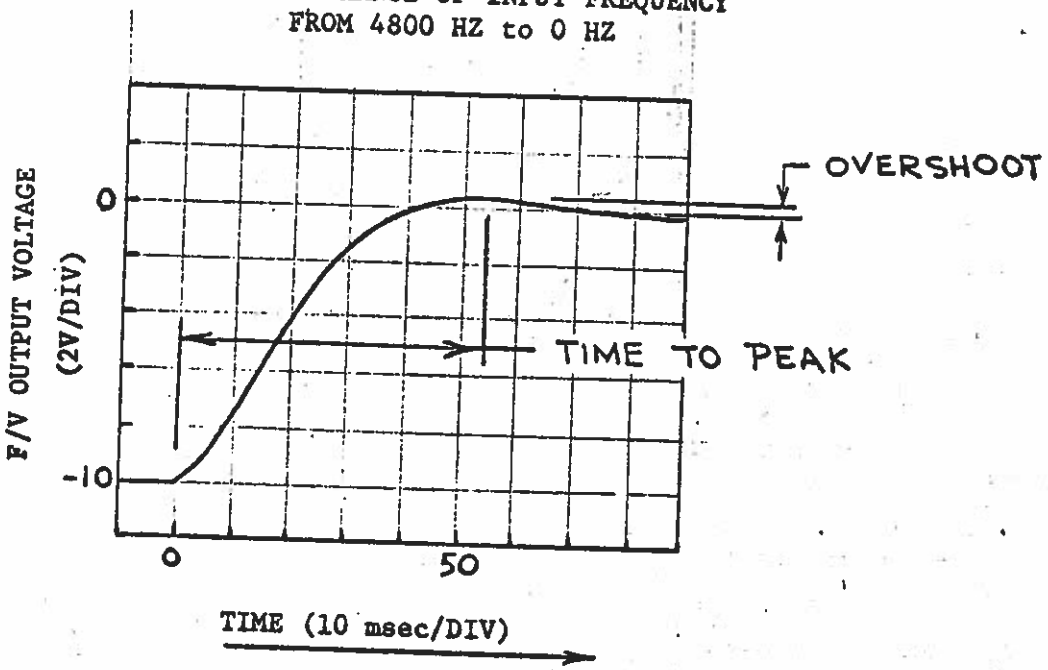
FIG. 14 F/V CONVERTER OUTPUT VOLTAGE TRANSIENT RESPONSE

FOR STEP CHANGE OF INPUT FREQUENCY FROM 4800 HZ to 0 HZ



NOTE:

UNDAMPED NATURAL FREQUENCY (ω_o) = 76.7 RAD/SEC.

DAMPING RATIO (ζ) = .689

MAX OVERSHOOT % = 5.1 ± 1.8

MAX OUTPUT VOLTAGE = +0.51 ± 0.18 VDC @ 56.5 ± 4.5 msec

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13. CHECK FREQUENCY COMPENSATION NETWORK

- Check IC1's input noise suppression lag filter specified in section III. A storage scope will be adequate for this check. Note that the output of the filter must be within 63% of the final valve in one time constant (1.3 usec).

14. CHECK UNIJUNCTION TIMING CAPACITOR

After all F/V board tests have been completed, apply Freon spray to the unijunction timing capacitor C4, and observe that the F/V output remains constant at -10.000 VDC (Input frequency = 4800 HZ). If the output goes to a new value, the capacitor must be replaced and the board rechecked and realigned.

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1 D.Y.Mone DEC 21 1972
4 D.Y.Mone SEP 18 1974

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TITLE

CIRCUIT BOARD TEST FOR FREQUENCY
TO VOLTAGE CONVERTER

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3 O.Moore DEC 2 1 1972 ... added

4 O.Moore SEP 1 8 1974 Revised

PREPARED BY J. Dombrosky E. Andrejko DATE 10-17-72
J. Dombrosky & E. Andrejko
CONTROL DESIGN ENGINEERING

APPROVED BY R Dellorfano DATE 10/26/72
R. Dellorfano
EHC TEST ENGINEER

APPROVED BY P C Callan DATE 10-27-72
P.C. Callan - MANAGER
CONTROL DESIGN ENGINEERING

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