1.0 SCOPE

The following covers the performance capabilities and test instructions for the 193X379AAG01 System Card. This card is designed to be a standard part of the AF-400 Inverter, and performs the following functions:

1.01 Provides minimum voltage and frequency detection logic and readout.
1.02 Provides start and stop logic and readout plus reference clamp control.
1.03 Includes special decelerate to minimum frequency control.
1.04 Provides fault trip readout and fault reset control.
1.05 Contains inverter frequency indicating light.
1.06 Provides inverse time overcurrent trip control and indication.
1.07 Provides inverter vs. external frequency discriminator logic.
1.08 Provides inverter to external frequency synchronization logic & readout.

2.0 PERFORMANCE CAPABITIES

All cards should be capable of the following performance while exposed to the conditions of section 4.0. In these specifications, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt.

2.01 Inputs/Outputs

Tabs 20, 21, 22, 25 and 32 are signal inputs. Signal sources connected to these tabs must each be capable of sinking 15 ma.

Tabs 6, 18, 19 and 29 are signal readouts. Each tab is capable of sinking 15 ma at a +1.0 to +1.5 volt output level.

Tabs 7, 8, 9, 10, 17 &27 are logic inputs. Logic sources connected to tabs 7, 8, 9 and 17 must each be capable of sinking 1.5 ma, and logic sources connected to tabs 10 and 27 must each be capable of sinking 3 ma.

Tabs 4, 5, 11, 12, 13, 23, 24, 30 and 31 are logic outputs. Tabs 4, 5, 11, 23 and 30 are each capable of sinking 10 ma and sourcing 1 ma, tabs 12 and 24 are each capable of sinking 7 ma and sourcing 1 ma, and tabs 13 & 31 are capable of sinking 3 ma and sourcing .5 ma, in their low and high states respectively.

Tabs 14, 16 & 26 are analog inputs, and tab 28 is an analog clamp output.

2.02 Minimum Voltage and Frequency Control

The minimum voltage level is detected by means of the LVF input at tab 26. The voltage level of this signal, relative to +10 volts, is proportional to the d.c. link voltage, as determined by the voltage feedback isolation resistor values external to this card. For an increasing d.c. link voltage from zero, when the inverter is stopped (ORI tab 24 high), OMVFRQ tab 19 will switch from low to high at a d.c. link voltage of 55 to 70 volts for a 230 volt drive and 110 to 140 volts for a 460 volt drive. For a decreasing d.c. link voltage, when the inverter is running (ORI tab 24 low), tab 19 will switch from high to low at a d.c. link voltage of 80 to 95 volts for a 230 volt drive and 160 to 190 volts for a 460 volt drive.

Chg 2.02 12/16/77 CEG
Chg 2.02 4/4/78 CEG
1 2

AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5QC(2BW)
5R(BW)
PRINTS TO

The minimum frequency level is detected by means of the 1MR logic input at tab 17. This logic signal is dependent on the level of the frequency reference voltage as detected on the Regulator card. This logic signal also determines the logic state of the OMVFRO at tab 19 in that both voltage and frequency must be detected to be at the minimum levels before tab 19 can be in its low state. 1MR tab 17 is high at the minimum frequency level.

2.03 Start and Stop Logic

The start and stop signal inputs at OSTART tab 20 and OSTOP tab 21 initiate inverter starting and stopping through the logic outputs at ORI tab 24 and 1RI tab 30. The start and stop inputs at tabs 20 and 21 are normally high and are operated by taking them low. They feed into a latching flip-flop so that only a momentary low input signal is needed to latch the flip-flop in the desired state. If both tab 20 and 21 are taken low, the stop input at tab 21 predominates in setting the latch. If neither input is taken low when +20 volt power is applied to the card, the flip-flop will automatically be latched in the stop position.

The output of the start-stop flip-flop feeds into logic latches which allow the desired logic outputs at tabs 24 and 30 only if the minimum voltage and frequency logic is in the correct state. Inverter starting can occur, after the start-stop flip-flop is latched in the start position, only if the inverter voltage and frequency are in their minimum ranges. Inverter operation can be stopped, after the start-stop flip-flop is latched in the stop position, only if the inverter voltage is in the minimum range. In order to achieve the minimum inverter operating levels for starting and stopping, the start-stop flip-flop also controls a reference clamp output at RFC tab 28, which is taken low whenever the flip-flop is in the stop position. RFC tab 28 is also held low when 1RI tab 30 is low, such that the reference clamp is not released until the inverter is actually started.

The inverter run readout at ORRO tab 18 is low when the inverter is running, since it switches with the ORI logic output at tab 24.

2.04 Decelerate to Minimum Frequency Control

The ODMF input at tab 32 is normally high. When this tab is taken low, the reference clamp output at RFC tab 28 and the fast rate output at OFR tab 31 are both taken low. This produces a deceleration to minimum frequency at the fast rate. When tab 31 is released to go high, both the reference clamp and fast rate are disengaged.

AW (BW)
5D (BK)
5E (3BK)
5K (BW)
5[illegible]
5QC (2BW)
5R (BW)
DS (REP)

PRINTS TO

2.05 Fault Trip and Fault Reset Logic

The fault trip logic input at OFT tab 27 is normally high. When a fault is detected on another card, this input goes low. This causes the start-stop flip-flop to latch in the stop position to produce a normal stop operation, as described in Section 2.03. Tab 27 going low also causes the fault trip readout at 1FTRO tab 29 to switch from low to high, to drop out an external fault relay.

The fault reset output at ORST tab 23, when it is low, resets the fault latches on other cards, which have latched on after a fault and caused the OFT input at tab 27 to be low. The conditions necessary for fault reset depend on whether the external fault reset input at 1XFR tab 22 is taken low or left in its normal high state. If tab 22 is left high, then ORST tab 23 will be low when:

1) The OSTOP input at tab 21 is low,
2) The ORI output at tab 24 is high.
3) The 1MR input at tab 17 is high.

This means that stopping the inverter by the normal means will initiate a fault reset. If 1XFR tab 22 is normally connected low, it means that this connection must be broken, in addition to conditions 1),2)&3) above, before a fault reset is initiated.

A reset timer is provided which operates only in the period following the application of 20 volt power to the card. This timer has a time period of 1.6 to 8 seconds when OFT tab 27 is low, and a time period of .15 to .25 seconds when tab 27 is high. The function of the reset timer is to reset the start-stop flip-flop or any fault flip-flops, which may have latched up incorrectly when card power was applied. In addition, it acts to reset the control undervoltage fault latch that is activated on the Inverter card because of the .4 to 1.3 second time delay of the delayed firing power after card power is applied. This timer provides these functions by causing the following logic action during its time period:

1) Causes the start-stop flip-flop to latch in the stop position irrespective of the inputs at tabs 20 and 21.

2) Causes the ORST output at tab 23 to go low irrespective of whether 1XFR tab 22 is held low.

The time period of this timer allows ample time for reset after card power is applied, and then will quickly time out after the OFT input at tab 27 goes high.

AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5[redacted]
5QC(2BW)
5R(BW)
DS(REP)
PRINTS TO

REVISIONS

2.06 Inverter Frequency Indicating Light

The IF light (LED2) will blink at the operating frequency of the control, irrespective of whether the inverter is operating or not. In a stopped or standby condition, the minimum frequency can be easily seen in the blinking frequency of the light. If the light is either off or fully on at standby, the frequency control is not operating properly. At high operating frequencies in the running condition, the light will appear to be fully on.

2.07 Inverse Time Overcurrent Trip

A switching type of current limit control contained on the Regulator card has an output signal which is mainly high below 100% current, consists of a train of pulses having an average +10 volt level at the current limit level, and is mainly low at currents substantially above the current limit level. If this signal is connected to OCL input tab 7, an inverse time trip function is obtained. At the current limit level (as set on the Regulator card), the timer will cause a current limit time trip if the current limit level persists for 40 seconds ± 15 seconds. At slightly below the current limit level, a time trip could still occur for an appreciably longer time period. At current levels higher than the current limit level, the time period for a time trip is reduced, becoming as low as 13.5 seconds ± 3.5 seconds when the OCL tab 7 input becomes continuously low.

An immediate overcurrent trip is produced if the rectifier current feedback signals at RCFP tab 16 and RCFN tab 14 reach the equivalent of 175% to 200% of rated motor current. During inverter synchronized operation when OSS tab 12 is low, the inverse time overcurrent trip is locked out. If an inverse time overcurrent trip occurs, its fault latch turns on ITOC light LED3 and causes OITOC tab 13 to go low. The fault latch is reset when ORST tab 23 goes low.

2.08 Frequency Discriminator

The frequency discriminator has an external, reference frequency input at EF tab 10, and an internal, feedback frequency input at IF tab 9. The frequency sources connected to these inputs may be in the form of either square wave or pulse signals, with the pulses being either high or low going and at least 10 μsec. in duration. However, the discriminator operates only on the low going edges of the two frequency signals.

The two outputs of the discriminator are 1FI tab 5 and 1FD tab 4. If the IF signal at tab 9 is lower in frequency than the EF signal at tab 10, the 1FD output at tab 4 will be continuously low, and the 1FI output at tab 5 will be a high-low pulse train whose frequency is the same as the lower of the two input frequency signals, and whose irregular pulse widths form a subharmonic frequency which is the difference between the tab 9 and tab 10 input frequencies. If the IF signal at tab 9 is higher in frequency than the EF signal at tab 10, the 1FI output at tab 5 will be continuously low and the 1FD output at tab 4 will exhibit the high-low pulse train.

Chg 2.07 3/7/78 CDR

AW(BW)
5B(8)M
5D(CD)
5E(3)BK
5R(2)BK

PRINTS TO

2.08 (continued)

When the two input signals at tabs 9 and 10 are at the same frequency and are exactly in phase with each other, both output tabs 4 and 5 will be low. If the two input signals are at the same frequency, but one lags the other in phase relationship, the outputs at tabs 4 and 5 will be similar to those for an input frequency difference except that the high-low pulse train will consist of identical width pulses.

This frequency discriminator therefore descriminates both frequency differences and phase differences between the two input frequency signals.

2.09 Frequency Synchronization Logic

The OSYNC input at tab 25 is normally high. When this tab is taken low, the reference clamp RFC tab 28 will switch to +15 volts or higher with 1 ma loading of tab 28, and OFR tab 31 will switch to low. This will cause the inverter frequency to increase at a fast rate. Tab 25 going low also enables the synchronizing logic. As soon as 1FD tab 4 goes into its high-low pulse train, indicating that the IF tab 9 frequency has reached and exceeded the EF tab 10 frequency, the start synchronizing output signal at OSS tab 12 switches to low. This causes the inverter frequency to stop increasing and to slowly decrease. As soon as 1FI tab 5 goes into its high-low pulse train, indicating that the IF tab 9 frequency is now slightly below the EF tab 10 frequency, the inverter synchronize output at OIS tab 11 switches to low. This causes the inverter frequency to be locked in synchronism with the external frequency.

When the IF tab 9 frequency is pulled into synchronism with the EF tab 10 frequency, the phase error between the two frequencies must be less than 2.0 to 2.5 electrical degrees before a synchronized readout is given. This readout consists of OSRO tab 6 switching to low and the SYNC light LED1 lighting.

After a synchronized readout is given, the phase error between the two frequencies must exceed 2.5 to 3.0 electrical degrees before the synchronized readout disappears; that is before tab 6 switches back to high and the SYNC light goes out. This 0.5 degree hysteresis is to allow for discriminator regulation.

The synchronizing logic will remain latched, that is tabs 11 and 12 will remain low, until either the OSYNC tab 25 is released to go high, the OSTOP tab 21 is taken low or the OFT tab 27 is taken low.

2.10 Power Supply Requirements

The 20 volt power supply requirements for this card are 85 ma ± 15%.

Chg 2.09 3/15/78 CEG

AW(BW)
5D(BK)
5E(3BK)
5B(8)M
5R(2)BW

3.0 TEST INSTRUCTIONS

In these instructions, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt, when 20 volts control power is applied to the card. A fixed midpoint voltage of +10 volts is applied to tab 3. A 15K, 1/2W resistor should be connected between tab 3 and tab 28. Connect both input tabs 8 and 9 to a square wave oscillator whose frequency is adjustable between 10 and 70 Hz. Connect input tab 10 to another square wave oscillator operating at 60 Hz. Both oscillators should have their commons connected to card common, with their "low" state outputs being 0 to 5 volts and their "high" state outputs being 10 to 20 volts.

3.01 Minimum Voltage and Frequency control

Connect LVF tab 26 to +10 volts at tab 3. With 1MR tab 17 connected to +20 volts, the OMVFRO output at tab 19 should be low. With tab 17 connected to common, tab 19 output should be high.

Connect tab 17 to +20 volts. Connect LVF tab 26 to a voltage source set at +10 volts, but which can be varied downward. Connect OSTOP tab 21 to common so that ORI tab 24 is high. When the tab 26 voltage is lowered from +10 volts, the OMVFRO tab 19 output should switch from low to high when the tab 3 to tab 26 voltage is between .82 to 1.0 volts. When the tab 26 voltage is raised toward +10 volts, tab 19 should switch back from high to low when the tab 3 to tab 26 voltage is between .85 to .67 volts. The difference between these two switching voltage levels should not be less than .05 volts.

Disconnect OSTOP tab 21 from common and connect OSTART tab 20 to common so that ORI tab 24 goes low. Now when the LVF tab 26 voltage is lowered again, the tab 19 output should switch from low to high when the tab 3 to tab 26 voltage is between 1.34 to 1.52 volts. When the tab 26 voltage is raised toward +10 volts, tab 19 should switch back from high to low when the tab 3 to tab 26 voltage is between 1.37 to 1.19 volts. The difference between these two switchin voltage levels should not be less than .05 volts.

3.02 Start and Stop Logic

Table 1 below is a step-by-step testing sequence to check that the proper logic outputs appear for a normal sequence of logic inputs. This table shows the correct logic levels if the sequence is followed from step1through step 12. The following input tabs should be connected as specified, throughout the tests; 1MR tab 17, OFT tab 27 and OCL tab 7 connected to +20 volts, ODMF tab 32, 1XFR tab 22 and OSYNC tab 25 left unconnected. In the table, the input and output logic levels are coded as follows:

H - high logic level (+18 to 20 volts)
L - low logic level (0 to +1 volt)
U - unconnected logic input (internally taken high)
9 - +9 volt input level
10 - +10 volt input or output level (input must be same potential as tab 3 voltage)

Chg. 3.01 12/16/77 CER
Chg 3.01 4/4/78 CER
M R2
AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5[redacted]W)
5QC(2BW
5R(BW)
DS(REP)
PRINTS TO

3.02 (continued)

Table 1

Steps in Sequence	INPUTS			OUTPUTS					
	LVF Tab 26	OSTOP Tab 21	OSTART Tab 20	OMVFRO Tab 19	ORRO Tab 18	ORI Tab 24	IRI Tab 30	RFC Tab 28	ORST Tab 23
1	10	L	U	L	H	H	L	L	L
2	10	U	U	L	H	H	L	L	H
3	10	U	L	L	L	L	H	10	H
4	10	U	U	L	L	L	H	10	H
5	10	L	U	L	H	H	L	L	L
6	9	L	U	H	H	H	L	L	L
7	9	U	L	H	H	H	L	L	H
8	10	U	L	L	L	L	H	10	H
9	8	U	L	H	L	L	H	10	H
10	8	L	U	H	L	L	H	L	H
11	10	L	U	L	H	H	L	L	L
12	10	L	L	L	H	H	L	L	L

In all of the steps in Table 1, output tabs 11, 12 and 31 should remain high and tab 29 should remain low.

3.03 Decelerate to Minimum Frequency Control

With the inputs and outputs in the condition of step 3 in Table 1 of section 3.02, OFR tab 31 should be high and RFC tab 28 should be at +10 volts. Now connect ODMF tab 32 to common. Tabs 28 and 31 should both go to the low state, but all other output tabs should stay the same. Disconnect tab 32 from common and tabs 28 and 31 should return to their previous states of +10 volts and high respectively.

3.04 Fault Trip and Fault Reset Logic

With the inputs and outputs in the condition of step 3 in Table 1 of Section 3.02, disconnect OFT tab 27 from +20 volts and connect to common. Output tabs 18, 24 and 29 should switch from low to high, tab 30 should switch from high to low and tab 28 should switch from +10 volts to low. Now disconnect tab 27 from common and reconnect to +20 volts. Output tabs 18, 24, 28, 29 and 30 should all switch back to their original levels.

AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5[redacted]W)
5QC(2BW
5R(BW)
DS(REP)

PRINTS TO

REVISIONS

3.04 (continued)

With the inputs and outputs in the condition of step 1 in Table 1 of Section 3.02, disconnect 1MR tab 17 from +20 volts and temporarily connect to common. ORST tab 23 should switch from low to high, and then return to low when tab 17 is reconnected to +20 volts. Connect 1XFR tab 22 to common, and tab 23 should switch back to high. Now disconnect OFT tab 27 from +20 volts and connect to common. Remove +20 volt control power from tab 1 for several seconds and then reapply. For a time period between 1.6 to 8 sec. after control power is reapplied, ORST tab 23 will remain low before switching to high. Now disconnect OFT tab 27 from common and reconnect to +20 volts. Repeat the removal and reapplication of +20 volt control power. The time period that tab 23 remains low after control power is reapplied is now only .15 to .25 sec. Disconnect 1XFR tab 22 from common and ORST tab 23 should return to low.

3.05 Inverter Frequency Indicating Light

Check the IF light (LED2) when the square wave oscillator connected to IPA tab 8 is adjusted to 10 Hz. It should be visibly blinking. When the oscillator frequency is increased to 70 Hz, the blinking frequency should increase.

3.06 Inverse Time Overcurrent Trip

With the inputs and outputs in the condition of step 3 in Table 1 of Section 3.02, with the square wave oscillator connected to input tabs 8 and 9 operating at 70 Hz, and with input tab 7 connected to +20 volts and input tabs 14, 16 and 25 left unconnected, output tab 13 should be high. Now disconnect OCL tab 7 from +20 volts and connect to tab 8. After a time period of from 30 to 60 seconds, OITOC tab 13 should switch to low and the ITOC indicating light (LED3) should light. Disconnect tab 7 from tab 8 and connect to +20 volts. Now momentarily connect OSTOP tab 21 to common to cause ORST tab 23 to go low. Output tab 13 should switch back to high and the ITOC light should go out.

Connect RCFN tab 14 to common and connect RCFP tab 16 to a voltage source which can be varied from 0 to +20 volts. As the tab 16 voltage is increased from zero, tab 13 should switch to low and the ITOC light should light when the tab 16 voltage is between 4.95 and 5.25 volts. Reduce the tab 16 voltage to zero. Now momentarily connect OSTOP tab 21 to common, and tab 13 should switch back to high and the ITOC light should go out.

Connect OSYNC tab 25 to common to cause OSS tab 12 to go low. Increase the tab 16 voltage from zero to +20 volts. The ITOC light should not light and tab 13 should remain high. Decrease the tab 16 voltage to zero and then disconnect tab 25 from common. The ITOC light should remain out and tab 13 should remain high.

3/7/78 cer
Chg 3.06
AW(BW)
5B(8)M
5D(CD)
5E(3)BK
5R(2)BW

PRINTS TO

REVISIONS

3.07 Frequency Discriminator

With the square wave oscillator connected to EF tab 10 operating at 60 Hz, and the square wave oscillator connected to IF tab 9 operating at 70 Hz, the 1FI tab 5 should be continuously low and the 1FD tab 4 should exhibit a high-low pulse train whose frequency is the same as the lower of the two input frequencies, and whose irregular width pulses form a subharmonic frequency which is the difference between the tab 9 and tab 10 input frequencies. Now gradually reduce the frequency of the oscillator connected to tab 9. At the instant when this frequency becomes lower than the tab 10 oscillator frequency, 1FD tab 4 should go into a continuously low state and 1FI tab 5 should exhibit the high-low pulse train. Continue reducing the tab 9 oscillator frequency down to 10 Hz. 1FD tab 4 should remain low and 1FI tab 5 should exhibit the "beat" frequency pulse train. Now gradually increase the tab 9 oscillator frequency. At the instant when this frequency becomes higher than the tab 10 oscillator frequency, 1FI tab 5 should go into a continuously low state and 1FD tab 4 should exhibit the high-low pulse train.

3.08 Frequency Synchronization Logic

With the inputs and outputs in the condition of step 3 in Table 1 of Section 3.02, with the oscillator connected to IF tab 9 operating at 50 Hz, and with input tabs 7, 17 and 27 all connected to +20 volts and input tabs 22, 25 and 32 left unconnected, output tabs 31, 12, 11 and 6 should be high, tab 4 should be low, and tab 5 should exhibit a high-low pulse train. Now connect OSYNC tab 25 to common. Output tab 31 should switch from high to low, tab 28 should switch from +10 volts to between +15.3 to 17.0 volts, but all other outputs should remain the same. Increase the IF tab 9 oscillator frequency to exceed the EF tab 10 oscillator frequency. At the instant the tab 9 frequency exceeds tab 10 frequency, output tabs 5 and 12 should switch to low and tab 4 should exhibit a high-low pulse train. Now decrease the tab 9 oscillator frequency below the tab 10 frequency. At the instant the tab 9 frequency becomes lower than the tab 10 frequency, output tabs 4 and 11 should switch to low and tab 5 should exhibit a high-low pulse train. Now disconnect IF tab 9 from its oscillator and connect it to the tab 10 oscillator. Output tab 5 should switch to low immediately. After a .30 to .37 second time delay, OSRO tab 6 should switch from high to low and the SYNC indicating light (LED1) should light.

Disconnect OSYNC tab 25 from common. Output tabs 31, 12, 11 and 6 should all switch from low to high, tab 28 should switch to +10 volts and the SYNC light should go out. Disconnect IF tab 9 from the tab 10 oscillator and connect to its original oscillator, and adjust its frequency to 50 Hz.

Connect OSYNC tab 25 to common. Repeat the procedure, as described in the first part of this section, of adjusting the frequency input to IF tab 9 to above and below the tab 10 frequency so that both output tabs 12 and 11 switch to low. Now connect OSTOP tab 21 to common. Output tabs 12 and 11 should switch back to the high state and tab 28 should switch to low. Disconnect OSYNC tab 25 from common. Tab 31 should switch back to high.

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AW(BW)
5B(8)M
5D(CD)
5E(3)BK
5R(2)BW

PRINTS TO

REVISIONS

3.08 (continued)

Disconnect the oscillator connected to EF tab 10 and connect tab 10 to tab 19. Disconnect tab 8 from IF tab 9, disconnect tab 17 from +20V, and connect tab 17 to tab 9. Disconnect OSTOP tab 21 from common, connect LVF tab 26 to tab 3, and connect both OSTART tab 20 and OSYNC tab 25 to common. Set the oscillator connected to tab 9 at a 60 Hz repetition rate, but adjust the width of the high period down to 90 μsec. The IFI tab 5 output should exhibit the same pulse frequency and pulse width as the oscillator.* OSR tab 6 should be low and the SYNC light (LED1) should be lit. Slowly increase the oscillator high pulse width. When the tab 5 high pulse width is between 115 to 140 μsec., tab 6 should switch to high and the SYNC light should go out. Now slowly decrease the oscillator high pulse width. When the tab 5 pulse width is between 90 to 115 μsec., tab 6 should switch to low and the SYNC light should light.

* It may be necessary to disconnect and reconnect tab 17 to 9 several times to obtain the desired tab 5 output and SYNC light.

4.0 OPERATING and TEST CONDITIONS

This card should be capable of operating within the performance specified in Section 2.0 and pass all tests specified in Section 3.0 while exposed to the following conditions:

4.01 DC Supply Voltage
+19.8 to +20.2 volts from tab 1 to tab 2.

4.02 Ambient Temperature
0 to +75°C

4.03 Humidity
24 hours in 90% relative humidity at 40°C.

4.04 Voltage to Ground
600 volts.

Chg 3.08 3/15/78 CER

AW(BW)
5D(BK)
5E(3BK)
5B(8)M
5R(2)BW

PRINTS TO