## 1.0 SCOPE

The following covers the performance capabilities and the test instructions for the 193X376AAG01 Inverter Card. This card is designed to be a standard part of the AF-400 Inverter, and performs the following functions:

1.01 Determines the inverter commutation interval and provides commutation pulse and flip flop trigger signals from a six times fundamental frequency input.

1.02 Detects commutation current and regulates the peak commutation current by providing an initial pulse signal suitably placed within the commutation interval.

1.03 Generates an inverter firing pulse train.

1.04 Produces a firing signal supply which is delayed on control power energization to allow for control circuit settling.

1.05 Provides control undervoltage detection and inverter shutdown logic, including fault indication.

1.06 Provides commutation overcurrent detection and inverter shutdown logic, including fault indication.

1.07 Provides selectable inverter overfrequency detection and inverter shutdown logic, including fault indication and readout.

1.08 Provides inverter shoot-through fault detection and inverter shutdown logic, including fault indication and readout.

1.09 Provides inverter shutdown logic for a d.c. link overvoltage condition detected and indicated on another card.

## 2.0 PERFORMANCE CAPABILITIES

All cards shall be capable of the following performance while exposed to the conditions of section 4.0. In these specifications, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt, when 20 volts control power is applied to the card.

2.01 Inputs/Outputs

Tabs 14, 15, 20 & 28 are logic inputs. Logic sources connected to these tabs must each be capable of sinking 6 ma.

Tabs 16, 17, 18, 19, 26, 27, 29, 30, 31 & 32 are logic outputs. Tabs 29 & 30 are each capable of sinking 2 ma, tab 17 is capable of sinking 7 ma, tabs 16, 18, 19, 26, 27 & 31 are each capable of sinking 12 ma, and tab 32 is capable of sinking 22 ma, all in their low logic states. All of these tabs are capable of sourcing 1 ma and tab 32 is capable of sourcing 2 ma, all in their high logic states.

Tab 10 is an analog output which is capable of supplying up to 40 ma at over 16 volts for firing signal supply.

AW (BW)
5D (BK)
5E (3BW)
5K (BW)
5QC (2BK
5R (BW)
PRINTS TO

2.01 (continued)

Tabs 4, 5, 9, 11, 12, 13 & 21 are analog inputs. Tabs 22, 23, 24 & 25 are for selecting the desired inverter overfrequency trip point.

2.02 Commutation Interval Control

The inverter commutation interval is determined by the outputs at tabs 17, 18, 19 and 26, which are in turn determined by the inputs at tabs 11, 12, 13 and 20. With no commutation current feedback inputs at tabs 11, 12, and 13, the outputs at tabs 17, 18, 19 and 26 are (for 460V) determined by the width of the OCP pulse input at tab 20, as shown by the dotted lines in Fig. 1. The flip flop trigger outputs at tabs 17 and 18 will directly and inversely follow the tab 20 signal, except that the low going output will always lead the high going output so that tabs 17 and 18 are never both high. The ICP tab 19 pulse will be the inverse of the tab 20 pulse, except that it will be extended from 2 to 7 μsec. The IIP tab 26 pulse will occur at the time that tab 18 goes low, and will be 10 to 12 μsec. wide.

With commutation current feedback inputs at tabs 11, 12 and 13, the outputs at tabs 17, 18, 19 and 26 are determined by the magnitude of the commutation current input signals, as shown by the solid lines in Fig. 1. The tab 19 output pulse will go low 2 to 7 μsec. after commutation current is detected. The tabs 17, 18 and 26 outputs are determined by the commutation current regulator when the peak voltage at input tab 11, 12 or 13 exceeds approximately 11 volts, as explained in section 2.03. Below this peak voltage input, the tabs 17, 18 and 26 outputs are determined by a time period which is selected to equal one-half of the oscillation period of the inverter commutation circuit. This time period begins with the start of the OCP tab 20 input pulse and at its end causes the ending of the tab 17 and 18 pulses and the initiation of the tab 26 pulse. This time period is from 17 to 23 μsec, when the 460V jumper is not connected, for low voltage inverters having nominal 40 μsec. long commutation oscillations. When the 460V jumper is connected, the time period is 34 to 46 μsec, for high voltage inverters having nominal 80 μsec. long commutation oscillations.

2.03 Commutation Current Regulation

When the commutation current peak input voltage at tab 11, 12 or 13 exceeds 11.2 volts ±7%, the tab 17 and 18 pulse widths are lengthened by the peak voltage regulator to produce a later initiation of the IIP tab 26 pulse. This reduces the commutation pump-up capabilities of the inverter to limit the commutation current magnitude. For stable operation, the gain of the peak voltage regulator is such that the peak input voltage at tab 11, 12 or 13 must increase from 1.6 to 2.0 volts, to 13.0 volts ±7%, to cause the IIP tab 26 pulse to move from the middle of the commutation current pulse to the end. Since the commutation pump-up capabilities of the inverter increase with increasing d.c. link voltage, a feedback of this voltage into LVF tab 21 acts as a positive feedback to increase regulator gain.

AW(BW)
5D(BK)
5E(3BW
5K(BW)
5QC(2B
5R(BW)
PRINTS TO

REVISION

2.03 (continued)

The tab 21 input voltage will be 10 volts at zero d.c. link voltage and approximately 5.5V at rated voltage. The performance of the commutation current regulator will vary somewhat depending on inverter rating and commutation component tolerances, but will try to regulate the peak commutation current inputs at tab 11, 12 and 13 to 12.0 volts ±10% over a 10 to 1 inverter frequency range.

The presence of a commutation current input at any one of tabs 11, 12 or 13 is indicated by a high logic output at ICC tab 16, as shown in Fig. 1.

2.04 Inverter Firing Pulse Train

The IIPT tab 27 provides a 24 kilohertz ±6% unsynchronized pulse train for inverter firing modulation. The high going pulses are 9.7 to 11.1 μsec. wide with alternate low periods of 31 to 36 μsec. The initial pulse at tab 26 also appears at tab 27 as an extra pulse in the pulse train, as shown in Fig. 1.

2.05 Delayed Firing Signal Supply

The DFS output at tab 10 is a controlled source of firing signal supply When +20 volt power is applied to the driver cards, tab 10 will remain in the low state so that firing signals are not inadvertently generated during the short period when the control is settling down. After .4 to 1.3 seconds, tab 10 will go high. Tab 10 can supply up to 40 ma at 16 volts or more. If tab 10 is shorted to common either directly or indirectly, the current is limited to a max. of 110 ma.

2.06 Control Undervoltage Shutdown

With a fixed 9.0 volt ±5% input at CRZ tab 5 (from the power supply card zener), a control undervoltage trip will occur if the voltage between tabs 1 and 2 decreases to 18.0 ± 1.1V or below. This will result in the following action:

1) Both the CUV and IFT fault lights will turn on
2) Both OIFT tab 30 and OIFL tab 32 will go to the low state
3) A 40 μsec. minimum train of low going pulses will appear at OIFP tab 31
4) DFS tab 10 will go to a low state after a 40 to 120 μsec. delay time.

A control undervoltage trip is also initiated if the DFS tab 10 is loaded so that its output voltage decreases to 14.2 ± 1.1V or below. This will result in the same shutdown action as with a +20V undervoltage except that DFS tab 10 is not caused to go low.

The firing signal supply at DFS tab 10 will be maintained below 2 volts for control power levels from the undervoltage trip level down to zero volts. This prevents any SCR firing due to control logic misoperation at low control voltages.

AW(BW)
5D(BK)
5E(3B)
5K(BW)
5QC(2)
5R(BW)
PRINTS TO

REVISION

2.07 Commutation Overcurrent Shutdown

A commutation overcurrent trip is produced when a commutation current input signal at either tab 11, 12 or 13 reaches 18.15 volts ±2.5%, and results in the following action:

1) Both the COC and IFT fault lights will turn on
2) Both OIFT tab 30 and OIFL tab 32 will go to the low state
3) A 40 μsec. minimum train of low going pulses will appear at OIFP tab 31.

2.08 Inverter Overfrequency Shutdown

An overfrequency trip is produced when the inverter frequency input signal at IPA tab 28 reaches the values given in the following table, depending on the jumper connection used between tab 22 and tabs 23, 24 and 25.

| Jumper Tab 22 to | Tab 22 | Tab 25 | Tab 24 | Tab 23 |
|---|---|---|---|---|
| Trip Frequency ±10% | 75 Hz | 110 Hz | 165 Hz | 275 Hz |

An overfrequency trip results in the following action:

1) The IOF fault light will turn on.
2) The OIOF tab 29 will go to the low state.

2.09 Inverter Fault Shutdown

An inverter fault trip is produced when the filter capacitor current input signal at FCC tab 4 reaches 10.5 volts ±3%, and results in the following action:

1) The IFT fault light turns on
2) Both OIFT tab 30 and OIFL tab 32 will go to the low state
3) A pulse train appears at OIFP tab 31, remaining as long as the tab 10 voltage exceeds 10.5 volts ±3%. This pulse train consists of 7 to 10 μsec. low pulses and 21 to 25 μsec. high periods.

2.10 DC Link Overvoltage Shutdown

A d.c. link overvoltage condition is detected and indicated on another cards. A logic signal from this trip is applied to OLOV tab 15 and results in the following action:

1) The IFT fault light turns on
2) Both OIFT tab 30 and OIFL tab 32 will go to the low state
3) A 40 μsec. minimum train of low going pulses will appear at OIFP tab 31.

1 Chg 2.09 7/21/77 cer

AW (BW)
5D (BK)
5E (3BW)
5K (BW)
5QC (2BW)
5R (BW)
PRINTS TO

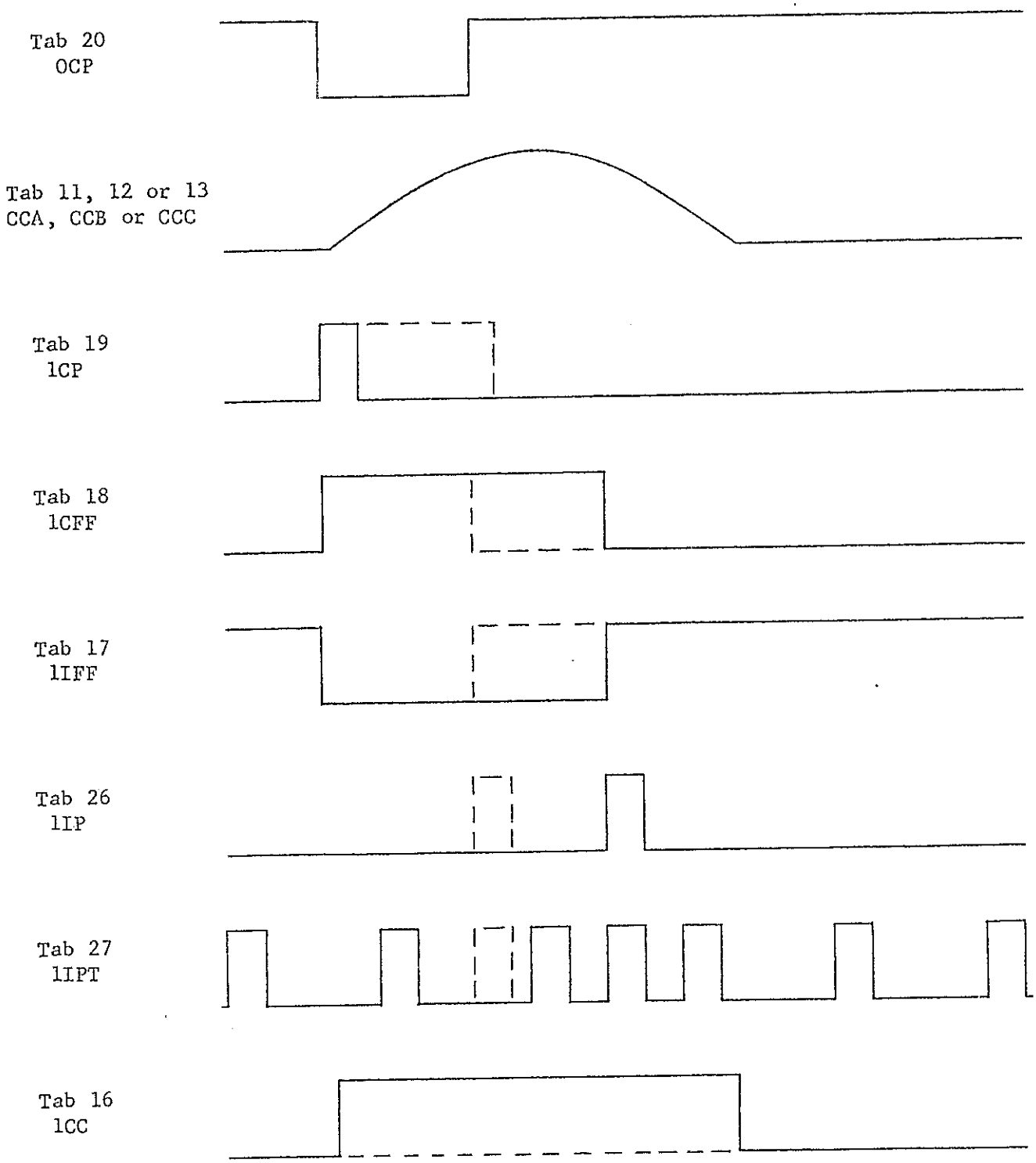
REV. NO. 0

224X409AA
CONT ON SHEET 6 SH NO. 5

TITLE
AF-400 INVERTER CARD
ENGINEERING SPEC & TEST INSTRUCTIONS

FIRST MADE FOR 193X376AAC01

REVISION




RELATIVE WAVESHAPES FOR 460V OPERATION

Figure 1

AW (BW)
5D (BK)
5E (3BW
5K (BW)
5QC (2P
5R (BW)
PRINTS TO

2.11 Fault Reset

All fault shutdowns described in sections 2.06 through 2.10 are maintained by logic latches. A momentary low input to ORST tab 14 will reset all fault latches, lights and readouts to their off state.

2.12 Power Supply Requirements

The 20 volt power supply requirements for this card will be 110 ma ±15%. (neglecting the delayed firing power supplied to other cards).

3.0 TEST INSTRUCTIONS

In these instructions, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt, when 20 volts control power is applied to the card. A fixed 9.0 volt control level is connected to CRZ tab 5. The OCP output of the circuit shown in Fig. 2, which is low for about 35 µsec. and high for about 5 milliseconds, is applied to OCP tab 20. When applying control power to this card, it will be necessary to momentarily connect ORST tab 14 to common to reset any fault lights which have latched on.

3.01 On-card 13 volt Power Supply

The four 555 timers are fed from an on-card 13 volt nominal power supply which can be measured by checking the voltage at tab 21 with a meter having a minimum input impedance of 10 megohms. The voltage at tab 21 should be at least 12.6 volts but no more than 13.2 volts.

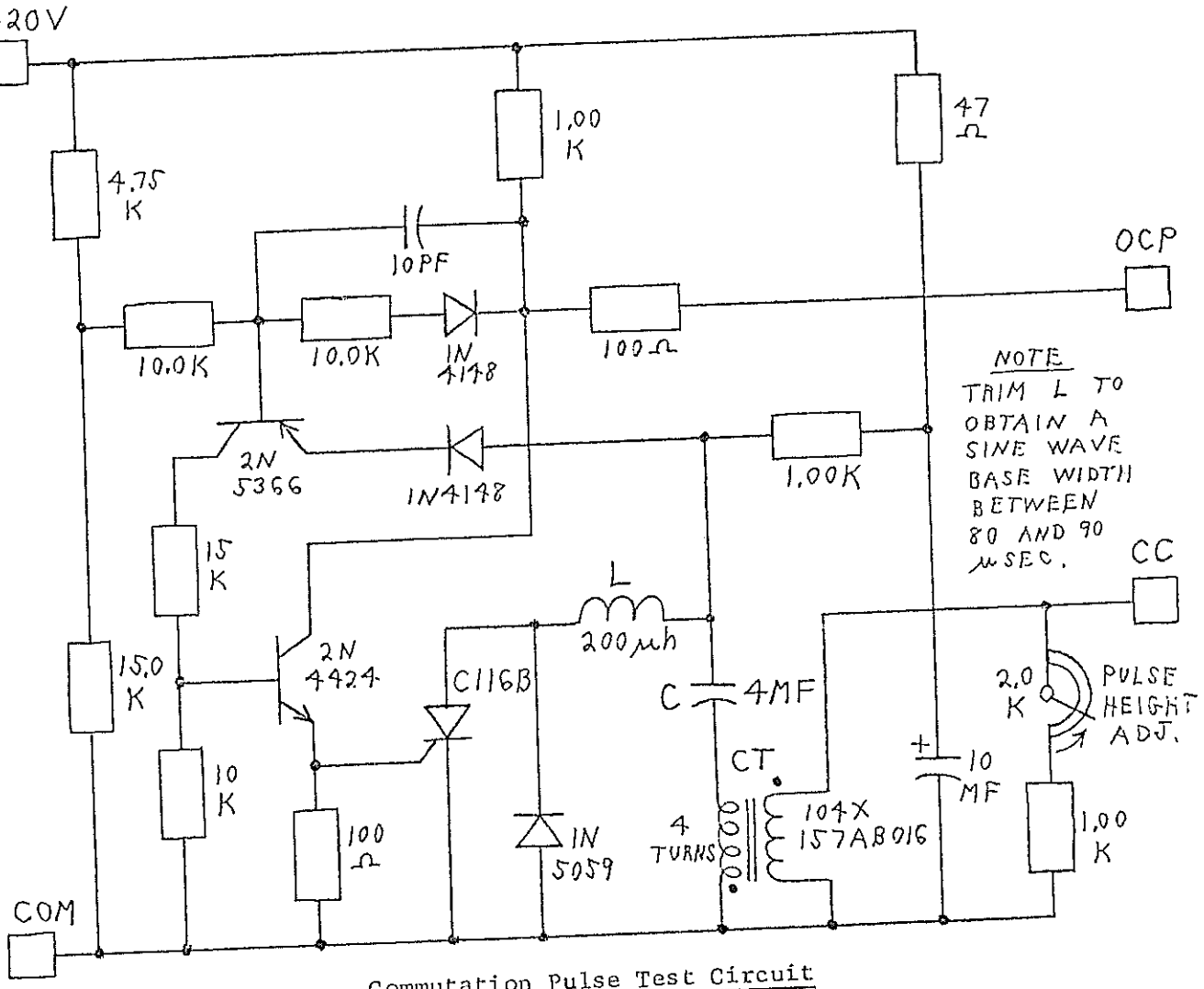
3.02 Commutation Pulse and Flip Flop Trigger Control (460V Jumper in)

The commutation pulse output, 1CP at tab 19, is triggered by the OCP input signal at tab 20 as shown in Fig. 1. Tab 19 should go high at the same time as tab 20 goes low. With no inputs at tabs 11, 12 and 13, tab 19 should remain high for as long as tab 20 is low, as shown by the dotted line in Fig. 1. After tab 20 goes high, tab 19 should remain high for a period of 2 to 7 µsec. before going low.

The flip-flop trigger outputs at 1CFF tab 18 and 1IFF tab 17 are both switched by the OCP input at tab 20, as shown by the dotted lines in Fig. 1. Tab 17 should switch identically with tab 20 while tab 18 should switch inversely. However tabs 17 and 18 should never both be high. The one going high should not switch until the one going low has switched.

Connect CC of Fig. 2 to input tab 11 to provide a dummy commutation current input signal. The output signals at tabs 19, 18 and 17 should change from the dotted line widths to the solid line widths shown in Fig. 1. The commutation pulse at tab 19 should be only 5 to 10 µsec. wide. The flip flop pulse widths at tabs 18 and 17 should now be determined by the commutation current regulator timer as covered in section 3.03. The same changes in output tab 19, 18 and 17 pulse widths should occur when CC is connected to input tabs 12 and 13 as when connected to tab 11.

AW (BW)
5D (BK)
5E (3BW
5K (BW)
5QC (2F
5R (BW)




Commutation Pulse Test Circuit

Figure 2

3.03 Commutation Current Regulator

With the 460V jumper in, and the commutation test circuit of Fig. 2 connected to OCP tab 20 and CC tab 11, 12 or 13, set the pulse height adj. pot of the test circuit at minimum. The pulse widths at tabs 17 and 18 should be 34 to 48 μsec. wide.

Connect LVF tab 21 to a voltage source which can be varied from +10 volts to common. No change in tabs 17 and 18 pulse widths should be observed until the tab 21 voltage is reduced down to 9.4 to 8.4 volts. At tab 21 voltages below this level, the tabs 17 and 18 pulse widths should increase and should reach 80 μsec. when the LVF tab 21 voltage has been reduced by 5.0 to 7.0 volts, down to 4.4 to 1.4 volts. Disconnect LVF tab 21 and tabs 17 and 18 pulse widths should return to their original value.

AW (BW)
5D (BK)
5E (3B
5L (BW)
5QC (2
5R (BW)
PRINTS 1

3.03 (Continued)

Increase the dummy commutation current signal CC by adjusting the pulse height pot of the Fig. 2 circuit. No change in tabs 17 and 18 pulse widths should be observed until the CC voltage into tabs 11, 12 or 13 reaches from 10.4 to 12.0 volts peak. As the CC voltage is increased above this level, the tabs 17 and 18 pulse widths should increase and should reach 80 μsec. when the CC voltage has been increased by 1.6 to 2.2 volts, to reach 12.1 to 13.9 volts peak. Continue increasing the CC pulse height. The tabs 17 and 18 pulse widths should stop increasing approximately 2 μsec. short of the CC sine wave (zero voltage) base width irrespective of the peak voltage level. Reduce the CC pulse height to minimum and the tabs 17 and 18 pulse widths should return to 34 to 48 μsec.

The ICC output at tab 16 should be high whenever there is an input at any one of tabs 11, 12 or 13 which exceeds 1.0 to 1.5 volts, as shown in Fig. 1.

3.04 Initial Pulse and Inverter Pulse Train

The 1IP output at tab 26 should go high at the time when ICFF tab 18 output goes low at the end of its pulse, as shown in Fig. 1. The tab 26 pulse should be from 10 to 12 μsec. wide.

The 1IPT output at tab 27 should be an unsynchronized pulse train as shown in Fig. 1, with the initial pulse of tab 26 appearing as an extra pulse in this pulse train. The high pulses should be from 9.7 to 11.2 μsec. wide with the low periods between pulses being from 31 to 36 μsec. wide.

3.05 Delayed Firing Supply

Connect a 1K, 2 watt pot, with all resistance in, from DFS tab 10 to common, and connect a 1.8K, 1/2W resistor from tab 10 to +20 volts.

When +20 volt power is applied to this card, output tab 10 should stay below 1.5 volts relative to common for .4 to 1.3 sec. after power is applied before going to its high state. In its high state with 1K output loading, the tab 10 voltage should be from 17.3 to 18.25 volts.

If the 1K pot is adjusted to reduce the loading resistance, the tab 10 output current should increase up to at least 40 ma when the tab 10 output voltage is still 16.0 volts or above. As the loading resistance is decreased further, the tab 10 output current will be limited such that when tab 10 is shorted to common, its output current will be between 45 and 110 ma. A control undervoltage trip should occur during this test and the ORST tab 14 will have to be momentarily tied to common to reset the fault lights.

AW (BW)
5D (BK)
5E (3BW
5K (BW)
5QC (2B
5R (BW)
PRINTS TO

3.06 Control Undervoltage Shutdown

With a fixed 9.0 volt input at tab 5, decrease the +20 volt control supply voltage applied to tab 1. When this voltage reaches a level between 18.2 and 17.8 volts, a control undervoltage shutdown should occur, producing the following results:

a) Turns on CUV light LED-1
b) Turns on IFT light LED-4
c) Causes both OIFT tab 30 and OIFL tab 32 to change from the high state to low.
d) Causes a 40to 120 μsec. long train of low going pulses to appear at OIFP tab 31
e) Causes DFS tab 10 to go from a high state to low, starting 40 to 150 μsec. after the shutdown signal, and decaying to zero on a 25 to 75 μsec. time constant,

The fault latches and lights should be reset by momentarily connecting ORST tab 14 to common, after returning the supply to the +20V level.

A control undervoltage trip can also be initiated by an undervoltage of the delayed firing supply at DFS tab 10. This voltage is decreased by increasing the tab 10 current loading as was done in section 3.07 using a 1K loading pot. When the tab 10 voltage reaches a level between 14.5 and 13.9 volts, a control undervoltage shutdown should occur, producing the following results:

a) Turns on CUV light LED-1
b) Turns on IFT light LED-4
c) Causes both OIFT tab 30 and OIFL tab 32 to change from a high state to low
d) Causes a 40 to 120 μsec. long train of low going pulses to appear at OIFP tab 31.

The fault latches and lights should be reset by momentarily connecting ORST tab 14 to common, after removing the tab 10 overload.

Slowly reduce the +20 volt control power at tab 1 from the under-voltage trip level down to zero volts. The voltage at DFS tab 10 should remain below 2 volts over this whole control undervoltage range.

3.07 Commutation Overcurrent Shutdown

Apply an adjustable voltage to any one of the CC tabs 11, 12 or 13 to simulate a commutation current. When this voltage reaches a level between 17.7 and 18.6 volts, a commutation overcurrent shutdown should occur, producing the following results:

a) Turns on COC light LED-2
b) Turns on IFT light LED-4
c) Causes both OIFT tab 30 and OIFL tab 32 to change from a high state to low
d) Causes a 40 to 120 μsec. long train of low going pulses to appear at OIFP tab 31.

3.07 (continued)

The fault latches and lights should be reset by momentarily connecting ORST tab 14 to common, after reducing the tab 11,12 or 13 voltage.

3.08 Inverter Overfrequency Shutdown

Connect an adjustable frequency, square wave voltage to IPA tab 28. The frequency should be variable from 60 to 300 Hz, with the high and low periods being exactly equal in time. The high voltage level should be from 14 to 20 volts.

There are four overfrequency trip points which are selectable by means of the FT tabs 22, 23, 24 and 25. In each case, when the overfrequency trip level is reached, an overfrequency shutdown should occur, producing the following results:

a) Turns on the IOF light LED-3

b) Causes OIOF tab 29 to change from a high state to low.

After each overfrequency trip, the fault latch and light should be reset by momentarily connecting ORST tab 14 to common.

The IPA tab 28 input frequency which should produce an overfrequency shutdown for each of the four FT75 tab 22 connections is given in the following table:

| FT tabs 22, 23, 24 and 25 connections | IPA tab 28 input frequency |
|---|---|
| 1. All FT tabs open | 68 to 83 Hz |
| 2. FT75 tab 22 - FT110 tab 25 | 99 to 121 Hz |
| 3. FT75 tab 22 - FT165 tab 24 | 151 to 186 Hz |
| 4. FT75 tab 22 - FT275 tab 23 | 248 to 303 Hz |

3.09 Inverter Fault Shutdown

Apply an adjustable voltage to FCC tab 4 to simulate an inverter shoot-through fault. When the tab 4 input voltage reaches a level between 10.2 and 10.8 volts, an inverter fault shutdown should occur, producing the following results:

a) Turns on IFT light LED-4
b) Causes both OIFT tab 30 and OIFL tab 32 to change from a high state to low.
a) Causes a pulse train to appear at OIFP tab 31 which should consist of 7 to 10 μsec. low pulses and 21 to 25 μsec. high periods. This pulse train should persist as long as the voltage at tab 4 exceeds the trip level, but should disappear when the tab 4 voltage is decreased below the trip level.

The fault latch and light should be reset by momentarily connecting ORST tab 14 to common, after removing the tab 4 voltage.

REVISIO

Chg 3.09 1/21/77 cgz

1

AW (BW

5D (BK

5E (3B

5K (BW

5QC (2

5R (BW

PRINTS T

3.10 Link Overvoltage Shutdown

If the OLOV tab 15 is connected to common, to simulate a d.c. link overvoltage trip as detected on another card, a shutdown should occur, producing the following results:

a) Turns on IFT light LED-4
b) Causes both OIFT tab 30 and OIFL tab 32 to change from a high state to low
c) Causes a 40 to 120 μsec. long train of low going pulses to appear at OIFP tab 31

The fault latch and light should be reset by momentarily connecting ORST tab 14 to common, but should reset only after tab 15 is disconnected from common.

4.0 OPERATING and TEST CONDITIONS

This card should be capable of operating within the performance specified in section 2.0 and pass all tests specified in section 3.0 while exposed to the following conditions:

4.01 DC Supply Voltage

+19.8 to +20.2 volts from tab 1 to tab 2.

4.02 Ambient Temperature

0 to +75°C.

4.03 Humidity

24 hours in 90% relative humidity at 40°C.

4.04 Voltage to Ground

600 volts.

AW (BW)
5D (BK)
5E (3BW)
5K (BW)
5QC (2BW)
5R (BW)
PRINTS TO