P3K-AL-0484-A01

TEST INSTRUCTIONS FOR INTERCEPT VALVE AMPLIFIER 1L1-G003
(ASS'Y DWG 118D1358 G1)

FIRST MADE FOR   EHC MARK II (LOAD CONTROL UNIT)

REVISIC

I. SCOPE

This instruction outlines the test specification for circuit board
1L1-G003 (Ass'y Drawing 118D1358 G1; Schematic 125D3663)

II. CIRCUIT DESCRIPTION

The purpose of the Intercept Valve Amplifier is to combine all of the
necessary control functions to produce a single intercept valve flow
reference signal.

This version of the IVA circuit is to be used on those turbines that
utilize the main stop valve bypass valve for rotor warming.

The circuit has input signals of speed error (pins 27, 28) and load
reference (pin 26). The load reference signal is modified by the control
valve regulation potentiometer that is mounted on the IVA circuit board.
In addition, an opening bias is provided by a voltage divider (mounted
on the board). These three (3) signals are summed by the operational
amplifier.

In absence of speed error and load reference, the opening bias is just
enough to keep IV's fully open. With zero load reference a 2% speed
error (+2 V at pin 27) is needed to fully close the IV's. With load
reference present a certain speed error is necessary before the IV's
start closing, and this depends on the load reference and CV regulation
pot setting; it is the same with the speed error which is needed to
fully close the control valves when in PA. Thus a coordination between
CV's and IV's is accomplished. After the IV's valves start closing an
additional 2% speed error is needed to close them fully.

The op amp requires a power stage to provide the necessary output current.
The operational amplifier with power stage has an output limit circuit
that is adjusted to establish the maximum IV flow reference signal for
normal operation and that is adjustable for reducing the IV flow reference
signal for the reheat safety valve check.

The IVA drives two, three, or four valve position loops (pins 33, 34, 35
and 36) whose individual impedances are 20 kilohms and nonvarying; it
also drives a voltage comparator (pin 32). On the board the same gated
amplifier signal drives a voltage follower used to provide a IVA signal
to the Standby Control Unit (pin 29) and to a meter (pins 30 and 31).

A positive bias is applied to the operational amplifier during rotor
warming to provide a fully closed IV flow reference signal during rotor
warming. During normal operation this bias is removed by connecting
pin 24 to pin 25.

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III. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

1. Power Supply 1: (Pin 37)
   +22.000 $\pm$ 0.002 VDC at 300 ma (Approx)

2. Power Supply 2: (Pin 41)
   -22.000 $\pm$ 0.002 VDC at 150 ma (Approx)

B. Operating Signal Levels

1. Input 1 (Speed Error Signal - Pin 28):
   $\pm$ 10 VDC (0 volts at speed, 1 volt/1% speed error)

2. Input 2 (Load Reference Signal - Pin 26):
   0 to -10 VDC (0 volts at no load, -10V at full load)

C. Output Loads

1. Load 1 (Pin 32):
   5 K Ohms $\pm$ 1% (max. load)

2. Load 2 (Pin 29):
   10 K Ohms $\pm$ 1%

3. Load 3 (Pin 30 - Pin 31):
   40 Ohms $\pm$ 1% (simulates meter)

D. Individual Stage Performance Specifications

1. Power Supply (CR1 - CR4):
   a. TP1: +15.7 $\pm$ 1.0 VDC
   b. TP2: -15.7 $\pm$ 1.0 VDC

   adj VR2 fully CW
   " VR3 " CCW
   Gnd TP9 SEE BACK OF this SHEET ALSO

2. Intercept Valve Amplifier (IC1, Q1)
   a. Acceptable offset at TP3
      (zero input): $\pm$ 1.0m VDC   *SET TO ϕ*
      (Adjustable through VR50 - Adjustment point should be
      at least two turns away from either pot ends)
   b. Transfer Function for Speed Error Signal (R3, R4, R11, C1)

   REMOVE JUMPER FROM TP7 TO GND

   $$\frac{TP3}{TP7} = \frac{-G_1}{1 + T_1 \cdot S}$$

   Where Gain (G1) = 5.000 $\pm$ 0.100 volts/volt
   Noise Suppression Lag Time Constant (T1) = 1.54 $\pm$ 0.17 msec.
   Noise Suppression Breakpoint (F1) = 105 $\pm$ 12 HZ

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III. CIRCUIT SPECIFICATIONS (continued)

    D. Individual Stage Performance Specifications (continued)

        2. (continued)

            c. Transfer Function for Load Reference Signal
                (VR1, R5, R6, R11, C2)   *REMOVE JUMPER FROM TP6 TO GND*

$$\frac{TP3}{TP6} = \frac{-G2}{1 + T_2 \cdot S}$$

                C1 CR1 fully counterclockwise
                Gain (G2) = 1.247 ± 0.058 volts/volt
                Noise Suppression Lag Time Constant (T_2) = $1.85 \pm .22$ msec.
                Noise Suppression Breakpoint (F2) = 86 ± 10 HZ

                C2 VR1 fully clockwise
                Gain (G2) = 3.755 ± 0.075 volts/volt
                Noise Suppression Lag Time Constant (T2) - 1.12 ± 0.12 sec.
                Noise Suppression Breakpoint (F2) = 144 ± 16 HZ

            d. Transfer function for Opening Bias
                (R8 and R11)   *REMOVE JUMPER FROM TP9 TO GND*

$$\frac{TP3}{TP9} = -G_3$$

                Gain (G3) = 1.000 ± 0.020 volts/volt

            e. Transfer Function for Closing Bias
                (R11, R19, R20, R21, C3)

GND TP9
Jumper 23 to 24
REMOVE JUMPER PIN 24 TO 25

$$\frac{TP3}{TP5} = \frac{-G4}{1 + T_4 \cdot S}$$

                Gain (G4) = 2.000 ± 0.040 volts/volt
                Noise Suppression Lag Time Constant (T4) = 932 ± 173 msec
                Noise Suppression Breakpoint (F4) = 0.17 ± 0.02 HZ

            f. Saturation Limits (TP8)
                ± 13 VDC (minimum)

        3. Meter Amplifier (IC2)

REMOVE JUMPER 23 to 24
GND TP9
GND PIN 32

            TP10
            a. Acceptable offset (zero input = ± 1.0m VDC
                (Adjustment point should be at least two turns away from
                either pot ends) *VR51   SET TO ∅*

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III. CIRCUIT SPECIFICATIONS (continued)

D. Individual Stage Performance Specifications (continued)

3. (Continued)

Remove GND from 32

b. Transfer Function for Meter Amplifier Output

$$\frac{TP10}{TP3} = G_5$$

Where Gain (G_5) = 1.000 volts/volt

c. Saturation Limits (10 K Ohm effective load) = $\pm$ 12.0 VDC (minimum)

Put 12U PIN 24
TP3 ≈ TP10 + >12
Remove PIN 24

4. Voltage Divider Network for Opening Bias (R7, R8, R9, VR4)

VR4 POSITION	VOLTAGE AT TP9
CCW	-9.596 ± 0.188 VDC
CW	-10.572 ± 0.110 VDC

5. Voltage Divider Network for Closing Bias (R17, R18, R19, R21)

Jumper PIN 23 TO 24

Voltage at TP5: 10.049 ± 0.109 VDC

6. Voltage Divider Network for Flow Ceiling Limit (R11, R14, R15, R16, VR2, VR3)

Remove Jumper 23 TO 24

1C1 driven into positive saturation.

VR2 POSITION	VR3 POSITION	VOLTAGE AT TP3
CCW	CCW	$-1.399 \pm .120$ VDC
CCW	CW	$-1.364 \pm .123$ VDC
CW	CCW	$6.666 \pm .396$ VDC
CW	CW	$11.458 \pm .120$ VDC

IV. SET POINTS

A. Adjustment of VR50

TP6   TP7

With zero input at IC1 (pins 26, 27 and TP9 ground, Pin 24 connected to Pin 25) and VR2 fully CW VR50 should be adjusted so that TP3 voltage is $\pm$ 1.0 mV. *SET TO ∅*

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IV.   SET POINTS (continued)

B.   Adjustment of VR51

With zero input to IC2 VR51 should be adjusted so that TP10 voltage is ± 1.0mV.

C.   Adjustment of VR2

VR2 should be adjusted fully CW.

D.   Adjustment of VR3

With IC1 driven into positive saturation VR3 should be adjusted so that TP3 voltage is 10.100 VDC.

E.   Adjustment of VR4

REMOVE TP9, PINS 26 + 27 FROM GND

TP7

With +2.000 VDC at pin 27 and pin 24 connected to pin 25 adjust VR4 so that TP3 voltage is ± 1mV. *SET TO Ø*

F.   Adjustment of VR1 for 5% CV regulation

TP6   *TP7*

With −10.000 VDC at pin 26, +7.000 VDC at pin 27 and pin 24 connected to pin 25, adjust VR1 so that TP3 voltage is ± 1mV.

G.   Adjustment of VR5   *Remove Jumper 24 to 25*

With meter connected between 30 and 31 adjust VR5 so that +10.000 VDC at TP3 produces full scale deflection of the meter.

└ 40mV between 30 + 31

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