g GE Energy	**Functional Testing Specification**
Parts & Repair Services ***Louisville, KY***	**LOU-GED-DS200DDTB-A**

Test Procedure for a DS200DDTBGxA "ADMA Terminal Board"

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1. SCOPE

1.1 This is a functional testing procedure for an ADMA Terminal Board.

2. STANDARDS OF QUALITY

2.1 Refer to the current revision of the IPC-A-610 standard for workmanship standards.

3. APPLICABLE DOCUMENTS

3.1 The following document(s) shall form part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue shall apply.

3.1.1 N:\Design Folders\DS\DS200\DS200D\DDTB\Louisville Test prints (AB).pdf
3.1.2 N:\Design Folders\DS\DS200\DS200D\DDTB\Louisville G2 Test prints (AB).pdf
3.1.3 N:\Design Folders\DS\DS200\DS200D\DDTB\GEI-100219.pdf
3.1.4 N:\Design Folders\DS\DS200\DS200D\DDTB\Design Req's (helpful explanations).pdf
3.1.5 N:\Design Folders\DS\DS200\DS200D\DDTB\ECN's
3.1.6 N:\Design Folders\DS\DS200\DS200D\DDTB\G1AB Material List.pdf
3.1.7 N:\Design Folders\DS\DS200\DS200D\DDTB\G2AB Material List.pdf

4. ENGINEERING REQUIREMENTS

4.1 Equipment Cleaning
4.1.1 Equipment should be clean and free of debris prior to applying power unless performing an initial check. Refer to the local documented procedures for cleaning guidelines.

4.2 Equipment Inspection
4.2.1 Equipment should be visually inspected for any defects prior to applying power. This inspection should include the following as a minimum:
4.2.1.1 Wires - broken, cracked, or loosely connected
4.2.1.2 Terminal strips / connectors - broken or cracked
4.2.1.3 Components - visually damaged
4.2.1.4 Capacitors - bloated or leaking
4.2.1.5 Solder joints - damaged or cold
4.2.1.6 Circuit board - burned or de-laminated
4.2.1.7 Printed wire runs / Traces - burned or damaged

5. EQUIPMENT REQUIRED

5.1 The following equipment is required to perform the process requirements. Equipment may be substituted provided that all accuracy's and test ratios are equivalent or better.

Qty	Reference #	Description
1		Fluke 87 DMM (or Equivalent)
1		Tenma Dual Power Supply (or Equivalent)
1	H188643	DS200DDTB TBPL Connector Breakout Board
1		5V TTL Logic Probe (optional)
1		5V TTL Logic Pulser Probe (optional)
1		480Vac single phase transformer

6. TESTING PROCESS

6.1 Setup

6.1.1 Plug the ribbon cable of the TBPL Connector Breakout Board into the TBPL connector of unit under test. From here on out, whenever a TBPL pin is called out for a connection, it's meant for you to connect to it using the pins provided on the breakout board.

6.1.2 On your power supply, you'll need (+) & (-) 15Vdc, and (+) 5Vdc, with the common of the 5Vdc tied to common of the +/-15Vdc. Common then connects to both the ACOM (TBPL-60) and DCOM (TBPL-1) of the breakout connector. +5V connects to TBPL-28, +15V connects to TBPL-52, and –15V connects to TBPL-48. Connect a few extra mini-grabber leads to COM and also to +5V. You will use them as HI or LOW inputs. All voltage readings taken at a TBPL pin shall be in respect to COM (ACOM/DCOM).

✍ **Note: Most of the pins on the TBPL connector have multiple functions and you will be re-visiting them as you progress through the test. This test is written following the prints according the order that the circuits appear, so as to aid in troubleshooting and overall understanding of what's happening. You may also use the GEI-100219 and the Design Requirements documents found in the DDTB folder in Design Folders to aid you in troubleshooting. ALSO NOTE that the G2 units have deleted several circuits, so you will see notes through parts of this test that mention "G1 Only" or "G1 & G2". If you have a G2 unit, refer to the G2 Test Note Prints for specifics. This test was written while testing a G2, and once we get a G1 in, we will need to confirm or revise its accuracy for G1 units.**

6.2 Testing Procedure

6.2.1 With unit powered up, you will need to take TBPL-27 to HI. This is an enable that sets multiple switches and MUX channels for the following steps. Its natural (open or unconnected) state is LOW. Later you will be testing some of these circuits again,

without TBPL-27 enabled (HI). But for now, leave this pin HI. The green DS-17 "ONLINE" LED should also be lit.

6.2.2 **Only on G1 units:** (See Sh.4BA) apply an input of 10Vdc across TB2-Y7 (+) & Y8 (-), and you should see +5Vdc output at TBPL-37. Reversing the polarity of the 10Vdc input to negative (–)10Vdc should cause the output to go to –5Vdc. Repeat test as follows:

Input + & -	**Output**
TB2-Y7 & Y8	TBPL-37
TB2-Y9 & Y10	TBPL-39
TB2-Y11 & Y12	TBPL-41
TB2-Y13 & Y14	TBPL-43

6.2.3 **Reference Bias** (Sh.4CA) These circuits can be set up for to provide a neutral (0.0Vdc) output when idle (with no input), or they can be set to provide a negative (-) 5Vdc output when idle. Check this bias accordingly: with jumpers JP3 & 9 (**G2 & G1**) and jumpers 6 & 12 (**G1 only**) set to 1-2, outputs at TBPL-45, 47, 49, & 51 should read 0.0Vdc. Move jumpers JP3, 9, 6 & 12 to position 2-3 and these same outputs should all be reading Neg –5Vdc. You can leave the jumpers there or move them back, as it will not affect the following step.

6.2.4 **For G2 units,** there will be only two circuits to test in this step. G1 Units will have to have all eight tested. Either way, when (+) or (-) 10Vdc is applied, the output will rail to either (+) or (-) 14Vdc according to what the input polarity is. There is a set of jumpers for each of these amplifiers that decides what input each circuit sees. The chart includes jumper settings for each circuit, input polarity, and output pin. Output polarity should go opposite as the input polarity is flipped, just like in step 6.2.2.

G1 or G2	**JUMPERS**	**INPUT**	**OUTPUT**
G1 & G2	JP1 & JP2 = 2-3	TB1-X1 & X2	TBPL-45
G1	JP1 & JP2 = 1-2	**TB2**-Y15 & Y16	TBPL-45
G1	JP4 & JP5 = 2-3	TB1- X1 & X2	TBPL-49
G1	JP4 & JP5 = 1-2	TB1- X7 & X8	TBPL-49
G1 & G2	JP7 & JP8 = 2-3	TB1- X3 & X4	TBPL-47
G1	JP7 & JP8 = 1-2	TB1- XA & XB	TBPL-47
G1	JP10 & JP11 = 2-3	TB1- X3 & X4	TBPL-51
G1	JP10 & JP11 = 1-2	TB1- X9 & X10	TBPL-51

6.2.5 **More op-amps**, (Sh.4DA). This step will seem like a repeat of 6.2.2, because it almost is. On G1 & G2 units, simply apply 10Vdc across TB1-X5 (+) & X6 (-). Output should be +5Vdc at TBPL-59. Reversing polarity of the input will cause output to swap polarity as well. Repeat test for G1 units only (may need verification at this point) for inputs TB1-X11 & X12, with output being on TBPL-53.

6.2.6 **480Vac attenuation,** Using a transformer to make 480Vac single phase from a standard 120Vac outlet, apply this voltage to TB3-1 and TB3-3. You should observe approximately 2.4Vac at TBPL-55. Repeat test with inputs TB4-1 & TB4-3, and output on TBPL-57, seeing the same 2.4Vac output. Remove 480Vac, you're done with it.

6.2.7 **Rectified inputs,** (Sh.4EA) **Don't confuse this to mean that AC get's applied here.** These are inputs meant to take 10Vdc of either polarity and rectify it so that you get a +5Vdc output regardless. Simply apply 10Vdc to each input of the following table, and observe the output go to +5Vdc, and then reverse the input polarity, and the output should return to **+**5Vdc. Also observe that the LED that corresponds to that particular circuit lights up as voltage is applied:

Input	Output	LED #
TB2-X7 & X8	TBPL-14	DS-1
TB2-X9 & X10	TBPL-15	DS-2
TB2-X11 & X12	TBPL-17	DS-3
TB2-X13 & X14	TBPL-18	DS-4
TB2-X15 & X16	TBPL-20	DS-5
TB2-YA & YB	TBPL-21	DS-6
TB2-Y1 & Y2	TBPL-23	DS-7
TB2-Y3 & Y4	TBPL-24	DS-8

6.2.8 **Relay contacts,** (Sh.4GA) There are four relays with corresponding DS LEDs that need to be tested. As you fire each one, check the continuity of it on both normally open and normally closed contacts. Each is listed on the following chart. Simply apply a LOW to the input, and you can test the relay before and after it's engaged:

Relay	LED#	Input	N/C	CMN	N/O
K1	DS-13	TBPL-8	TB2-X4	TB2-XB	TB2-X2
K2	DS-14	TBPL-9	TB2-X3	TB2-XA	TB2-X1
K3	DS-15	TBPL-11	TB5-1	TB5-3	TB5-2
K4	DS-16	TBPL-12	TB5-5	TB5-6	TB5-4

6.2.9 **Opto-coupled open-collector outputs,** (SH.4GA) These circuits have an open collector output that fires when you give the circuit a LOW input. These four circuits also tie in with mux addressing, but we won't worry about that until later. From your 5Vdc power supply positive lead, connect a 10K ohm resistor in series with the positive of your meter to make a pull-up circuit. Connect the positive of your meter now to the positive of the circuit (as defined in the table below) and tie the (-) portion of each output to COM. As you fire each circuit, you are looking to see the output to transition from HI to LOW. Observe the corresponding LED light as well. See table below:

Input	Led#	Meter (+) & 5V Pull-up	Meter (-) & Com
TBPL-2	DS-9	TB1-Y9	TB1-Y10
TBPL-3	DS-10	TB1-Y11	TB1-Y12
TBPL-5	DS-11	TB1-Y13	TB1-Y14
TBPL-6	DS-12	TB1-Y15	TB1-Y16

6.2.10 **More Op-amps,** (SH.4HA) the next four op-amps are 2 to 1 gain circuits. Apply 0-7Vdc to the inputs, and observe that the output rails at approximately 14Vdc. Reverse polarity on the input and output polarity will swap to match it:

Input	Output
TBPL-29	TB1-X13
TBPL-31	TB1-YA
TBPL-33	TB1-Y3
TBPL-35	TB1-Y5

6.2.11 **6.2.10 Continued…** Now connect a 1.2K-Ohm resistor across output TB1-X15 and X16. Connect your meter to read across this resistor, with (+) being at TB1-X15. Apply 0-7Vdc to TBPL-29, and you should observe the voltage across your load resistor go from 14Vdc down to almost 0.5Vdc. Now reverse polarity on TBPL-29 re-apply 0-7Vdc and you should read between 14 & 22Vdc across the output. Repeat this step for input TBPL-31, with outputs TB1-Y1 (+) & TB1-Y2 (-).

6.2.12 Test the Data ID chip to ensure it is programmed correctly using the Chip ID pc. You may wish to wait until you've completed functional testing because it requires the unit under test AND the breakout board be carried over to the Chip ID pc for testing. You'll be reminded at the end of testing.

6.2.13 **ATEST and MUX Addressing,** (SH.4JA) **Last and longest step:** All odd numbered outputs on TBPL from TBPL-37 through TBPL-59 are set up on switches that can be

controlled by the enable function of the "ONLINE" circuit of TBPL-27. When you remove the HI from TBPL-27, it's natural state takes it LOW, which, when NAND gated with the natural (HI) state of inputs TBPL-5, 6, & 8, causes the odd numbered outputs between TBPL-37 & TBPL-59 to switch over to a MUX network that can be clocked through four different addresses to apply pre-chosen signals to these outputs. To test these MUXes, first take a reading of the following outputs: TBPL-37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, & 59. If there is nothing connected to TBPL-2 or 3, then they should all be tied to COM. TBPL-2 and TBPL-3 are tied to the MUX address lines through inverters, so both inputs being open leaves them in their natural HI state, which inverts to LOW on the MUXes and gives an address of 00, which is tied to ACOM. Now apply a LOW to TBPL-2. When inverted, this calls for address 01, which is tied to +5Vdc. All of the aforementioned outputs should now read +5Vdc. Remove LOW from TBPL-2 and apply it to TBPL-3. The inverters turn this into address 10, which is tied to -5Vdc, and now all outputs should be reading -5Vdc. Simple enough? Now for the last address, 11, which is achieved by applying a LOW to both TBPL-2 & TBPL-3. This connects the outputs by groups of three to the inputs you previously tested in step 6.2.10. The outputs at this stage will naturally sit in the LOW state, so the easiest way to test them would be to follow the following table and apply either +5Vdc and observe the outputs, or use a TTL pulser probe to drive the inputs while observing with a TTL logic probe or meter to see that the outputs follow the inputs. Use the table below:

Inputs (with TBPL-2 & 3 LOW)	Outputs
TBPL-29	TBPL-37, 45, & 53
TBPL-31	TBPL-39, 47, & 55
TBPL-33	TBPL-41, 49, & 57
TBPL-35	TBPL-43, 51, & 59

6.3 Post Testing Burn-in Required ___ Yes _X_ No

Note: DON'T FORGET TO TEST THE ID CHIP IF YOU OPTED TO SKIP THAT STEP AND RETURN TO IT LATER …

TBPL-26=DATA, TBPL-1=DCOM

6.4 ***TEST COMPLETE ***

7. NOTES

7.1

8. ATTACHMENTS

8.1