g GE Energy	**Functional Testing Specification**
Inspection & Repair Services ***Louisville, KY***	**LOU-GEF-MPU1** **1050HL Board**

Test Procedure for MPU1 Printed Circuit Board for a 1050HL Control

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Functional test procedure for 1050HL MPU1 Printed Circuit Board

1. SCOPE

1.1 The instructions apply to all MPU1 boards in test.

2. STANDARDS OF QUALITY

2.1 Refer to the current revision of the IPC-A-610 standard for workmanship standards.

3. APPLICABLE DOCUMENTS

3.1 The following document(s) shall form part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue shall apply.
3.1.1 GEK-71770

4. ENGINEERING REQUIREMENTS

4.1 Description
4.1.1 The 1050 Control is a solid-state, integrated circuit controller/processor system using LSI circuits for data processing and control. The static logic circuits are arranged on modular, plug in, printed circuit boards, clearly identified by type. The circuit boards are mounted with functional grouping. In addition, a board identification number marks each rack slot.

4.2 Equipment Cleaning
4.2.1 Equipment should be clean and free of debris prior to applying power unless performing an initial check. Refer to the local documented procedures for cleaning guidelines.

4.3 Equipment Inspection
4.3.1 Equipment should be visually inspected for any defects prior to applying power. This inspection should include the following as a minimum:
4.3.1.1 Wires broken or cracked
4.3.1.2 Terminal strips / connectors broken or cracked
4.3.1.3 Loose wires
4.3.1.4 Components visually damaged
4.3.1.5 Capacitors leaking
4.3.1.6 Solder joints damaged or cold
4.3.1.7 Circuit board burned or de-laminated
4.3.1.8 Printed wire runs burned or damaged

5. EQUIPMENT REQUIRED

5.1 The following equipment is required to perform the process requirements. Equipment may be substituted provided that all accuracy's and test ratios are equivalent or better.

Qty	Reference #	Description
1	GE 1050HL	Control with axis cart

6. Purpose:

6.1 To describe the procedure for testing the circuitry of the MPU1 board using the 1050HL simulator.

7. General:

7.1 The MPU1 test exercises the 8080A instructions set using the system's resident diagnostics software.

8. TESTING PROCESS

8.1 Procedure

8.1.1 Remove the test MPU1 board from slot 11 and insert the board to be tested.
8.1.2 Special Mode Switch should be on (UP).
8.1.3 Press "ON".
8.1.4 "00" or "20" should appear in the message display and "?" in the alphanumeric display
8.1.5 Press "P4", "1", and "ENTER". This instructs the control to read from the resident diagnostics boards (DPMA and DPMD).
8.1.6 A "T" will appear in the alpha display. Press "100" and "ENTER". This instructs the control to read the block of diagnostics hat contains the MPU1 board test. See Exhibit A.
8.1.7 Press "FWD".
8.1.8 An "I" will appear in the alpha display. Press "ENTER" to run test once or press "00" and "ENTER" to iterate testing.
8.1.9 An "S" will appear in the alpha display. Press "ENTER" to stop if an error is detected or "N" and "ENTER" to continue testing.
8.1.10 A "V" will appear in alpha display. Press "FWD" to begin testing.
8.1.11 Any detected errors will be displayed in the message display. The meaning of these error codes can be found in Exhibit A.

8.2 ***TEST COMPLETE ***

8.3 Exhibit A

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EXHIBIT A

ROM Board Diagnostics for the 1050N Control
Test Descriptions - Data Controller
Processor Test

DATA CONTROLLER PROCESSOR TEST

Identification Number: 9100

Boards Tested: MPC

Commands: None

Displays: Standard displays only

Error Numbers: See below

General Comments:

Detection of an error causes the appropriate error number to be displayed in the message display. This test does not attempt to continue after detection of an error. In no case can more than one error be detected per pass.

With the exception of the HLT, NOP, DI, EI and the 8 RST instructions, this test exercises the 8080A instruction set. Initially, each flag is alternately set and tested, then cleared and tested by each instruction that can affect the flag. Subsequently, all instructions except those 12 mentioned above are exercised and tested.

Table 4.
DATA CONTROLLER PROCESSOR TEST - ERROR CODES

ERROR NUMBER	DETECTED FAILURE
10	Zero flag fails to set.
11	Zero flag fails to clear.
12	Carry flag fails to clear.
13	Carry flag fails to set.
14	Sign flag fails to set.
15	Sign flag fails to clear.
16	Parity flag fails to set.
17	Parity flag fails to clear.
18	MVI, CPI, CMP instructions fail.
19	CMA instruction fail.
20	MOV instructions fail.
21	ADD R instructions fail.
22	ADC R instructions fail.
23	SUB R instructions fail.
24	SBB R instructions fail.
25	ANA R instructions fail.
26	XRA R instructions fail.
27	ORA R instructions fail.
28	ADI instruction fail.
29	ACI instruction fail.
30	SUI instruction fail.
31	SBI instruction fail.
32	ANI instruction fail.
33	XRI instruction fail.
34	ORI instruction fail.
35	INR R instructions fail.
36	DCR R instructions fail.
37	LXI R instructions fail.
38	INX R instructions fail.
39	DAD R instructions fail.
40	DCX R instructions fail.
41	LDA, LDAX R, LHLD instructions fail.
42	STA, STAX R, SHLD instructions fail.
43	SPHL, DAD SP, LXI SP, INX SP, DCX SP instructions fail.
44	XTHL instruction fail.
45	XCHG instruction fail.
46	PUSH, POP instructions fail.
47	CALL, CALL ON CONDITION instructions fail.
48	RETURN, RETURN ON CONDITION instructions fail.

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