g GE Energy *Parts & Repair Services* *Louisville, KY*	**Functional Testing Specification** **LOU-GE-DS200FGPA**

Test Procedure for an LS2100 LCI Firing Gate Pulse Amplifier Card

DOCUMENT REVISION STATUS: Determined by the last entry in the "REV" and "DATE" column

REV.	DESCRIPTION	SIGNATURE	REV. DATE
A	Initial release, copied over from FGPAG1.doc factory test, with updates generated in Louisville	John Madden	11-26-08
B	Upgraded test fixture for burn-in and troubleshooting capabilities and to eliminate function generator, added test for optical STATUS mux monitoring (which now requires the use of a variac)	John Madden	1-13-09
C	Added data sheet Page 13 to document.	C. Wade	2/12/2009
D	Components affected by extending Crowbar Testing, Section 6.2	C. Wade	8/17/2011
E	Had to remove above number step because it through off the data sheet step orientation. Left it as a special note in section 6.1	C. Wade	10/5/2011

PREPARED BY	REVIEWED BY	REVIEWED BY	QUALITY APPROVAL
John Madden			Charlie Wade
DATE	**DATE**	**DATE**	**DATE**
January 13, 2009			2/12/2009

1. **SCOPE**

1.1 This is a functional testing procedure for an LCI Firing Card.

2. **STANDARDS OF QUALITY**

2.1 Refer to the current revision of the IPC-A-610 standard for workmanship standards.

3. **APPLICABLE DOCUMENTS**

3.1 The following document(s) shall form part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue shall apply.

3.1.1 N:\Design Folders\DS\DS200\DS200F\FGPA

4. **ENGINEERING REQUIREMENTS**

4.1 Equipment Cleaning

4.1.1 Equipment should be clean and free of debris prior to applying power unless performing an initial check. Refer to the local documented procedures for cleaning guidelines.

4.2 Equipment Inspection

4.2.1 Equipment should be visually inspected for any defects prior to applying power. This inspection should include the following as a minimum:

4.2.1.1 Wires - broken, cracked, or loosely connected
4.2.1.2 Terminal strips / connectors - broken or cracked
4.2.1.3 Components - visually damaged
4.2.1.4 Capacitors - bloated or leaking
4.2.1.5 Solder joints - damaged or cold
4.2.1.6 Circuit board - burned or de-laminated
4.2.1.7 Printed wire runs / Traces - burned or damaged

5. **EQUIPMENT REQUIRED**

5.1 The following equipment is required to perform the process requirements. Equipment may be substituted provided that all accuracy's and test ratios are equivalent or better.

Qty	Reference #	Description
1		Fluke 87 DMM (or Equivalent)
1	H033944	FGPA test fixture & kit
1		0-120Vac Variac
1		2 channel digital O-scope

6. TESTING PROCESS

6.1 Setup is described in the test steps.

Note: Experience and data from Salem indicates that many of these cards tend to burn up the push-pull FET drivers, including the series resistors in line with these FETs, and the TC427 driver ic's that operate them. A couple of ECN's were issued pertaining to regulation of the P15 bus, yet they still burn these components up on occasion. Salem's failure analyses have also found that C410 in the buck regulator circuit has failed in some cases, which might explain the problems in P15 bus regulation, yet they haven't issued any ECN's on the subject. We here in Louisville recommend replacement of C410, 104X122AA__415, on all units, because when we found the failure descriptions in Salem's FRATS system, we checked some units here and they failed tolerance and leakage testing on C410.

All units from revision AEC and later, shall be upgraded to at least AHD revision, see section 7. AEB and older should not be repaired without customer's consent due to instability problems. I would recommend that unit be replaced with AHD or later revisions, either with new or if we have them from legacy. C. Wade (QA)

See the ECN folder in N:\Design folders \DS\DS200\DS200F\FGPA for what to do. Attached in 7.1 is a listing of these revisions.

Special Note of parts requiring change out.

The U106/206 and D106/206 are thought to be the components most affected by extended Crow bar testing. Due to cards subjected to incorrect crowbar testing, we will immediately require replacement of these 4 components every time a board comes in for repair. For more information see model number folder – emails.

U106 & U206 – 68A9814P3=HV017

D106 & D206 – 68A9933P1=HV017

6.2 Testing Procedure: The following steps are copied from FGPAG1.doc test procedure:

6.2.1 Fixture Connections: Connect the FGPAG1A Fixture to the AGATE1 (Red), AGATE2 (White), BGATE1 (Red), & BGATE2 (White) Fastons on the card.

6.2.2 Connect Oscilloscope CH. 1 to the AGATE bnc jack and CH.2 to the BGATE bnc jack of the fixture.

6.2.3 Connect 115/120Vac to FGPAG1A fixture using the computer cord jack on the rear of the unit.

6.2.4 Connect 115 VAC (using the AC adapter cable) to P1-1 and P1-3. Make sure to plug this cable into a variac that is set to roughly 115-120Vac. Turn power on.

6.2.5 Connect the DVM between P5 (TP401 [*J6*]) and Common (GND faston, TP402 [*F12*] or TP403 [*G12*]). Adjust R4 until DVM reads 5.02 ± 0.02. **(Note: if this voltage isn't correct from the beginning, check the electrolytic caps before adjusting R4. You may simply have a leaking or blown cap causing the problem)**

6.2.6 **AGATE Testing:** Connect the FGPAG1A Fixture AGATEIN Fiber Optic transmitter to AGATEIN on the card under test, but wait before connecting BGATEIN of fixture to BGATEIN of card.

6.2.7 Verify the correct Voltages are present:

P15 (TP404 [*F7*]) to Com (GND faston, TP402 or TP403) = 13.5 to 14.5 VDC
(**P15= >10VDC on AHD & later revs**)
P90 (TP405 [*A7*]) to Com (GND faston, TP402 or TP403) = > 81.0 VDC
P40 (TP406 [*A6*]) to Com (GND faston, TP402 or TP403) = > 25 VDC

6.2.8 Verify that PSOK (DS401 [*J6*]) Green LED is ON.

6.2.9 Verify that DS101 (GATEA RX [*I2*]) Red LED is ON

6.2.10 Waveform on scope (AGATE) should look like the figure 1 below **(NOTE: the actual frequency of the "back porch", or the part of the waveform that follows the initial negative spike, will be set by the FGPA card and is not affected by the frequency adjustment of the fixture. The factory test pattern here shows approximately 25KHz, and the GEI-100223 manual for the FGPA card lists approximately 33KHz, so anything in between the two should be fine. The frequency adjustment of the fixture pertains to the 60Hz [16.6mSec] pulse of the optical drivers. @ 50% duty cycle, each gate should be turned on for 8.3mSec each. See photo 8.3 for clarity)**:

Scope Setup: Vert. 5.00 V
Horiz: 20.0 us
+ Edge Trigger @ - 14.0 V

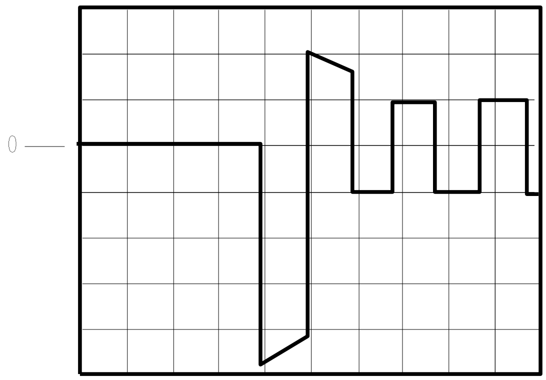


Figure 1

6.2.11 Waveform on scope (AGATE) should look like the figure 2 below:

Scope Setup: Vert. 5.00 V

Horiz. 2.0 ms

Edge Trigger @ - 14.0 V

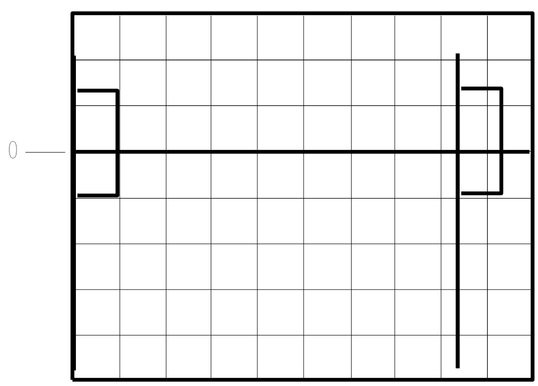


Figure 2

6.2.12 **BGATE Testing:** Now connect the FGPAG1A BGATEIN Fiber Optic cable to BGATEIN (DO NOT leave one in AGATEIN). Observe Scope CH. 2.

6.2.13 Verify that DS201 (GATEB RX [*I2*]) Red LED is ON.

6.2.14 Waveform on scope (BGATE) should look figure 3 below **(see bold print NOTE in 6.2.10)**:

Scope Setup: Vert. 5.00 V

Horiz. 20.0 us
+ Edge Trigger @ - 14.0 V

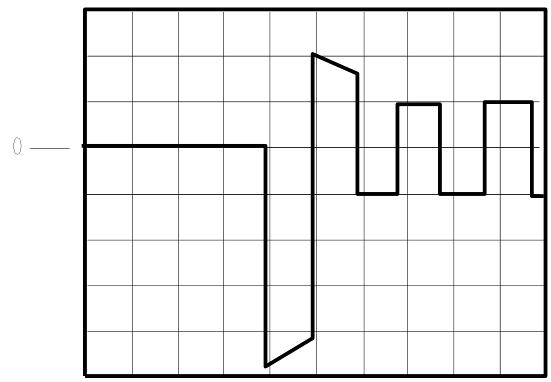


Figure 3

6.2.15 Waveform on scope (BGATE) should look figure 4 below:

Scope Setup: Vert. 5.00 V
Horiz. 2.0 ms
Edge Trigger @ - 14.0 V

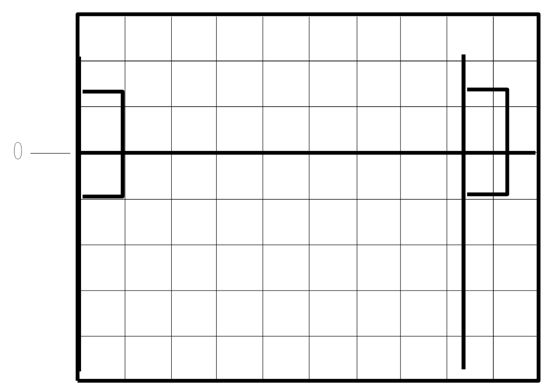


Figure 4

6.2.16 **AGATE & BGATE Testing:** Now connect both AGATEIN & BGATEIN optical drivers and run the unit. You should see the waveforms exhibited in 8.1-8.5. If you feel one side or the other is performing poorly, you can troubleshoot using the phasing button on the fixture. By pushing this button, you will bring the patterns into phase, which will make them overlap on the scope screen for comparison. There will be some variances, mostly in peak voltage, about 2 or 3 volts in either direction, and sometimes slightly in "back porch" frequency. You should see 16-20Vp-p on the "back porch", and about

35Vp-p on the "pedestal", which is the term for the initial negative spike of the waveform. ***DO NOT run it very long with the phasing button pushed in, because the board wasn't designed to run both sides in phase and it will overload the switching supply, causing it to cut out intermittently. Use this only as a comparison tool or for troubleshooting.***

6.2.17 **STATUS Optical Multiplexer Circuit:** For the time being, disconnect the A & B Gate fiber optic cables, while leaving the unit running. Connect a fiber optic cable between the STATUS transmitter U318 on the board and the STATUS receiver on the FGPAG1A Fixture. Disconnect the BNC cables on CH. 1 & CH. 2. Now connect a BNC cable from CH. 1 to the MUX WAVEFORM jack on the left side of the fixture. Use the Auto set feature of the scope, and you will see a waveform similar to the one in photo 8.6. Now, as you take a small flashlight (the Maglight issued to you in your toolbox), slowly sweep from CSTAT12 on the left all the way to CSTAT1 on the right, and you should observe a single "blip" walk from left to right on the scope as you trigger each individual receiver and the signal gets multiplexed into one stream. You are looking at the raw data being fed from transmitter U318. Sometimes you may encounter a ghost image on the scope travelling the opposite direction, but this is due to the scope having trouble triggering correctly for this kind of signal. Do not be alarmed by this. What you are looking for are any "holes" or "gaps" in the sweep that may indicate a bad receiver, or no sweep at all, which may indicate a bad transmitter or multiplexer circuit. Also watch the individual LED's behind each receiver to observe their status as an input is given, they should light up as well. 8.6 through 8.11 show some of the progression. For a complete picture of all waveforms see the Design folders, N:\Design Folders\DS\DS200\DS200F\FGPA\New FGPA test\Optical Mux Waveforms

6.2.18 **Power Supply Undervoltage Testing:** While still observing the STATUS output on the scope, slowly turn the variac down. At approximately 40-50Vac input power, you should see the waveform for Power Supply Undervoltage as P5, P90, or P40 drop below acceptable levels. See Photo 8.12. Now bring the power back up to 120Vac, and connect AGATEIN and BGATEIN optical drivers from the fixture so the unit can run both gates while you observe the STATUS output. Try hitting the phase button. You will see the Undervolt signal sent out at the same time you hear the switching supply sputtering. This shows the momentary overloading that happens when you hold this button down. Release the button. Now connect the scope channels 1 & 2 back to the AGATE &

BGATE BNC jacks as before. Set scope up to observe photo 8.3 or similar image. Continue with the factory test as follows:

6.2.19 Connect the DVM between P5 (TP401 [*J6*]) and DCOMA (TP402 [*F12*]).

6.2.20 Lower variac voltage until scope trace disappears.

6.2.21 DVM reads 4.4 to 4.6 volts.

6.2.22 Verify PSOK (DS401) LED is OFF.

6.2.23 Return Variac to 115VAC and PSOK (DS401) LED should come back ON and the trace should reappear. **(If you were running the unit and triggered a P5 undervolt situation, you may need to cycle power to clear the trip, or try tapping the phase button a few times)**

6.3 Post Testing Burn-in **Required _X_ Yes ___ No**

✍ **Note: Burn-in should be performed (Gate A & Gate B). The fixture now has the capability to run the two sides together, 180 degrees out of phase, so the switching supply isn't overloaded (as long as you aren't sitting there holding the phase button down). Be sure to have a fan blowing across the board to adequately cool it if you run it for more than 10-15 minutes. You can run the board as long as you like, as long as you provide adequate cooling.**

6.4 TEST COMPLETE

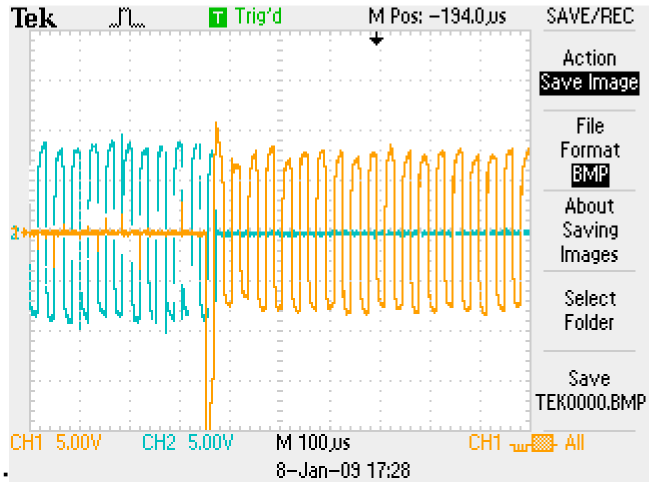
7. NOTES

7.1 Listing of ECN upgrades

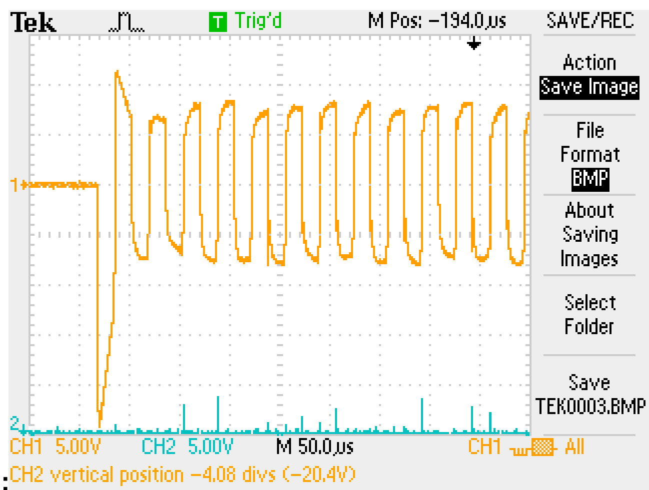
Label unit AHD once the following have been performed (see specific ECN's for details):

AEC to AFC: replace DN43 with 68A9930P3, and piggyback D400 18V transient suppressor 68A7952P2 across C418, reverse biased in relation to C418.
AFC to AGC: add jumper wire on solder side of card from pin 4 of T401 to anode of D404.
AGC to AGD: artwork incorporated from previous rev's, ignore for repair purposes.
AGD to AHD: replace T403 with 246B1459G5
AHD to AJD: changed test posts from machine insertion to manual insertion, ignore for repair purposes
AJD to AKD: changed heatsinks from epoxy to tin-plated, ignore for repair purposes

8. ATTACHMENTS

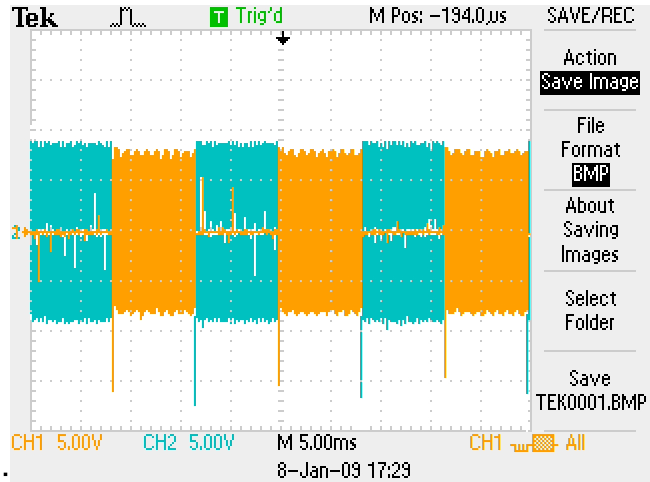


8.1 A to B transition:

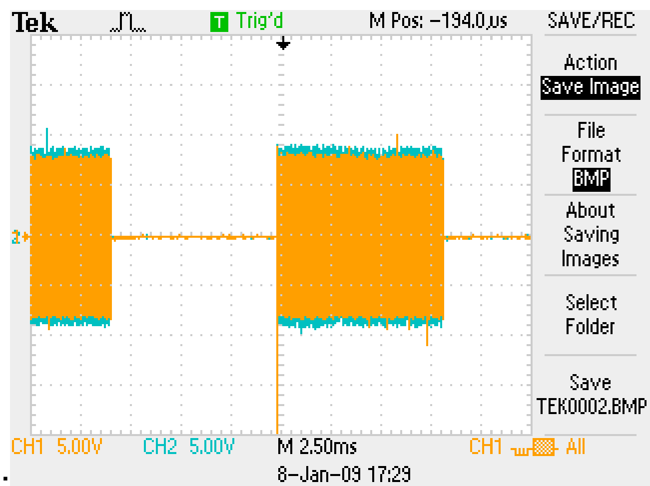


8.2 Stand Alone:

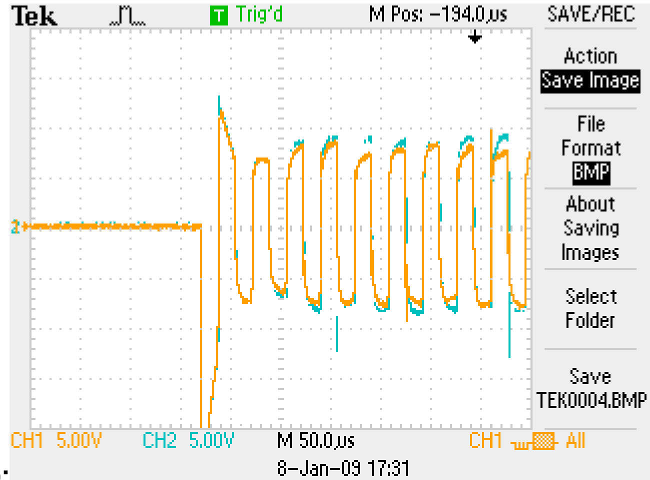
8.3 Normal 180 Phase:



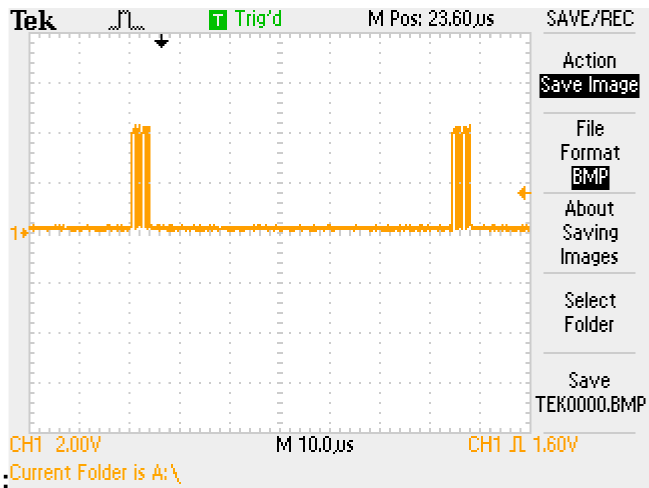
8.4 In Phase Overlap 1 (Troubleshooting only):



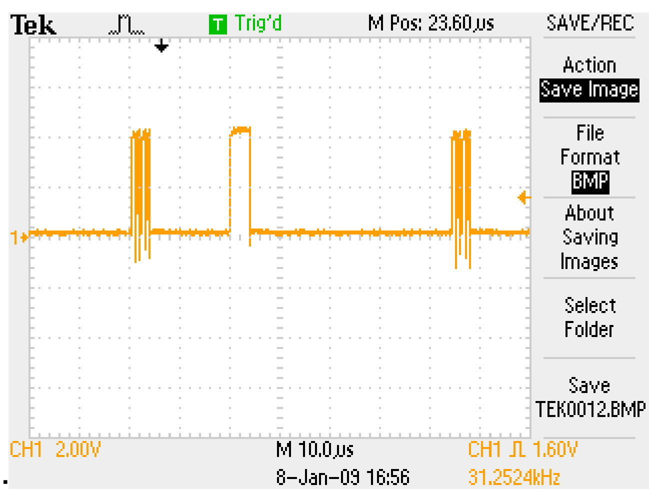
8.5 In Phase Overlap 2 (Troubleshooting Only):

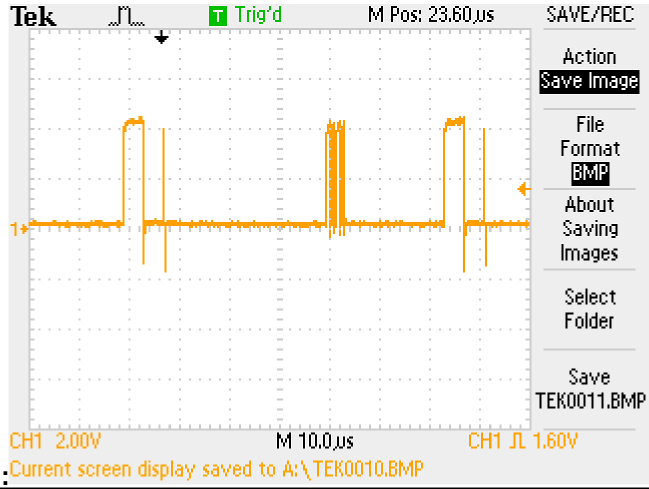


8.6 Mux Waveform Idle:

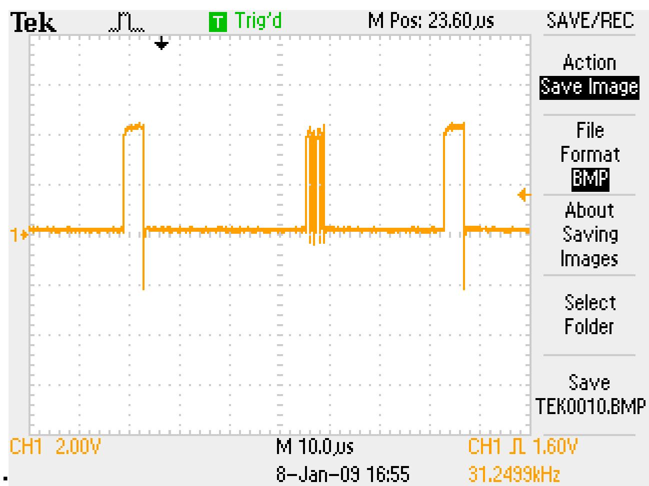


8.7 Mux CSTAT12:

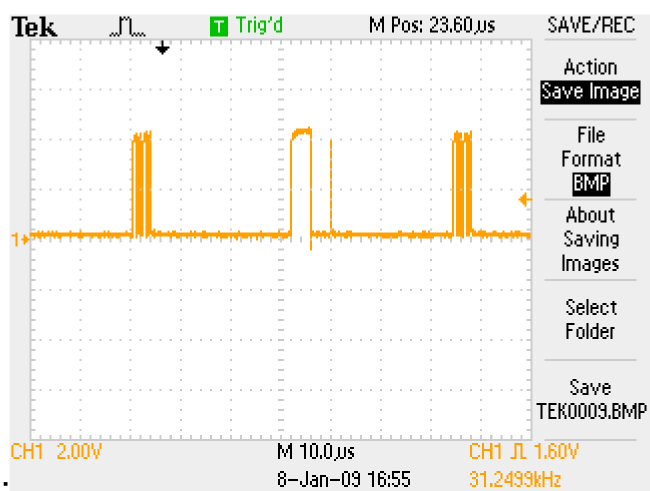




8.8 Mux CSTAT11:

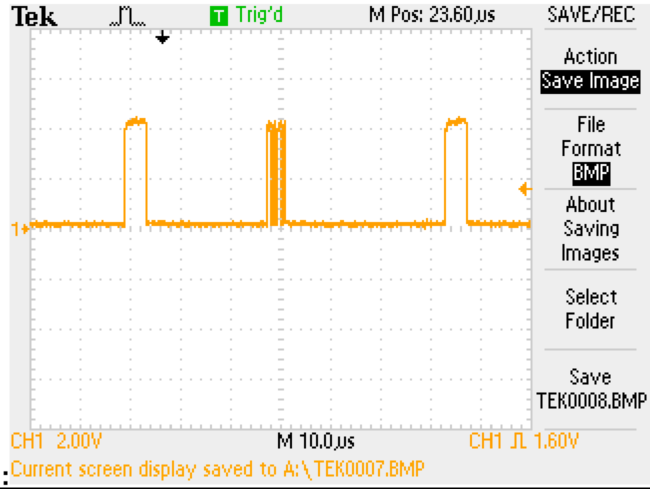


8.9 Mux CSTAT10:

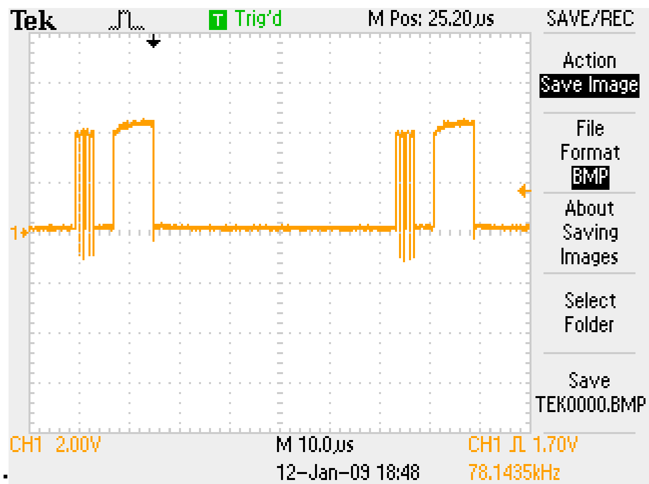


8.10 Mux CSTAT9:

8.11 **Mux CSTAT8:**



8.12 **Power Supply Undervoltage:**



Data Sheet for Test Procedure (DS200FPGA)

Test Procedure Step	Nominal	Lower Limit	Results	Upper Limit	Pass/Fail
6.2.5 P5 (TP401)	5.0VDC	4.98VDC		5.02VDC	
6.2.7 P15 (TP404)	14.0VDC	13.5VDC		14.5VDC	
6.2.7 P90 (TP405)		≥81.0VDC		-	
6.2.7 P90 (TP406)		≥25.0VDC		-	
6.2.8 PSOK (DS401)	ON	ON		ON	
6.2.9 DS101 (GATEA RX)	ON	ON		ON	
6.2.10 AGATE	25KHz	22,500Hz		27,500Hz	
6.2.11 AGATE	5KHz	4,500Hz		5,500Hz	
6.2.13 DS201 (GATEB RX)	ON	ON		ON	
6.2.14 BGATE	25KHz	22,500Hz		27,500Hz	
6.2.15 BGATE	5KHz	4,500Hz		5,500Hz	
6.2.16 AGATE & BGATE Pedestal	35V p-p	31.5V p-p		38.5V p-p	
6.2.16 AGATE & BGATE Back Porch	13V p-p	11.7V p-p		14.3V p-p	
6.2.17 Square Wave - Pos Pulse CSTAT12	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT11	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT10	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT9	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT8	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT7	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT6	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT5	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT4	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT3	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT2	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.17 Square Wave - Pos Pulse CSTAT1	4V @ 4uS	3.6V @ 4uS		4.4V @ 4uS	
6.2.18 Ch1 and Ch2	15V p-p@ 8.5mS	13.5V p-p@ 8.0mS		16.5V p-p@ 9mS	
6.2.21 TP401	4.5VDC	4.4VDC		4.6VDC	
6.2.22 PSOK (DS401)	OFF	OFF		OFF	
6.2.23 PSOK (DS401)	ON	ON		ON	