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1.0 SCOPE

The following covers the performance capabilities and test instructions for the 193X378AAG01 Regulator card. This card is designed to be a standard part of the AF-400 Inverter and performs the following functions:

1.01 Produces +10 volt midpoint power supply from +20 volt control power.

1.02 Provides a separately adjustable acceleration and deceleration linear time function of reference input.

1.03 Provides a fast linear time rate when initiated by a logic input signal.

1.04 Contains an external input to clamp or override the reference input.

1.05 Provides an adjustable motor current limit function.

1.06 Provides reference switching control as a function of external synchronization and frequency discriminator logic.

1.07 Contains minimum reference detection control.

1.08 Provides voltage regulation control including a volts/Hz adjustment.

1.09 Provides an adjustable voltage limit function.

1.10 Provides an adjustable voltage boost function.

1.11 Provides a readout voltage proportional to frequency.

1.12 Provides an output frequency proportional to the reference voltage, depending on the maximum frequency selection and adjustment, both internal and external to the card.

1.13 Provides an adjustable minimum frequency control.

1.14 Provides motor stabilization and motor slowdown control.

2.0 PERFORMANCE CAPABILITIES

All cards should be capable of the following performance while exposed to the conditions of section 4.0. In these specifications, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt, when 20 volts control power is applied to the card.

2.01 Inputs/Outputs

Tabs 6, 10, 14, 16, 17 and 20 are logic inputs. Logic sources connected to tabs 6, 10, 14 and 20 must each be capable of sinking 2 ma, and logic sources connected to tabs 16 and 17 must each be capable of sinking 4 ma, in the low state.

Tabs 15, 18 and 29 are logic outputs. Tab 15 is capable of sinking 1.5 ma, tab 18 is capable of sinking 6 ma, and tab 29 is capable of sinking 10 ma, in their low states. All three are each capable of sourcing .5 ma in their high states.

Tabs 7, 11, 12, 19, 22, 24, 26, 27, 28, 30 and 32 are analog inputs. Tabs 4 & 25 are the positive and negative rectified outputs of the current feedback inputs at tabs 26, 27 & 28.

AW (BW)
5D (BK)
5E (3BW)
5K (BW)
5QC (2BW)
5R (BW)

PRINTS TO

REVISIONS

2.01 (continued)

Tabs 8, 9, 21, 23 and 31 are analog outputs. Tabs 8, 9 and 31 are each capable of being loaded up to .5 ma and tabs 21 and 23 are each capable of being loaded up to 1 ma.

Tab 13 is a base frequency selection means and tab 5 is a frequency voltage readout, which is capable of being loaded up to 2 ma.

2.02 +10 Volt Midpoint Power Supply

Tab 3 is an on-card regulated power supply level which is within ± 1% of the midpoint voltage between the +20 volt tab 1 and the common tab 2. This power supply is of limited capacity so that no more than 2.5 ma of current can be furnished by tab 3.

This 10 volt power supply level is generated to provide a midpoint around which the regulating operational amplifiers can swing both positive and negative. Level translation is used so that the analog reference input and analog readout voltages are all relative to the common potential of tab 2, whereas most of the internal analog signals are relative to the +10 volt midpoint potential of tab 3.

2.03 Linear Timing

A reference signal of from zero to +15 volts applied to REF tab 30 will produce a voltage at TREF tab 31 of equal magnitude ± .05 volts. When the tab 30 voltage is applied as a step change, the tab 31 voltage will change on a linear ramp until it reaches the tab 30 voltage. The increasing or accelerating time is adjustable by means of the ATIM (P7) potentiometer while the decreasing or decelerating time is adjustable by means of the DTIM (P6) potentiometer. Both time ranges may be adjusted from a minimum of from 1.8 to 2.6 seconds to a maximum of from 26 to 52 seconds, for a 15 volt change.

2.04 Fast Linear Time Rate

If the OFR tab 6 is taken low, the linear timing is modified to provide a substantially faster rate of acceleration and deceleration. This rate is affected to a limited extent by the settings of the ATIM (P7) and DTIM (P6) potentiometers, being from 1.2 to 1.8 seconds for minimum pot settings and from 3.6 to 5.2 seconds for maximum pot settings.

2.05 Reference Clamp

The RFC tab 32 input may be used to override the reference input at tab 30, either by clamping the reference to zero or by inserting a higher reference voltage. If tab 32 is connected to common when tab 30 is at any voltage level, the voltage at TREF tab 31 will be 0 to .05 volts relative to common and the voltage at RFV tab 8 will be 0 ± .12 volts relative to +10V tab 3. If tab 32 is taken to the +15.0 level when tab 30 is at any voltage level, the voltage at tab 31 will be +15.0 ± .05 volts relative to common and the voltage at tab 8 will be 6.03 ± .18 volts relative to +10V tab 3.

AW(BW)
5D(BK)
5E(3BW)
5K(BW)
5QC(2BW)
5R(BW)
PRINTS TO

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2.06 Current Limit

The motor current feedback inputs at CFA tab 28, CFB tab 27 and CFC tab 26 are each connected to one terminal of a resistance loaded current transformer in each motor phase, the opposite terminals being connected to common. The current transformer loading resistors on the Current Feedback Card are selected to provide a 1.0 volt rms current feedback signal level for rated rms motor current. This card monitors the motor current feedback on a three-phase, full wave basis, comparing the rectified signal to the setting of the CLIM (P8) potentiometer. Whenever the current feedback exceeds the current limit setting of the pot, OCL tab 15 will switch from high to low. When the width of the low periods of tab 15 equals the width of the high periods, the normal reference input at tab 30 will be overridden and the internal reference voltage at RFV tab 8 will decrease toward zero.

The current limit level is adjustable by means of the CLIM (P8) potentiometer from a minimum level of 45% to 55% of rated motor current to a maximum level of 150% to 180% of rated motor current, based on a 1.0 volt rms current feedback signal for rated rms motor current.

The rate at which the RFV tab 8 is forced toward zero during current limit operation is adjusted by the CLST (P4) potentiometer, and will vary from 3.5 to 6.5 seconds for minimum pot setting to .3 to .5 seconds for a maximum pot setting, for a full tab 8 voltage excursion. This potentiometer is provided for adjusting the current limit stability based on motor and load inertia, since the slowdown rate is dependent on the loading and the inertia.

2.07 Synchronizing and Discriminator Control

The function of this control is to disconnect the normal analog reference control upon command, and to substitute another reference controlled by a digital discriminator on the System card, so that the Inverter frequency generated by this card will be synchronized to an external frequency. This control also locks the timing circuit output to the discriminator reference, so that upon the command to switch back to the analog reference, the transfer will be on the linear time ramp if the analog reference is at a different level.

The OSS tab 17 logic input goes low to start the transfer to synchronized operation, but goes low only when the inverter frequency exceeds the external frequency as determined by control on the System card. Tab 17 going low produces the following changes:

1. The REF tab 30 and TREF tab 31 are disconnected from controlling RFV tab 8.
2. An override signal is connected to the linear time circuit so that TREF tab 31 voltage is controlled by RFV tab 8.
3. A slow decelerating signal is temporarily connected to decrease the RFV tab 8 voltage and thus the inverter frequency.

AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5QC(2BW)
5R(BW)
PRINTS TO

REVISIONS

2.07 (continued)

The OIS tab 16 logic input goes low when control on the System card detects that the inverter frequency is just below the external frequency. Tab 17 going low completes the transfer to synchronized operation by producing the following changes:

1. Disconnects the temporary slowdown signal.
2. Connects the discriminator reference, as determined by 1FI tab 14 and 1FD tab 10 logic inputs from the discriminator on the System card, to control the RFV tab 8 voltage and thus the inverter frequency.
3. Disconnects the motor stability/motor slowdown control from affecting inverter frequency.

During synchronized operation, 1FI tab 14 will go high to increase inverter frequency and 1FD tab 10 will go high to decrease inverter frequency, as a function of the discriminator control on the System card.

When the command to transfer from synchronized to analog control is initiated on the System card, both OIS tab 16 and OSS tab 17 will go high, producing the following changes:

1. Disconnects the discriminator reference from controlling RFV tab 8.
2. Disconnects the TREF tab 31 from the control of RFV tab 8.
3. Connects the control of RFV tab 8 from TREF tab 31.
4. Connects the motor stability/motor slowdown control so that it can affect motor frequency.

2.08 Minimum Reference Detection

The 1MR tab 29 output indicates when the RFV tab 8 is at minimum reference by being in the high state. Tab 29 will switch from low to high state between 2.3% to 3.3% of rated reference, and will switch from high to low between 3.8% and 4.8% of rated reference. (Rated reference at REF tab 30 is 15.0 volts)

2.09 Voltage Regulator and Volts/Hertz Adjustment

The voltage regulator portion compares the converter voltage feedback signal at CVF tab 19 with the reference voltage to produce an output signal at CVR tab 21 which controls the Converter card. The reference to the voltage regulator is RFV tab 8 voltage modified by the setting of the V/Hz (P3) potentiometer. This pot provides a vernier adjustment of volts per hertz between 89% and 121% of nominal.

If an inverter fault shutdown occurs, the OFT tab 20 going low will cause the voltage regulator to go to a zero output.

AW (BW)
5D (BK)
5E (3BW)
5K (BW)
5QC (2BW)
5R (BW)
PRINTS TO

REVISIONS

2.10 Voltage Limit

The function of the voltage limit is to cause the base inverter voltage to be the same as the a.c. supply voltage for optimum transfer of the a.c. motor from inverter to a.c. line and back. The VLIM (P9) potentiometer obtains its voltage from VRL tab 24 which is fed from the Converter card and is directly proportional to the a.c. supply voltage. The VLIM pot has no limiting effect on the voltage regulator at its maximum setting, but will limit the reference to the voltage regulator to approximately 80% of rated at its minimum setting, dependent on the a.c. supply voltage level.

2.11 Voltage Boost

The VB (P5) potentiometer may be adjusted to provide zero boost at its minimum setting up to from 6.3% to 7.6% (of rated reference) boost to the voltage regulator at its maximum setting. This boost is constant over the whole operating range except for the minimum reference level, as indicated at 1MR tab 29, where the voltage boost input to the voltage regulator is switched off.

2.12 Frequency Voltage Readout

The output voltage level at FVRO tab 5 is proportional to the frequency output at OCP tab 18, and is, therefore, porportional to the inverter frequency. This proportionality is made accurate within $\pm$1% of maximum values by frequency calibration of this card in card test. The inverter frequency will be 5 times the tab 5 voltage for the lower frequency range and 10 times the tab 5 voltage for the upper frequency range. The frequency error will be within $\pm$2% of the maximum frequency; that is, within $\pm$1.5 Hz for the lower frequency range and within $\pm$ 3 Hz for the upper frequency range. The maximum current which can be drawn from Tab 5 is 3.0 milliamps, or a maximum loading of 5.0K.

2.13 Frequency Adjustment and Accuracy

The frequency output at OCP tab 18 is 6 times the inverter fundamental frequency. The tab 18 frequency is calibrated in card test by selecting the proper resistor to attach to either card posts U and V or W and X. For a 15.0 volt output of FVRO tab 5, the tab 18 frequency is calibrated to be 450 $\pm$ 4.5 pulses/second when BFR tab 13 is connected to common, and is calibrated to be 900 $\pm$9 pulses/second when tab 13 is left open.

The BFR tab 13 is used to select the two inverter base frequency ranges by connecting it either low or letting it go high. The nominal maximum inverter base frequency for the lower range is 75 Hz whereas it is 150 Hz for the upper range. Within these two ranges, the BF(P1) potentiometer is used to adjust for the desired base frequency. An external base frequency adjustment may be obtained by connecting a 5000 ohm potentiometer from BFP tab 9 to +10V tab 3, with the pot wiper connected either to BFI tab 11 to increase the base frequency

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AW(BW)
5B(8)M
5D(CD)
5E(3)BK
5R(2)BW

PRINTS TO

REVISIONS

2.13 (continued)

over the internal setting, or connected to BFD tab 12 to decrease the base frequency under the internal setting.

The effect of the base frequency selections and adjustments on the frequency obtained from a set reference input is given by the following formulae:

$f_I = K1 \times K2 \times REF$ $\qquad f_o = 6\ f_I$

where f_I = inverter fundamental frequency in hertz
f_o = OCP tab 18 frequency in pulses/sec.
REF = tab 30 input voltage which can vary from 0 to 15 volts
K1 = 5 for BFR tab 13 connected to common
= 10 for BFR tab 13 not connected
K2 = .38 to .50 for minimum BF (P1) pot setting
= 1.01 to 1.21 for maximum BF (P1) pot setting
= .5 to 1.0 minimum range adjustment of BF (P1) pot

When an external 5000 ohm base frequency potentiometer is used with its wiper connected to BFI tab 11, the above formula is modified as follows:

$f_I = K1 \times (K2 + K3) \times REF$

where K3 = 0 for minimum external base frequency pot setting
= .50 to .62 for max. external base frequency pot setting
= 0 to .5 min. range adjustment of the external base freq.pot

When the external 5000 ohm base frequency potentiometer has its wiper connected to BFD tab 12, the formula becomes:

$fI = K1 \times (K2 - K4) \times REF$

where K4 = 0 for min. external base frequency pot setting
= .53 to .65 for max. external base frequency pot setting
= 0 to .5 min. range adjustment of the external base freq.pot

The following temperature drift and linearity specifications apply to this card when used in the AF-400 Driver, using the 193X380AAG01 (20 volt) Power Supply card and with the reference at tab 30 coming from a 10 turn, 5000 ohm potentiometer 104X138BF001 connected to the Driver in the prescribed manner.

Temperature drift of frequency (10° to 70°C):
.75% per 15°C change, based on frequency at 15 volt reference
2.5% for full 10° to 70°C change

Humidity (90% RH for 24 hours at 50°C)
.25% based on frequency at 15 volts reference

Linearity of Frequency (to Reference)
.15% based on 15 volt reference

Long term drift of frequency
.05% based on frequency at 15 volts reference

AW(BW)
5D(BK)
5E(3BW)
5K(BW)
5QC(2BW)
5R(BW)
PRINTS TO

REVISIONS

2.14 Minimum Frequency

The MINF (P2) potentiometer adjusts the minimum frequency of OCP tab 18, and thus the inverter frequency, as a percentage of base frequency. The minimum frequency may be adjusted from 3% ±.4% of the set base frequency at the minimum setting of MINF pot, up to 12% ±1% of the set base frequency at the maximum setting of MINF pot.

The MINF (P2) pot acts only to limit the minimum frequency of OCP tab 18, and has no effect on frequency above the minimum frequency level.

2.15 Motor Stability/Motor Slowdown Control

The function of this control is threefold as follows:

1. To provide stabilizing for motors at their underdamped operating points.
2. To override the reference control, when it calls for faster than motor coast slowdown, to keep the volts/hertz applied to the motor within limits.
3. To provide system stabilizing during slowdown and current limit operation.

This control accomplishes the above by comparing the d.c. link voltage feedback signal at LVF tab 22 with the voltage regulator reference voltage. If there is any discrepancy between these two voltages, either transiently or steady state, a correcting signal will appear at SSDO tab 23. If this tab is connected to SSDI tab 7, this correcting signal will modify the output frequency at OCP tab 18 in order to keep the volts/hertz within limits.

This control is switched off, when OIS tab 16 goes low, so that it cannot affect frequency during synchronized operation. If this control is not desired during normal operation, SSDI tab 7 should be disconnected from SSDO tab 23.

2.16 Fault Shutdown

If an inverter fault shutdown occurs, the OFT tab 20 going low will cause the voltage regulator output at CVR tab 21 to go to zero (relative to tab 3).

2.17 Power Supply Requirements

The 20 volt power supply requirements for this card are 65 ma ±15%.

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AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5QC(2BW)
5R(BW)
PRINTS TO

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3.0 TEST INSTRUCTIONS

In these instructions, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt, when 20 volts control power is applied to the card. Connect BFR tab 13 to common to select the frequency range. Connect VRL tab 24 to a d.c. voltage source which is set to be +5.0 volts relative to tab 3 (+10V). Connect REF tab 30 to a d.c. voltage source which can be adjusted to provide a 0 to 15 volt reference input.

3.01 +10 Volt Midpoint Power Supply

The tab 3 to tab 2 voltage should be +10.0 volts ±.1 voltage when +20.0 volts is applied between tab 1 and tab 2. The tab 3 voltage should be 10 volts ± .2 volts for a 20 volts ± .2 volts power supply.

3.02 Linear Timing

Turn the ATIM (P7) and DTIM (P6) pots fully counter-clockwise. Switch the REF tab 30 voltage from 0 to +15 volts. The TREF tab 31 should change from 0 to +15 volts on a linear ramp in from 1.8 to 2.6 seconds. Switch the tab 30 voltage back to zero volts and tab 31 should change from +15 to zero volts on a linear ramp in from 1.8 to 2.6 seconds.

Turn the ATIM and DTIM pots fully clockwise. Switch the REF tab 30 voltage from zero to +15 volts, and then back to zero as before. The TREF tab 31 voltage should change from 0 to +15 volts, and then back to zero, both the increase and decrease being linear ramps which should be 26 to 52 seconds each.

3.03 Fast Linear Time Rate

Connect OFR tab 6 to common. Repeat the linear time tests of section 3.02. The increasing and decreasing voltage ramps at tab 31 should measure 1.2 to 1.8 seconds for fully counter-clockwise ATIM and DTIM pot settings, and should measure 3.6 to 5.2 seconds for fully clockwise pot settings.

Disconnect tab 6 from common and set the tab 30 input voltage at zero. Remove +20 volt card power for 1 second and then reapply. The tab 31 voltage should be below 0.8 volt in less than 0.2 seconds after card power is applied.

Turn the ATIM and DTIM pots back to the fully counter-clockwise settings.

3.04 Reference Clamp

Set the voltage at REF tab 30 to be +15.0 volts. The output at TREF tab 31 should be +15.0 ±0.5 volts (relative to common) and the output at RFV tab 8 should be +6.03 volts ±.18 volts (relative to the tab 3 voltage). Connect RFC tab 32 to common. The tab 31 voltage should change to 0 to .05 volts, and the tab 8 voltage should change to 0 ± .12 volts (relative to tab 3). Disconnect tab 32 from common and the tabs 31 and 8 voltages should return to the original levels.

AW (BW)
5D (BK)
5E (3BK)
5K (BW)
5QC (2BW)
5R (BW)
PRINTS TO

REVISIONS

3.05 Current Limit

Turn the CLIM (P8) pot fully counter-clockwise, and turn the CLST (P4) pot fully clockwise. Connect CFA tab 28 to a 0 to +10 volt adjustable d.c. voltage source and connect CFB tab 27 to common. Set the voltage at REF tab 30 to be +15 volts so that the RFV tab 8 output is +6.03 volts ± .18 volts (relative to tab 3).

Increase the tab 28 voltage from zero while monitoring RFV tab 8 and OCL tab 15. At the point when tab 15 switches from high to low, the tab 28 voltage should be between 1.0 to 1.5 volts. The tab 8 voltage should then begin decreasing, reaching zero volts (relative to tab 3) in .3 to .5 seconds after tab 15 switches permanently to low. Decrease the tab 28 voltage to zero. Tab 15 should switch back to high before the tab 28 voltage goes below 1.0 volt, and the tab 8 voltage should then increase back up to the original 6.03 volts ± .18 volts in .3 to .5 seconds from the 0 ± .15 volt level (relative to tab 3). (Tab 8 will clamp at approx. -.6 volt when tab 15 is low.)

Turn the CLIM (P8) pot fully clockwise, turn the CLST (P4) pot fully counter-clockwise, and repeat the above test. The results should be the same except that the tab 28 voltage should have to be increased to from 3.55 to 4.15 volts before tab 15 switches low. In addition, the time for the tab 8 voltage to change 6 volts should now be 3.5 to 6.5 seconds in either direction.

The results should be the same when using the other two combinations of tabs 26, 27 and 28 for signal input.

3.06 Synchronizing and Discriminator Control

Connect 1FI tab 14 and 1FD tab 10 to common. Set the REF tab 30 input voltage at +15.0 volts so that the TREF tab 31 voltage is 15.0 volts and the RFV tab 8 voltage is 6.03 ± .18 volts (relative to tab 3).

Connect OSS tab 17 to common. The tab 8 to tab 3 voltage and the tab 31 to common voltage should both decrease, both reaching their zero levels in from 25 to 50 seconds.

Disconnect tab 17 from common and both tab 8 and tab 31 voltages should return to their original levels.

Disconnect 1FD tab 10 from common, keeping 1FI tab 14 connected to common. Connect tab 16 to tab 17 and then connect them both to common. Both RFV tab 8 (to tab 3) voltage and TREF tab 31 (to common) voltage should decrease to zero in from 0.4 to 0.7 seconds, with the tab 8 voltage exhibiting an initial 1.7 to 1.8 volt downward step (which the tab 31 voltage catches up with). Disconnect tabs 16 and 17 from common. The tab 8 and tab 31 voltages should return to their original levels.

Connect 1FD tab 10 to common and disconnect 1FI tab 14 from common. Set the REF tab 30 input voltage to zero so that the TREF tab 31 is at common and the RFV tab 8 is at the tab 3 (+10V) level. Connect tab 16 to tab 17 and connect them both to common. Both the tab 8 and tab 31 voltages should increase till they saturate, tab 8 reaching

AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5QC(2BW)
5R(BW)
PRINTS TO

3.06 (Continued)

6 Volts (relative to tab 3) and tab 31 reaching 15 volts, in from 0.4 to 0.7 seconds, with the tab 8 voltage exhibiting an initial 1.7 to 1.8 volt upward step. Disconnect tabs 16 and 17 from common. The tab 8 and tab 31 voltages should return to their original levels.

3.07 Minimum Reference Detection

Increase the REF tab 30 voltage from zero while monitoring RFV tab 8 and 1MR tab 29. Tab 29 should switch from high to low when the tab 8 voltage increases to +0.25 ± .03 volts (relative to tab 3). Now decrease the tab 30 voltage to zero. Tab 29 should switch from low to high when the tab 8 voltage decreases to +0.18 ± .03 volts (relative to tab 3).

3.08 Voltage Regulator

Connect CVF tab 19 to CVR tab 21, turn the VB (P5) pot fully counter-clockwise, and turn both the V/Hz (P3) and VLIM (P9) pots fully clockwise. Set the REF tab 30 input voltage at +15.0 volts. The CVR tab 21 to +10V tab 3 voltage should be -5.35 ± .2 volts. Turn the V/Hz pot fully counter-clockwise. The tab 21 voltage should change to -4.0 ± .25 volts (relative to tab 3).

3.09 Voltage Limit

Turn the V/Hz (P3) pot fully clockwise. With the VLIM (P9) pot fully clockwise and the REF tab 30 at +15.0 volts, the CVR tab 21 should be -5.35 ± .2 volts relative to tab 3. Turn the VLIM pot fully counter-clockwise. The tab 21 voltage should change to -3.9 ± .2 volts (relative to tab 3). Now reduce the VRL tab 24 voltage to +10V. The tab 21 voltage should reduce only slightly and should not become less than -3.4 volts relative to tab 3. Return the tab 24 voltage to +5.0 volts relative to tab 3. Return the VLIM pot to the fully clockwise setting.

G03 only: With VRL = +10V the tab 21 voltage will be -1.25 ± .2 volts relative to tab 3.

3.10 Voltage Boost

With the V/Hz (P3) pot fully clockwise and the REF tab 30 input voltage at zero, turn the VB (P5) pot fully clockwise. CVR tab 21 should remain at 0 ± .15 volts (relative to +10V tab 3). Slowly increase the tab 30 input voltage while monitoring tabs 21 and 29. When the 1MR tab 29 switches from high to low, the tab 21 voltage should make a -0.31 ± .02 volt step change from -0.25 ± .05 volts (relative to tab 3). Now turn the VB pot fully counter-clockwise. The tab 21 voltage should change back to the unboosted level of -0.25 ± .05 volts.

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AW(BW)
5B(8)M
5D(CD)
5E(A&S)
5P(1)BM
5R(2)BM
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3.11 Frequency Voltage Readout

Turn the BF (P1) pot fully clockwise and set the REF tab 30 input voltage at +15.0 volts. The FVRO tab 5 voltage should be between +15.1 and +18.1 volts. Adjust the BF pot to obtain 15.0 volts output at tab 5.

3.12 Frequency Calibration and Adjustment

With both the REF tab 30 and the FVRO tab 5 at +15.0 volts, and BFR tab 13 connected to common, the output frequency at OCP tab 18 should be 450 ± 80 pulses per second. Disconnect tab 13 from common and the tab 18 frequency should double to 900 ± 160 pulses per second. Trim the frequency at tab 18 to be 450 ± 4.5 pulses/sec. with tab 13 connected to common and 900 ± 9 pulses/sec. with tab 13 disconnected. If the untrimmed frequency is too low, select a 1%, 100 PPM resistor, from 1 megohm down to 33.2 K ohm, and solder between posts W and X (R62), to achieve the desired frequency tolerance. If the untrimmed frequency is too high, select a 1%, 100 PPM resistor, from 1 megohm down to 100K ohm, and solder between posts U and V (R61), to achieve the desired frequency tolerance.

Adjust the BF (P1) pot to obtain a frequency of exactly 450 pulses/sec. at OCP tab 18, with tab 13 connected to common, for a 15.0 volt input at REF tab 30. Reduce the tab 30 voltage to 3.0 volts. The tab 18 frequency should be 90 ± 2.7 pulses/sec. Now adjust the BF (P1) pot to set the tab 18 frequency at exactly 90 pulses/sec. The FVRO tab 5 voltage should be 3.0 ± .15 volts.

Increase the REF tab 30 to 15.0 volts and turn the BF (P1) pot fully counter-clockwise. The OCP tab 18 frequency should be 170 to 225 pulses/sec.

Adjust the BF (P1) pot to obtain a frequency of 225 pulses/sec. at OCP tab 18. Connect a 5000 ohm, 1% resistor between BFP tab 9 and tab 3 (+10V) and connect BFI tab 11 to tab 9. The tab 18 frequency should increase to 450 to 505 pulses/sec. Disconnect tab 11 from tab 9 and adjust the BF pot to obtain a frequency of 450 pulses/sec. at tab 18. Now connect BFD tab 12 to tab 9. The tab 18 frequency should decrease to 155 to 215 pulses/sec. Disconnect tab 12 from tab 9. The tab 18 frequency should return to 450 pulses/sec. and the FVRO tab 5 voltage should be 15.0 ± .15 volts.

The pulse width of the OCP tab 18 pulses should be 33 ± 3 μsec.

3.13 Minimum Frequency

With the REF tab 30 at 15.0 volts and the OCP tab 18 output frequency set at 450 pulses/sec., adjust the MINF (P2) pot over its whole range. There should be no effect on tab 18 frequency.

AW(BW)
5D(BK)
5E(3BW)
5K(BW)
5QC(2BW
5R(BW)
PRINTS TO

REVISIONS

3.13 (continued)

Reduce the REF tab 30 voltage to zero, and turn the MINF pot fully counter-clockwise. The tab 18 output frequency should be between 11.7 and 15.3 pulses/sec. and the tab 5 voltage should be .35 to .55 volts. Now turn the MINF pot fully clockwise. The tab 18 frequency should change to 50 to 60 pulses/sec. and the tab 5 voltage should change to 1.6 to 2.0 volts. Slowly increase the tab 30 voltage. The tab 5 voltage should remain the same or increase only slightly until both tab 5 and tab 30 voltages reach about 2 volts, above which they should both increase at the same rate.

3.14 Motor Stability/Slowdown Control

Set the tab 30 voltage to obtain a RFV tab 8 to tab 3 voltage of +3.0 volts and adjust the BF (P1) pot to obtain +7.5 volts from FVRO tab 5 to common. With the V/Hz (P3) pot set fully clockwise, connect SSDO tab 23 to SSDI tab 7.* The tab 5 voltage should decrease to +1.7 ±.5 volts. Now connect an adjustable voltage to LVF tab 22 and set the tab 22 to tab 3 voltage to -2.70 volts. The tab 5 voltage should return to +7.5 ± .15 volts. Increase the tab 22 to tab 3 voltage to -5.00 volts. The tab 5 voltage should increase to +15.0 ± .6 volts. Now connect OIS tab 16 to common. The tab 5 voltage should return to +7.5 volts to common. (* With VB (P5) pot fully counterclockwise)

3.15 Fault Shutdown

Set the tab 30 voltage to obtain a CVR tab 21 to tab 3 voltage of about -5 volts. Connect OFT tab 20 to common. The tab 21 to tab 3 voltage should change to +.6 volts. Disconnect tab 20 from common and reconnect to +20 volts. The tab 21 voltage should return to its original level.

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AW(BW)
5D(BK)
5E(3BK)
5K(BW)
5QC(2BW)
5R(BW)
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1 | Chg 3.16 P5 & P9 5/17/77 ejk

3.16 Potentiometer Settings

The final settings of the card mounted potentiometers should be as follows:

P1	-	BF	:	Set at midpoint
P2	-	MINF	:	Set fully CCW
P3	-	V/Hz	:	Set at midpoint
P4	-	CLST	:	Set 1/4 of turn from CCW end
P5	-	VB	:	Set fully CCW
P6	-	DTIM	:	Set 1/3 of turn from CW end
P7	-	ATIM	:	Set 1/3 of turn from CW end
P8	-	CLIM	:	Set 1/3 of turn from CW end
P9	-	VLIM	:	Set at midpoint

4.0 OPERATING & TEST CONDITIONS

This card should be capable of operating within the performance specified in Section 2.0 and pass all tests specified in Section 3.0 while exposed to the following conditions:

4.01 DC Supply Voltage - +19.8 to +20.2 volts from tab 1 to tab 2.

4.02 Ambient Temperature - 0 to +75°C.

4.03 Humidity - 24 hrs. in 90% relative humidity at 40°C.

4.04 Voltage to Ground - 600 volts

AW (BW)
5D (BK)
5E (3BK)
5K (BW)
5QC (2BW)
5R (BW)
PRINTS TO