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TITLE
CIRCUIT BOARD TEST INSTRUCTIONS FOR
TRACKING VC   148D2649G2   1M3, 1T3

FIRST MADE FOR   EHC MARK II

1M3, 1T3

REVISIONS

15580

A. Power Supplies

   1. $14.7 < V_{TP1} < 16.7$

   2. $-16.7 < V_{TP2} < -14.7$

B. Input Differential Amplifier (IC1)

   1. Ground TP13 and TP14 and Null IC1.

   2. SS Gain

$$-5.05 < V_{TP50}/(V_{TP14} - V_{TP13}) < -4.95 \quad (V_{TP14} > V_{TP13})$$
$$4.95 < V_{TP50}/(V_{TP14} - V_{TP13}) < 5.05 \quad (V_{TP13} \quad V_{TP14})$$

$$|V_{TP14} - V_{TP13}| < 0.6$$

$$V_{TP50}/(V_{TP14} - V_{TP13}) = 0$$
$$3.5 < |V_{TP50_{MAX}}| < 4.0$$
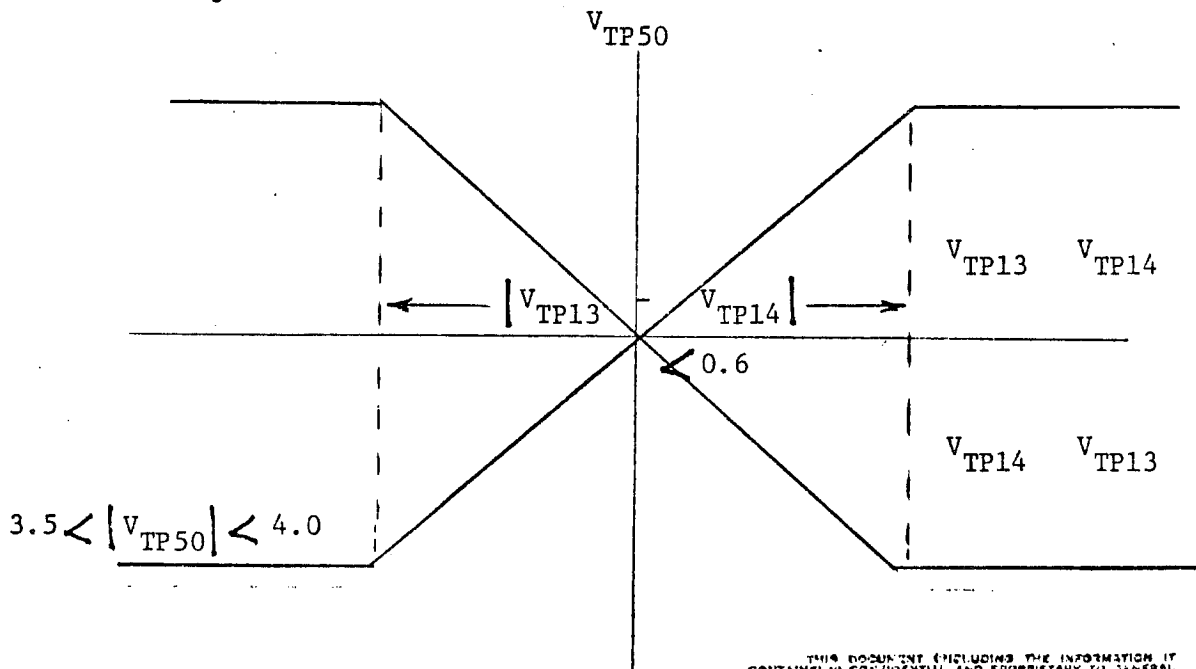
$$|V_{TP14} - V_{TP13}| > 0.7$$

See Figure 1.

FIGURE 1: SS Gain – IC1

273-2
273-12²
273-71
273-138
273-221
273-227

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B. Input Differential Amplifier IC1 (continued)

   3. Dynamic Gain

$$-2.13 < V_{TP50}/V_{TP14} < -1.48 \quad (V_{TP13} = 0,\ V_{TP14} = 1 \ @ \ f = 5 \text{ KHz})$$

$$1.48 < V_{TP50}/V_{TP13} < 2.13 \quad (V_{TP14} = 0,\ V_{TP13} = 1 \ @ \ f = 5 \text{ KHz})$$

C. Input Differential Amplifier (IC3)

   1. Ground TP15 and TP16 and Null IC3.

   2. SS Gain

$$\left.\begin{array}{l} -5.05 < V_{TP51}/(V_{TP16} - V_{TP15}) < -4.95 \quad (V_{TP16} > V_{TP15}) \\[2mm] 4.95 < V_{TP51}/(V_{TP16} - V_{TP15}) < 5.05 \quad (V_{TP15} > V_{TP16}) \end{array}\right\} \quad \begin{array}{l} |V_{TP16} - V_{TP15}| \\ < 0.6 \end{array}$$

$$\left.\begin{array}{l} V_{TP51}/(V_{TP16} - V_{TP15}) = 0 \\[2mm] 3.5 < |V_{TP51_{MAX}}| < 4.0 \end{array}\right\} \quad |V_{TP16} - V_{TP15}| > 0.7$$

   3. Dynamic Gain

$$-2.13 < V_{TP51}/V_{TP16} < -1.48 \quad (V_{TP15} = 0,\ V_{TP16} = 1 \ @ \ f = 5 \text{ KHz})$$

$$1.48 < V_{TP51}/V_{TP15} < 2.13 \quad (V_{TP16} = 0,\ V_{TP15} = 1 \ @ \ f = 5 \text{ KHz})$$

D. Input Differential Amp (IC5)

   1. Ground TP17 and TP18 and Null IC5.

   2. SS Gain

$$\left.\begin{array}{l} -5.05 < V_{TP52}/(V_{TP18} - V_{TP17}) < -4.95 \quad (V_{TP18} > V_{TP17}) \\[2mm] 4.95 < V_{TP52}/(V_{TP18} - V_{TP17}) < 5.05 \quad (V_{TP17} > V_{TP18}) \end{array}\right\} \quad \begin{array}{l} |V_{TP18} - V_{TP17}| \\ < 0.6 \end{array}$$

$$\left.\begin{array}{l} V_{TP52}/(V_{TP18} - V_{TP17}) = 0 \\[2mm] 3.5 < |V_{TP52_{MAX}}| < 4.0 \end{array}\right\} \quad |V_{TP18} - V_{TP17}| > 0.7$$

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D. Input Differential Amplifier IC5 (continued)

3. Dynamic Gain

$$-2.13 < V_{TP52}/V_{TP18} < -1.48 \quad (V_{TP17} = 0, \; V_{TP18} = 1 \; @ \; f = 5 \; KHz)$$

$$1.48 < V_{TP52}/V_{TP17} < 2.13 \quad (V_{TP18} = 0, \; V_{TP17} = 1 \; @ \; f = 5 \; KHz)$$

E. VC1 (IC2)

1. Voltage Range

$$1.45 < V_{TP3} < 2.02 \quad (VR1 \; CCW)$$

$$7.3 < V_{TP3} < 8* \quad (VR1 \; CW)$$

$$-2.02 < V_{TP4} < -1.45 \quad (VR2 \; CCW)$$

$$-8 < V_{TP4} < -7.3* \quad (VR2 \; CW)$$

2. Adjustments

a) Positive

1) Adjust VR1 → V_{TP3} = 3.0   *1.0*

2) Apply V_{TP50} = 2.500   *.833 V.*

3) Adjust VR1 → K1 (and DS1) just energize

4) Reduce V_{TP50} → K1 (and DS1) just de-energize

Record V_{TP50} = _____ (D.O.)   *.820 V.*

* Design Note: To conform to the 711 spec that the differential
   input voltage be < 5V, R8, 11, 24, 27, 40, 43 = 10K should be
   changed to 2K which will give:

$$0.355 < V_{TP3}, \; etc < 0.437 \quad (VR1, \; etc. \; CCW)$$

$$3.60 < V_{TP3}, \; etc < 3.74 \quad (VR1, \; etc. \; CW)$$

1K - G1
10K - G2
→ to 2K ?

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E. VC1 (IC2) (continued)

   2. Adjustments (continued)

      b) Negative

         1) Adjust VR2 ⟶ V_{TP4} = -3.0   -1.0

         2) Apply V_{TP50} = -2.500   -.833

         3) Adjust VR2 ⟶ K1 (and DS1) just energize

         4) Reduce V_{TP50} ⟶ K1 (and DS1) just de-energize

            Record V_{TP50} = _____ (D.O.)   -.890

   3. Hysteresis

$$\text{Hyst} = \left| V_{TP50_{PU}} - V_{TP50_{DO}} \right| < 0.3$$
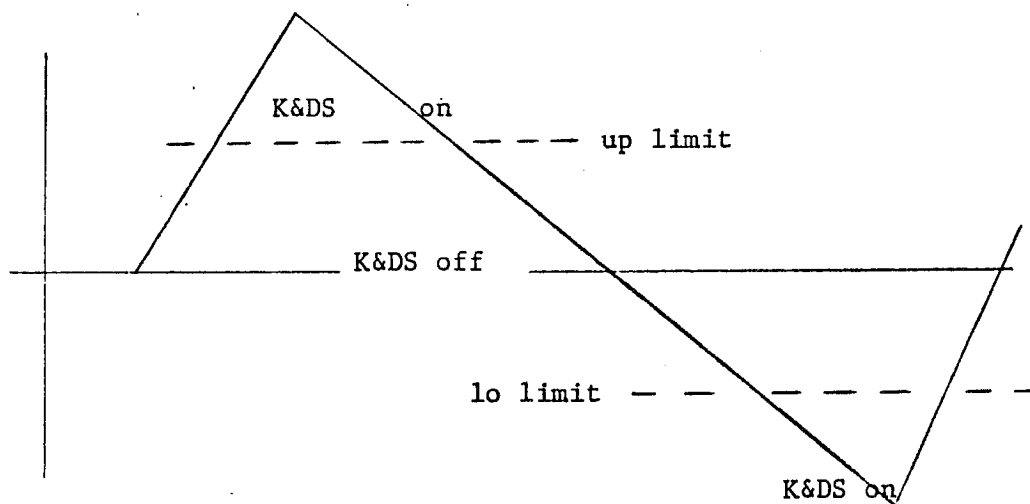
      .890
      .822
      ―――――
      .068

      for a) and b) above.

   4. Logic

      See Figure 2.

FIGURE 2: VC Logic

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F. VC2 (IC4)

1. Voltage Range

$1.45 < V_{TP6} < 2.02$ (VR3 CCW)

$7.3 < V_{TP6} < 8*$ (VR3 CW)

$-2.02 < V_{TP7} < -1.45$ (VR4 CCW)

$-8 < V_{TP4} < -7.3*$ (VR4 CW)

2. Adjustments

a) Positive

1) Adjust VR3 ⟶ $V_{TP6} = 3.0$

2) Apply $V_{TP51} = 2.500$

3) Adjust VR3 ⟶ K2 (and DS2) just energize

4) Reduce V_{TP51} ⟶ K2 (and DS2) just de-energize

Record $V_{TP51} = $ _____ (D.O.)

b) Negative

1) Adjust VR4 ⟶ $V_{TP7} = -3.0$

2) Apply $V_{TP51} = -2.500$

3) Adjust VR4 ⟶ K2 (and DS2) just energize

4) Reduce V_{TP51} ⟶ K2 (and DS2) just de-energize

Record $V_{TP51} = $ _____ (D.O.)

3. Hysteresis

$Hyst = \left| V_{TP51_{PU}} - V_{TP51_{DO}} \right| < 0.3$

for a) and b) above.

4. Logic

See Figure 2.

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G. VC3 (IC6)

1. Voltage Range

$$1.45 < V_{TP9} < 2.02 \qquad \text{(VR5 CCW)}$$

$$7.3 < V_{TP9} < 8* \qquad \text{(VR5 CW)}$$

$$-2.02 < V_{TP10} < -1.45 \qquad \text{(VR6 CCW)}$$

$$-8 < V_{TP10} < -7.3* \qquad \text{(VR6 CW)}$$

2. Adjustments

a) Positive

1) Adjust VR5 → V_{TP9} = 3.0

2) Apply V_{TP52} = 2.500

3) Adjust VR5 → K3 (and DS3) just energize

4) Reduce V_{TP52} → K3 (and DS3) just de-energize

Record V_{TP52} = _____ (D.O.)

b) Negative

1) Adjust VR6 → V_{TP10} = -3.0

2) Apply V_{TP52} = -2.500

3) Adjust VR6 → K3 (and DS3) just energize

4) Reduce V_{TP52} → K3 (and DS3) just de-energize

Record V_{TP52} = _____ (D.O.)

3. Hysteresis

$$\text{Hyst} = \left| V_{TP52_{PU}} - V_{TP52_{DO}} \right| < 0.3$$

for a) and b) above.

4. Logic

See Figure 2.

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CIRCUIT BOARD TEST INSTRUCTIONS FOR
TRACKING VC   148D2649G2   1M3, 1T3

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REVISION

PREPARED BY: _____   DATE 6/30/83

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APPROVED BY: _____   DATE 7-1-83

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