

REV NO. ( )

TITLE

CONT ON SHEET 2 SH NO. 1

P3K-AL-0380-A01

CONT ON SHEET 2 SH NO. 1

TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING ~~118D1574 G1, 118D1337 G1~~  
FIRST MADE FOR EHC MARK II

I. CIRCUIT DESCRIPTION

1TM2-A001 CIRCUIT BOARD REVISION #1  
1TM2-A002 CIRCUIT BOARD REVISION #0

This board contains the 125 volt trip system and the 24 volt trip system. The 125 volt trip system energizes the Master Trip Solenoid (MSTV) under abnormal conditions and causes the Emergency Trip System to trip the turbine. The 24 volt trip system de-energizes both Electrical Trip Solenoid Valves (ETSV) under abnormal conditions and causes the ETS to trip the turbine.

A 125 volt trip will be locked-up and cause 24 volt trip and a 24 volt trip (unless caused by Trip Anticipator action) will be locked-up and cause 125 volt trip.

Thus two lines of defense are provided at this level.

A loss of the 24V power on this board causes 24V trip and 125V trip. Loss of the 125V power causes 24V trip when speed is below 75% of rated.

Many functions on the board are performed by three relays with two out of three logic arrangement of contacts. This decreases considerably both the probability of erroneous trip command and the probability of inaction during a trip condition.

118D1374

|        |      |
|--------|------|
| ACTIVE | FOR  |
| BY     | DATE |

REVISIONS

273-2  
273-12  
273-71  
273-136  
273-221  
273-221

PRINTS TO

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|                 |                 |
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|       |  |
|-------|--|
| TITLE | TEST INSTRUCTIONS FOR 125 VOLT/<br>24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002<br>ASS'Y DRAWING 118D1574-01, 118D1337-01<br>FIRST MADE FOR EHC MARK II |
|-------|--|

1374

REVISIONS

## II. CIRCUIT SPECIFICATIONS

### 1. DIODE REDUNDANCY

Before the board is coated each diode should be checked in the reverse direction to insure redundancy is effective.

### 2. PERMANENT CONTINUITY

Each terminal in the following groups of terminals must show permanent continuity with all other terminals of the same group (Resistance less than 0.1 Ohms):

- a. 1, 3, 6, 9, 14, 51, 54, 57, 67, 111, 114, 20, 27, 87, 40, 42, 46, 163, 171, 172, 175
- b. 2, 157
- c. ~~107~~, 152, 179, ~~188~~
- d. ~~107~~, 150 HPE 12/2/86
- e. 34, 36
- f. 4, 5
- g. 7, 8
- h. 12, 13
- i. 15, 16
- j. 52, 53, 55, 56
- k. 60, 61
- l. 62, 63
- m. 64, 70, 71, 72
- n. 17, 18
- o. 23, 24, 30
- p. 98, 99
- q. 100, 101
- r. 94, 95
- s. 92, 93

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CODE 10001 100

REV NO. 0  
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TITLE  
TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1574 G1, 118D1337 G1  
FIRST MADE FOR EHC MARK II

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II. CIRCUIT SPECIFICATIONS (continued)

2. PERMANENT CONTINUITY (continued)

- t. 164, 165
- u. 153, 154
- v. 166, 167, 168
- w. 107, 106
- x. 105, 104
- y. 148, 149, 151
- ~~z. 191, 192~~ omit JDC
- aa. 182, 183
- bb. 181, 180
- cc. 184, 185

3. FUSED CONTINUITY

The following fuses are rated 1/8A and establish conductive paths between the two corresponding terminals, which otherwise are isolated from each other.

- a. F1: 160-108
- b. F4: 1-103
- c. F5: 1-102
- d. F6: 90-100
- e. F7: 89-98
- f. F8: 88-97
- g. F9: 84-96
- h. F10: 83-94
- i. F11: 85-92
- j. F12: 1-91

(Fuses F2 and F3 are rated 1/8A and are not observable from terminal points - their continuity is checked in subsequent steps).

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CONT ON SHEET 4 SH NO. 3

CODE IDENT

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CONT ON SHEET 5 SH NO. 4

TITLE TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1374 G1, ~~118D1337 G1~~  
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## II. CIRCUIT SPECIFICATIONS (continued)

### 4. LOGIC

To check the logic the following connections should be made:

Terminal 1: 125 VDC

2: 125 VDC common

73: 24 VDC

74: 24 VDC common

33: 115 VAC

34: 115 VAC common

158: 1.74K Ohms  $\pm 1\%$ , 9W load (other end of load to terminal 157)

149: 17.5 Ohms  $\pm 1\%$ , 33W load (other end of load to terminal 150)

151: 17.5 Ohms  $\pm 1\%$ , 33W load (other end of load to terminal 150)

After power supply connections are made the circuit should be RESET by momentarily applying 125 VDC to terminal 159. In subsequent discussion the term RESET as defined here will be used freely. All voltages are DC unless otherwise specified. In each section some of the logic outputs responses to inputs are omitted if specified in previous or subsequent sections.

#### 4.1 Non-Latching 125V Trip

With 125 VDC connected to terminal 159 (after the circuit is RESET) the following voltages should exist:

MASTER  
24VDC P53

Terminal 158: 125 V

TP18: 0V

TP19: 0V

Upon removal of this voltage from terminal 159 all three points should have 0 VDC.

#### 4.2 Typical Latching 125V Trip

This can be caused by applying 125 VDC to terminal 164; the conditions that should exist prior to and after the trip are shown in the following table:

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SH NO. 4

CODE 10741 M

## II. CIRCUIT SPECIFICATIONS (continued)

### REVISIONS

### 4.2 Typical Latching 125V Trip (continued)

TABLE I

| INPUTS AT    |                         | CORRECT OUTPUTS AT                |                            |                     |                            |              | REMARKS  |
|--------------|-------------------------|-----------------------------------|----------------------------|---------------------|----------------------------|--------------|--|
| 164          | 153<br>(RESET<br>INPUT) | 158<br>161<br>162<br>TP18<br>TP19 | 184<br>186<br>TP30<br>TP31 | 193<br>TP23<br>TP24 | TP20<br>TP21<br>TP22       | TP16<br>TP17 |  |
| OV           | OV                      | OV                                | OV                         | 24V                 | <del>24V</del><br>0        | OV           | Res. between TP16-TP17, TP17-161, TP30-TP31 and TP31-186 should be more than 10M Ohms. |
| 125V<br>125V | OV<br>OV                | 125V<br>125V                      | 24V<br>24V                 | OV<br>OV            | <del>24V</del><br>0<br>24V | OV<br>125V   | After 0.1 + 0.02 sec.  |
| OV           | OV                      | 125V                              | 24V                        | OV                  | <del>24V</del><br>24       | 125V         | Res. between TP23-RP24 and TP24-193 should be more than 10M Ohms.                      |
| OV           | 24V                     | OV                                | OV                         | 24V                 | 0 <del>24V</del>           | OV           |  |
| OV           | OV                      | OV                                | OV                         | 24V                 | 0 <del>24V</del>           | OV           |  |

The time intervals between the moment at which voltage at terminal 193 goes from 24V to OV and the moments at which voltages at TP20, TP21, and TP22 go from ~~24V~~ to ~~OV~~ should be ~~0.03~~ sec. + 0.02 sec.

The correct function of the 2 out of 3 logic of relays K18, 19, 20, and 23, 24, 25 is verified by the resistance measurements under REMARKS (Table I) and in addition by the following:

- With circuit reset and any one of K18, 19, or 20 removed (unplugged) voltage at 193 should be 24V.
- With circuit tripped and any one of K18, 19 or 20 unplugged voltage at 186 should be 24V.
- With anyone of K23, 24, 25 unplugged the circuit trip is still being latched in (24V at 158 after removal of input at 164).

125V  
9336  
9-23-91

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SH NO. 5

REV NO. 1  
P3K-AL-0380-A01  
CONT ON SHEET 7 SH NO. 6

TITLE TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1374 G1, 118D1374 G2  
FIRST MADE FOR EHC MARK II

## II. CIRCUIT SPECIFICATIONS (continued)

### 4.3 Other Latching 125V Trips

The following conditions should also cause latching 125V trip. It is not necessary to verify the compliance with Table I, since this was done for the case 4.2 (terminal 164). The occurrence of trip is sufficiently verified by observing 125V at terminal 158. The circuit should be RESET after each condition is created and the trip verified before creating the next condition.

a. Momentary application of 125 V to terminal 4 causes 125 V trip. (Momentary here and subsequently means having a duration more than 0.2 sec. but not sustained; essentially it is a short way to say that the trip is latched after removal of the input).

b. Momentary application of 125 V to terminal 7 causes 125 V trip.

c. Momentary application of 125 V to terminal 12 while 24 V is applied to only one or none of the terminals 76, 77, 78 causes 125 V trip, and 125 V voltage to appear at TP1 and TP2. (All 4 cases should be verified). *(TP1, TP2 Read 125V only while 125V is APPLIED. To Terminal 10, 158 should read 125V until Ckt is reset)*

On the contrary momentary application of 125 V to terminal 12 while 24 V is applied to any two, or to all three of the terminals 76, 77, 78 does not cause trip. (At least the first 3 of the 4 cases should be verified).

d. Momentary application of 125 V to terminal 15 causes 125 V trip.

e. Momentary application of 125 V to terminal 52 causes 125 V trip.

f. Momentary application of 125 V to terminal 60 causes 125 V trip. In addition as long as 125 V is applied to terminal 60 the voltage of terminal 80 becomes 0V while otherwise it is 24 V.

g. Momentary application of 125 V to terminal 62 causes 125 V trip.

h. Application of 125 V to terminal 64 <sup>118D1374 G1, G2, G3</sup> causes after 10 sec.  $\pm$  1 sec. this voltage to appear at ~~TP1, TP2~~, TP4, TP3, and terminal 32 and produces a trip. Subsequent removal of the input makes all points to return to 0V while the trip is latched. (For board 118D1337G1 the time is 5 min.  $\pm$  0.5 min.)

These statements hold true even if any one of relays K51, K52, K53 is unplugged. When 64 voltage is 0V, the resistance between TP3-TP4 and 32 - TP3 should be more than 10M Ohms, and TP4 voltage 0V.

i. Momentary application of 125 V to terminal 17 causes 125 V trip.

j. Momentary application of 125 V to terminal 23 causes 125 V trip.

\*In this case the trip is resettable even if the input is still on.

The details of the function of this part of the circuit are given in

\*NOT TRUE ON 118D1374 G1, G2, G3

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CONT ON SHEET 7 SH NO. 6

REV. NO. 1  
P3K-AL-0380-A01  
CONT ON SHEET 8 SH NO. 7

TITLE TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 11M2-A001, 11M2-A002  
ASS'Y DRAWING 118D1374 G1, ~~118D1337 G1~~  
FIRST MADE FOR EHC MARK II

## II. CIRCUIT SPECIFICATIONS (continued)

### 4.3 Other Latching 125V Trips (continued)

j. (continued)

*\* NOT USED ON 118D1374 G1, G2, G3*

Table II:

| INPUTS AT |                | CORRECT OUTPUTS AT |      |      |     |     |     |     |
|-----------|----------------|--------------------|------|------|-----|-----|-----|-----|
| 23        | 153<br>(RESET) | 158<br>(TRIP)      | 19   | 31   | 81  | 82  | 121 | 122 |
| OV        | OV             | OV                 | OV   | OV   | 24V | OV  | 24V | OV  |
| 125V      | OV             | 125V               | 125V | OV   | OV  | 24V | OV  | 24V |
| 125V      | 24V            | OV                 | OV   | 125V | 24V | OV  | OV  | 24V |
| 125V      | OV             | OV                 | OV   | 125V | 24V | OV  | OV  | 24V |
| OV        | OV             | OV                 | OV   | OV   | 24V | OV  | 24V | OV  |
| 125V      | OV             | 125V               | 125V | OV   | OV  | 24V | OV  | 24V |
| OV        | OV             | 125V               | OV   | OV   | 24V | OV  | 24V | OV  |
| OV        | 24V            | OV                 | OV   | OV   | 24V | OV  | 24V | OV  |
| OV        | OV             | OV                 | OV   | OV   | 24V | OV  | 24V | OV  |

TABLE II

+ THIS PART  
OF CHART  
DOES NOT  
APPLY  
TO  
118D1374  
G1, G2, G3

k. Momentary application of 125V to terminal 89 or 83 causes 125 V trip. This is the Thrust Bearing Wear Detector Trip. The logic permits testing the circuit without tripping, continuous monitoring of the actuating pressure switch contacts, interlocking between the two testing circuits and other fail safe features.

The function of this circuit is described in Table III. This is in fact two tables with different headings and identical entries superimposed. The upper heading corresponds to the lower bearing circuit and vice versa.

Part of the circuit logic is not included in Table III for clarity. It is given in Table IV.

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SH NO. 7

TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1374 GL, ~~118D1374 GL~~  
MADE FOR EHC MARK II

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12/5/20

SH NO. 8.

CODE IDENT #



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NO.

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P3K-AL-0380-A01

CONT ON SHEET 10 SH NO. 9

TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1374 G1, ~~118D1337 G1~~  
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TABLE IV

[illegible]

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REV NO. 1  
P3K-AL-0380-A01  
CONT ON SHEET 11 SH NO. 10

TITLE TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1374 G1, 118D1337 G1  
FIRST MADE FOR EHC MARK II

## II. CIRCUIT SPECIFICATIONS (continued)

### 4.4 24V Trip, Non Latching, Non-Crosstripping

- a. Applying 24V to any two or all three of terminals 141, 144, 147 causes 24V trip, ie. deenergizes the two Electrical Trip Solenoids connected to terminals 149, 151. In addition to the trip these inputs energize relay K55 on the circuit board.

The term non crosstripping implies that these inputs do not cause a 125V trip. (This refers to the circuit board level; at the system level a given condition may create simultaneous 125V trip by energizing two inputs to the board.) When the inputs are removed, the circuit resets by itself (non latching).

The function of this part of the circuit is described in Table V.

The logic related to K55 will be specified later.

- b. Application of 24V to terminal 140 causes 24V nonlatching non-crosstripping trip. To verify the trip here and in subsequent steps it is sufficient to observe OV at terminal 148.

### 4.5 24V Trip, Latching, Non-Crosstripping

- a. Application of 24V to terminal 139 causes 24V to appear at TP38 and (after 0.03  $\pm$  0.002 sec) at TP40.

Application of 24V to terminal 143 causes 24V to appear at TP42 and (after 0.04  $\pm$  0.002 sec) at TP44.

Application of a 24V to terminal 146 causes 24V to appear at TP46 and (after 0.04  $\pm$  0.002 sec) at TP48.

Application of 24V to anyone (only one) of these terminals does not cause a 24V trip.

Simultaneous application of 24V for over 0.12 sec. to any two or all three of terminals 139, 143 or 146 causes 24V trip that is latched after removal of the inputs and can be reset (only after removal of the inputs) by applying 24V to terminal 153 (as for 125V trips).

During this trip 24V should appear also at TP27, TP28, TP29 and terminal 184.

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TITLE TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD ~~1TM2-A001~~, 1TM2-A002  
ASS'Y DRAWING 118D1374 G1, ~~118D1397 G1~~  
FIRST MADE FOR EHC MARK II

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CONT ON SHEET 12 SH NO. 11

**II. CIRCUIT SPECIFICATIONS (continued)**

REVISIONS

**4.5 24V Trip, Latching, Non-Crosstripping (continued)**

- b. Application of 24V for over 0.12 sec to terminal 181 causes 24V latching trip.
- c. Disconnecting the 125 VDC power supply to the board (terminal 1) causes 24V to appear at terminal 79. In addition to the above disconnecting the 125V supply to the board and at the same time applying 24V to anyone of terminals 76, 77, or 78 causes 24V to appear at TP34, 35, or 36 respectively, but not a trip.

Finally disconnecting the 125V supply and at the same time applying 24V to any two or all three of terminals 76, 77, or 78 causes 24V latching trip. (All other output conditions are non latching).

**4.6 24V Trip, Latching, Crosstripping**

- a. Application of 24V to any one ( only one) of terminals 138, 142 or 145 causes 24V to appear at the corresponding TP37, 41 or 45 but not a 24V or a 125V trip and does not cause 24V to appear at terminal 156. Application of 24V to any two or all three of terminals 138, 142, or 145 causes (1) 24V latching trip, (2) 125V trip, (3) 24V to appear at 156, TP32 and TP33, and (4) 125V to appear at 107 (only if F2 is in place), 105 (only if F3 is in place, and 160.
- b. Application of 24V to terminal 182 causes latching 24V trip and 125V trip.

**4.7 Auxiliary Logic**

Table VI specifies the function of minor parts of the circuit board which was not included in the previous sections mainly to prevent excessive complexity of the tables there.

**4.8 Lamp Test Circuit**

With +24 VDC power supply disconnected from terminal ~~80~~ and connected to terminal 75, <sup>Common 186</sup> a voltage of 24V or slightly less will appear at the following terminals: <sup>187</sup>

80, ~~81~~, ~~82~~, 121, 122, 124, 125, 128, 129, ~~130~~, ~~131~~, 189, 190.

The exact voltage value is 24 volts minus the voltage drop across the 68.1 ohms resistors and depends on the loading during the measurement, and should be observed to detect any erroneous resistance values. (e.g. for 10 MA loading the acceptable voltage drop is  $681 \pm 7$  mV.)

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24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1374G1, 118D1337-01  
FIRST MADE FOR EHC MARK II

TABLE V

REVISIONS

| INPUTS AT TERMINALS |     |     |     | CORRECT OUTPUTS AT TERMINALS<br>OR TEST POINTS |      |      |      |      |     |
|---------------------|-----|-----|-----|--|------|------|------|------|-----|
|                     |     |     |     | 1  | 2    | 3    | 4    | 5    | 6   |
|                     | 141 | 144 | 147 | TP39   | TP43 | TP47 | TP25 | TP26 | 177 |
| 1.                  | 0   | 0   | 0   | 0  | 0    | 0    | 0    | 0    | 0   |
| 2.                  | 24  | 0   | 0   | 24   | 0    | 0    | 125  | 0    | 0   |
| 3.                  | 0   | 24  | 0   | 0  | 24   | 0    | 125  | 125  | 0   |
| 4.                  | 0   | 0   | 24  | 0  | 0    | 24   | 0    | 0    | 0   |
| 5.                  | 24  | 24  | 0   | 24   | 24   | 0    | 125  | 125  | 125 |
| 6.                  | 24  | 0   | 24  | 24   | 0    | 24   | 125  | 125  | 125 |
| 7.                  | 0   | 24  | 24  | 0  | 24   | 24   | 125  | 125  | 125 |
| 8.                  | 24  | 24  | 24  | 24   | 24   | 24   | 125  | 125  | 125 |

(continued below)

| CORRECT OUTPUTS AT TERMINALS OR TEST POINTS |                 |                 |                 |                 |                 |
|---|-----------------|-----------------|-----------------|-----------------|-----------------|
|   | 7               | 8               | 9               | 10              | 11              |
|   | 117             | 118             | 119             | 120             | 148             |
| 1.  | 23.865 ± 0.003V | 23.865 ± 0.003V | 23.865 ± 0.003V | 23.865 ± 0.003V | 23.729 ± 0.005V |
| 2.  | 23.600 ± 0.008V | 23.733 ± 0.006V | 23.600 ± 0.008V | 23.733 ± 0.006V | 23.333 ± 0.013V |
| 3.  | 23.734 ± 0.005V | 23.468 ± 0.011V | 23.379 ± 0.012V | 23.468 ± 0.011V | 23.290 ± 0.014V |
| 4.  | 23.822 ± 0.004V | 23.912 ± 0.003V | 23.822 ± 0.004V | 23.556 ± 0.008V | 23.290 ± 0.014V |
| 5.  | 0.000V          | 0.000V          | 0.000V          | 0.000V          | 0.000V          |
| 6.  | 24.000V         | 24.000V         | 24.000V         | 24.000V         | 0.000V          |
| 7.  | 24.000V         | 24.000V         | 0.000V          | 0.000V          | 0.000V          |
| 8.  | 0.000V          | 0.000V          | 0.000V          | 0.000V          | 0.000V          |

Measurements made with a 24.000V power supply to the board.

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24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001, 1TM2-A002  
ASS'Y DRAWING 118D1374 G1, ~~118D1377 G1~~  
FIRST MADE FOR EHC MARK II

CODE 10057 2.

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TITLE

TEST INSTRUCTIONS FOR 125 VOLT/  
24 VOLT TRIP BUS CIRCUIT BOARD 1TM2-A001  
ASS'Y DRAWING 118D1374  
FIRST MADE FOR EHC MARK II

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CONT ON SHEET

SH NO. 14

REVISION

TEST INSTRUCTION  
PREPARED BY

*D. Economou*

DATE

*9/24/1973*

D. Economou  
EHC DESIGN ENGINEERING

APPROVED BY

*P.C. Callan*

DATE

*9-6-77*

P.C. Callan - MANAGER  
EHC DESIGN ENGINEERING

TEST PROCEDURE

REVIEWED BY

*R. Debertolis*

DATE

*9/24/77*

R. Debertolis  
EHC TEST ENGINEER

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