REV NO. 01734

P3K-AL-0305-A01
CONT ON SHEET 2 SH NO. 1

TITLE
TEST INSTRUCTIONS FOR FREQUENCY TO VOLTAGE CONVERTER

FIRST MADE FOR EHC MARK II

115D2220 G2

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I. SCOPE

This test instruction outlines the specifications for the FREQUENCY TO VOLTAGE (F/V) converter circuit board 115D2220 G1, G2

II. CIRCUIT DESCRIPTION

The F/V converter circuit consists of a voltage comparator (IC1), 2 flip-flops (IC2 & IC4), 2 switching transistors (Q1 & Q2), a unijunction (Q3) and an output amplifier (IC7). The circuit also contains 3 additional IC's (IC3, IC5 & IC6) which are used to LOCK UP the output (hold output voltage constant) when the input frequency exceeds 6000 Hz.

The comparator (IC1) converts the input sine waves from the speed pickup on the turbine to square waves of equal frequency. IC2 is used for wave shaping and its output is differentiated to produce a spike waveform which triggers flip flop IC4 and turns Q1 on and Q2 off. When Q1 is switched on, the unijunction timer circuit is initiated, and when Q2 is switched off, a fixed voltage is applied to amplifier IC7.

When the unijunction times out and fires, it produces a reset pulse back to flip-flop IC4 which switches Q1 off and Q2 on; thus removing the fixed voltage from amplifier IC7. Note that Q1 initiates the unijunction timer and Q2 applies a fixed voltage to the output at the start of each incoming positive going pulse and that the fixed voltage is turned off when the unijunction circuit times out causing the flip flop to change state. Since this constant voltage is switched on for a precise time, a constant amplitude, fixed pulse width results (note that the amplitude is fixed by the zener voltage (+9 V), width is held constant by the unijunction circuit (~156 usec) and the pulse occurance corresponds to the input frequency).

Test starts on page 11

Power Supply Requirements on page 7

Do not use MKII UNIV Fixture

USE Just Plain UNIV Fixture

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273-2
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PRINTS 1

GENERAL DESCRIPTION (continued)

The output amplifier (IC7) along with a 2nd order, multiple feedback, low pass active filter, converts the input pulses to a dc output which is proportional to frequency.

The characteristic frequency to voltage curve which the F/V converter circuit produces is shown below. As the input frequency increases from 0 to 6000 Hz, the output voltage increases linearly from 0 to -12.50 volts. At rated speed (4800 Hz), the output voltage = -10.000 volts.

For all frequencies greater than 6000 Hz, the LOCK UP circuit will hold the output constant at approximately -13.3 volts.

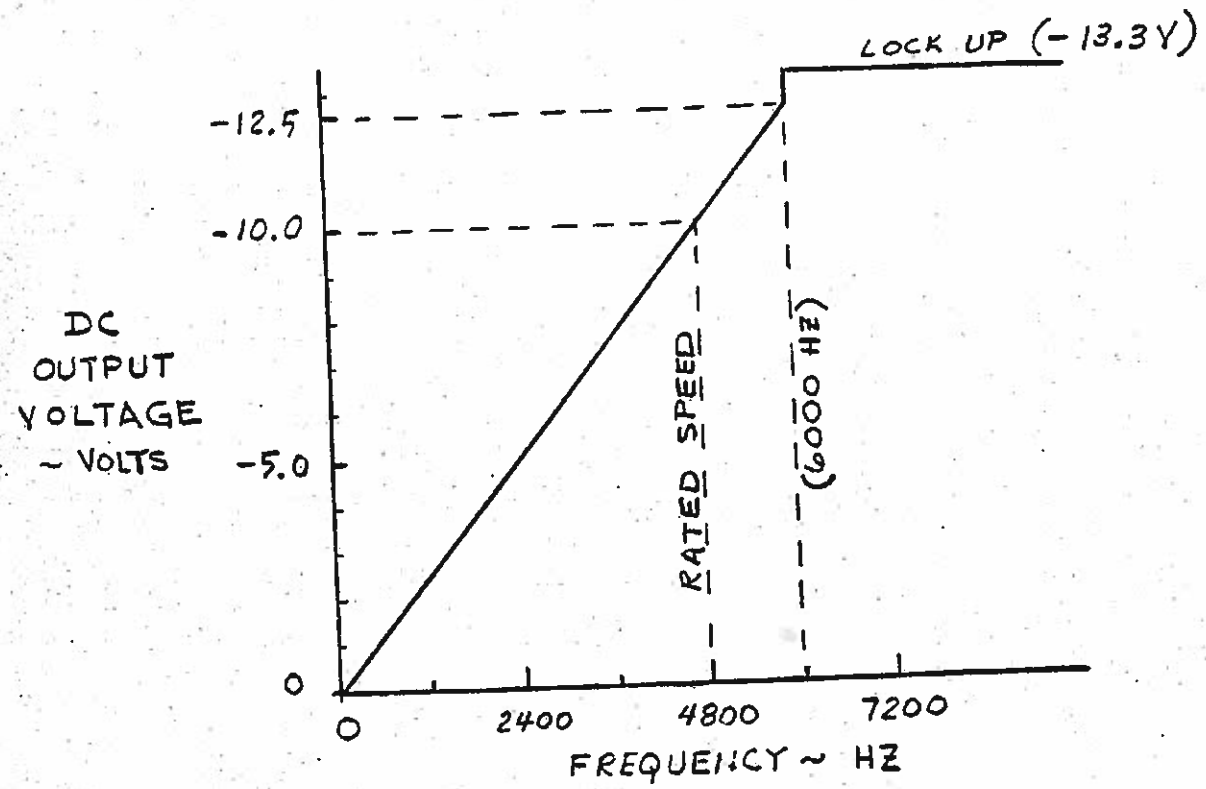

FIG. 1 FREQUENCY/VOLTAGE CHARACTERISTIC CURVE

DUTY FACTOR

The duty factor of the F/V circuit is 75% at rated speed (4800 Hz), placing the 100% duty factor at 6400 Hz. The duty factor is 93.5% at LOCK UP (6000 Hz).

LOCKUP DETECTOR

The lockup detector is a 9601 one-shot, which is retriggerable and remains set when inputs occur at a period shorter than its operating time. Inputs that occur while the one-shot is set are counted by a binary counter, so that one interfering pulse cannot actuate a lockup. When the counter is full, IC5 causes the F/V converter to LOCK UP and also inhibits the counter. When a clear cycle occurs with no interference, the counter is reset when the one-shot times out, removing the lockup.

The circuit requires a minimum of 13 inputs shorter than the timing of the 9601 one shot to achieve lockup. Since lock up occurs at a frequency below that at which the unijunction begins to skip, the unijunction timer flip-flop is still running properly. The output jumps up to the locked-up level when the time period of the input frequency is equal to the one shot time. At lockup (6000 Hz) the output jumps from -12.5 V up to -13.3 V.

BINARY COUNTER

A 4-stage binary counter as shown in Figure 2 counts input triggers that occur while the one shot is on. The counter is reset to zero whenever the one shot is off, so that inputs (combination of interference and normal) must occur closer together than the one shot time in order for the count to accumulate. The counter can accomodate up to 15 inputs, although only 13 are actually used in the final system, in order to optimize the gate circuits. When the count reaches 13, NAND gate G2 enables, and its output turns off the input to the counter via NAND gate G1, thereby sustaining the counter in state 13. It also goes to AND gate G3, which locks up the output from the main flip-flop.

The 13 count delay in applying lock-up to the output can be tolerated because it will occur in 13 cycles of the input frequency while it is between the 95% and 100% duty factor points. In this region, flip-flop 1 is still running normally. With 100% speed in the kilocycle region, only about 10 milliseconds is required to actuate the lock-up, and even manual ramping of an oscillator frequency source is not fast enough to produce any observable down-scale transient when raising the frequency past 100%.

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NOISE IMMUNITY

For interference occurring near the operating frequency, seven spurious inputs are required to actuate the lock-up circuit. Together with the 6 adjacent normal inputs, the count of 13 is achieved as shown in Figure 3. However, the frequency of the interference needs to be only slightly lower in order to cease having any effect at all on the d-c output. This is the frequency which will allow the one-shot to time out just before the lock-up count gets to 13. The limit involves the duty factor of the one shot at the frequency of the normal input. For our application where the duty factor is 75%, the result is immunity to any interfering frequency below 91.2% of the normal input. This result is not strongly dependent on the counter capacity. A count 15 would only raise it to 92.4%. A three stage counter with a capacity of 7 is still immune to interference up to 84% of the normal frequency.

The basic noise immunity of the unijunction timer also depends on its action when noise occurs in the time that its flip-flop is off. This condition will start a premature timing cycle, but will not effect the output through the filter since the result is to move the position of that cycle without affecting its duration. This is true as long as the next normal input occurs while the unijunction is still timing, which will be the case for any location of the interference as long as the duty factor of the unijunction flip-flop is 50% or greater. At lower input frequencies, interference can inject a complete extra unijunction time cycle between its normal ones, thereby raising the output. Therefore, the system design uses a normal duty factor of 75%. As typically used for speed feedback, the increase in output that interference can cause at low speeds is in the safe direction.

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TITLE
TEST INSTRUCTIONS FOR FREQUENCY TO VOLTAGE CONVERTER

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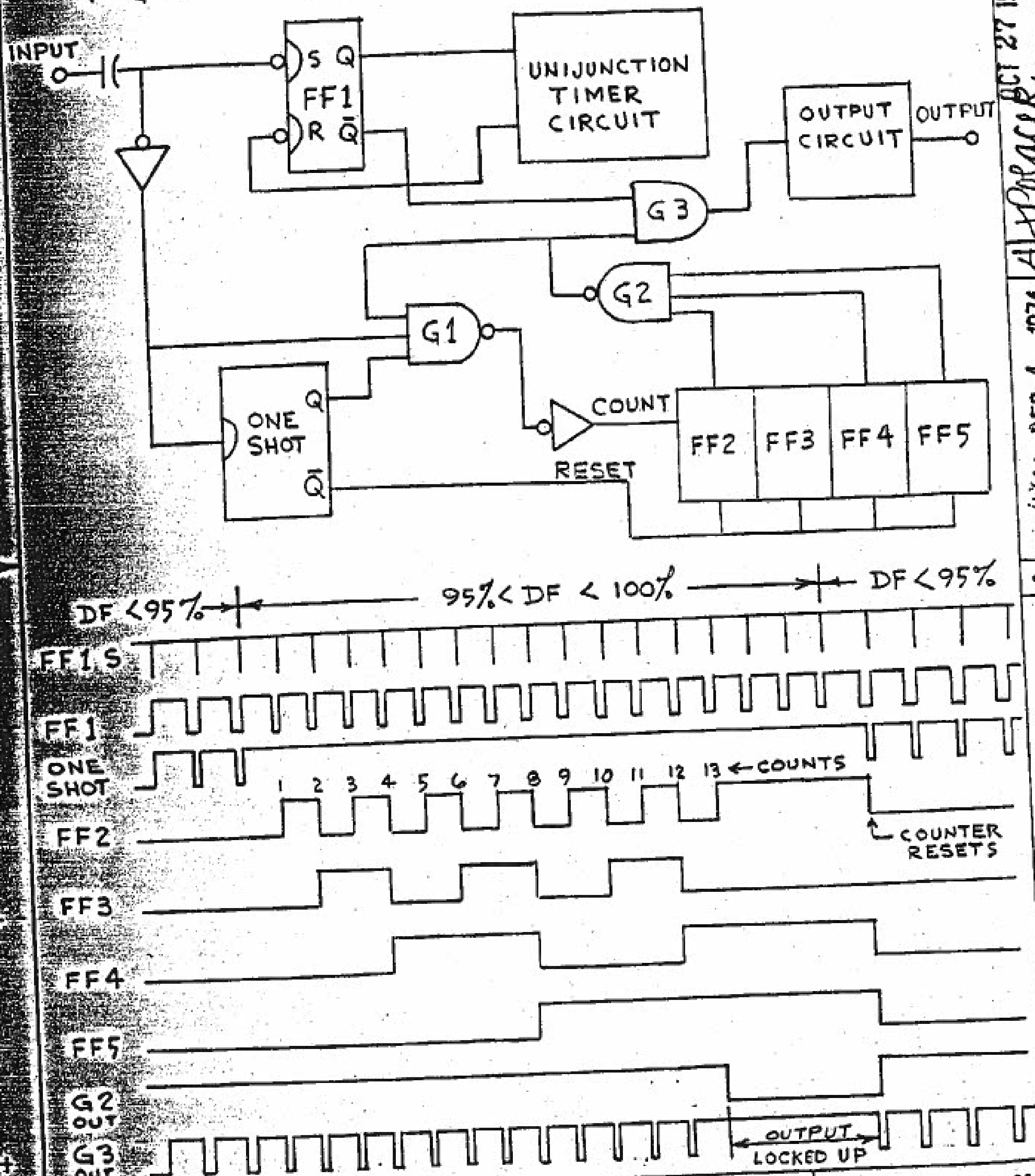
FIG 2 FREQ/VOLTAGE CONVERTER BLOCK DIAGRAM



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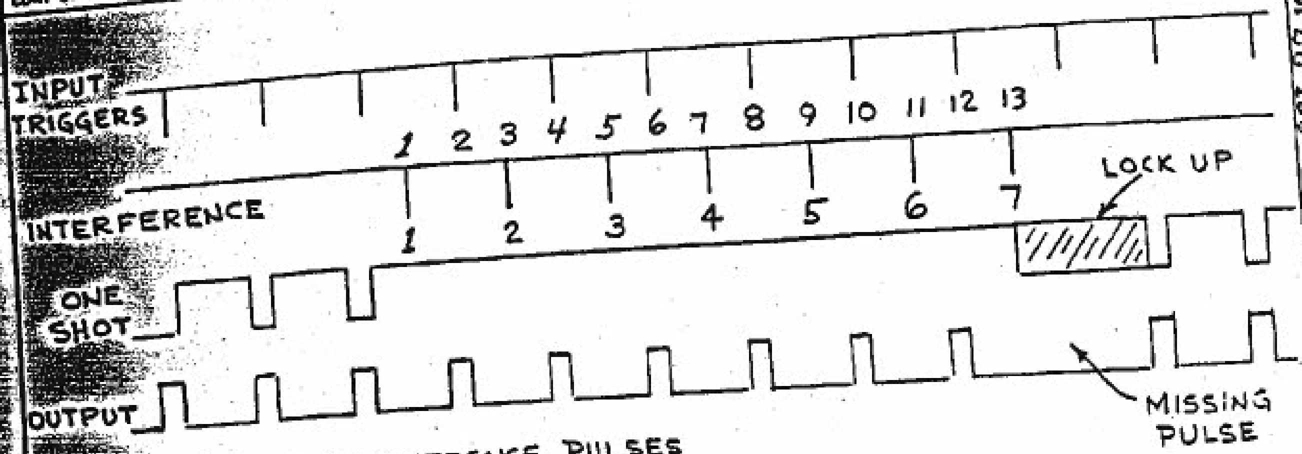
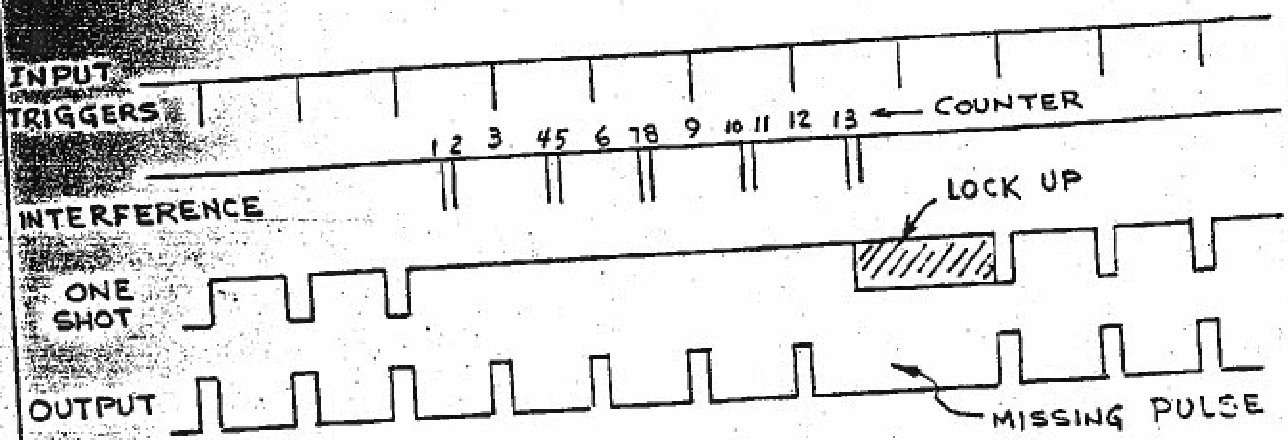


NOTE: 6 INTERFERENCE PULSES SHOULD NOT AFFECT THE OUTPUT

FIG 3a EFFECT OF INTERFERENCE (ONE PULSE PER INPUT CYCLE)



NOTE: 4 INTERFERENCE PULSE PAIRS SHOULD NOT AFFECT THE OUTPUT

FIG 3b EFFECT OF INTERFERENCE AT ONE PULSE PAIR PER INPUT CYCLE

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III. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

+Power Supply: (Pin 37) +22.000 ± .002 VDC (plus supply draws approx. 200ma)

-Power Supply: (Pin 41) -22.000 ± .002 VDC (minus supply draws approx. 50ma)

B. Operating Signal Levels @ com 39 (Pins 28 & 24)

Input Frequency: 4.8 HZ to 10,000 HZ.

Input Amplitude: 50mV to 80V p-p sinewave

Input Amplitude Required to Turn on F/V
(Input Level Adjust at 480 HZ sinewave)

Range:	G1	max. = 100 ± 25 mV p-p	VR50 full CCW
		min. = 40mV p-p (approx.)	VR50 full CW or less
	G2	max. = 200 ± 100 mV p-p	VR50 full CCW
		min. = 40 mV p-p (approx.)	VR50 full CW or less

Set Point: 50 mV p-p

Input Noise Suppression lag

Breakpoint: G1 = 122.5 ± 7.5 KHz
G2 = 5.6 ± 0.4 KHz

C. Output Load (Pin 6)

Refer to test setup - Figure 4.

D. Zener Regulated Voltages

CR3 = +5.1 ± 5% ±.25V ✓ TP52 RED
CR4 = +9.0 ± 1% ±.09 V ✓ TP55 GREEN
CR5 = +11.7 ± 5% ±.59V ✓ TP53 BLACK
CR6 = +16.0 ± 5% ±.80V ACROSS CR6
CR7 = +12.0 ± 5% ±.60V TP54 BROWN
CR8 = -16.0 ± 5% ±.80V TP56 ORN

E. Output Characteristics (TP6)

Saturation Level of IC7: -14.0 ± .8V & +11.25 ± .6V

DC OUTPUT = -10.000 ± .001V at 4800 ± 1 HZ

DC OUTPUT: Must increase linearly with input frequency (0 to -12.5 VDC for 0 to 6000 HZ).

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III. CIRCUIT SPECIFICATIONS

E. Output Characteristics (TP6) (continued)

DC OUTPUT: Must remain constant at -13.30 ± .20 VDC for input frequencies > 6000 HZ.

DC OUTPUT: Must be adjustable above and below -10.000V when input frequency is held constant at 4800 ± 1 HZ.

VR1 full CW DC OUTPUT VOLTAGE ≧ -10.200 VDC
VR1 full CCW DC OUTPUT VOLTAGE ≦ - 9.800 VDC

DC OUTPUT: Must be sensitive to changes of input frequency and insensitive to changes of input amplitude.

ACCEPTABLE OFFSET: 1 mV after nulling output.

TEMPERATURE STABILITY: DC OUTPUT must not change more than 5mV when temperature is varied between 20 to 55°C, & frequency is held constant at 4800 HZ.

Output Noise

Inherent Low Frequency Noise generated by the F/V converter at rated input frequency and rated output load:

G1 = 50 to 200 uV p-p of flicker noise (1 to 10 HZ)
G2 = less than 50 uV p-p of flicker noise (1 to 10 HZ)

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III. CIRCUIT SPECIFICATIONS (continued)

E. OUTPUT CHARACTERISTICS (TP6) (continued)

DC OUTPUT VOLTAGE TRANSFER FUNCTION (WHEN 9V APPLIED TO INPUT OF ACTIVE FILTER)

$$\frac{E_o}{E_1} = \frac{-k}{\frac{s^2}{\omega_o^2} + \frac{2\zeta}{\omega_o} s + 1}$$

$$= \frac{-k\,\omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}$$

$$= \frac{(-1.475)(76.7)^2}{s^2 + 2(.507)(76.7)s + (76.7)^2}$$

$$= \frac{-8677}{s^2 + 77.77s + 5883}$$ { NOMINAL VALUES

WHERE:

k = GAIN = $1.475 \pm .030$ V/V

ζ = DAMPING RATIO = $.507 \pm .028$

ω_o = UNDAMPED NATURAL FREQUENCY = 76.7 ± 5.0 RAD/SEC.

f_o = UNDAMPED NATURAL FREQUENCY = 12.2 ± 0.8 HZ

NOTE:

The transfer function for the F/V converter results from the multiple feedback active filter, amplifier IC7. This low pass quadratic filter is underdamped, and the characteristics k & ζ change when Q2 switches R17 in and out of the active filter network. As a result, the output voltage transfer function changes as follows:

OUTPUT VOLTAGE TRANSFER FUNCTION
(WHEN ZERO VOLTS APPLIED TO INPUT OF ACTIVE FILTER)

$$\frac{E_o}{E_1} = \frac{-k\,\omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}$$

$$= \frac{(-2.95)(76.7)^2}{s^2 + 2(.689)(76.7)s + (76.7)^2}$$

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III. CIRCUIT SPECIFICATIONS (continued)

E. OUTPUT CHARACTERISTICS (TP6) (continued)

$$\frac{E_o}{E_1} = \frac{-17354}{s^2 + 105.7s + 5883}$$ { NOMINAL VALUES

WHERE:

k = GAIN = $2.950 \pm .060$ V/V

ζ = DAMPING RATIO = $.689 \pm .042$

ω_o = UNDAMPED NATURAL FREQUENCY = 76.7 ± 5.0 RAD/SEC.

f_o = UNDAMPED NATURAL FREQUENCY = 12.2 ± 0.8 HZ

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TEST SETUP

EQUIPMENT REQUIRED (or Equivalent)

1. Frequency Source — HP Model 200 AB
2. Frequency Counter — HP Model 5223L
3. Digital Voltmeter — Fluke Model 8120A
4. Oscilloscope — Tektronix Model 565 Equipped with Two Dual Trace Amplifiers Type 3A72

OR

Tektronix model 7514 storage scope with two dual trace amplifiers type 7A18

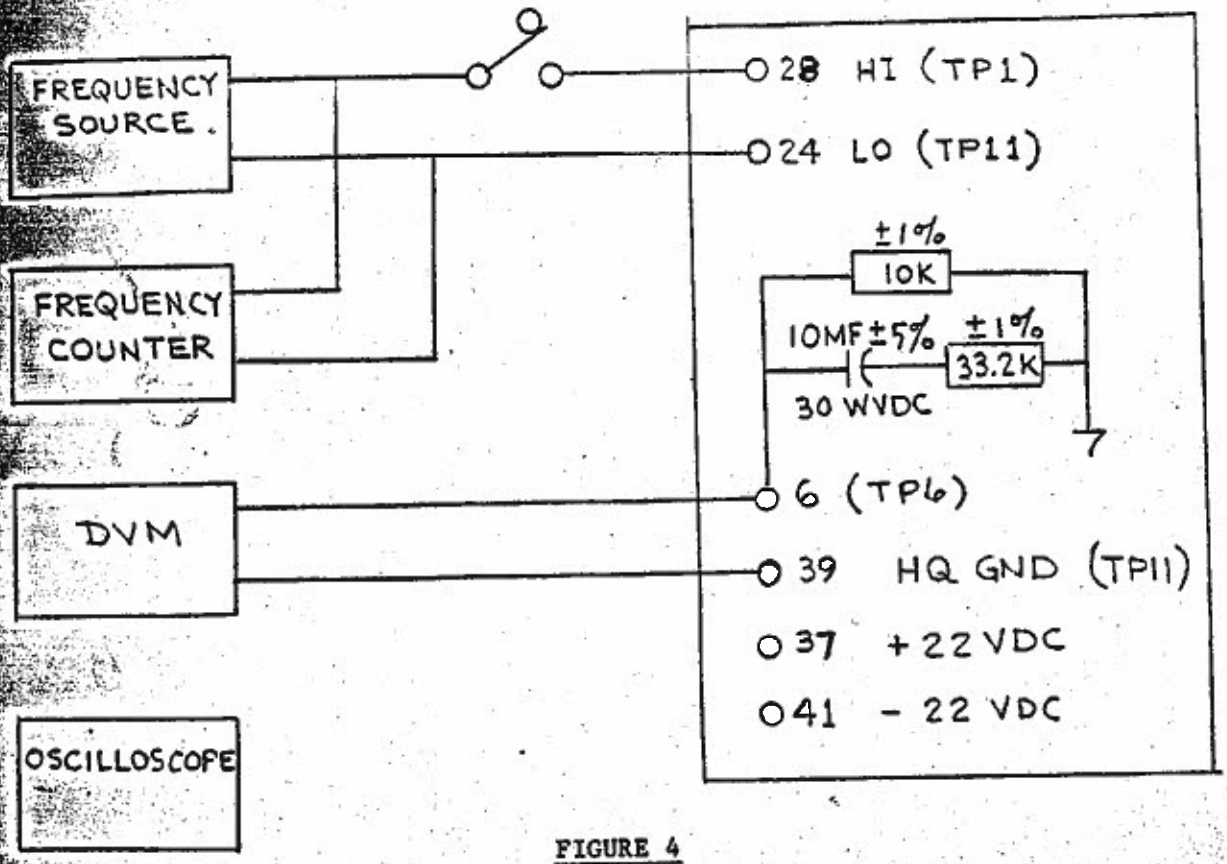

FIGURE 4

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IV. TEST INSTRUCTIONS

*All notes are intended for information purposes and for trouble shooting aids**

*NOTE: Positive logic is used thru out entire F/V digital design.

1. CONNECT F/V circuit board per test set-up shown in Figure 4.
2. CHECK ZENER VOLTAGES on the card per circuit specifications sheets. Sh.7
3. ADJUST LOCKUP CIRCUIT OUT OF LINEAR REGION:

 • Adjust trimpot VR52 full CCW.

 *NOTE: Adjusting VR52 full CCW sets the reset time of the Binary Counter to approx. 140 usec. (measured on scope at IC6 pin 2). As a result, the lock up circuit will not function until the input frequency is approx. 7000 HZ, which is well above the normal linear working region of 0 to 6000 HZ.

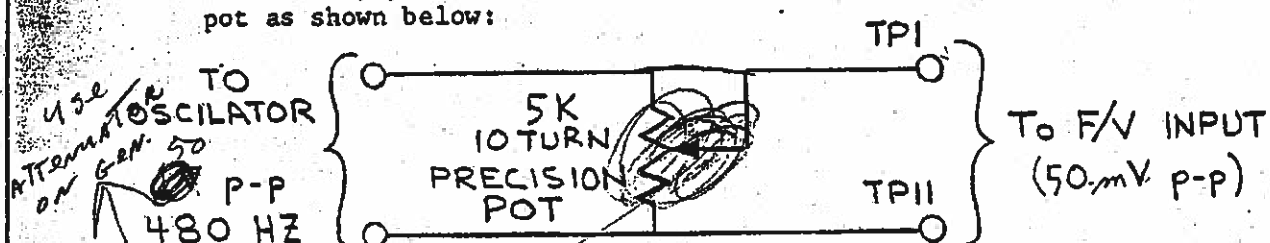
4. NULLING OUTPUT AMPLIFIER:

 • Apply dc power to the F/V card but keep the input signal from the sine wave oscillator turned off.

 • Adjust trimpot VR51 for zero volts output (± .001V) at TP6.

5. SETTING INPUT LEVEL TO BE DETECTED

 • Set oscillator frequency at 480 HZ and sine wave amplitude to 1V p-p.
 • Reduce 1V p-p signal down to approx. 10 to 20 mV p-p with a 10 turn pot as shown below:



 • Adjust INPUT LEVEL ADJUST pot VR50 full CCW.
 • Slowly increase amplitude and determine that magnitude required to just turn on converter (F/V output = -1.0V) meets following criteria:

 G1 Input amplitude required to turn on F/V with VR50 full CCW shall be 100 ± 25 mV p-p.

 G2 Input amplitude required to turn on F/V with VR50 full CCW shall be 200 ± 100 mV p-p.

 • Reduce 1V p-p signal down to 50 mV p-p.
 • Observe output of IC1 (TP2) on scope and slowly adjust INPUT LEVEL ADJUST trimpot VR50 CW until a stable square wave can be obtained as shown below:

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5. SETTING INPUT LEVEL TO BE DETECTED (continued):

* NOTE: A stable dc output voltage from the F/V card will result when the pot is properly adjusted.

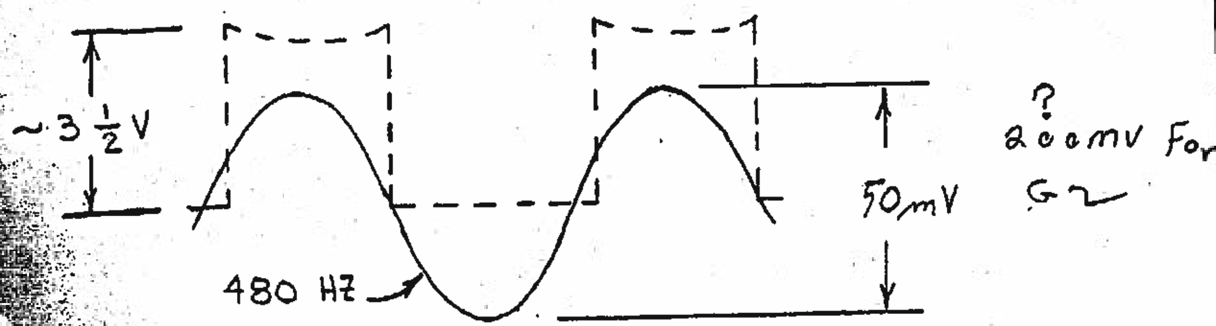

FIG. 5 ADJUSTING TRIMPOT VR50 TO OBTAIN SQUARE WAVE OUTPUT FROM IC1 AT TP2

* NOTE: The primary purpose of trimpot VR50 is to adjust the detection level of comparator IC1 so that low amplitude input signal (approx. 50mV) can produce a stable square wave output. As soon as the input level is much > 50mV, this adjustment is insignificant. After VR50 is adjusted, note that signals < 50MV p to p will go undetected and the F/V converter will not produce any dc output.

6. CHECKING & RECORDING CRITICAL VALUES:

- ~~Remove the 5K alternating pot from the oscillator input.~~

* NOTE: This pot should be removed because it may produce noise problems in the test setup when the lock up circuit is checked out.

- Measure and record the voltage at CR4 (zener voltage must be +9.0V ± 1%). 8.94 9.082 9.01
- Set the oscillator amplitude at approx. 2V p to p and the frequency at exactly 4800 ± 1 Hz.
- Adjust VR1 full CW and record the dc output voltage at TP6 (voltage must be ≥ -10.200 volts). For example, an output voltage of -10.400 V is acceptable but an output of -10.100 V is unacceptable. -10.25 -10.44

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6. CHECKING & RECORDING CRITICAL VALUES (continued):

- Adjust VR1 full CCW and record the dc output voltage at TP6 (voltage must be ≦ -9.800 volts). For example, an output voltage of -9.600 V is acceptable but an output of -9.900 is unacceptable. -9.37 -9.61

9.416 *NOTE: The output voltage will vary approx. 0.8V when VR1 is adjusted from end to end. Trimpot VR1 adjusts the unijunction time from approx. 150 to 162 usec.

The unijunction time controls the width of the pulses to IC7. This time can be measured on the scope at TP3 as shown below:

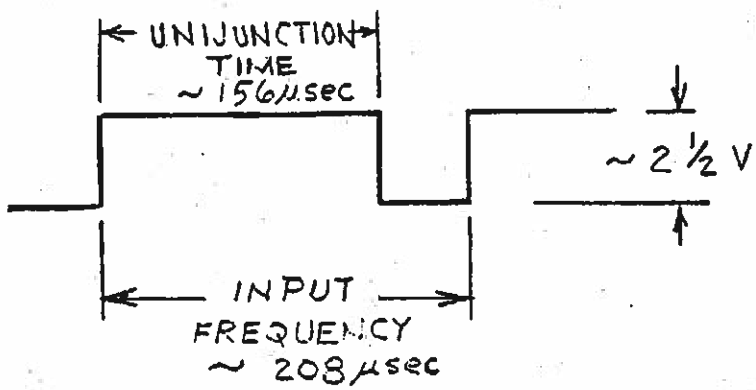

FIG. 6 WAVEFORM AT TP3 (INPUT FREQ. = 4800 HZ)

NOTE: DUTY FACTOR = 75%

*NOTE: The same pulse shape as shown above can also be observed at the input to the output amplifier IC7 except that the amplitude will be approx. 4 1/2 volts (measured at collector of Q2).

VR1	OUTPUT VOLTAGE dc	UNIJUNCTION TIME
Full CCW	-9.600	150 usec
Center of Pot	-10.000	156 usec
Full CW	-10.400	162 usec.

TYPICAL VALUES ASSOCAITED WITH ADJUSTING VR1

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7. CALIBRATING F/V OUTPUT VOLTAGE

- Set the oscillator frequency at exactly 4800 ± 1 Hz and amplitude at approx. 2V p to p.
- Adjust trimpot VR1 until output at TP6 equals -10.000 ± .001 volts.
- Increase and decrease the oscillator amplitude from 2V p to p to 20 V p to p. Note that the dc output should not be sensitive to changes in input amplitude, but only to changes in frequency.
- Check the output voltage at several additional frequency points shown below:

INPUT FREQUENCY (Hz)	DC OUTPUT VOLTAGE
6000	-12.500 ± .002 V
4800	-10.000 ± .001 V
2400	- 5.000 ± .002 V
480	- 1.000 ± .002 V
48	Approx. -0.10 V
4.8	Approx. -0.01 V

*NOTE: When the input frequency = 4800 Hz, the output voltage will be -10.000 V, and the duty factor will be 75% as shown in Fig. 6.

- Return the oscillator frequency to exactly 4800 Hz, and observe that output at TP6 equals -10.000 volts.
- Set the heat probe at 55°C and apply the probe to the unijunction for 30 sec. Remove the probe and observe that the output voltage must return to within ± 3 mV of the original -10.000V setting. (The unijunction heat test is repeated in order to insure that the correct temperature compensation resistor has been previously selected). Use Timer (designed for temp. compensating test) to measure 30 sec. interval that heat probe is applied.

CRITERIA F/V output must return to within ± 3mv of the original -10.000V setting when heat probe test is repeated.

If production F/V fails to meet above criteria, refer to next page for corrective action.

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TEST INSTRUCTIONS FOR FREQUENCY
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7. CALIBRATING F/V OUTPUT VOLTAGE

Procedure to Correct Temperature Compensation to be within ± 3 mv Criteria

If Production F/V output (matched parts installed) fails to meet ± 3 mv change in output when unijunction is retested with heat probe, use the following procedure to reduce the change to be within the ± 3 mv criteria:

1. Replace R11 (temp. compensation resistor)

   If F/V output increases more than 3 mV (-10.000V increases to more than -10.003V) when heat probe test is performed, reduce R11.

   If F/V output decreases more than 3 mV (-10.000V decreases to less than -9.997V) when heat probe test is performed, increase R11. Note that F/V output changes 3mV for every change in resistor step (1%).

2. If value of resistor R11 cannot be increased because it's already at a maximum, replace +11.7V zener CR5. Note that 1% change in zener voltage CR5 will cause approximately 1 mV change in F/V output.

   If F/V output increases more than 3 mV (-10.000V increases to more than -10.003V) when heat probe test is performed, select a new CR5 which has lower zener voltage than original value.

   If F/V output decreases more than 3 mV (-10.000V decreases to less than -9.997V) when heat probe test is performed, select a new CR5 which has a higher zener voltage than original value.

3. If value of zener CR5 cannot be increased or decreased to temperature compensate the Unijunction transistor to within 3 mV, replace all matched components and start over.

IF Last Test step OK Bypass This page

matched set # 244A5240G0001 R11+R3

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J. Polacek Oct. 26, 1978 APPROVALS

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7. CALIBRATING F/V OUTPUT VOLTAGE (continued)

*NOTE: When the F/V is operating in the linear region, the output voltage can be calculated as follows:

$$Vo = (V\ in)\ (-GAIN\ IC7)$$

$$Vo = \left(VCR4\right)\left(\frac{\text{Period of unijunction}}{\text{Period of input frequency}}\right) \qquad (-GAIN\ IC7)$$

WHERE:

VCR4 = Input zener voltage to output amplifier IC7.

$\left(\frac{\text{Period of unijunction}}{\text{Period of input frequency}}\right)$ = Ratio of the zener voltage CR4 ON time to the total time.

GAIN IC7 = GAIN of output amplifier IC7.

$$= -R20/(R17 + R18)$$

$$Vo\ @\ 4800\ HZ = \left(9V\right)\left(\frac{156\ usec}{208\ usec}\right)\left(\frac{113K}{38.3K + 38.3K}\right)$$

Vo @ Rated Frequency = -10.00 volts.

As the period of the input frequency approaches the period of the unijunction, (100% duty factor), the maximum output voltage which can be obtained from the circuit is as follows:

$$Vo\ max = \left(9V\right)\left(\frac{156\ usec}{156\ usec}\right)\left(-\frac{113K}{38.3K + 38.3K}\right)$$

$$= -13.3\ volts$$

Therefore, the upper frequency limit is also a function of the unijunction time. Note that when the period of the input frequency becomes less than or equal to the period of the unijunction timer, the flip flop will start missing input pulses.

(8) SETTING LOCK UP LEVEL:

- Increase the input frequency slowly from 4800 Hz to 6000 Hz (note that the output must increase linearly from -10.000 to -12.50 volts).
- Observe that the output voltage does not decrease or fall off before reaching 6000 Hz.
- Adjust VR52 CW until the output voltage jumps from -12.50 to -13.30 ± .20 volts. -13.32 -13.13 -13.22
- After setting the lockup point at 6000 Hz, increase the input frequency from 6000 Hz up to 10,000 Hz and back down. Observe that the output voltage does not change in the lockup region.

* NOTE: The result of adjusting VR52 is to set the reset time (which clears the binary counter) to approx. 165 μsec. This reset time can be observed on the scope at IC6 pin 2 as shown below:

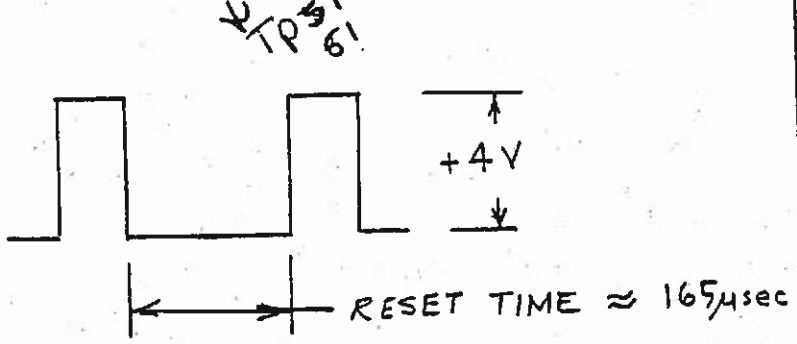

FIG.7 RESET WAVEFORM (FREQ. = 4800 HZ)

Adjusting VR52 full CCW sets the reset time to approx. 140 μsec. while adjusting VR52 full CW should produce a reset time of approx. 200 μsec. The reset time will normally be set at 165 μsec (6000 Hz).

* NOTE: The voltage level at TP4 will change from HI to LO, as soon as the frequency reaches 6000 Hz and the binary counter registers 13 pulses as shown below:

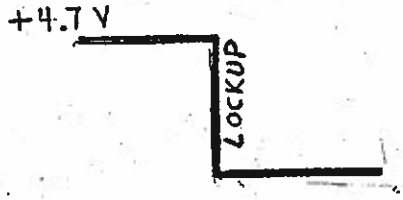

FIG.8 TP4 WAVEFORM AT LOCKUP

here

8. SETTING LOCK UP LEVEL (continued):

NOTE:

When TP4 is switched from HI to LO, the output of flip-flop IC4 at TP5 is also hold LO (OFF). As a result, Q2 will be held off, CR4 will be held on, and the output jumps up to - 13.3 volts. This output voltage measurement can be used to check the gain of the active filter amplifier (IC7) as follows:

$$(Vin)\ (-GAIN\ IC7) = V_o$$

$$(V_{CR4})\left(-\frac{R20}{R17 + R18}\right) = V_o$$

$$(9V)\left(-\frac{113K}{38.3K + 38.3K}\right) = V_o$$

$$(9V)\ (-1.475) = -13.3V \quad \{\text{TYPICAL VALUES}$$

Therefore, in order to obtain the gain of IC7, divide the measured output voltage (at Lock Up) by the measured zener voltage.

$$GAIN\ IC7 = \frac{Vout}{V_{CR4}} \leftarrow \text{at lockup}$$

Therefore, when TP4 switches from HI to LO, the output voltage will jump up to -13.3 V, which indicates that lock up has occurred.

This lock up condition results when the frequency pulses occur faster than IC3 can reset (clear) the binary counter. Since IC3 is reinitiated on each incoming pulse, it cannot time out and reset the counter. As a result, whenever the frequency period is shorter than the reset time (~165 μsec) for at least 13 pulses, lock up occurs. The first pulse whose frequency is less than 6000 Hz (period 165 usec), allows IC3 to reset the counter; IC7 will immediately be able to respond to the incoming frequency pulses and produce a dc output which is proportional to frequency.

9. OBSERVING OUTPUT FOR OSCILLATIONS & CHECKING RIPPLE AT TP6

Vary oscillator frequency from 480 Hz to 10 K Hz and observe the output on the scope. The dc ripple or noise riding on the DC output should not exceed 10 MV p to p.

Vary frequency from 4.8 Hz up to 480 Hz and observe on the scope that the ac ripple does not exceed the values listed below.

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9. OBSERVING OUTPUT FOR OSCILLATIONS (continued)

FREQUENCY (Hz)	DC OUTPUT VOLTAGE (volts)	AC OUTPUT VOLTAGE (V p to p)	WAVE SHAPE
4.8	- .01	100 mV	
12	- .025	80 mV	
24	- .05	60 mV	
48	- .10	40 mV	
120	- .25	20 mV	
240	- .50	10 mV	
480	- 1.0	10 mV	

10. CHECKING OPERATION OF FLIP FLOP IC4, UNIJUNCTION TIMING CIRCUIT, AND LOCK UP TIME SETTING:

- Return oscillator frequency to 4800 Hz.
- Connect TP3 to scope external trigger input.
- Connect TP3 & TP5 to scope inputs. (outputs of FLIP FLOP IC4)
- Increase oscillator frequency to 6000 Hz, and observe that waveform at TP5 will dissappear before waveform at TP3 begins to skip (this condition occurs at the lock up frequency). At frequencies less than lock up, the waveform at TP3 will be the inverse of the waveform at TP5.

* NOTE: When lock up occurs at 6000 Hz, TP5 will be held LO (OFF), due to TP4 being held LO. However, FLIP FLOP IC4 (Pin 1) will continue to respond to incoming frequency pulses, and the unijunction will continue to time out and produce reset pulses back to IC4. As a result, pulses can be observed on the scope at TP3 and IC4 pin 5 even though TP5 is held off when LOCK UP occurs (Output voltage jumps to 13.3 volts). Also note that at LOCK UP, a duty factor of approx. 93.5% can be observed on the scope at TP3 as shown below:

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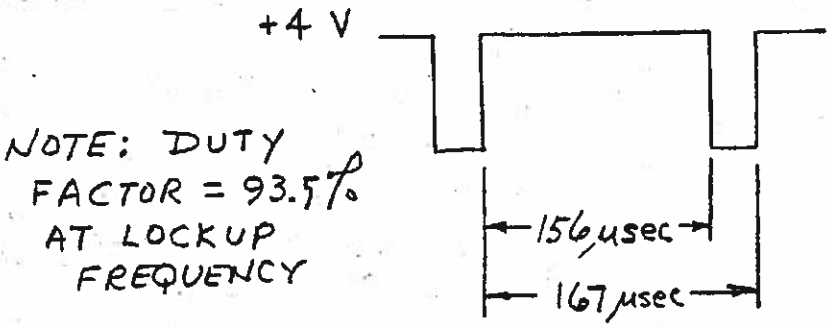
10. CHECKING OPERATION OF FLIP FLOP IC4, UNIJUNCTION TIMING CIRCUIT, AND LOCK UP TIME SETTING (continued):



NOTE: DUTY FACTOR = 93.5% AT LOCKUP FREQUENCY

FIG. 9 WAVEFORM AT TP3 (FREQ. = 6000 HZ)

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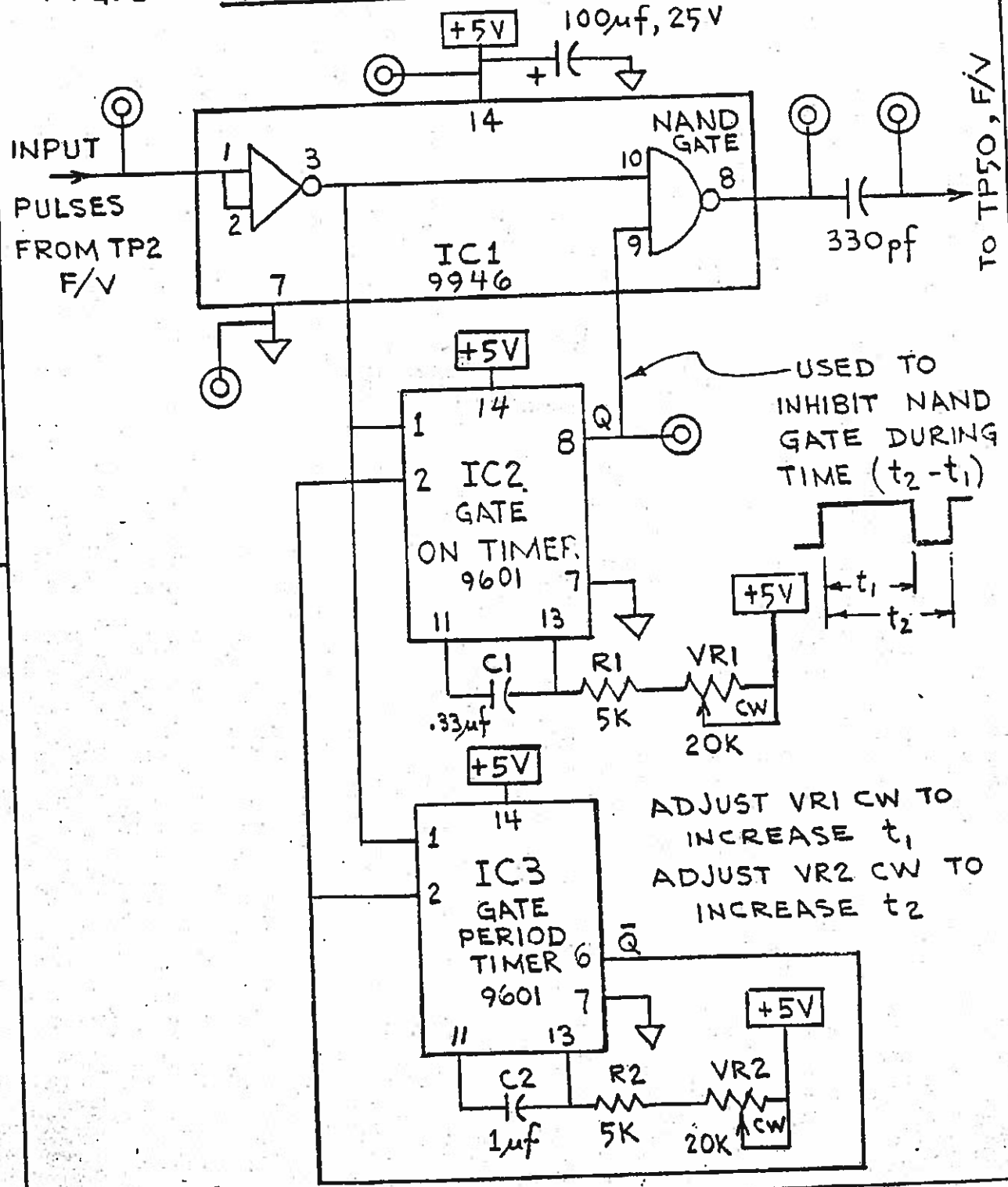
FIG. 10 F/V LOGIC "TEST UNIT" WITH ADJUSTABLE GATE



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~~11.~~ CHECKING LOCK UP CIRCUIT

Do not perform steps 11–14

TEST DESCRIPTION

The test which follows uses a separate digital TEST UNIT to inject additional pulses into the F/V converter and cause lock up to occur. The entire test which follows will be observed on the scope and is intended to functionally check out the lock up circuit for the following:

1. The ability of the One Shot (IC3) to detect input frequencies > 6000 Hz.
2. The ability of the binary counter to count exactly 13 pulses (frequency = 6000 Hz) and cause the output of IC5 (TP4) to change state from HI to LO, thus inhibiting the unijunction flip-flop output at TP5.
3. The ability of IC5 to inhibit the counter once 13 pulses have been registered.
4. The ability of IC3 to reset (clear) the counter and unlock the F/V, as soon as the input frequency drops below 6000 Hz.

In order to achieve a lock up condition, a minimum of 13 consecutive input pulses whose time period is shorter than the One Shot time, are required. Therefore in order to test this portion of the F/V, exactly 13 pulses whose period is shorter than the One Shot reset time (~ 165 µsec.) will be injected into the LOCK UP circuit. These pulses will be generated by summing 7 pulses from a separate TEST UNIT board along with 6 normal frequency pulses. The TEST UNIT pulses will be spaced midway between the frequency pulses (4800 Hz = 208 usec) as shown below:

NOTE:
INPUT FREQ. = 4800 HZ

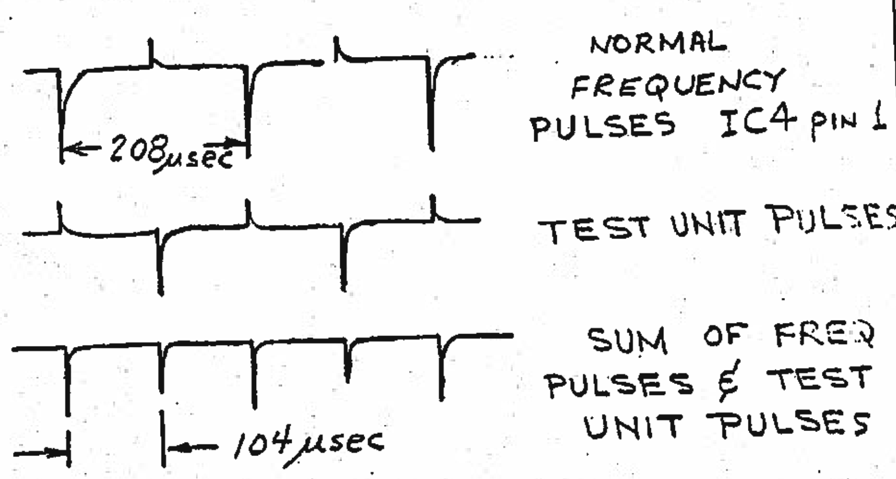

FIG.11 PULSE TRAIN TO LOCKUP CIRCUIT

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H. CHECKING LOCK UP CIRCUIT (continued)

TEST DESCRIPTION (continued)

The result of injecting 13 continuous pulses whose period is approx. 104 usec will prevent the One Shot from resetting the Binary Counter. Therefore the counter will count the 13 pulses and cause IC5 at TP4 to change state from HI to LO. This condition will cause the output at TP5 to also be held off. As a result, Q2 will be held off, CR4 will be held on (for a longer time than normal), and the F/V output voltage will jump up to a value greater than -10V (approx. -10.3V).

Since the next input frequency pulse (14th) will have a normal period of 208 usec, the One Shot will be able to reset (clear) the counter and unlock the F/V.

TEST UNIT

The digital TEST UNIT consists of 3 IC's. IC1 (946) is used to pass or inhibit noise pulses to the F/V. IC2 and IC3 (9601 ONE SHOTS) form an ADJUSTABLE GATE circuit which controls the number of pulses which are passed by IC1.

The adjustable gate circuit consists of a timing circuit (IC2) which controls the ON time (t1) and a second timing circuit (IC3) controls the PERIOD (t2) as shown below:

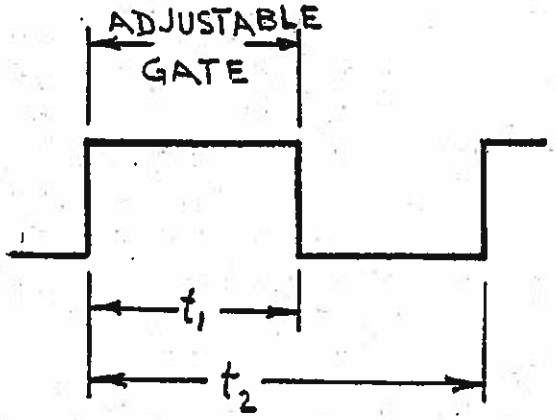

FIG. II A

ADJUSTABLE GATE USED TO INHIBIT NAND GATE

WHERE t1 is adjustable from .5ms to 2 ms
t2 is adjustable from 1.5ms to 6ms but is set at approximately 3ms.

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11. CHECKING LOCK UP CIRCUIT (continued)

TEST UNIT (continued)

Both ONE SHOT timers are triggered simultaneously on the falling edge of the input pulse to IC2 & IC3 (which is the leading edge of the input pulse to the TEST UNIT) and both IC's start timing. The output of the GATE ON timer (IC2 pin 8) will remain HI until IC2 times out (t1 is reached) and then held ON until IC3 times out (t2 is reached). Note that the output of the GATE PERIOD timer (IC3 pin 6) will remain LO inhibiting both timers from retriggering until time t2 is reached.

While the GATE ON timer output is HI, the input pulses to the TEST UNIT are passed thru IC1 into the F/V at TP50. When the output of the GATE ON timer is LO, IC1 is inhibited from passing any pulses into the F/V.

By adjusting GATE ON timer, TEST UNIT can produce from 2 to 9 output pulses. When the GATE is set to produce exactly 7 pulses, LOCK UP of F/V results for 1 pulse period. If 8 pulses are injected, LOCK UP occurs for 2 consecutive pulses, etc. LOCK UP should not occur for less than 7 pulses from the TEST UNIT.

NOTE: It will be necessary to observe good grounding practices as well as minimum lead lengths in order to prevent noise from falsely triggering the LOCK UP circuit during testing. If false triggering does occur, this condition can be observed on the scope and the test set up should be corrected

TEST SET UP

- Connect TEST UNIT as shown in Fig. 10 (use separate 5 VDC supply to power TEST UNIT).
- Set oscillator frequency into F/V at 4800 HZ.
- Check TEST UNIT PERIOD TIMER & adjust VR2 if necessary to obtain a 3 ms period (t2 = 3ms, measure at IC2, pin 8).
- Display following signals an four channel scope with time base set at 200 us/DIV.

  1. TEST UNIT GATE PULSE (IC2 pin 8), 5V/DIV
  2. TEST UNIT OUTPUT PULSES (IC1 pin 8), 5V/DIV
  3. F/V lock up at TP4, 5V/DIV
  4. F/V pulse train at TP5, 5V/DIV

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11. CHECKING LOCK UP CIRCUIT (continued)

TEST SET UP (continued)

- Connect scope EXTERNAL TRIGGER TO TEST UNIT GATE PULSE (IC2 pin 8).
- Adjust VR1 TEST UNIT GATE ON TIME so that 6 complete output pulses occur at IC1 pin 8.

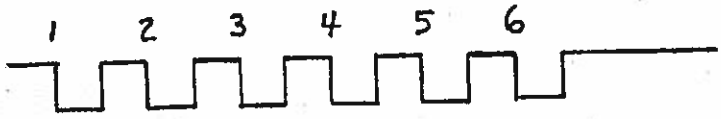

FIG. 11B "TEST UNIT" OUTPUT PULSES

NOTE: that 6 TEST UNIT output pulses will cause 12 differentiated pulses (whose frequency equals 9600 HZ) to occur at TP50 of F/V. Since LOCK UP requies 13 consecutive pulses whose frequency > 6000 HZ, LOCK UP SHOULD NOT occur and F/V output should remain at -10 VDC.

- See Fig. 12A for the four signal waveforms which will result when 6 TEST UNIT output pulses occur.
- Increase TEST UNIT GATE ON time (t1), by adjusting VR1 CW so that 7 output pulses occur at IC1 pin 8 as shown:

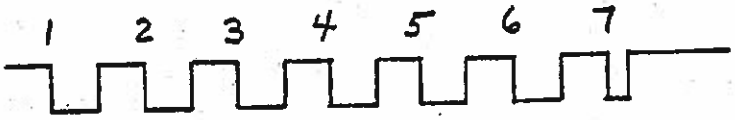

FIG. 11C "TEST UNIT" OUTPUT PULSES

NOTE that 7 TEST UNIT OUTPUT PULSES CAUSES exactly 13 differentiated pulses (frequency > 6000 HZ) to occur at the input to LOCK UP circuit (TP50 of F/V). As a result, LOCK UP occurs for only one cycle and one pulse dissappears from TP5 of F/V. Also note that dc output from F/V increases from -10.0 volts to approximately -10.30 when LOCK UP occurs at TP4 and one pulse dissappears from TP5.

- See Fig. 12B for the four signal waveforms which will result when 7 TEST UNIT output pulses cause LOCK UP to occur for 1 pulse.

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FIG. 12A SCOPE TRACES, NO LOCKUP

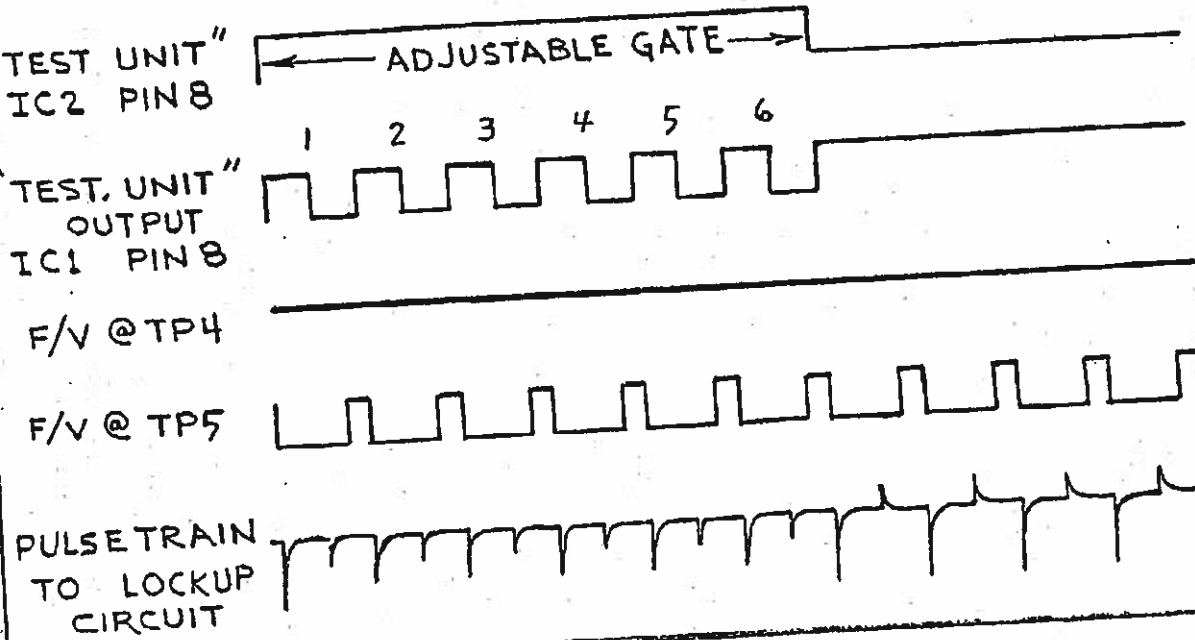
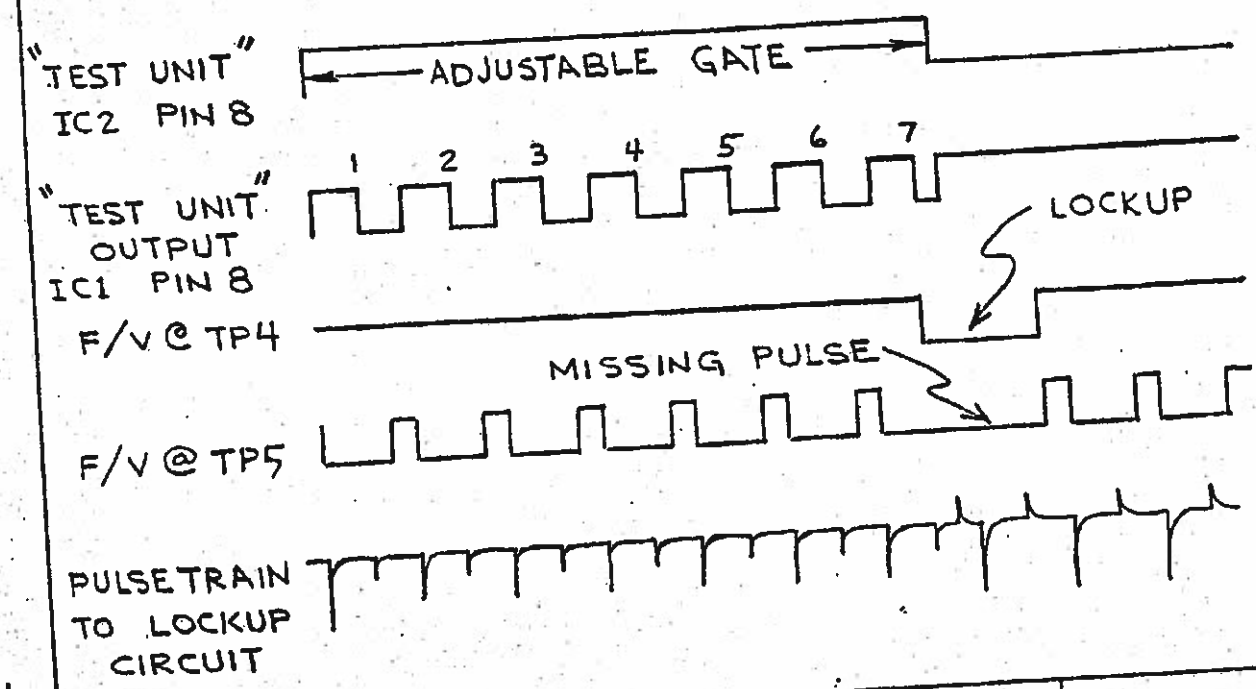


FIG. 12B SCOPE TRACES, LOCKUP OCCURS



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(12) CHECK ACTIVE FILTER FREQUENCY COMPENSATION NETWORK BY OBSERVING THE TIME RESPONSE TO A STEP INPUT.

- Switch the Input Frequency at TP1 from 0 HZ to 4800 HZ, and observe the change, in output voltage @ TP6. (Use a storage scope to capture the transient time response on the screen).
- Fig. 13 shows the waveshape, % overshoot, time to peak, and tolerances which must be observed.

*NOTE:

The above time response test is used to check the active filter characteristics (Damping Ratio = .507 & Undamped Natural Frequency = 76.7 RAD/SEC) when transistor Q2 is OFF and CR4 applies 9V to the input of the active filter amplifier IC7.

- Switch the input frequency at TP1 from 4800 HZ to 0 HZ, and observe the change in output voltage @ TP6 (Use a storage scope to capture the transient time response on the screen).
- Fig. 14 shows the waveshape, % Overshoot, Time to Peak, and Tolerances which must be observed.

*NOTE:

The above time response test is used to check the active filter characteristics (Damping Ratio = .689 and Undamped Natural Frequency = 76.7 RAD/SEC) when zero volts is applied to the input of the active filter amplifier IC7.

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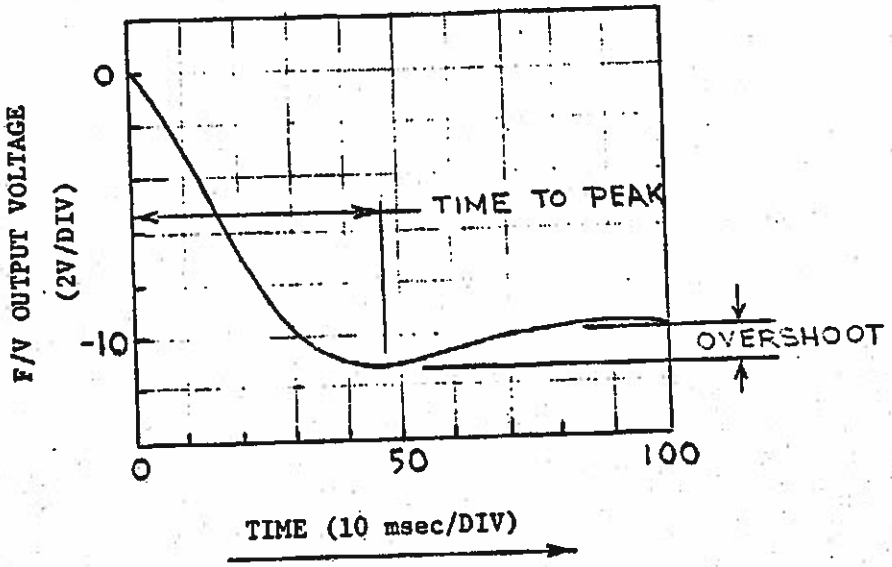
FIG. 13 F/V CONVERTER OUTPUT VOLTAGE TRANSIENT RESPONSE

FOR STEP CHANGE OF INPUT FREQUENCY FROM 0 HZ to 4800 HZ



NOTE:

UNDAMPED NATURAL FREQUENCY (ω_o) = 76.7 RAD/SEC.

DAMPING RATIO (ζ) = .507

MAX OVERSHOOT % = 15.7 ± 2.3%

MAX OUTPUT VOLTAGE = -11.57 ± 0.23 VDC @ 47.5 ± 1.5 msec

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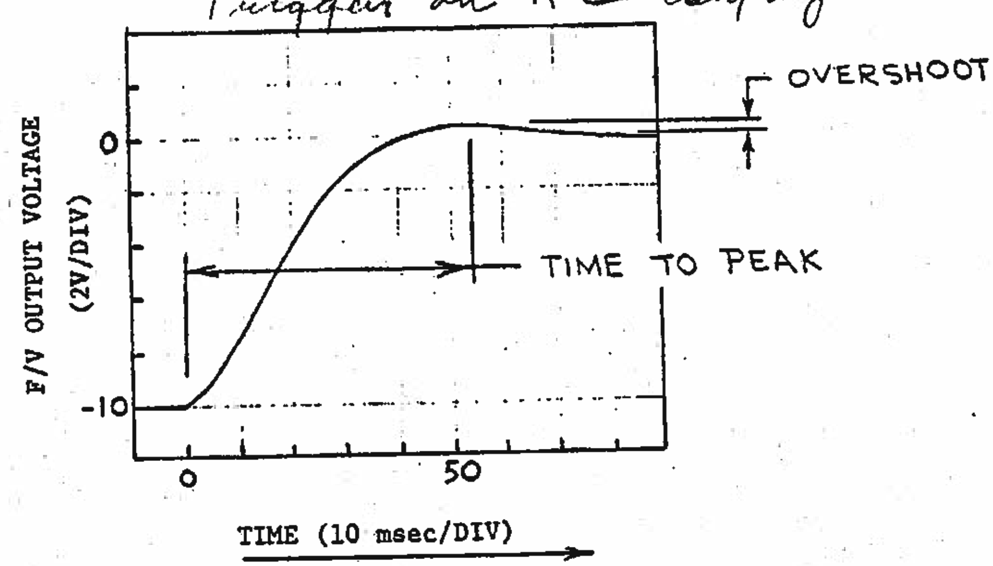
FIG. 14 F/V CONVERTER OUTPUT VOLTAGE
TRANSIENT RESPONSE

FOR STEP CHANGE OF INPUT FREQUENCY
FROM 4800 HZ to 0 HZ
Trigger on A C coupling



NOTE:

UNDAMPED NATURAL FREQUENCY (ω_o) = 76.7 RAD/SEC.

DAMPING RATIO (ζ) = .689

MAX OVERSHOOT % = 5.1 ± 1.8

MAX OUTPUT VOLTAGE = +0.51 ± 0.18 VDC @ 56.5 ± 4.5 msec

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MADE BY D.Mone Dec. 15, 1972
ISSUED
APPROVALS
Steam Turbine DIV OR DEPT.
Schenectady, N.Y. LOCATION

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13. CHECK FREQUENCY COMPENSATION NETWORK

~~Check IC1's input noise suppression lag filter specified in section III. A storage scope will be adequate for this check. Note that the output of the filter must be within 63% of the final valve in one time constant (1.3 usec).~~

14. CHECK UNIJUNCTION TIMING CAPACITOR

After all F/V board tests have been completed, apply Freon spray to the unijunction timing capacitor C6, and observe that the F/V output remains constant at -10.000 VDC (Input frequency = 4800 HZ). If the output goes to a new value, the capacitor must be replaced and the board rechecked and realigned.

END OF TEST

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IV. TEST INSTRUCTIONS

Test Instructions prepared by the EHC Test Engineer and approved by EHC Control Engineering.

APPROVED BY _____ DATE _____
EHC TEST ENGINEER

PREPARED BY _____ DATE _____
EHC CONTROL ENGINEER

APPROVED BY _____ DATE 10-2-72
EHC CONTROL ENGINEERING - MANAGER

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