GENERAL ELECTRIC

QUALITY STANDING INSTRUCTION

SPEED VARIATOR DEPARTMENT

QSI NUMBER #2081

TITLE

PREAMPLIFIER - 193X227BBG01 AND G02
193X227BCG01 AND G02

REVISION 3

1.0 Applicable Documents

1.1 Material List
1.2 Elementary diagram

2.0 Equipment

2.1 Test stand
2.2 Patchboard

3.0 Procedure (General)

3.1 Set V5 dial at (7.50) and lock
3.2 Set V5 polarity (+)
3.3 Set V5 range (10 volts)
3.4 Set scope CH1 & CH2 to 0.1V/Div, AC, and 5msec/div, line sync.
3.5 Turn card pots max. CCW and check shaft and label orientation per Figure #1.
3.6 Check polarized capacitors for correct polarity orientation per Figure #2.

Set up on BB G01 + BC G01

mode - CHOP

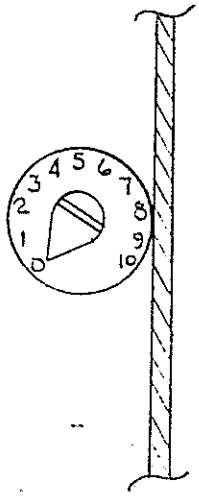

FIGURE NO. 1

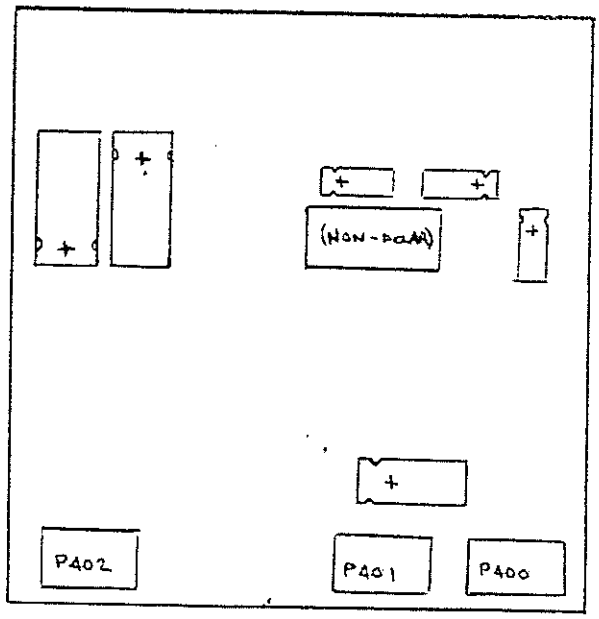

FIGURE NO. 2

DISTRIBUTION	QTY.
Mgr. Eng.	
Mgr. Mfg.	
Mgr.Prod.Eng.	
Mgr. Mat.	
Mgr.Sys.Eng.	
Eng. Supv.	
Foreman-Test	
Foreman-Insp.	

*Change or Addition

4.0

4.1 193X227BBG01 & 193X227BCG01 Test

4.1.1	Test on	DVM≤(±0.030) volts
4.1.2	RS1 (2) DMM TAB 28	DVM≤(-0.700) volts
4.1.3	RS1 (3) DMM TAB 16	DVM≤(+0.700) volts
4.1.4	S1 DN 7.5VDC TO TAB 30	DVM≤(+0.700) volts
4.1.5	RS1 (2) DMM TAB 28	DVM (+5.00) (+10.00) volts
* 4.1.6	S1 UP TAB 30 TO ½ P400 CW RS1 (1) DMM TAB 2 S1 ~~SC~~ DN TAB 30 TO 7.5V	DVM (-6.00) (-9.00) volts Scope CH1≤(0.2V P.P.) in 8-12 seconds
* 4.1.7	V5 Pol (-)	DVM (+6.00) (+9.00) volts Scope CH2≤(0.2V P.P.) in 16-24 seconds
4.1.8	P400 CCW RS1 (2) DMM TAB 28	DVM≤(-0.700) volts
4.1.9	RS1 (3) DMM TAB 16	DVM (-5.00) (-10.00) volts
4.1.10	S1 UP TAB 30 TO ½ RS1 (4) DMM TAB 25	DVM (+19.5) (+20.1) volts
4.1.11	S2 DN Remove GRN FROM TAB 27	DVM≤(+0.050) volts
4.1.12	End of test for production cards with FIXIT stamp. Continue for all others.	
4.1.13	S2 UP PUT GRND ON TAB 27 S3 DN +20V TAB 23 RS1 (3) DMM TAB 16	DVM (-0.312) (-0.468) volts
4.1.14	S3 UP Remove +20V FROM TAB 23 S4 DN -20V TO TAB 19 RS1 (2) DMM TAB 28	DVM (+0.312) (+.468) volts
4.1.15	S4 UP Remove -20V FROM TAB 19 S5 DN O-SCOPE CH2 TAB 5 S6 DN O-SCOPE CH1 TAB 9	Scope CH1≤(0.25V P.P.) Scope CH2≤(0.25V P.P.)
4.1.16	RS1 (5) DMM TAB 9	DVM (+3.76) (+5.64) volts
4.1.17	P402 (CW)	DVM reading should decrease slightly
4.1.18	RS1 (6) DMM TAB 5	DVM (-3.76) (-5.64) volts
4.1.19	P402 (CCW)	DVM reading should decrease slightly

ENSURE 6.3V RMS IS ON TAB 6+8

4.1.20	S5 UP S6 UP V5 (1 volt range) RS1 (2) RS2 (2)		DVM (+1.13) (+1.77) volts
4.1.21	RS2 (3)		DVM (+1.78) (+2.75) volts
4.1.22	RS2 (4)		DVM (+0.594) (+0.966) volts
4.1.23	RS1 (7)		DVM ≤(+0.010) volts
4.1.24	Turn P401 CW		DVM reading should momentarily increase and return to ≤(±0.010) volts
4.1.25	Turn P400 CW RS1 (1) RS2 (1) V5 (10V) range S1 DN		DVM time to (6.0) (9.0) volts in (8) (12) seconds
4.1.26	End of test		

* 4.2 193X227BBG02, BCG02 Test

4.2.1	Test ON	DVM	≤(±0.030) volts
4.2.2	RS1 (2) Adjust P402 for	DVM	(zero ±0.030) volts
4.2.3	RS1 (3)	DVM	≤(±0.030) volts
4.2.4	S9 DN	DVM	(-3.07) (-4.10) volts
4.2.5	V5 POL (-)	DVM	(+3.07) (+4.10) volts
4.2.6	S9 UP P400 CW RS1 (1) S1 DN	DVM	(+6.00) (+9.00) volts in 8-12 seconds
4.2.7	RS1 (2)	DVM	(-5.00) (-10.00) volts
4.2.8	RS1 (1) V5 POL (+)	DVM	(-6.00) (-9.00) volts in 16-24 seconds
4.2.9	RS1 (2)	DVM	(+5.00) (+10.00) volts
4.2.10	RS1 (4)	DVM	(+19.5) (+20.1) volts
4.2.11	S2 DN	DVM	≤(+0.050) votls
4.2.12	End of test for production cards with FIXIT stamp. Continue others.		

4.2.13 S2 UP connect 37 to ½
RS1 (7) DVM TAB 21 — DVM ≤ (+0.010) volts

4.2.14 Turn P401 CW — DVM reading should momentarily increase and return to ≤ (+0.010) volts .5V

Time 4.2.15 RS1 (1) DVM TAB 2
P400 CW ALREADY THERE
S1 UP 30 TO ½ (Remove from 31) — DVM time to zero in (8) (12) seconds

4.2.16 RS1 (2) DVM 28
S7 DN TAB 7 TO -20V — DVM (+0.950) (+1.430) volts 1.23V

4.2.17 S7 UP Remove TAB 7 from -20V
S8 DN TAB 8 TO -20V — DVM (+0.800) (+1.200) volts 1.042

4.2.18 V5 (1V range)
S8 UP Remove -20V
RS2 (2) +.75V TAB 15 — DVM (-1.32) (-2.06) volts -1.58

4.2.19 RS2 (3) +.75 TAB 14 — DVM (-1.71) (-2.65) volts -2.18

4.2.20 RS2 (4) +.75 TAB 12 — DVM (-0.562) (-0.918) volts -0.76

4.2.21 End of Test

5.0 Scope of Test

193X227BBG01, BCG01

5.1 Test steps 4.1.1 through 4.1.3 checks the linear time, plus driver, and minus driver outputs with the preamp. ref. at common potential.

5.2 Test steps 4.1.4 through 4.1.6 checks the linear time, plus driver and minus driver outputs with the preamp, ref. at +7.5 volts.

5.3 Test steps 4.1.7 through 4.1.9 checks the linear time, plus driver, and minus driver outputs with the preamp ref. at -7.5 volts.

5.4 Test steps 4.1.10 and 4.1.11 checks T400 collector voltage (Tab 25) with zero base current and 2 MA base current (Tab 27).

5.5 Test steps 4.1.13 and 4.1.14 checks R414 (Tab 19) and R419 (Tab 23) by connecting them to 20 volts and measuring the resultant voltages at the plus and minus driver outputs.

5.6 Test step 4.1.15 checks the ripple at tabs 5 and 9 with 6.3V RMS between tabs 6 and 8.

5.7 Test step 4.1.16 through 4.1.19 checks the DC voltage produced at tabs 5 and 9 with 6.3V RMS between tabs 6 and 8. The effect of P500 is al

5.8 Test step 4.1.20 through 4.1.22 checks the output at tab 28 as tabs 12, 14 and 15 are alternately connected to -0.75 volts.

5.9 Test step 4.1.23 and 4.1.24 checks the leakage of C407, C408 and the operation of the response pot by monitoring the voltage produced across a load resistor at tab 21.

5.10 Test step 4.1.25 checks the maximum timing settable with P400. A step input of 7.5 volts at tab 30 is used to produce the timed output as monitored at tab 2.

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5.11 Test step 4.2.1 checks the timing output (tab 2) with the preamp ref (tab 30) at common potential.

5.12 Test step 4.2.2 checks the output at tab 28 and adjusts P402 (zero adjust) for zero output.

5.13 Test steps 4.2.3 through 4.2.5 checks the output at tab 16 with zero, +7.5, and -7.5 volts at tab 13.

5.14 Test step 4.2.6 through 4.2.9 checks the timing output (tab 2) and the driver ref. (tab 28) with +7.5 and -7.5 volts input at the preamp ref. (tab 30).

5.15 Test step 4.2.10 and 4.2.11 checks T400 collector voltage (tab 25) with zero and 2MA base current (tab 27).

5.16 Test step 4.2.12 and 4.2.14 checks the leakage of C407 and C408 and the operation of the response pot by monitoring the voltage produced across a load resistor at tab 21.

5.17 Test step 4.2.15 checks the maximum timing settable with P400. The output at tab 2 is monitored as the input at tab 30 is stepped from 7,5 volts to zero.

5.18 Test steps 4.2.16 and 4.2.17 checks the output at tab 28 as tab 7 and tab 8 are alternately connected to -20 volts.

5.19 Test steps 4.2.18 through 4.2.20 checks the output at tab 28 as +0.75 volts is alternately connected to tabs 12, 14 and 15.

QSI NO. 2CB1
REV: #3
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(V5 SWITCH)
RS2

1	TAB 30 via 31
2	TAB 15
3	TAB 14
4	TAB 12
5	TAB 13

(DVM SWITCH)
RS1

1	TAB 2
2	TAB 28
3	TAB 16
4	TAB 25
5	TAB 9
6	TAB 5
7	TAB 21