

REVISIONS

ELEMENTARIES

IC3600TRLH1 SH. 3.0, 3.1

IC3600TRLJ1 SH. 3.0, 3.1

TEST EQUIPMENT

1. DIFFERENTIAL VOLTMETER 1%
2. OSCILLOSCOPE
3. DECADE RESISTOR BOX
4. TFCU AND TPSA CARDS
5. VARIAC 115V, 0.5 AMP
6. WAVETEK OSCILLATOR
7. SIMPSON VOLTMETER OR EQUIVALENT
8. MISC. PARTS PER FIG. 1
9. NOTE: SAME SET UP MAY BE USED FOR TESTING TRLA, TRLB, TRLC, TRLD, AND TRLH, AND TRLW

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PRINTS TO

GENERAL ELECTRIC

68A999325

CONT ON SHEET 3 SH NO. 2

REV NO. A

TITLE

REVERSING LOGIC TEST SPECIFICATIONS

68A999325

CONT ON SHEET 3

SH NO. 2

FIRST MADE FOR ICS800VRLM1, TRJ1

REVISION

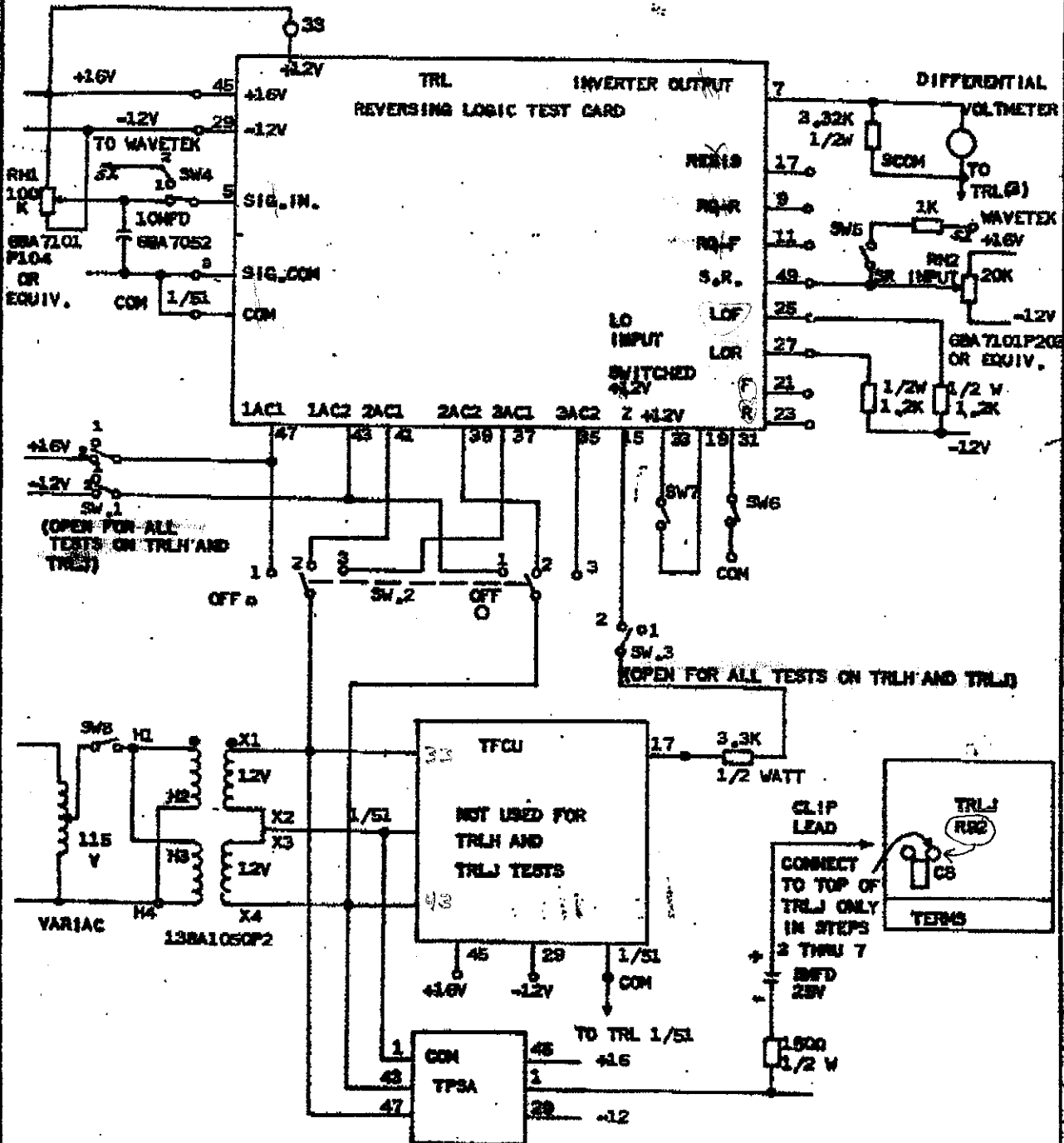


FIG. 1

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APPROVED

INDUSTRY CONTROL

SALEM, VIRGINIA

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LOCATION

CONT ON SHEET 3

SH NO. 2

COMPONENT

FF-803-WF (12-67)
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P.3/5

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REV
NO. A

TITLE

CONT ON SHEET 4 SH NO. 3

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REVERSING LOGIC
TEST SPECIFICATIONS

CONT ON SHEET 4 SH NO. 3

FIRST MADE FOR SCR EXCITERS (TRLH1)

REVISIONS

1. INVERTER -

A) INITIAL CONDITIONS:

SW ₁ - POS. 1 (OPEN)	SIG. INPUT - 0V	SW5 OPEN
2 - POS. 1 (PH.1)	S.R. INPUT - 0V	SW6 OPEN
3 - POS. 1 (OPEN)	VARIAC - 115V \pm 3V	SW7 OPEN
4 - POS. 1 (ON POT)		SW8 CLOSED

B) VARY RH1 TO VARY SIG. INPUT. INSURE THE FOLLOWING IS MET USING A DIFF. VTM.

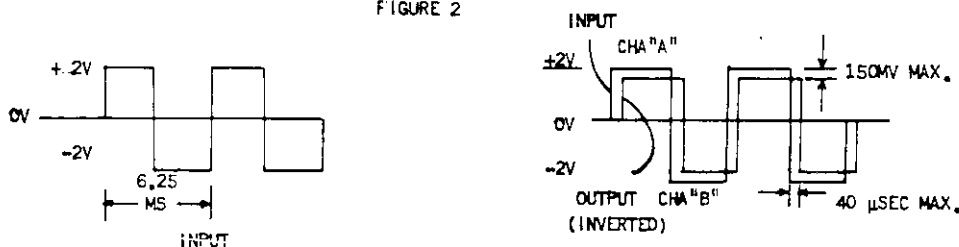
VSIG. IN. (5) INVERT. OUT (7)

+2 \pm .01V	-2 \pm .1V
0 \pm .01V	0 \pm .04V
-1 \pm .01V	+ .93 \pm .05

RETURN INPUT TO ZERO

- C) PUT SW₄ TO POS. 2. APPLY A 160 HZ \pm 4V SQUARE WAVE TO THE SIGNAL INPUT. (PIN 5). OBSERVE THE INVERTER OUTPUT AND INPUT ON AN OSCILLOSCOPE. USE EXT. SYNC. FROM WAVETEK WITH RESPECT TO 1/517. THE OUTPUT MAGNITUDE SHOULD FOLLOW THE INPUT TO WITHIN 150 MV AND THE WAVEFORM SHOULD LAG LESS THAN 40 μ SEC. SEE FIGURE 2.

FIGURE 2



INPUT AND OUTPUT

(NOTE: TRY TO NOT CHANGE WAVETEK OR SCOPE SYNC. AS THEY WILL BE USED IN STEPS 3 AND 4)

2. TRIGGER -

A. INITIAL CONDITIONS (SAME AS FOR STEP 1)

SW ₁ POS. 1 (OPEN)	SIG. INPUT - 0V	SW5 OPEN
2 POS. 1 (PH.1)	S.R. INPUT - 0V	SW6 OPEN
3 POS. 1 (OPEN)	VARIAC - 115V \pm 3V	SW7 OPEN
4 POS. 1 (ON POT)		SW8 CLOSED

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LOCATION

CONT ON SHEET 4

SH NO.

3

REV
NO. A

TITLE

CONT ON SHEET 5

SH NO. 4

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REVERSING LOGIC
TEST SPECIFICATIONS

CONT ON SHEET 5

SH NO. 4

FIRST MADE FOR SCR EXCITERS

(SW4 Down)

- B) MONITOR TRL PINS 9 AND 11, AND SIG. INPUT WITH SIMPSON METERS OR OSCILLOSCOPE WITH RESPECT TO 1/51. INITIALLY PIN 9 SHOULD BE AT +12V AND PIN 11 AT 0V. (IF THIS IS NOT THE CASE MAKING THE INPUT +1V SHOULD CHANGE THEIR STATES) THE FOLLOWING CHART OUTLINES THE STEPS TO BE PERFORMED.

V SIG. INPUT	VP9 (APPROX.)	VP11 (APPROX.)
0 TO -200 ± 50 MV	12V	0V
-200 ± 50 MV TO $-3V$	0V	8V
$-3V$ TO $+200 \pm 50$ MV	0V	8V
$+200 \pm 50$ MV TO $+3V$	12V	0V

THE INPUT SIGNAL WILL HAVE TO BE VARIED SLOWLY AND CAREFULLY TO DETERMINE THE LEVEL AT WHICH THE 9 AND 11 VOLTAGES CHANGE.
IF THE TRIP POINTS DO NOT FALL WITHIN TOLERANCE, CHANGE R40 POT.
IF THE TRIP POINTS ARE LOW (NEGATIVE), DECREASE OHMS (CW); IF THE TRIP POINTS ARE HIGH, INCREASE OHMS (CW).
SEAL POT WITH RTV AFTER ADJUSTING.

3. TRIGGER DELAY, OVERLAP OF LOCKOUTS, AND EXTERNAL LOCKOUT

A) INITIAL CONDITIONS

SW.1 - POS 1 (OPEN)	SW.5 OPEN	SIG INPUT - 0V
SW.2 - POS 1 (PH. 1)	SW.6 OPEN	SR INPUT - 0V
SW.3 - POS 1 (OPEN)	SW.7 OPEN	VARIAC - $115V \pm 3V$
SW.4 - POS 2 (WAVETEX)	SW.8 CLOSED	

- B) WAVETEX $\pm 2V$ SQUARE WAVE 20 Hz
SCOPE 5 MS/DIV, EXTERNAL SYNC ON WAVETEX
CHANNEL A ON WAVETEX - CHANNEL B ON TERM 25 OR TP4 (LOF)
C) CONNECT 5 MFD TO R92 ON TRLJ (SEE FIG. 1)
D) CHECK WAVE SHAPES PER FIG. 3 (TWO UPPER TRACES)

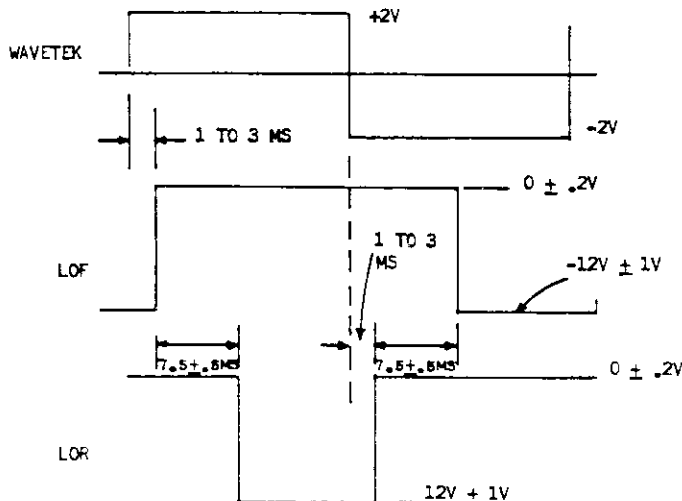


FIG. 3

REVISIONS

M. L. 11-16-70

J. L. 11-16-70

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LOCATION

CONT ON SHEET 5

SH NO. 4

REV NO. 68A999325 CONT ON SHEET 6 SH NO. 5	TITLE <h2 style="text-align: center;">REVERSING LOGIC TEST SPECIFICATIONS</h2> FIRST MADE FOR SCR EXCITERS
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REVISIONS

- E. MOVE CHANNEL B TO TERM 27 OR TP7 (LOR) AND CHECK TOP AND BOTTOM TRACES OF FIG. 3.
 - F. MOVE CHANNEL A TO TERM 25 OR TP4 (LOF) AND CHECK ONLY THAT BOTH TRACES ARE UP FOR THE 7.5 MS TIMES IN FIG. 3.
 - G. CLOSE SW6 AND BOTH LOCKOUTS OF FIG. 3 REMAIN IN UP (OR ZERO) STATE.
 - H. OPEN SW6.
4. OPERATION OF LOCKOUTS WITH AC VOLTAGE
- A. INITIAL CONDITIONS - SAME AS AT END OF STEP 3
 - B. CHANGE SCOPE TO .1 SEC/CM AND WAVETEX FREQUENCY TO ONE HZ. OPEN SW8 TO SHUT OFF AC. SCOPE SHOULD STILL BE TRIGGERING FROM WAVETEX.
 - C. CLOSE SW8 WHILE SCOPE TRACE IS ON LEFT SIDE OF SCREEN. REPEAT SEVERAL TIMES TO CHECK FIGURES IN FIG. 4.

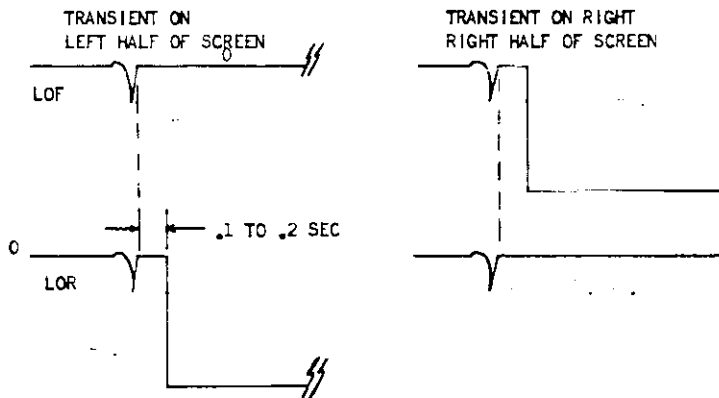


FIG. 4

- D. REPEAT WHILE TRACE ON RIGHT HALF OF SCREEN CHECKING FIG. 4.
- E. CLOSE SW8 AND SW7 AND START REDUCING AC VOLTAGE ON VARIAC. THE TRACES OF THE LOCKOUTS (FIG 3) WILL SLOWLY SHRINK AS THE BUS VOLTAGE DECREASES, BUT AT SOME POINT THE CURVES START SWITCHING ERRATICALLY TO ZERO. THIS MUST OCCUR AT AN AC RMS VOLTAGE UNDER 70 VOLTS.
- F. REDUCING AC FURTHER WILL CAUSE LOCKOUTS TO STAY AT ZERO. THIS MUST OCCUR ABOVE 45V. RMS.
- H. RETURN VARIAC TO 115V, OPEN SW7,

1 BAB 9/5/72
2 RBA 3-27-13

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REV. NO. 6 8 A 9 9 9 3 2 5
CONT ON SHEET 7 SH NO. 6

TITLE
REVERSING LOGIC
TEST SPECIFICATIONS
FIRST MADE FOR SCR EXCITERS

REVISIONS

5. FLIP FLOP MEMORY

A. INITIAL CONDITIONS (SAME AS AFTER STEP 4 H)

SW. 1 - POS 1 (OPEN) SW. 5 OPEN RH1 SIG INPUT OV (5)
SW. 2 - POS 1 (PH. 1) SW. 6 OPEN RH2 SR INPUT OV (49)
SW. 3 - POS 1 (OPEN) SW. 7 OPEN VARIAC - 115V \pm 3V
SW. 4 - POS 2 (WAVETEK) SW. 8 CLOSED
CONN. SMFD CAP TO R92 ON TRJ (SEE FIG. 1)

B. WAVETEK 20 HZ \pm 1V SQUARE WAVE

SCOPE 5 MS/DIV, EXTERNAL SYNCH ON WAVETEK
CHANNEL A ON 21 (F), CHANNEL B ON 23 (R)
CHECK VOLTAGES PER FIG. 5.

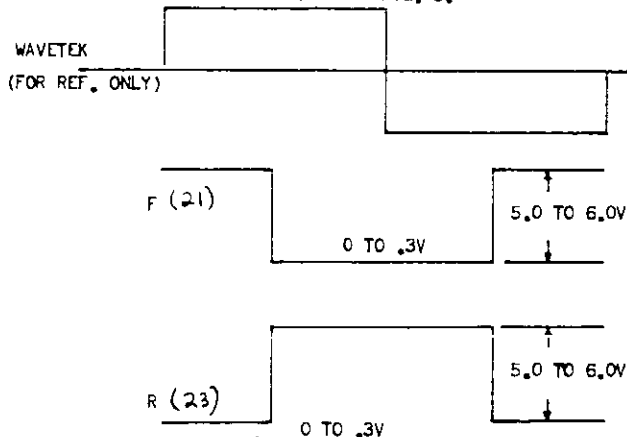


FIGURE 5

C. TURN SR VOLTS NEGATIVE TO -12V BUS. F AND R WILL STOP FLIPPING AND ASSUME F STAYS ZERO AND R, 6V.

D. SLOWLY REDUCE VARIAC UNTIL R ERRATICALLY GOES TO ZERO (OR -.5V) DUE TO ELECTRONIC SWITCH (Q7) OPENING. THIS MUST OCCUR BELOW 70 VRMS AC INPUT.

E. REDUCE VARIAC UNTIL R STAYS ZERO WHICH MUST OCCUR ABOVE 55V RMS.

F. SET AC VOLTS BETWEEN D AND E AND WATCH F FOR 3 SECONDS. F MUST NEVER GO ABOVE +.5V (FF ALWAYS COMES BACK TO SAME STATE).

G. AC VOLTS BACK TO 115V. TURN SR VOLTS FROM 0 TO -12V UNTIL FF STAYS IN OPPOSITE STATE FROM C. REPEAT D, E, AND F FOR THIS STATE OF FF.

H. AC VOLTS BACK TO 115V. SR VOLTS TO ZERO.

J. CLOSE SW7. REDUCE AC VOLTAGE UNTIL F AND R (FIG. 5) STOP SWITCHING. A AC VOLTS TO BE ABOVE 45V. OPEN SW7. RETURN AC TO 115V \pm 3V.

6. FF SET CIRCUITS (TROUBLE SHOOTING ONLY: OMIT IF STOP 5 IS OK)

A. INITIAL CONDITIONS AS AT END OF STEP 5

B. SCOPE PICTURE IS LIKE FIG. 5.

C. MOVE CHANNEL A TO TP5 AND 1V/DIV.

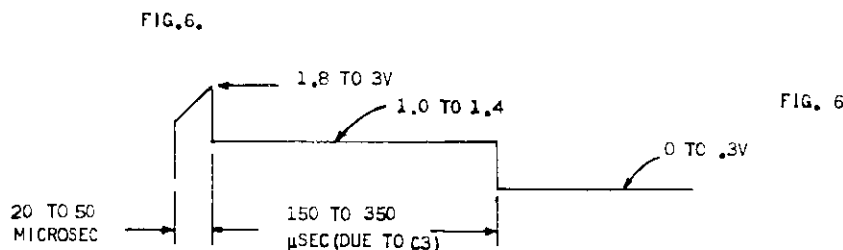
D. SHOULD SEE TWO FAINT LINES LINING UP WITH TRANSITIONS OF R. CHANGE SCOPE TO INTERNAL POSITIVE TRIGGER IN CHANNEL A, 50 MICROSEC/DIV AND CHECK PER

1 BAB 9/5/72
2 RBA 3-29-73
3) 8/10/86 JMT

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MADE BY RG MUCKENFUSS	APPROVALS <i>[Signature]</i>	INDUSTRY CONTROL SALEM, VIRGINIA	DIV OR DEPT. LOCATION	6 8 A 9 9 9 3 2 5 CONT ON SHEET 7 SH NO. 6
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REV. NO. A 6 8 A 9 9 9 3 2 5 CONT ON SHEET 8 SH NO. 7	TITLE <p style="text-align: center;">REVERSING LOGIC TEST SPECIFICATIONS FIRST MADE FOR SCR EXCITERS</p>
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7. COMPARATOR AND C6 TIME DELAY

A. INITIAL CONDITIONS

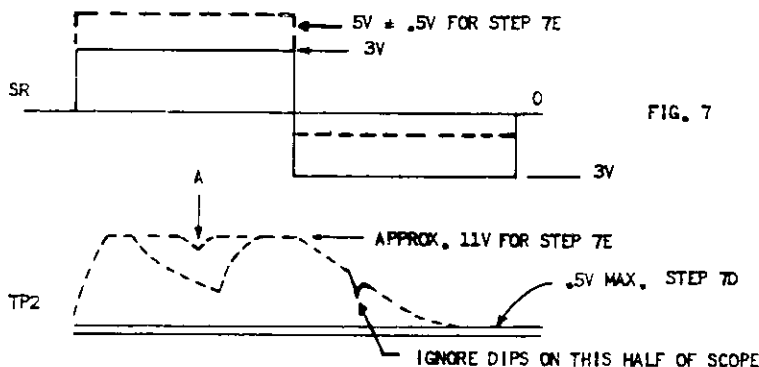
SW1 - POS 1 (OPEN)	SW5 - CLOSED (WAVETEK)	SIG INPUT OV
SW2 - POS 1 (PH.1)	SW6 - OPEN	SR INPUT OV
SW3 - POS 1 (OPEN)	SW7 - OPEN	VARIAC 115V \pm 3V
SW4 - POS 1 (ON POT)	SW8 - CLOSED	

B. SCOPE CHANNEL A ON 49 (SR INPUT) (2V/DIV) } MUST BE ON DC
 SCOPE CHANNEL B ON TP2 (OGO) (5V/DIV) }
 SET WAVETEK FOR 6V PP, 50. HZ SQUARE WAVE AT 49.
 EXTERNAL TRIGGER ON WAVETEK (USE AC COUPLING AS LEVEL WILL CHANGE DURING TEST)
 2 MS/CM

ON TRIGGER ONLY, NOT ON CHANNELS

C. SHORT 21 TO 23 TO 1

D1. CHECK PICTURE PER FIG. 7. TP2 MUST STAY UNDER .5 VOLTS. (SOLID CURVE)



D2. CHANGE SWITCH 2 TO POSITIONS 2, THEN 3. TP2 (FIG. 7) REMAINS UNDER .5V IF ALL INPUT DIODES ARE OK. (OMIT ON TRLH)

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2) 8 MAY 86 JMT

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1 BAB 9/5/72

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REV
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CONT ON SHEET FL.

SH NO. 8

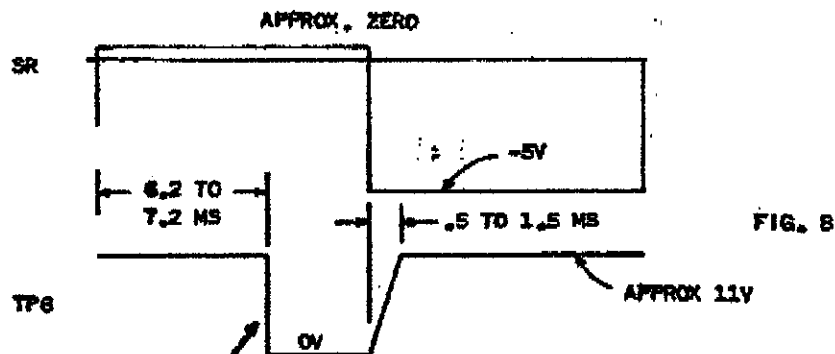
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CONT ON SHEET FL. SH NO. 8

FIRST MADE FOR SCR EXCITERS

REVISION

- (RH2)
E. TURN SR POT IN POSITIVE DIRECTION. TP2 WILL START GOING TO +11V AS SHOWN IN DOTTED CURVE OF FIG. 7. CONTINUE TURNING UNTIL TP2 HAS NO DIP IN THE MIDDLE OF THE LEFT HALF OF SCREEN (AT A). AT THIS POINT SR MUST BE $+6V \pm .5V$. *PEAK WAVEFORM WILL MOVE UP 5V ON SCOPE*
(RH2)
F. TURN SR POT NEGATIVE, TP2 WILL HAVE THE SAME DOTTED WAVESHAPE AS 7 EXCEPT ON RIGHT HALF OF SCREEN. AS MIDDLE DIP DISAPPEARS SR MUST BE $-6V \pm .5V$. *PEAK WAVEFORM OF (19) WILL MOVE DOWN 5V ON SCOPE*
G. TURN SR POT UNTIL CHANNEL A IS $-6V$ AND CHANGE CHANNEL B TO TP6. CHECK TIME PER FIG. 8.



IF THIS CURVE MOVES WITH RESPECT TO THE TOP CURVE, INCREASE WAVETEK VOLTS UNTIL IT "LOCKS IN".

- H. REMOVE 21 TO 23 TO 1 JUMPERS.

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CONT ON SHEET FL.

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