TITLE

INTERCEPT VALVE AMPLIFIER CIRCUIT BOARD TEST (PWR)

FIRST MADE FOR 117D7331 G-1, 2, 3, 4

REVISIONS

1 D.DeNora AUG 20 1974 Added G2 3 4 (1H)

GENERAL DESCRIPTION

This board sums the speed error signal, the load reference signal, the valve opening bias signal, to produce a d-c signal at the output for the intercept valve position loops. Zero volts or less drives the valves to the closed position; +5 volts call for the valves to go wide open. A biasing network limits the output to +5 volts if a higher voltage is called for, and drives the output negative (via contact KT101 opening) on an emergency trip. The transistor circuit is used only for current amplification - the base to emitter drop may be neglected.

The intercept valves will be biased full open (+5 volts output) during start-up and loading, by -5 volts at TP6.

If an overspeed occurs, the resulting speed error will act to cancel the bias voltages and load reference signal. The intercept valves have a regulation of 2%; therefore, the speed error resulting from a 2% overspeed will cancel 5 volts at the output. At 40% load (load reference of -2 volts), the intercept valves will start to close at 102% of rated speed, and will be fully closed (0 volts output) at 104%. At 100% load, (load reference -5 volts, 5% control valve regulation) the intercept valves will start to close at 5% overspeed, and will be fully closed at 107% of rated speed. The overspeed required to start the intercept valves closing is due to the fact that more than 5 volts must be cancelled at the output.

ACTIVE FOR ____ BY ____ DATE ____

ET-273
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273-71

PRINTS TO

TITLE

INTERCEPT VALVE AMPLIFIER CIRCUIT BOARD TEST (PWR)

FIRST MADE FOR 117D7331 G-1, 2, 3, 4

REVISIONS

1 D. Mac AUG 20 1974 Added C2, 3 4/1H

Input voltage should be set to ± 10 MVDC, output voltages should be read within ± 100 MVDC of stated values, unless specified otherwise.

1. Close S1, S2. Set speed error to 0.0 volts.
2. Set load reference to 0.0 volts.
3. Adjust R5 for -5.0 volts at TP6.
4. Set 5K pot fully CW. Set 50K pot fully CCW.
5. Set +2.5 volts on the speed error input and -5.0 volts on the load reference input.
6. Adjust the 50K pot until the output is +5.0 volts. Note the number of turns moved from the max CCW position.
7. Increase the speed error input to +3.5 VDC. The voltage at TP8 should be 0.0 volts.
8. Set speed error to -5.0 volts.
9. Adjust 5K pot until output at TP8 is +5.0 volts.
10. Open S2. The voltage at TP8 should be (-) 12.5 ± 1.0 VDC.
11. Close S2. Set speed error to 0.0 volts.

FAILURES: Any values that are not obtained, or any adjustments that cannot be reached is condition for rejection and Control Engineering should be notified.

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PRINTS TO

GENERAL ELECTRIC

P3-AL-0160-A01

CONT ON SHEET 4 SH NO. 3

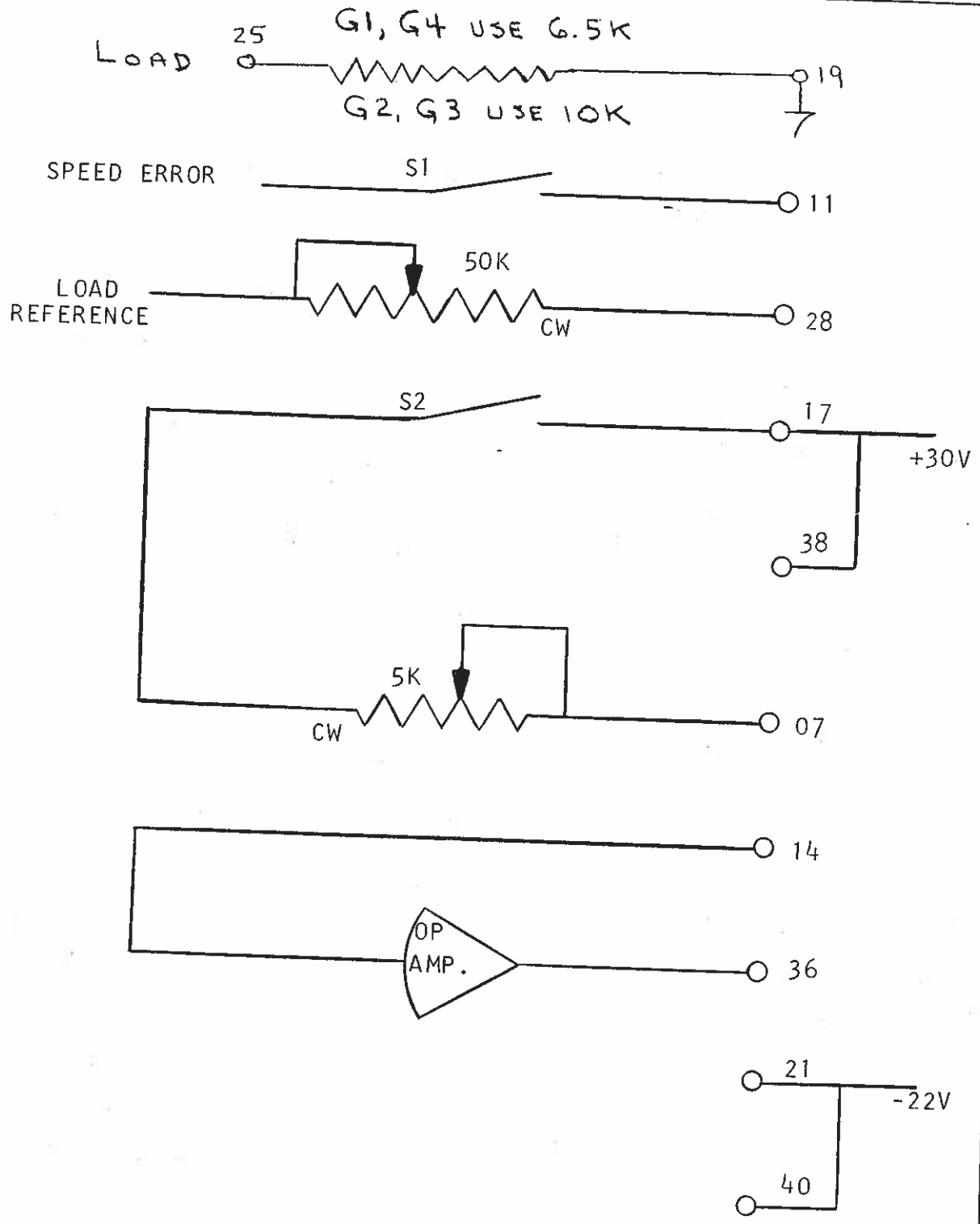
REV NO. 01

CONT ON SHEET SH NO.

TITLE

INTERCEPT VALVE AMPLIFIER CIRCUIT BOARD TEST

FIRST MADE FOR TB (EHC) 117D7331-G1, 2, 3, 4



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PRINTS

MADE BY D.DeNora Feb. 29, 1972

ISSUED MAR 1 1972

APPROVALS 2/17/72

TURBINE DIV OR DEPT.

SCHENECTADY LOCATION

P3-AL-0160-A01

CONT ON SHEET 3

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TB-G6

GENERAL ELECTRIC

P3K-AL-0160-A01

CONT ON SHEET --- SH NO. 4

REV. NO. 1

P3K-AL-0160-A01

CONT ON SHEET --- SH NO. 4

TITLE

INTERCEPT VALVE AMPLIFIER CIRCUIT BOARD TEST (PWR)

FIRST MADE FOR 117D7331 G-1, 2, 3, 4

REVISIONS

1 D.Y.Ch. AUG 20 1974 Add-1 (G2 34/Ht)

PREPARED BY M.J. Sindoni DATE Feb 17, 1972

M.J. Sindoni
EHC DESIGN ENGINEERING

APPROVED BY R. Dellorfano DATE [illegible]

R. Dellorfano
EHC TEST ENGINEER

APPROVED BY P.C. Callan DATE 2-24-72

P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

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PRINTS TO

MADE BY D.DeNora Feb. 29, 1972

ISSUED MAR 1 1972

APPROVALS

Steam Turbine DIV OR DEPT.

Schenectady, N.Y. LOCATION

P3K-AL-0160-A01

CONT ON SHEET --- SH NO. 4

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