

Lot# _____
PO# _____

ASSEMBLY DRAWING
4136J54G01

PC BOARD DRAWING
4136J34-2

SERIAL # _____
DATE TESTED _____
TESTER _____

SCHEMATIC DRAWING
4136J23

TEST KIT
Universal Test Kit

1.0 INSPECTION

- 1.1 IDENTIFICATION _____ 1.2 COMP./ CONN. _____
- 1.3 SOLDER/WIRE _____ 1.4 TEMP CYCLE _____
- 1.5 KEY SLOT _____ 1.6 _____
- 1.7 _____

REMARKS:

changes made 1/22/88 mlt

check for jumpers at CR1 & CR2

2.0 PREPARATION

2.1 CONNECT PER FIGURE 1.

(use watch dog probe)

3.0 CHECKOUT

A02 Row 7 use 2 white jacks
on end of box

* 1 (REFERENCE SCHEMATIC 4136J23 FOR THIS STEP).

SET OSCILLATOR FOR .1 VRMS SINE WAVE, 4160 HZ. ADD C3, C4, C5, AND C10
AS NECESSARY TO CAUSE THE AC VOLTAGE AT TP2 TO PEAK (AROUND .06 VRMS)

3.2 SET OSCILLATOR AT 2000 HZ, 1 VRMS.

CONNECT PIN 32 TO -5.5 VDC.

WHILE PUSHING RST MOMENTARILY,

TP1 SHOULD READ +24 VDC.

TP3 SHOULD READ -2 TO -6 VDC.

TP5 SHOULD READ APPROXIMATELY +14 VDC.

PIN 40 SHOULD READ LESS THAN 0.4 VDC.

voltage will peak and fall
could be higher! *off peak*

3.3 SET THE OSCILLATOR TO 0 VRMS.

TP5 SHOULD READ +14.00 VDC.

PIN 40 SHOULD READ LESS THAN 0.4 VDC

3.4 CONNECT PIN 32 TO VARIABLE DC SOURCE AND APPLY BETWEEN -6.1 V AND -7.6 VDC

TP5 WILL GO TO -13.30 AND PIN 40 WILL GO TO +24.00 DC.

REMOVE VARIABLE DC SOURCE

mlt
3/2/88

3.5 SET OSCILLATOR AT 3600 HZ, 1.40 VRMS.

USING A COUNTER AND RST PB AS NECESSARY, RAISE THE OSCILLATOR FREQUENCY
AND VERIFY THAT TP1 DROPS TO 0 VDC AT 4060 ± 10 HZ.

3.6 VARY OSCILLATOR OUTPUT LEVEL FROM 1.2 VRMS TO 1.6 VRMS WHILE REPEATING STEP 5. DROP POINT SHOULD NOT VARY BY MORE THAN ± 30 HZ.

* use decade cap. box. do thru entire test then
select C3, C4, C5, C10 as required to match cap. of
Box.

LPL
12/23/92



PERFORMANCE REQUIREMENTS

SIGNATURES		DATE	REV
DRAMA		A 01289	1284J68
ISSUED			SH X 2

2X HS