1.0 SCOPE

The following covers the performance capabilities and the test instructions for the 193X475AAG01 Phase Logic Card. This card is designed to be a standard part of the AF-400X Inverter, and performs the following functions:

1.01 Generates a three-phase fundamental frequency in a forward ABC or reverse ACB phase sequence from a six times fundamental input frequency.

1.02 Provides steering logic which allows firing of each SCR only during its proper time within the three-phase sequence. This effectively causes the input commutation pulses, initial pulses and inverter pulse train to be steered only to the proper SCR's dependent of the three-phase sequence.

1.03 Provides amplified output firing signals from a delayed firing supply to fire six commutation SCR's, three auxiliary commutation charging SCR's and six main inverter SCR's.

1.04 Produces the proper SCR firing order to start and stop the inverter.

1.05 Provides the means to lock out all the normal SCR firing signals, but allows the firing of the main inverter SCR's from a separate input, after an inverter fault has occurred.

2.0 PERFORMANCE CAPABILITIES

All cards shall be capable of the following performance while exposed to the conditions of section 4.0. In these specifications, a "high" logic state refers to 12 to 13 volts and a "low" logic state refers to 0 to 1 volt when 20 volts control power is applied to the card. Only tabs 4, 28 & 31 should have a high input of +20V rather than +13V.

2.01 Inputs/Outputs

Tabs	Nomen.	Description
1	(+20V)	+20V power supply input
2	(COM)	Signal common input
3	(MR)	Minimum reference logic input
4	(REV)	Reverse phase sequence logic input
5	(ACN)	SCR firing signal outputs, ph.A, comm neg.
6	(ACP)	" Ph.A, comm pos.
7	(AA)	" ph.A, auxiliary
8	(AIN)	" ph.A, inv. neg.
9	(AIP)	" ph.A, inv. pos.
10	(BCN)	" ph.B, comm neg.
11	(BCP)	" ph.B, comm pos.
12	(CCN)	" ph.C, comm neg.
13	(CCP)	" ph.C, comm pos.
14	(CA)	" ph.C, auxiliary
15	CIP)	" ph.C, inv. pos.
16	(CIN)	" ph.C, inv. neg.
17	(BIP)	" ph.B, inv. pos.
18	(BIN)	" ph.B, inv. neg.
19	(BA)	" ph.B, auxiliary
20	(IFP)	Inverter fault pulse input
22	(IFL)	Inverter fault lockout input

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Tabs	Nomen	Description
23	(CP)	Commutation pulse input
24	(IP)	Initial pulse input
25	(TR)	Pulse train input
26	(RFC)	Reference clamp output
28	(DFS)	Delayed firing supply power input
29	(IBL)	Inverter blanking input
31	(RI)	Inverter run logic input
32	(IPA)	Inverter phase A square wave output

2.01.1 Tabs 3,4,20,22,23,24,25,29 & 31 are logic inputs. Logic sources connected to these tabs must be capable of sinking 1.0ma during their low logic state.

2.01.2 Tabs 26 & 32 are logic outputs, capable of sinking 8ma in the low logic state. Tab 32 can source 1ma in its high logic state.

2.01.3 Tab 28 is the firing signal voltage supply input. Tabs 5 thru 19 are the SCR firing signal outputs and are each capable of delivering pulses of 20ma at more than 12V in the high state, and of accepting 10ma at 2 volts in the low state.

2.02 Three Phase Generation - Tab 20 is connected high to +12V. Tabs 28 & 31 are connected high to +20V and tabs 22 and 27 are connected low to common. A 6 times fundamental frequency pulse train, of the form shown in Figure 1, is connected to tab 29.

If tabs 23, 24 & 25 are all connected to a high frequency pulse train, the firing signal outputs at tabs 5 through 19 will inhibit waveshapes as shown in Figure 1. The main inverter firing outputs, tabs 8 & 9 for phase A, tabs 18 & 17 for phase B and tabs 16 & 15 for phase C will exhibit the three phase waveshapes shown in Figure 1. Each succeeding phase will follow the preceeding phase by 120 electrical degrees, with the positive and negative half cycles being 180° out of phase. The gaps between the pulse train portions of the positive and negative half cycles is equivalent to the width of the high portions of the IBL pulse train & represent the commutation time of the Inverter.

Tab 32 provides a phase A signal which goes high at the same time as the firing output signal at tab 9, but does not go low until tab 8 goes high. This produces a full 180° signal irrespective of the commutation interval.

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2.03 Steering Logic

The pulse train portions of the waveshapes shown in Figure 1 indicate the periods of the three phase sequence during which each output tab is allowed to produce a firing signal (high state). This is illustrated by connecting the commutation pulse input tab 23, the initial pulse input tab 24 and the inverter pulse train tab 25 all to a high frequency pulse train, as was done in Section 2.02. Normally the inputs to tabs 23 and 24 are single pulses which can only appear within the periods illustrated by the pulse train portions. This means that the six times fundamental frequency commutation pulses at tab 23 and initial pulses at tab 24 are effectively steered to the proper commutation or auxiliary firing signal output, as shown by the heavy pulse marks within the pulse train areas for tabs 5, 6, 7, 10, 11, 19, 12, 13 & 14 in Figure 1. Normally the commutation pulse at tab 23 appears about 10 usec. after tab 29 goes high and the initial pulse at tab 24 appears at the same instant that tab 29 goes low. A 25% high, 75% low duty cycle pulse train is normally applied to input tab 25.

2.04 Firing Signal Outputs

Each firing logic signal is amplified by an output transistor whose collector is connected to the delayed firing supply input tab 28. This means that tab 28 must be in the high state before normal firing output signals from tabs 5 through 19 can be obtained. When any of these output tabs are at the low state, they can sink at least 10ma of electrical noise signal on the firing leads to prevent false firing of the SCRs.

2.05 Start and Stop Logic

2.05.1 To start the inverter, input tab 31 goes high. Tab 31 goind high immediately releases the lockout on the commutation and auxiliary SCR firing outputs at tabs 5, 6, 7, 10, 11, 19, 12, 13 & 14. However, the lockouts of the inverter SCR firing outputs at tabs 8, 9, 18, 17, 16 & 15 are not immediately released when tab 31 goes high. A second condition must be met which is the appearance of an auxilairy SCR firing pulse for that phase. Tabs 8 & 9 are released when tab 7 goes high, tabs 18 & 17 are released when tab 19 goes high and tabs 16 & 15 are released when tab 14 goes high. This means that on starting, the Inverter SCR firing outputs in each phase begin separately at the time when the auxiliary SCR firing pulse for that phase appears.

2.05.2 To stop the inverter, input tab 31 goes low. Tab 31 going low immediately locks out any further inverter SCR firing outputs at tabs 8,9,18,17,16 & 15. However, the lockouts of the commutation and aux. SCR firing outputs are not immediately applied when tab 31 goes low. A second condition must be met, which is the appearance of a positive commutation firing pulse for that phase. Tabs 5, 6 & 7 are locked out after tab 6 has gone high, tabs 10, 11 & 19 are locked out after tab 11 has gone high, and tabs 12, 13 & 14 are locked out after tab 13 has gone high. This means that on stopping, the commutation and auxiliary SCR firing

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outputs in each phase end separately at the time when an actual positive commutation occurs in that phase.

2.05.3 The commutation and auxiliary firing start-stop lockout logic is also affected by two other signals. On initial energization of the control, the delayed firing supply input at tab 28 does not immediately go high. Its initial low state sets up the commutation and auxiliary lockout logic to its locked out state. If an inverter fault occurs, the input at tab 22 goes high and resets the commutation and auxiliary lockout logic to its locked out state without any commutation pulses being required.

2.06 Fault Logic

When the fault lockout input signal at tab 22 goes high, all normal firing output signals are immediately locked out. However, a low input pulse at tab 20 will bypass the fault lockout and will simultaneously produce a firing pulse at all inverter SCR firing outputs, tab 8,9,18,17,16 & 15.

2.07 Power Supply Requirements

The 20V power supply requirements will be 100ma ±15%. There is an additional 10 to 20ma average current required for the SCR firing outputs, but this is supplied through tab 28 from the 20V supply of the Inverter card.

2.08 Reversing Logic

To generate a reverse, ACB, phase sequence the reversing logic input, REV, tab 4 is taken high to +20V.

If the inverter is running forward, the phase sequence will remain ABC as long as the minimum reference input, MR, tab 3, is low, but the reference clamp output, RFC, tab 26, goes low to initiate a stopping sequence. When a low frequency is reached, MR goes high, the phase sequence is reversed and the reference clamp is disabled letting the drive re-accelerate to set speed in the reverse direction.

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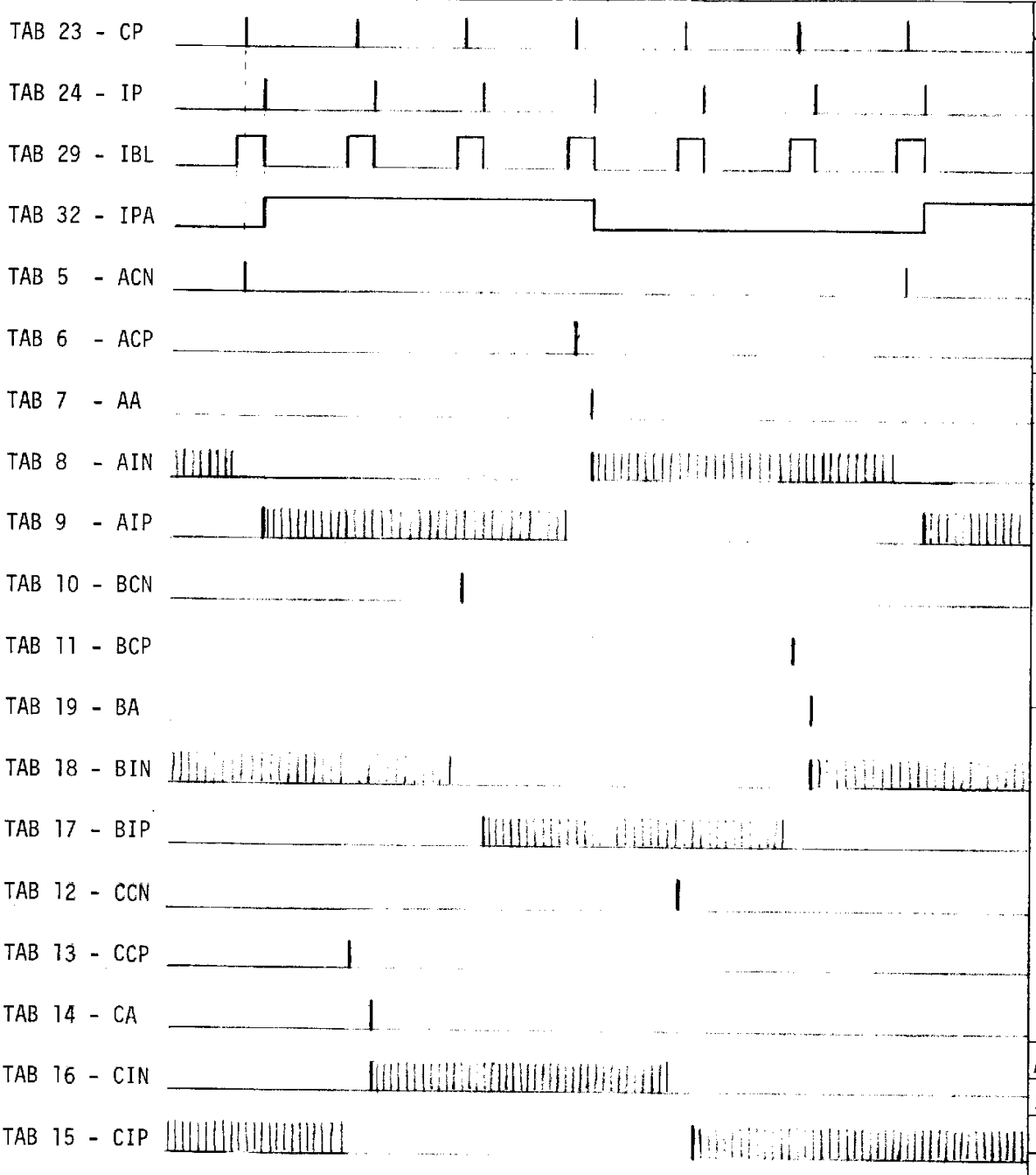

FIGURE 1

ABC PHASE SEQUENCE

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3.0 TEST INSTRUCTIONS

In these instructions, a "high" logic state refers to 12 to 13 volts and a "low" logic state refers to 0 to 1 volt. A 560 ohm, 2 watt loading resistor should be connected from each firing output, tabs 5 through 19, to common. Tabs 28 & 31 are connected high to +20 volts and tabs 27 & 22 are connected low to common. A 1.4 to 1.5 kilohertz square wave pulse train, which is high for about 100 μsec. and low for about 600 μsec. is applied to tab 29. Tab 20 is connected high to +13 volts. No input voltage should exceed +13V except tabs 3, 4, 28 & 31 which may be +20V. A 25 to 50 kilohertz square wave pulse train, which is high 25% of the time and low 75% of the time, is applied to tabs 23, 24 & 25. Connect a 1K resistor from +20V to RFC, tab 26.

3.01 Inverter Firing Outputs

The firing outputs from tabs 8 & 9 for phase A, tabs 18 & 17 for phase B and tabs 16 & 15 for phase C should exhibit the three phase wave shapes shown in Figure 1. Each succeeding phase should follow the preceeding phase by 120 electrical degrees, or 2 periods of the tab 29 input pulse train, with the positive and negative half cycles being 180 electrical degrees out of phase. A full cycle in each phase covers 6 pulses of the tab 29 input pulse train. The gap between positive and negative half cycle "on" periods should be the same width as the tab 29 high pulses.

The "on" periods of each output should consist of the 25 to 50 kilohertz pulse train applied to tab 25, with the pulses being from 13 to 16.5 volts high. If tab 25 is temporarily disconnected from the pulse train and connected to common, tabs 8, 9, 18, 17, 16 & 15 should stay in the low or "off" state.

3.02 Commutation Firing Outputs

The firing outputs from tabs 5 & 6 for phase A, 10 & 11 for phase B and 12 & 13 for phase C should appear in the relationship with the inverter firing outputs as shown in Figure 1. Tab 5 pulse should follow the tab 8 "on" period, tab 6 pulse should follow the tab 9 "on" period, tab 10 should follow the tab 18 "on" period, tab 11 pulse should follow the tab 17 "on" period, tab 12 pulse should follow the tab 16 "on" period and tab 13 pulse should follow the tab 15 "on" period.

The "on" periods of each output should consist of the 25 to 50 kilohertz pulse train applied to tab 23, with the pulses being from 13 to 16.5V high. If tab 23 is temporarily disconnected from the pulse train and connected to common, tabs 5, 6, 10, 11, 12 & 13 should stay in the low of "off" state.

3.03 Auxiliary Commutation Firing Outputs

The firing outputs from tab 7 for phase A, tab 19 for phase B and tab 14 for phase C should appear in the relationship with the positive commutation firing outputs as shown in Figure 1. Tab 7 pulse should begin at the same time as the tab 8 pulse, tab 19 pulse should begin at the same time as the tab 18 pulse and tab 14 pulse should begin at the same time as tab 16 pulse.

The "on" periods of each output should consist of pulses 13 to 16.5V high. If tab 24 is temporarily disconnected from the pulse train and connected to common, tabs 7,19 & 14 should stay in the low or "off" state

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3.04 Phase A Output

The output signal at tab 32 should be a 230 to 250 Hz square wave which is essentially in phase with the tab 9 output, going high when tab 9 goes high, but going low when tab 8 goes high.

3.05 Inverter Firing Stop/Start

Tab 31 controls the starting and stopping of the inverter firing outputs. When tab 31 is disconnected from +20V and connected to common, inverter output tabs 8, 9, 18, 17, 16 & 15 should all immediately go to the low or "off" state.

Disconnect tab 24 from the pulse train input and connect it to common so that auxiliary output tabs 7, 19 & 14 will stay low. Reconnect tab 31 from common to +20 volts to start inverter. Inverter output tabs 8, 9, 18, 17, 16 & 15 should remain in the low state because they need an auxiliary output pulse to unlatch the stop lockout. When tab 24 is disconnected from common and reconnected to the pulse train, the inverter output tabs should return to their half cycle "on" states as shown in Figure 1. Tabs 8 & 9 should be released by a tab 7 pulse, tab 18 & 17 by a tab 19 pulse and tab 16 & 15 by a tab 14 pulse.

3.06 Commutation and Auxiliary Firing Stop/Start

Tab 31 controls the starting and stopping of the commutation and auxiliary firing outputs. When tab 31 is disconnected from +20V and connected to common, the commutation and auxiliary firing output pulses should be stopped on an individual phase basis. Tabs 5, 6 & 7 should be locked outafter tab 6 pulses for an instant (about a .1 usec. wide pulse), tabs 10,11 & 19 should be locked out aftertab 11 pulses for an instant, and tabs 12,13 & 14 should be locked out aftertab 13 pulses for an instant.

Reconnect tab 31 from common to +20V. Tabs 5, 6, 7, 10, 11, 19, 12, 13 & 14 should all immediately begin pulsing at their proper times as shown in Figure 1.

3.07 Delayed Firing Supply

With all firing outputs operating as shown in Figure 1, disconnect tab 28 from +20V and connect to common. All firing outputs should go to the low state. When tab 28 is reconnected to +20V, all the firing outputs should return to their normal operating mode.

3.08 Fault Logic

With all firing outputs operating as snown in Figure 1, disconnect tab 22 from common and connect to +13V. All firing outputs should immediately be locked out to the low state. Now disconnect tab 20 from +13V and connect to the 25 to 50 kilohertz pulse train. All inverter output tabs 8, 9, 18, 17, 16 & 15 should exhibit an inverted image of this pulse train continuously until tab 20 is disconnected from the pulse train and reconnected to +13 volts. The commutation and auxiliary firing outputs should not be affected by tab 20 and should remain off.

When tab 22 is reconnected from +13V to common. all firing outputs should return to their normal operating mode shown in Figure 1.

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3.09 Reversing Logic

With the card operating with an ABC phase sequence apply a logic high, +20V, to the REV input, tab 4. The phase sequence should remain ABC, but the reference clamp output, RFC, tab 26 should go low to less than 1 volt.

Apply a logic high, +13V, to the minimum reference input, MR, tab 3. The phase sequence should reverse to ACB and the voltage at RFC, tab 26, should go high. With a reverse ACB phase sequence the Figure 1 signals on tabs 10, 11, 19, 18 & 17 are interchanged with those on tabs 12, 13, 14, 16 and 15 respectively. Disconnect +13V from tab 3.

Repeat steps 3.05 through 3.08.

With the card operating with a reverse ACB phase sequence disconnect the REV input, tab 4, from +20V. Again the phase sequence should remain ACB, but the RFC output, tab 26, should go low.

Apply +13V to MR, tab 3. The phase sequence should return to ABC and RFC, tab 26, should go high.

4.0 OPERATING and TEST CONDITIONS

This card should be capable of operating within the performance specified in Section 2.0 and pass all tests specified in Section 3.0 while exposed to the following conditions:

4.01 DC Supply Voltage
+19.8 to +20.2 volts from tab 1 to tab 2.

4.02 Ambient Temperature
0 to 75°C.

4.03 Humidity
24 hours in 90% relative humidity at 40°C.

4.04 Voltage to Ground
600 volts

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