

REV. NO. / /	TITLE
P3K-AL-0415-A01	TEST INSTRUCTIONS FOR LOAD SET CIRCUIT BOARD 1L1-C001 (ASSEMBLY DRAWING 117D6684 G1)
CONT ON SHEET 2	SH NO. 1

FIRST MADE FOR EHC MARK II	CIRCUIT BOARD REV. #3	REVISIONS
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① JPAWIS OCT 27 1981
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I. CIRCUIT DESCRIPTION

The Load Set Circuit Board transforms the position signal which is provided by the Load Set Motor Drive to a DC signal referred to as a Load Set signal. The board contains the following circuits:

- a. A 3 KC sinewave oscillator whose output (6 VRMS) is used to excite the demodulator.
- b. A demodulator to which the RVDT is connected and whose output is a fully rectified sine wave with maximum value and polarity varying with the RVDT position.
- c. A filter which smooths the demodulator output to provide the Load Set signal, which is one output of the board. This is a DC signal ranging approximately from -5.6V to +5.6V and back to -5.6V for a complete revolution of the RVDT; the useful portion of its range is 0V (no load) to +2.000 VDC (full load).
- d. A meter amplifier which provides another output signal proportional to the Load Set Signal for indication purposes.
- e. Four (4) zener power supplies for the integrated circuits of parts (a) and (d).

II. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

1. Power Supply 1: (Pin 37): $+22.000 \pm 0.002$ VDC at 45 ma (approx.)
2. Power Supply 2: (Pin 41): -22.000 ± 0.002 VDC at 45 ma (approx.)

B. Input Connections

RVDT: CLIFTON LINEAR TRANSFORMER TLH-11-E-5

Red Lead: Pin 35
Black Lead: Pin 34
Yellow Lead: Pin 21
Blue Lead: Pin 19

C. Output Loads:

- ✓ 1. Load 1: $20K \pm 1\%$ Pin 13 (loading rates and load set limit board)
2. Load 2: $4.75M \text{ ohms} \pm 1\%$ Pin 11 (Voltage Comparator)

REF 35

BLK 34

YEL 21

BLU 19

273-2

273-12

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273-15

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II. CIRCUIT SPECIFICATIONS (continued)

C. Output Loads: (continued)

6 3. Load 3: 4.75 M Ohms \pm 1%
 Pin 12 (Voltage Comparator) MC

7 4. Load 4: 40 Ohms \pm 1% 0 - 1 mA SET VR1 CCW 3 turns
 Pin 10 (Milliammeter connected between pins 10 and 8)

8 5. Load 5: > 1M Ohms 7030P100H
 Pin 14 (Digital voltmeter connected between pins 14 and 15)

D. Individual Stage Performance Specifications

1. Power Supplies

- a. TP1: +15.7 \pm 1.0 VDC
- b. TP2: -15.7 \pm 1.0 VDC
- c. Node of R13, C5, C7, CR6, IC3 case: (before coating the board)
 -15.0 ± 1.0 VDC
- d. Node of R14, C6, C8, CR7, IC3 Pin8: (before coating the board)
 $+15.0 \pm 1.0$ VDC

2. 3 KHz Oscillator

All tests, except that for temperature sensitivity, are to be done with the oscillator normally loaded. (RVDT and 20K ohms load connected)

a. Initial Starting

Adjust VR50 to mid range and observe TP3 with a scope (2 volt/div amplitude, 50 μ s/div. sweep). If necessary readjust for a non-distorted sine wave.

b. Distortion

1. FET (2N3822) Distortion

Adjust VR50 too far CW will cause the output TP3 to distort. Check distortion by centering the signal on both the amplitude and sweep coordinates as shown in Figure 1. Distortion occurs when $|T_1 - T_2| > 10 \mu$ sec and can be eliminated by backing down on VR50 (TP5).

2. Saturation Distortion

Saturation will occur when $V_{peak\ TP3} > V_{zener}$ and is eliminated by decreasing VR51.

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FIGURE 1

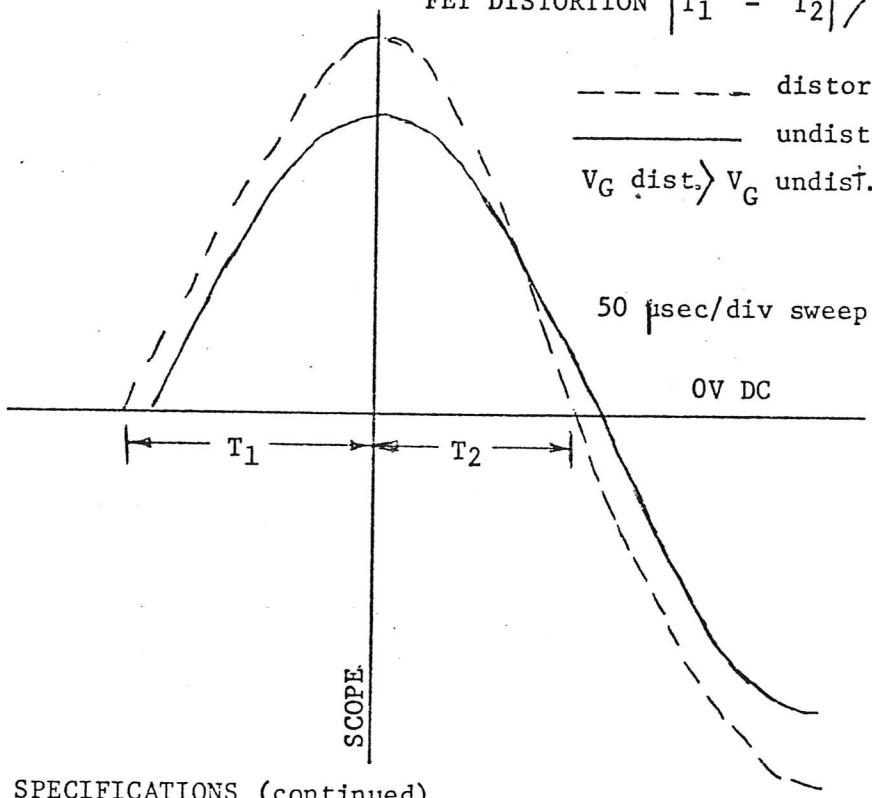
FET DISTORTION $|T_1 - T_2| > 10 \mu\text{sec}$

— dashed — distorted
 — solid — undistorted
 $V_G \text{ dist.} > V_G \text{ undist.}$

50 $\mu\text{sec/div}$ sweep

0V DC

SCOPE



II. CIRCUIT SPECIFICATIONS (continued)

③ D. Individual Stage Performance Specifications (continued)

2. (continued)

c. V_{GATE} (VTP50) Setting

Adjust VR50 so that the oscillator runs at the upper limit of linearity ($|T_1 - T_2| \cong 10 \mu\text{sec}$); i.e.:

$$|V_{GATE}| \cong |V_{GATE \text{ FET DIST}}| - .010$$

Operation around this point give maximum temperature and load change stability. A sampling of 25 FET's has shown the upper limit to be:

$$-2.6 < V_{GATE} < -1.0$$

d. Amplitude Setting

Adjust VR51 for $V_{TP3} = 6.000 \pm .010 \text{V RMS}$.

④ *

e. Frequency

$$3000 < f < 3400 \text{ Hz}$$

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II. CIRCUIT SPECIFICATIONS (continued)

D. Individual Stage Performance Specifications (continued)

2. (continued)

⑤ f. Regeneration

The oscillator must restart in all of the following situations:

1. Simultaneously interrupt the +22 VDC and the -22 VDC power.
2. Interrupt the +22 VDC power. Reconnect.
3. -22 VDC power. Reconnect.
4. Withdraw and insert the Load Set Board.

⑥ g. Temperature Stability

This test may be conducted with oscillator unloaded.

With V_G set as in Step 3 at ambient temperature (T_A) then:

$$|\Delta V_{TP3}| \leq .060 \text{ V RMS} \quad (T_A \leq T \leq 130^\circ\text{F})$$

A small change in V_G may be necessary to meet this spec.

If $\Delta V_{TP3} > +.060$ for $T_A \leq T \leq 130^\circ\text{F}$, decrease V_{GATE} .

If $\Delta V_{TP3} > -.060$, increase V_{GATE} .

⑦ h. Load Variance

No combination of transducer positions should change V_{TP3} more than 15 mv RMS.

$$|\Delta V_{TP3}| \leq .015 \text{ V RMS}$$

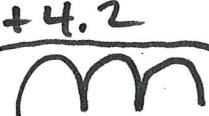
⑧ i. Envelope Modulation

Envelope modulation should not exceed .015V ptp.

ii. 3. Demodulator and Filter

$$V_{TP3} = 6 \text{ V RMS}$$

⑨ RVDT and 20K Ohms load connected.



- a. RVDT positioned for maximum (positive) V_{TP7}, V_{DEMOD} (Voltage at CR8, CR9, L1 Node) should be a clean full-wave-rectified sine wave with peak value of 10.0 ± 0.5 volts.

$V_{TP7} = 5.60 \pm 0.30$ Volts DC $+2.250$ 1 end $-0-$ (-3.00) other end



Typical V_{TP3} , V_{DEMOD} and V_{TP7} for this case are shown in Fig. 2.

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TEST INSTRUCTIONS FOR LOAD SET CIRCUIT BOARD 1L1-C001
(ASSEMBLY DRAWING 117D6684 G1)

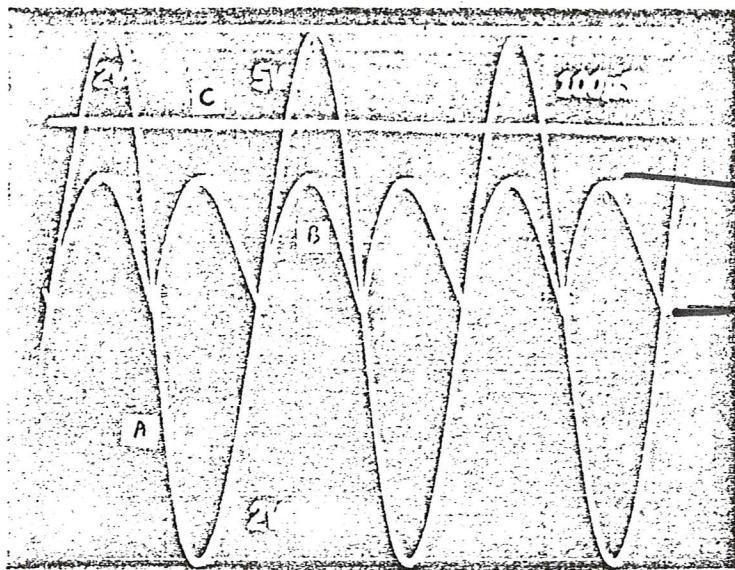
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FIGURE 2



4 Volts Peak

V_{TP3} (A) 2V/divOV V_{DEMOD} (B) 5V/divA,B,C V_{TP7} (C) 2V/div

6 Volts peak

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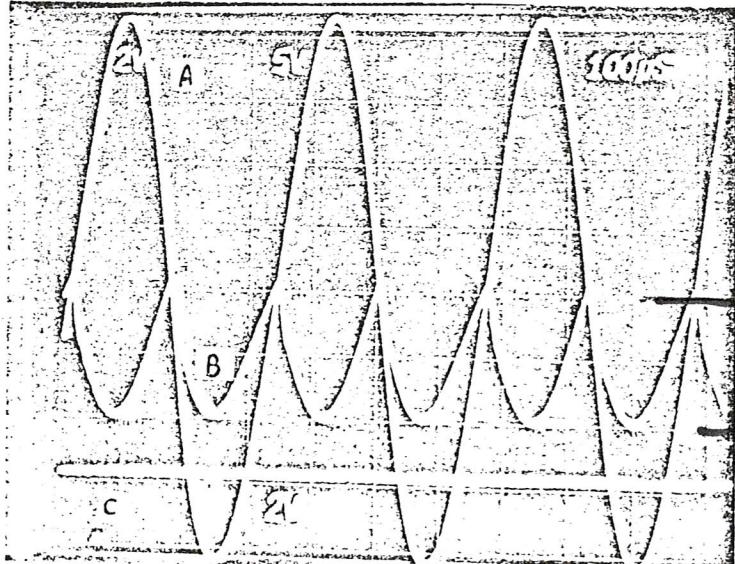
- ⑩ b. RVDT positioned for ^{MAX} minimum (negative) V_{TP7}. V_{DEMOD} should be a clean full-wave-rectified sine wave with peak value of -10.0 + 0.5 volts.

$$V_{TP7} = -5.60 + 0.30 \text{ volts DC}$$

V_{TP7} ripple (max) = 10m V ptp 3 KHz fundamental

Typical V_{TP3}, V_{DEMOD} and V_{TP7} for this case are shown in Fig. 3.

FIGURE 3

V_{TP3} (A) 2V/divOV V_{DEMOD} (B) 5V/divA,B,C V_{TP7} (C) 2V/div

400 to 6 Volts Peak

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TEST INSTRUCTIONS FOR LOAD SET CIRCUIT BOARD 1L1-C001
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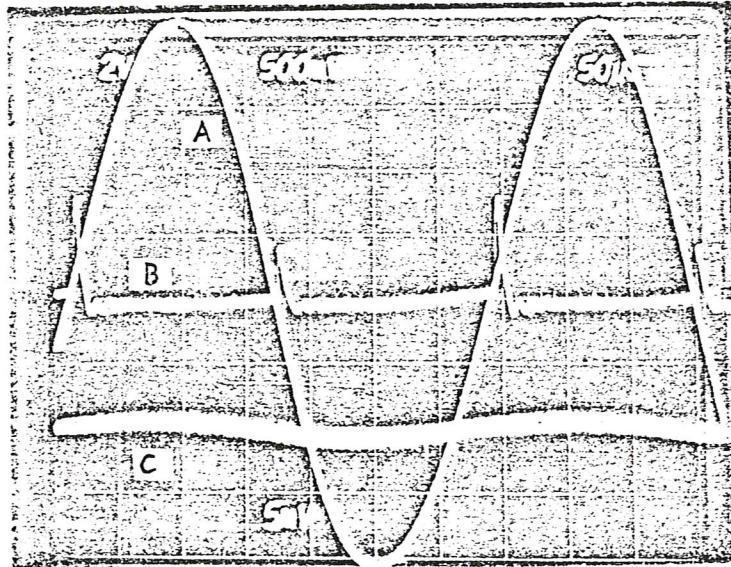
II. CIRCUIT SPECIFICATIONS (continued)

D. Individual Stage Performance Specifications (continued)

(11) 3. (continued)

c. RVDT positioned for $V_{TP7} = 0.000 \pm 0.001$ VDC V_{DEMOD} should have a DC component of 0.000 ± 0.005 volts and be $|V_{DEMOD}| \leq 0.100$ volts except for possible short duration spikes at the oscillator output zero crossover moments. V_{TP7} ripple (max) = 4m V ptp 3 KHz fundamental.Typical V_{TP3} , V_{DEMOD} and V_{TP7} for this case are shown in Fig. 4.

FIGURE 4

 V_{TP3} (A) 2V/div V_{DEMOD} (B) 500mV/div V_{TP7} (C) 5mV/div

OV

OV

OV

d. With the board inactive:

$$0.88 < V_{TP7} / V_{DEMOD} < 0.94 \quad (f \leq 100\text{Hz})$$

(12) 4. Meter Amplifier

DO STEP 110,5C Here, SPC/6/16/89

a. DC offset: ± 0.001 volts (adjustable through VR52 - adjustment point should be at least 2 turns away from either pot end)

b. Gain: 1.000 volts/volt

c. Saturation limits (minimum): ± 10.0 volts.Adj RVDT For 1V at TP7 - 3V
TP6 should Read 1V. Adj VR1 For 1MA

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D. Individual Stage Performance Specifications (continued)

13 (13) 5. Miscellaneous

- a. Pins 1, 8, 15, 39, and TP11 are permanently connected with each other.
- b. Pins 11, 12, 13 and TP7 are permanently connected with each other.
- c. Resistance between TP6 and Pin 10:

10K ohms \pm 10% (VR1 CCW) and \swarrow ~~10~~ ohms (VR1 CW)

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TEST INSTRUCTIONS FOR LOAD SET CIRCUIT BOARD 1L1-C001
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PREPARED BY

D. Economou

DATE

6/11/1974

D. Economou
EHC DESIGN ENGINEERING

MJS 7/24/81

APPROVED BY

P.C. Callan

DATE

9-12-77

P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE

REVIEWED BY

R. Debertolis

DATE

9-9-77

R. Debertolis
EHC TEST ENGINEER

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