# TEST INSTRUCTIONS - 137D5195 PARTIAL ARC AMPLIFIER

Distribution: PWA Test Source File: 137D5195.doc

CIRCUIT DESCRIPTION

The circuit is a two-stage DC amplifier.

The first stage input is applied at Pin 8. Output voltages are clamped at 0V, for negative-only operation. First stage output is available at Pin 10, and feeds the second stage at R10. IC1 offset is nulled using VR50. Gain is calibrated for -1 using VR1.

The second stage input is applied at R10. The output is available from Pin 32. IC2 offset is nulled using VR51. Adjustable +/- DC bias can be applied using VR2 & VR3. DC bias sensitivity can be adjusted using VR52. The output voltage range is clamped between upper and lower limits (normally set for +10V and 0V). These limits can be adjusted using VR5 & VR6. VR5 moves the upper and lower limits together. VR6 moves just the lower limit. The second stage has two gains that can be adusted using VR54 and VR4. VR54 affects both the high and low gains. VR4 affects only the low gain. VR53 can be adjusted to set the output voltage level where the gain changes from low to high.

TEST PROCEDURE

1.0 Applicable Documents
- MRP Bill of Material for 137D5195 G1
- Elementary 137D5195 SH2
- Test Instructions for MKII Partial Arc Amplifier P3K-AL-0549-A01 (reference only)

2.0 Equipment
(2) 40K Ohm load resistors
(2) DC Power Supply, 22V
Adjustable Voltage Source, 1mV to +10V
Signal Generator, Triangle Wave Output, -2V to +12V
4 1/2 digit DVM
Two-Channel Oscilloscope with XY display mode

3.0 Visual Inspection

3.1 Verify assembly is free of solder bridges.

3.2 Verify all IC's and semiconductors are mounted with correct orientation.

3.3 Verify polarized capacitors are mounted with correct orientation.

3.4 Verify keying slots at connector pins 17 & 35.

4.0 Electrical Test
All signal sources and jumpers are assumed to be disconnected after each test step unless otherwise noted. All voltages are monitored with respect to 0V reference using DVM unless otherwise noted.

4.1 Apply loads & external DC power supplies.
Pin 10: 40K Ohms to Common
Pin 32: 40K Ohms to Common
Pin 37: +22V
Pin 39: 0V (Common)
Pin 41: -22V

4.2 Verify zener diode voltage regulators.
TP1: +18.7V +/- 0.5V
Pin 39: 0V (Reference)
TP2: -18.7V +/- 0.5V

4.3 Null IC1 output offset voltage.
Monitor Pin 10 voltage.
Adjust VR50 for 0V +/- 2mV at Pin 10.

4.4 Calibrate first stage gain.
Monitor Pin 10 voltage.
Apply +1V +/- 2mV at Pin 8.
Adjust VR1 for -1V +/- 2mV at Pin 10.

4.5 Verify Pin 10 voltage is clamped to 0V for negative inputs.
Monitor Pin 10 voltage.
Apply -10V at Pin 8.
Verify 0V +/- 5mV at Pin 10.

4.6 Null IC2 output offset voltage.
Monitor Pin 32 voltage.
Set VR5 full CCW.
Set VR6 full CW.
Kill all second stage input signals:
Apply -10V at Pin 8.
Jumper TP51 to Pin 39.
Jumper TP52 to Pin 39.
Adust VR51 for 0V +/- 2mV at Pin 32.

4.7 Verify DC bias voltage divider range.
Monitor TP51 voltage.
Set VR2 & VR3 full CCW.
Adust VR2 CW more positive than +9V at TP51.
Return VR2 full CCW.
Adjust VR3 CW more negative than -9V at TP51.
Return VR3 full CCW.

4.8 Verify bias sensitivity range.
Monitor TP51 voltage.
Adust VR3 for -1V +/- 2mV at TP51.
Monitor VR52 wiper voltage.
Verify VR52 wipes from -0.75V to -0.4V.
Leave VR52 full CCW.

The following tests use the two-channel scope in XY mode to display the amplifier transfer characteristic. A triangle wave is applied to the input to sweep the full input range. The input and output voltages are displayed simultaneously, with the input measured along X-axis (horizontal) and output measured along Y-axis (vertical).

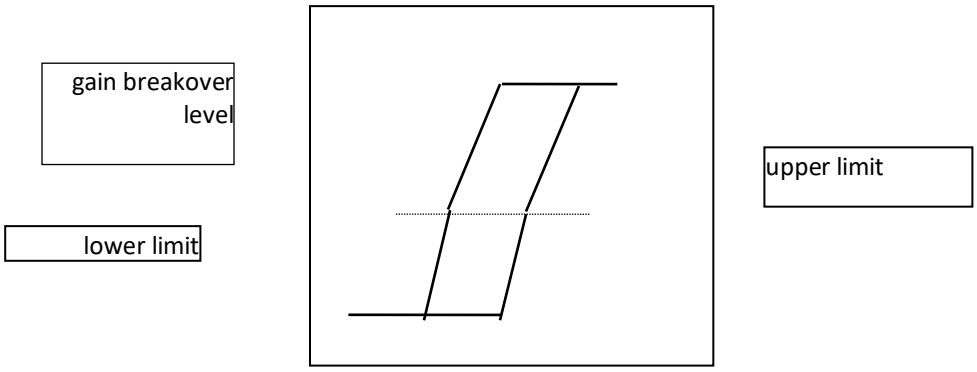
4.90 Set up input sweep signal.
Monitor triangle wave signal on scope channel 1.
Using normal time-base sweep mode, adust triangle for -2V to +12V p-p amplitude.

Adjust frequency to 50Hz (period = 20ms).

4.91 Set up XY display.
Select XY sweep mode.
Set Ch.1 & Ch.2 attenuators for 2V/div scale factor.
Set 0,0 origin point for XY display:
Ground Ch.1 & Ch.2 and observe stationary dot on CRT.
Adjust horizontal position to place dot three divisions from left side.
Adjust Ch.2 vertical position to place dot one division up from bottom.
Select DC coupling for Ch.1 & Ch.2.

4.92 Apply input signal to UUT.
Connect signal generator common to Pin 39.
Connect signal generator 50 Ohm output to Pin 8.

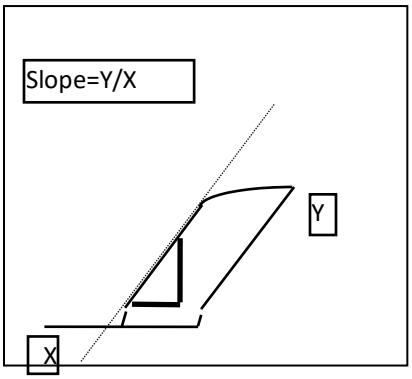
4.93 Verify output clamping level range.
Set VR4 full CW.
Set VR5 full CW.
Set VR6 full CW.
Set VR53 full CW.
Set VR54 full CW.
Adjust VR3 as needed to force output into upper clamping limit.
Adjust VR2 as needed to force lower output limit to lowest level.
Adjust VR5 to set upper clamping limit to +10V.
Adjust VR6 to set lower clamping limit to 0V.




4.94 Verify gain breakover range.
Using VR53, verify gain breakover level can be adjusted from upper output limit level to lower output limit level.

4.95 Verify low-gain range.
Adjust VR53 full CCW to set gain breakover level to lower output limit level.
Set VR54 full CW.
Set VR4 full CCW.

Verify slope is <= 1.3.
Set VR4 full CW.
Verify slope is >= 2.8.




4.95 Verify high-gain range.
Adjust VR53 CW to set gain breakover level to upper output limit level.
Verify VR54 can be adjusted for slope of +2.
Verify VR54 can be adjusted for slope of +10.

END OF TEST

Power down test signal source, then external power supplies.

Disconnect UUT.

Apply T-stamp if all steps passed.

REVISION HISTORY

| REV. | Date | Init. | Description of Change |
|---|---|---|---|
| 0 | 02/27/95 | ADM | Re-issued from original P3K-AL-0549-A01 |