III. CIRCUIT SPECIFICATIONS (continued)

B. Operating Signal Levels

1. Oscillator Output (TP1 to TP5)

a. Voltage: 6.0 VRMS
b. Frequency: 3050 ± 150 HZ

2. Board Output (TP7 to TP5)

a. Voltage: 0 to +10 VDC for 0° to ~~+25°~~ 100° rotational travel of the RVDT.

C. Output Loads

1. The oscillator is loaded by the demodulator circuit including the RVDT. Red to pin 34 Black to pin 35 Yellow to pin 19 Blue to pin 18 (of RVDT)

2. The board output (pins 10 and 23): 2K Ohms.

D. Continuity

1. Continuity exists between pins 23 and 25.

IV. REQUIRED TESTS AND SETTINGS

A. 3 KHZ Oscillator

All tests, except that for temperature sensitivity, are to be done with the oscillator normally loaded with the transformer, and RVDT, and the demodulator.

1. Initial Starting

Adjust VR50 to mid range and observe TP1 with a scope (2 volt/div. amplitude, 50 usec/div. sweep). If necessary readjust for a non-distorted sine wave.

2. Distortion

a. FET (2N3822) Distortion

Adjusting VR50 too far CW will cause the output TP1 to distort. Check distortion by centering the signal on both the amplitude and sweep coordinates as shown in Figure 1. Distortion occurs when the absolute value of $T_1 - T_2$ is greater than 10 usec. and can be eliminated by backing down on VR50 (TP6).

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TEST INSTRUCTIONS FOR PLANT COMMUNICATIONS
ANALOG (LOAD LIMIT SET MOTOR POSITION INDICATOR)
FIRST MADE FOR FOR EHC MARK II (PLANT COMMUNICATIONS)

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IV. REQUIRED TESTS AND SETTINGS (continued)

A. 3 KHZ Oscillator (continued)

a. (continued)

a. (continued)

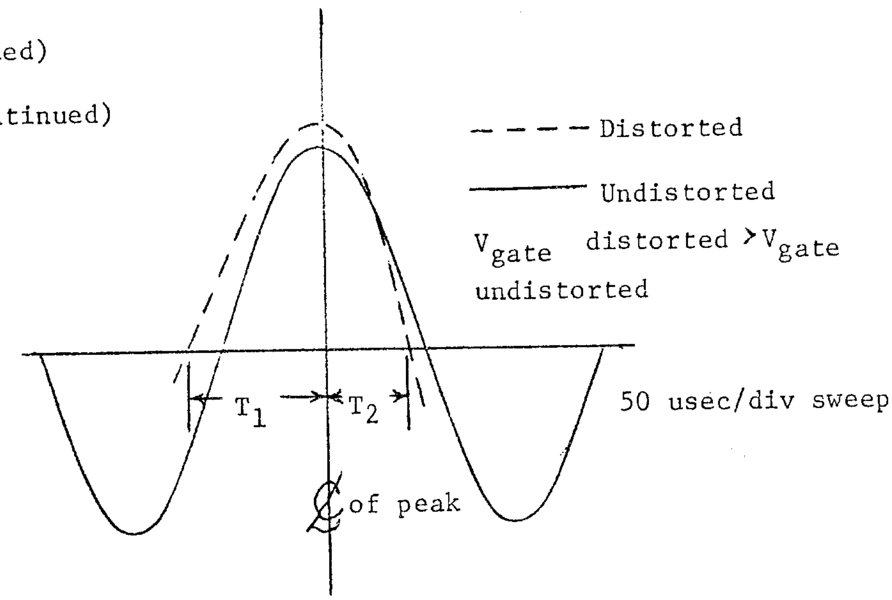

FIG. 1 FET DISTORTION $|T_1 - T_2| > 10$ usec

b. Saturation Distortion

Saturation will occur when V_{peak} of TP1 is greater than the supply voltage (15V). It is eliminated by decreasing VR51.

3. V_{gate} (TP6) Setting

→ Adjust VR50 so that the oscillator runs at the upper limit of linearity (absolute value of $T_1 - T_2$ approaches 10 usec); i.e.: Set V_{gate} so that its magnitude is approximately 10 mv below the distortion level. Operation around this point gives maximum temperature and load change stability. A sampling of 25 FET's has shown the upper limit of V_{gate} to be between -2.6 and -1.0.

→ 4. Amplitude Setting

Adjust VR51 for $V_{TP1} = 6.000 \pm .010$ RMS.

5. Frequency

→ * $3000 < f < 3400$ Hz

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IV. REQUIRED TESTS AND SETTINGS (continued)

A. 3 KHZ Oscillator (continued)

6. Regeneration

The oscillator must restart in all of the following situations:

a. Simultaneously interrupt the +15 VDC and the -15 VDC power. Reconnect.

b. Interrupt the +15 VDC power. Reconnect.

c. Interrupt the -15 VDC power. Reconnect.

d. Withdraw and reinsert the Load Limit Set Motor Position Indicator board.

7. Temperature Stability

This test may be conducted with the oscillator unloaded.

With V_{gate} set as in step 3 at ambient temperature, the absolute magnitude of the voltage at TP1 must not vary more than ± .060V RMS as the temperature ranges between ambient and 130°F.

A small change in V_{gate} may be necessary to meet this spec. If the change at TP1 exceeds +.060, decrease the V_{gate}. If the change at TP1 exceeds -.060, increase V_{gate}.

8. Load Variance

No angular change in the RVDT between ± 25° should cause the voltage at TP1 to vary more than ± .015V RMS.

9. Envelop Modulation

Envelop modulation should not exceed .015V peak to peak.

B. Output Setting

Gnd TP8 and adj. VR52 for 0 Volts. Remove TP8 from Gnd

1. Adjust VR1 so that the output (pin 10 and TP7) is +10.0 VDC for ~~25°~~ 100° displacement of the RVDT from zero.

2. Confirm that the output is linear within ± 1%.

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TEST INSTRUCTIONS FOR PLANT COMMUNICATIONS ANALOG (LOAD LIMIT SET MOTOR POSITION INDICATOR)

FIRST MADE FOR EHC MARK II (PLANT COMMUNICATIONS)

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PREPARED BY George W. Kessler DATE 1/16/75

SSA 10/5/81

G.W. Kessler
EHC DESIGN ENGINEERING

APPROVED BY P C Callan DATE 9-12-77

P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE REVIEWED BY R. Debertolis DATE 9-9-77

R. Debertolis
EHC TEST ENGINEER

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