

REV NO. 0	TITLE BOARD TEST SPECIFICATION - VOLTAGE SENSOR, 24 VDC 1P3-E005 - SCHEMATIC 117D7368 FIRST MADE FOR
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REVISIO

1. PURPOSE

- A. The purpose of this specification is to convey the proper information needed to test the referenced circuit board for its correct function.
- B. To enable the skilled Test Engineer to produce the detailed Test Procedure for the referenced circuit board.

2. DOCUMENTS PERTAINING TO THIS SPECIFICATION

- A. Voltage Sensor - 24 VDC - 117D8509
- B. AC/DC Power Ground System - 117D7762
- C.

3. EQUIPMENT NEEDED TO TEST

- A. DC Power Supply - 24 VDC nominal, 2 ampere rating.
- B. DC Power Supply - 0 to 28 VDC nominal, 1 ampere rating.
- C. 2 switches - SPST - 1 ampere rating, 24 VDC nominal.
- D. 3 Push-button Switches - SPST - 1 ampere rating, 24 VDC nominal each.
- E. 3 Indicating devices - 24 VDC nominal, 80 ma rating each.
- F.

4. CIRCUIT DESCRIPTION

This board consists of a Voltage Sensor and associated components to monitor the output voltage of the 24 VDC Power Supply. The outputs of the board logic are brought out to allow indication and control functions.

5. CIRCUIT INTEGRATION


The voltage sensor continuously monitors the output voltage of the Power Supply. Whenever this voltage exceeds a pre-set limit, a latching relay energizes, sending a signal to an indicator and the Malfunction Bus. If the voltage falls to within the pre-set value, this signal can be overridden.

If the voltage falls below a pre-set limit, a different relay will send a signal to another indicator and the Malfunction Bus. As before, if the voltage rises above the preset value, logic circuitry can be activated to override the signal.



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6. TEST SPECIFICATION

- A. Connect the board as shown in Figure 1.
- B. With PS1 set at 0 volts and 24 VDC set on PS2, close S1 and S2. Indicators 1 and 2 shall indicate, indicator 3 shall not.
- C. Press in succession PB1, PB2, and PB3. No change shall occur in the indicators.
- D. Increase the voltage between TP52 and TP53 at a ^{PS2} 1 volt per second rate. Stop when the voltage reaches 24 ± 0.5 VDC. There shall be no change in the indicators.
- E. Press and release PB1. Indicator^s 1 and 2 shall cease indicating.
- F. Reduce the PS1 voltage at a 1 volt per second rate. Stop when the voltage reaches 20 ± 0.5 VDC.
- G. Indicators 1 and 2 shall indicate where the voltage between TP52 and TP53 is $22 + 1 - 0$ VDC. Increase the voltage to 24 ± 0.5 volts.
- H. Press and release PB2. Indicators 1 and 2 shall cease to indicate.
- I. Press and release PB3. There shall be no change in the status of the indicators.
- J. Increase the voltage between TP52 and TP53 at the ^{PS2} 1 volt per second rate to 28 ± 0.5 VDC. Indicators 2 and 3 shall indicate when the voltage reads $26 + 0, -1$ VDC.
- K. Reduce the voltage between TP52 and TP53 to ^{PS2} 24 ± 0.5 VDC. There shall be no changes in the status of the indicators.
- L. Press and release PB3. Indicators 2 and 3 shall cease indicating.
- M. Repeat steps J and K. Press and release PB2. Indicators 2 and 3 shall cease indicating.
- N. Reduce PS1 and PS2 to 0 VDC. Open S1 and S2.

7. REPORT SHEET

<u>ACTION</u>	<u>REACTION</u>	<u>YES</u>	<u>NO</u>
A. Close S1 & S2	Ind. 1, 2 indicate Ind. 3 not indicate		

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1P3-EO05 - SCHEMATIC 117D7368
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7. REPORT SHEET (continued)

<u>ACTION</u>	<u>REACTION</u>	<u>YES</u>	<u>NO</u>
B. PB1, PB2, PB3 pressed.	Ind. 1,2,3; No change		
C. PS1: Increase 0 → 24 VDC.	Ind. 1,2, indicate Ind. 3, not indicate		
D. PB1 pressed.	Ind. 1,2,3 not indicate		
E. PS1: Decrease 24VDC → 20.5 VDC.	Ind. 1,2 indicate Ind. 3 not indicate		
F. PS1: Increase 20.5 VDC → 24.5 VDC.	Ind. 1,2 indicate Ind. 3 not indicate		
G. PB2 pressed.	Ind. 1,2 de-indicate Ind. 3 no change		
H. PB3 pressed.	Ind. 1,2,3, no change		
I. PS1: Increase 24.5 VDC → 28.5 VDC.	Ind. 2,3 indicate Ind. 1, not indicate		
J. PS1: Decrease 28.5 VDC → 24.5 VDC.	Ind. 1,2,3 no change		
K. PB3 pressed.	Ind. 2,3 de-indicate Ind. 1, no change		
L. PB2 pressed.	Ind. 2,3 de-indicate Ind. 1, no change		

8. NOTES

1. If any indicator does not indicate as described, the board shall be rejected.

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BOARD TEST SPECIFICATION - VOLTAGE SENSOR, 24 VDC
1P3-E005 - SCHEMATIC 117D7368
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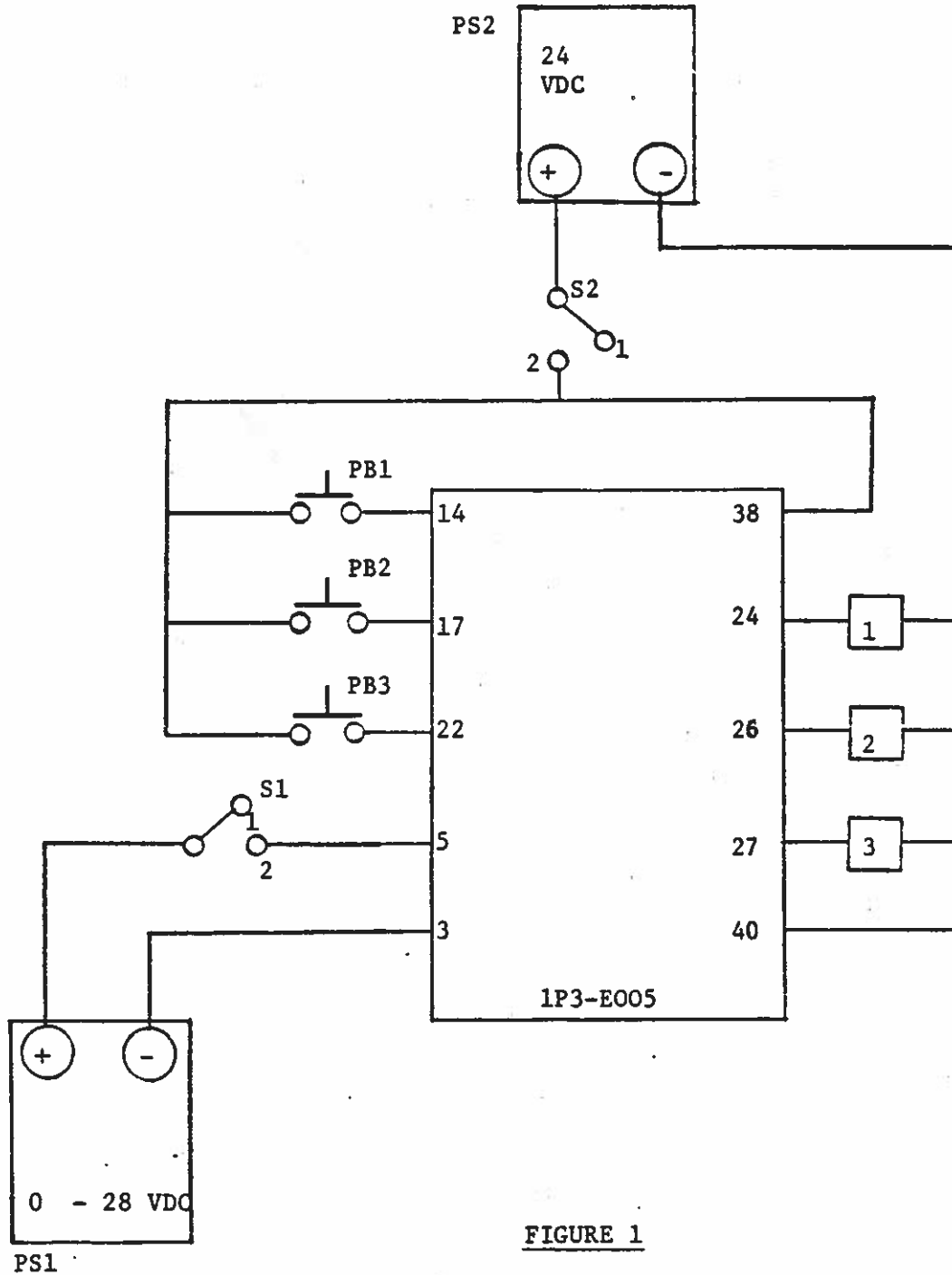


FIGURE 1

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TITLE
BOARD TEST SPECIFICATION - VOLTAGE SENSOR, 24 VDC
1P3-EO05 - SCHEMATIC 117D7368
FIRST MADE FOR

Assm. 117D8509
Sch. 117D7368
Patchboard No. _____
PCR _____

REVISION

The 24 VDC sensor monitors the output voltage level of its specific power supply. If the voltage level falls below 22 to 23 VDC, K1 de-energizes, contact K1-1 closes to apply a signal to pins 24 and 26. If the voltage level rises above 25 to 26 VDC, KL-1 energizes, contact K1-1 closes to apply a signal to pins 27 and 26. A reset signal applied to pins 14 or 17 will pick up K2 allowing K1-1 to latch in. Similarly, a reset signal applied to pins 22 or 17 will pick up K1-1.

Test Procedure

1. Patched program is as shown in Fig. A.
2. All switches down.
3. Read voltage of VS1 from TP53 to TP52.
4. Adj. VS1 for 0 VDC
5. Procedure:

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P3K-AL-0334-A01

BOARD TEST SPECIFICATION - VOLTAGE SENSOR, 24 VDC

1P3-E005 - SCHEMATIC 117D7308

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	PROCEDURE	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
6	Initial conditions												
7	S3 up	X			X	X							
8	S3 down - S4 up		X		X	X							
9	S4 down - S5 up			X	X	X							
10	S5 down				X	X							
11	Adj. VSL for +24.00 VDC				X	X							
12	S3 up	X											
13	S3 down												
14	Decrease VSL volts until L4 goes on				X	X							
15	Check VSL volts for +22.00 to 23.00 VDC				X	X							
16	Adj. VSL for +24.00 VDC				X	X							
17	S4 up		X										
18	S4 down												
19	Adj. VSL for +27.00						X						
20	S3 up	X					X						
21	S3 down - S4 up		X				X						

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1P3-EO05 - SCHEMATIC 117D7368
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REVISIONS

PROCEDURE	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12
22 S4 down - S5 up												
23 S5 down												
24 Adj. VSI for +24.00 VDC												
25 S5 up												
26 S5 down												
27 Increase VSI volts until L6 goes on												
28 Check VSI volts for +25.00 to 26.00 VDC												
29 Adj. VSI for +24.00 VDC												
30 S4 up												
31 S4 down												
32 End of Test												

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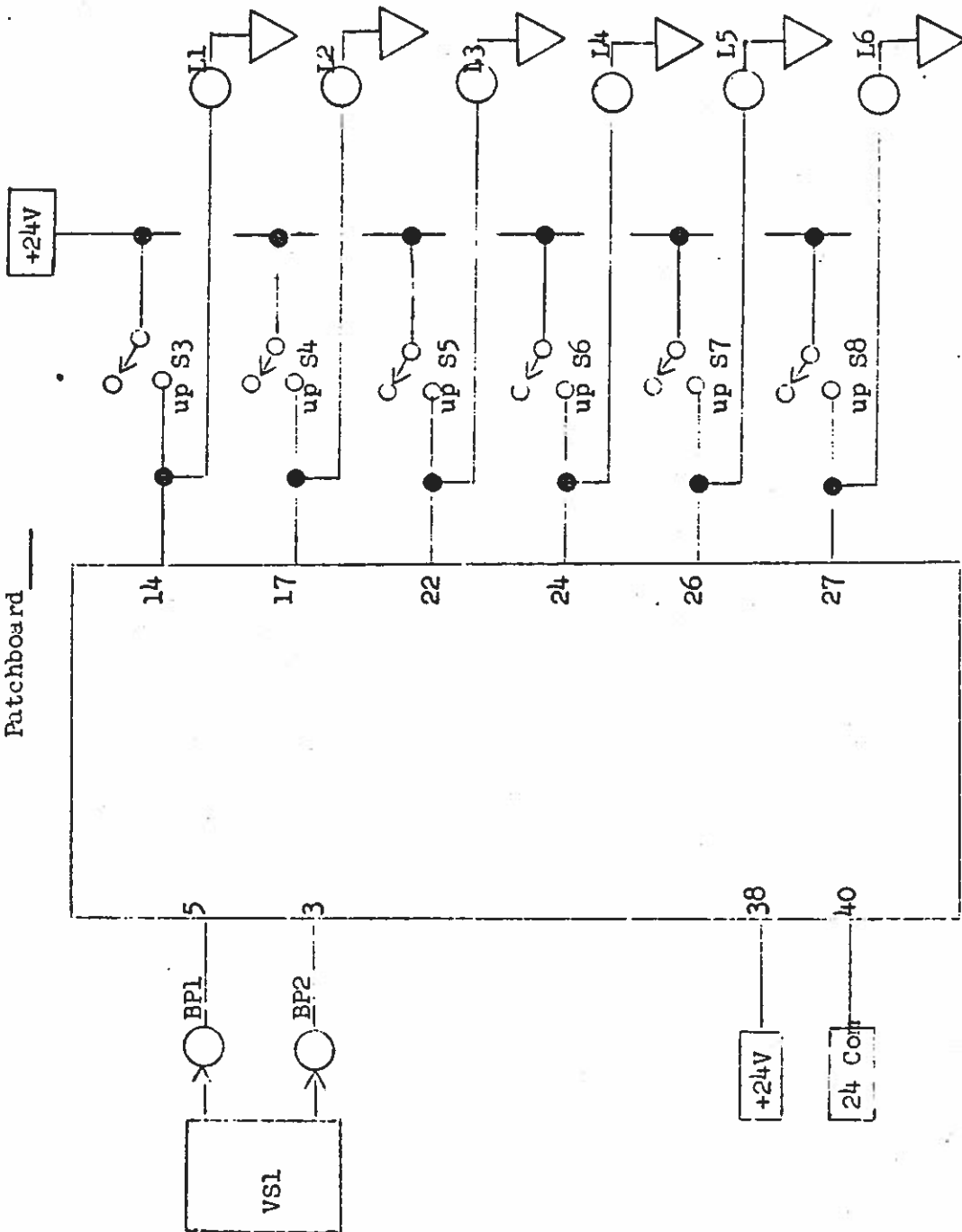
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BOARD TEST SPECIFICATION - VOLTAGE SENSOR, 24 VDC
 1P3-EO05 - SCHEMATIC 117D7356
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Figure A

Patchboard



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BOARD TEST SPECIFICATION - VOLTAGE SENSOR, 24 VDC
1P3-E005 - SCHEMATIC 117D7368

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PREPARED BY

C.J. Barrigher

DATE

3/8/73

C.J. Barrigher
EHC DESIGN ENGINEERING

APPROVED BY

P.C. Callan

DATE

6-4-73

P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE
PREPARED BY

C. Bugg

DATE

5/15/73

C. Bugg
EHC TEST ENGINEER

TEST PROCEDURE APPROVED BY

C.J. Barrigher

DATE

5/29/73

C.J. Barrigher
EHC DESIGN ENGINEERING

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MADE BY *D.P. Mac* *June 11, 1973*
ISSUED *5/22/73*

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