TITLE
TEST INSTRUCTIONS FOR SPEED ERROR FILTER (SEF)
FIRST MADE FOR MHC MARK II

REVISIONS

## I. SCOPE

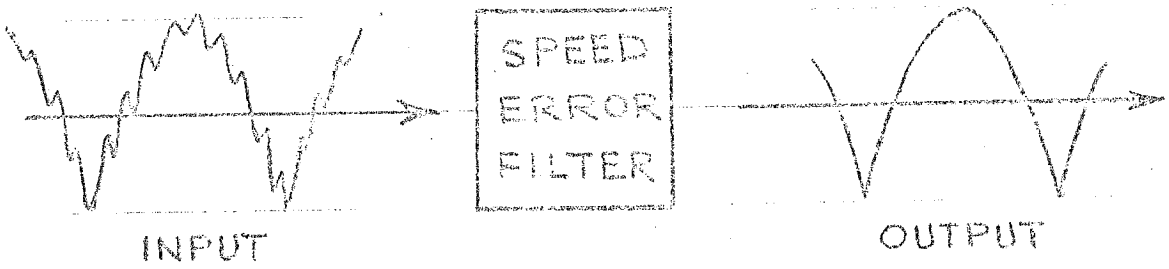
This test instruction outlines the specifications for the Mark II Speed Error Filter circuit board (originally referred to as Dynamic Dead Band).

| | |
|---|---|
| Circuit Board | 143D1129 G1 |
| Schematic | 142D7535 |
| Ident. No. | 1S1-E001 |

## II. CIRCUIT DESCRIPTION

The Speed Error Filter (SEF) circuit is designed to track all slow changes in Speed Error from DC up to 0.2 HZ, but attenuate all rapid fluctuations (frequencies > 0.2 HZ) which fall within a small window about the speed error signal. The net affect of the SEF circuit is to "clean up" the speed error signal in order to cut down on needless valve motion.

If the line frequency is changing rapidly, the speed error will reflect these variations on a 1 to 1 basis, and in turn cause needless valve motion. In other words, the purpose of the SEF circuit is to track the grid for regulation purposes but attenuate fluctuations which are occurring about the grid frequency.




Another important function of the SEF circuit is to track all fast changes which exceed the window. The SEF circuit employs a floating window (referred to as the dynamic dead band) which centers itself about the DC level. Whenever the DC level changes, the window moves and recenters itself about the new level. If the DC level is slowly varying (typical rate is 10 sec. or 0.1 HZ), the window will track the DC level and remain centered. If a rapid change is riding on the DC level and falls within the window, the fast change will be attenuated or smoothed out. If the level changes in a step fashion and exceeds the window, the circuit will track the input.

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II. CIRCUIT DESCRIPTION (continued)

The SEF window contains an adjustable single stage low pass filter. The break point of the lag circuit is adjustable from 0.1 HZ to 5 HZ. The break point is typically set at about 0.2 HZ in order to achieve 5/1 attenuation of a 1 HZ sinewave.

The SEF window is adjustable from zero to ± 50 mV. The window is typically set at about ± 30 mV (Note that 60 mV change in speed error is equivalent to 0.06% change in speed).

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## III. CIRCUIT SPECIFICATIONS

### A. Power Supply Requirements

+Power Supply: +22.000 ± .002 VDC
(Pin 37) (plus supply draws approx. 90 ma)

-Power Supply: -22.000 ± .002 VDC
(Pin 41) (minus supply draws approx. 70 ma)

### B. Operating Signal Levels
(Pins 33, 34)

DC Input Level = +10V to -10V

AC Input Level = 0 to 1V p-p

Frequency Range = 0.1 to 500 HZ

Input Noise Suppression Lag = 80 ± 5 HZ

### C. Output Load
(Pins 17, 18, 19, 20)

750 Ω ± 5% (Fixed)

### D. Zener Regulation Voltages

TP1 = +15.7 VDC ± 1.0V
TP2 = -15.7 VDC ± 1.0V

### E. Overall Characteristics (TP3/TP8)

DC Gain = +1.000 V/V for all input changes from -10.0 VDC to +10.0 VDC Apply input to pin 8 output on pin 3

Inherent Offset = zero ± 6 mV (no adjustment)

Output Limited to ± 10.0 VDC ± .50V

Window Adjust

Range: Max. = 50 mV ± 5 mV (VR1, max. CW)
Min. = 0 mV ± 3 mV (VR1, max. CCW)

III. CIRCUIT SPECIFICATIONS (continued)

E. (continued) Set VR1 for 30mV @ TP6

Setpoint: = +30 mV @ TP6 with input grounded

TP6 = +30 mV, TP5 = $\binom{+0\ mV}{-5\ mV}$, TP7 = -30 mV (varies between -30 mV to -35mV)

Window Response Adjust (Response within window)
(input AC signal amplitude less than window)

Range: Max. Response — VR2 max. CCW
Lag Bkpt @ 5.3 ± .5 HZ

Min. Response — VR2 Max. CW
Lag Bkpt @ 0.1 ± 0.01 HZ

Setpoint: Adjust VR2 for 5/1 attenuation of 1 HZ
(50 mVp-p input, 10 mVp-p output)
Lag Bkpt. at 0.2 HZ
Window = ± 30 mV

NOTE: VR2 adjusts tracking response of window (quickness of window to recenter when input change occurs), which in turn sets small signal response (response within window).

Large Signal Response (Response outside window)
(input AC signal amplitude exceeds window)

$V_{in}$ = 1Vp-p sinewave for frequency of 0.1 to 30 HZ

$V_{out}$ = 1Vp-p sinewave; frequency same as input

Overall Response: $V_o/V_i$ = TP3/TP8 = Lag Bkpt @ 80 ± 10 HZ

Speed Error Filter Oscillations

$V_{out}$ must be free of Hi frequency oscillations, when capacitors (100 pf, .001 uf, .01 uf and .1 uf) applied across load.

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## IV. TEST INSTRUCTIONS

1. Check Power Supply Voltages @ TP1 & TP2

   TP1 = +15.7 VDC ± 1V

   TP2 = -15.7 VDC ± 1V

2. Check inherent offset @ TP3

   Ground input @ TP8 and check that output @ TP3 is zero ± 6 mVDC

3. Preliminary Adjustments

   Adjust VR1 max. CCW (zero window)

   Adjust VR2 max. CCW (max. response)

   With input grounded @ TP8, check that TP3, TP4, TP5, TP6, TP7 near zero (±6 mV)

   Remove ground from input. TP8

4. Check overall DC gain ($V_o/V_{in}$ = +1.0 V/V)
   (Load Resistor = 750Ω)

   Use digital power supply to apply input and DVM to check voltages.

   Apply +1.000 VDC input @ TP8; check that output @ TP3 = +1.000V (±6mV)
   Apply +5.000 VDC input @ TP8; check that output @ TP3 = +5.000V (±6mV)
   * Apply +10.000VDC input @ TP8; check that output @ TP3 = +10.000V ~~(±20mV)~~ ±200mV
   Apply -1.000 VDC input @ TP8; check that output @ TP3 = -1.000V (±6mV) 10/17/88
   Apply -5.000 VDC input @ TP8; check that output @ TP3 = -5.000V (±6mV)
   * Apply -10.000VDC input @ TP8; check that output @ TP3 = -10.000V ~~(±20mV)~~ ±200mV

* Input Limiter zeners CR3 & CR4 may start limiting at less than 10V. If this happens and board approaches 10V ~~before~~ when limiting starts, it is still acceptable.

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IV. TEST INSTRUCTIONS (continued)

5. Check that output is limited to ±10.0V (± .5V)

Use Digital Power Supply to apply input and DVM to check output.

Apply +11V @ input TP8; check that output @ TP3 is limited to +10.0V.

Apply -11V @ input TP8; check that output @ TP3 is limited to -10.0V.

OK

6. Check frequency response of input filter (TP4/TP8)

(Input lag @ 80 HZ)

Use Function Generator HP 3310B to apply input and scope to check output.

Apply 1Vp-p of 150 HZ sinewave @ input TP8; check that output @ TP3 approx. .5Vp-p.

Apply 1Vp-p of 300 HZ sinewave @ input TP8; check that output @ TP3 approx. .25Vp-p.

7. Check Frequency response of overall circuit (TP3/TP8)

(Input lag @ 80 HZ, Output lag @ 338 HZ)

Use Function Generator HP 3310B to apply input and scope to check output.

Apply 1Vp-p of 500 HZ sinewave @ input TP8; check that output @ TP3 approx. .1Vp-p.

Apply 1Vp-p of 900 HZ sinewave @ input TP8; check that output @ TP3 approx. .033Vp-p.

8. Check max. range of window adjustment (VR1)

Ground input @ TP8; Adjust VR1 max. CW.

Check window range as follows:

TP6 = +50 mV (±5 mV)

TP5 = zero (±5 mV)

TP7 = -50 mV (±5 mV)

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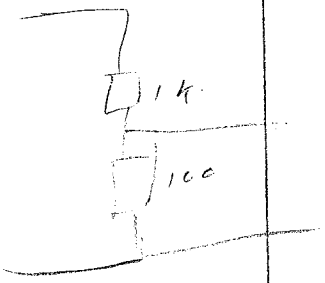
IV. TEST INSTRUCTIONS (continued)




9. Final Window Setting of VR1

Ground input @ TP8; Adjust VR1 until TP6 = +30 mV.

Check that TP6, TP5 and TP7 are set as follows:

TP6 = +30 mV
TP5 = zero (varies from zero to -5mV)
TP7 = -30 mV (varies from -30mV to -40mV)

Remove ground from input.

10. Check max. small signal response (Input amplitude less than window)

Adjust VR2 full CCW (Bkpt @ 5.3 HZ)

Use Function Generator HP 3310B (Lo Output) to apply input.

Use Chart Recorder to check response; Refer to Fig. 1B

Apply 40 mVp-p of 5 HZ @ input TP8; check output @ TP3 = 28 mVp-p

Apply 40 mVp-p of 10 HZ @ input TP8; check output @ TP3 = 16 mVp-p

Apply 40 mVp-p of 20 HZ @ input TP8; check output @ TP3 = 8 mVp-p

11. Check min. small signal response (Input amplitude less than window)

Adjust VR2 full CW (Bkpt @ .1 HZ)

Use Function Generator HP 3310B (Lo Output) to apply input.

Use Chart Recorder to check response; Refer to Fig. 1A.

Apply 40 mVp-p of .1 HZ @ input TP8; check output @ TP3 = 28 mVp-p

Apply 40 mVp-p of .2 HZ @ input TP8; check output @ TP3 = 16 mVp-p

Apply 40 mVp-p of .4 HZ @ input TP8; check output @ TP3 = 8 mVp-p

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IV. TEST INSTRUCTIONS (continued)

12. Final small signal response setting of VR2

(Input amplitude less than window)

Adjust VR52 for 5/1 attenuation of 1HZ.

Use Chart Recorder to set attenuation; Refer to Fig. 2

Apply 50 mVp-p of 1HZ sinewave @ input TP8; Adjust VR2 until output @ TP3 = 10 mVp-p.

13. Check combined step response & small signal response

(Step changes greater than window & small signals less than window)

Apply 50 mVp-p of 1HZ sinewave @ TP8; check for 5/1 attenuation @ output TP3.

Use Chart recorder to check attenuation; Refer to Fig. 3

Apply DC offset (both +100 mV and -100 mV steps).

Note that output tracks step changes, but attenuates 1 HZ sinewave.

14. Check Large Signal Response (Input amplitude exceeds window)

Use chart recorder to check response; Refer to Fig. 4

Apply 1.0 Vp-p of .1 HZ @ TP8; check that output tracks input.

Apply 1.0 Vp-p of 1 HZ @ TP8; check that output tracks input.

Apply 1.0 Vp-p of 10 HZ @ TP8; check that output tracks input.

15. Check SEF for HI frequency oscillations

Ground input @ TP8.

Use scope to check for Hi frequency oscillations @ output TP3.

Apply 100 pf (in parallel with scope) across output load @ recheck for oscillation.

Apply .001 uf across output load @ recheck for oscillation.

Apply .01 uf across output load @ recheck for oscillation.

Apply .1 uf across output load @ recheck for oscillation.

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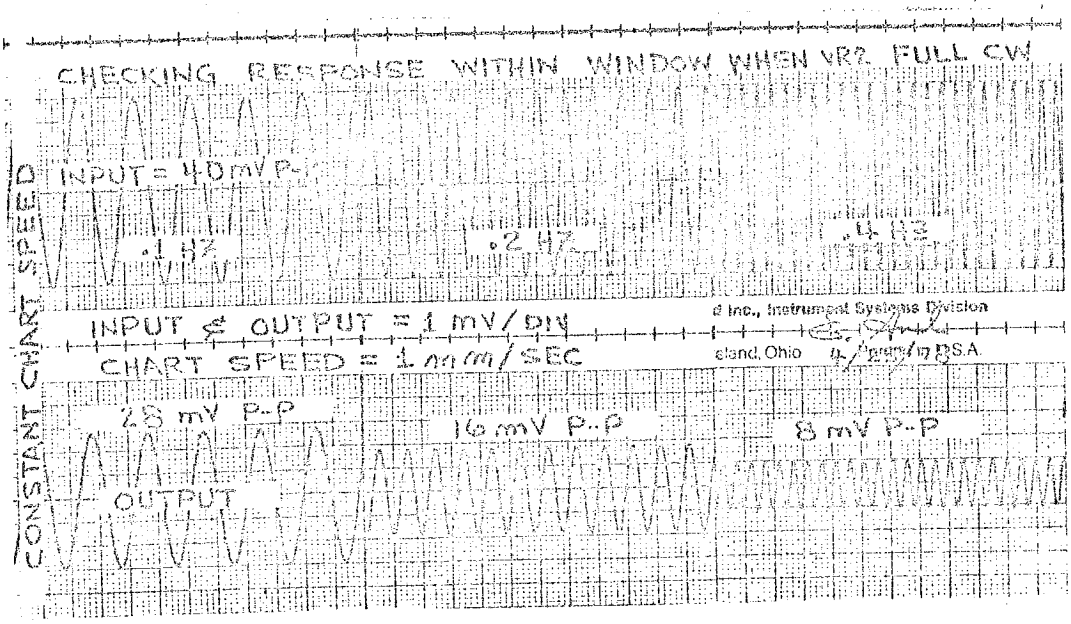
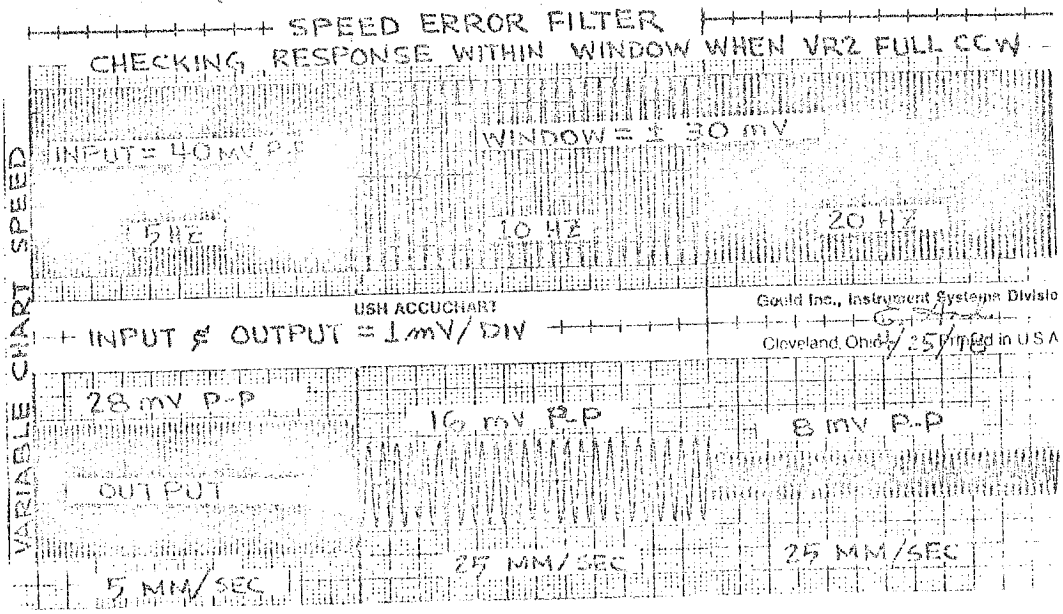
## FIG 1A SPEED ERROR FILTER
(MIN RESPONSE WITHIN WINDOW)




## FIG 1B SPEED ERROR FILTER
(MAX RESPONSE WITHIN WINDOW)

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APPROVALS

Steam Turbine DIV OR DEPT.
Schenectady, N.Y. LOCATION

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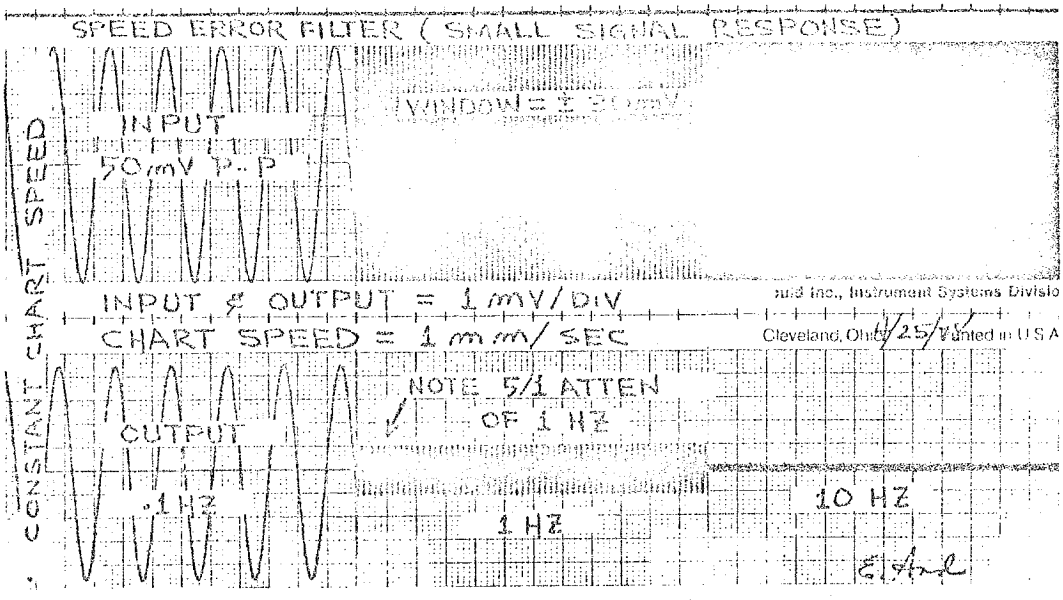
# FIG 2 SPEED ERROR FILTER

## SMALL SIGNAL RESPONSE
## (INPUT LESS THAN WINDOW)



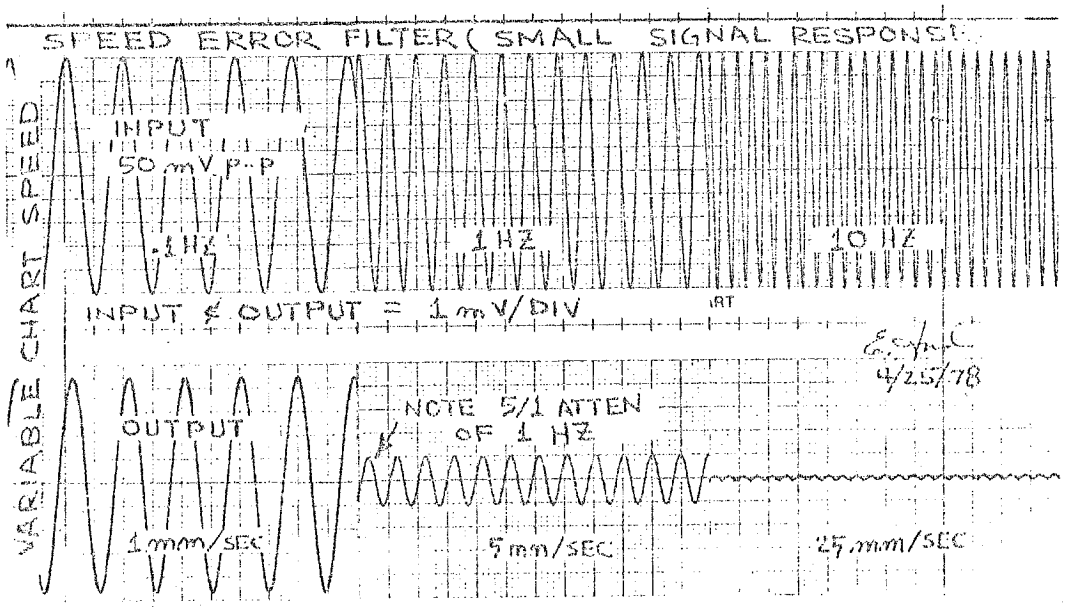




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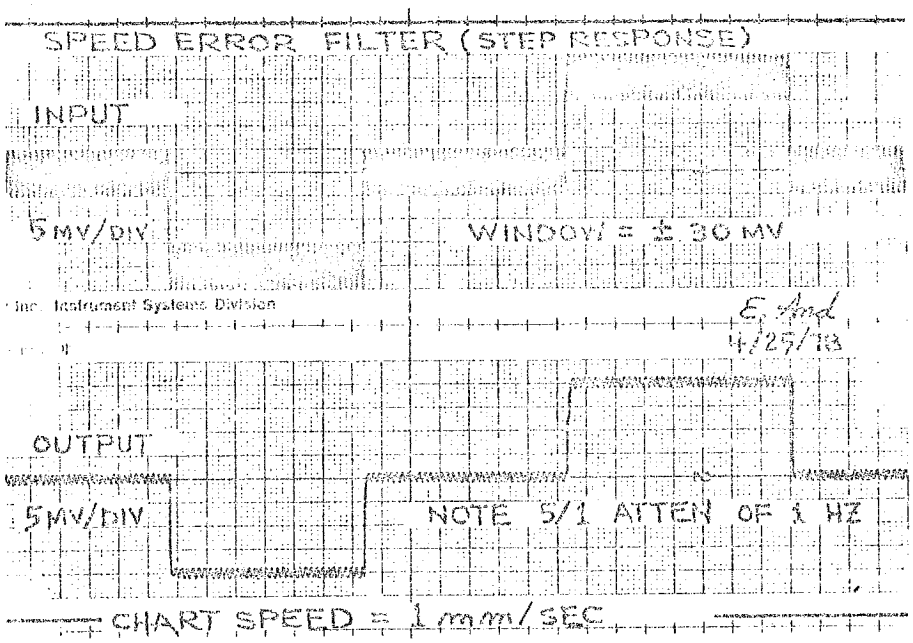
FIG 3 MK II "SPEED ERROR FILTER"

STEP RESPONSE



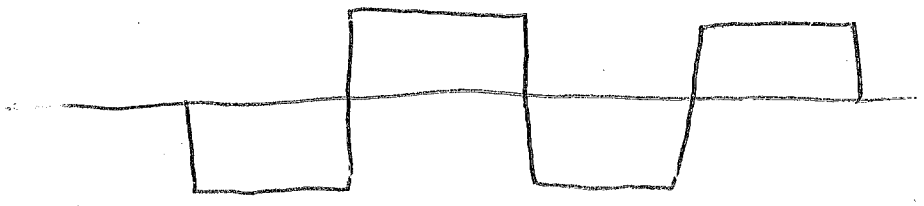



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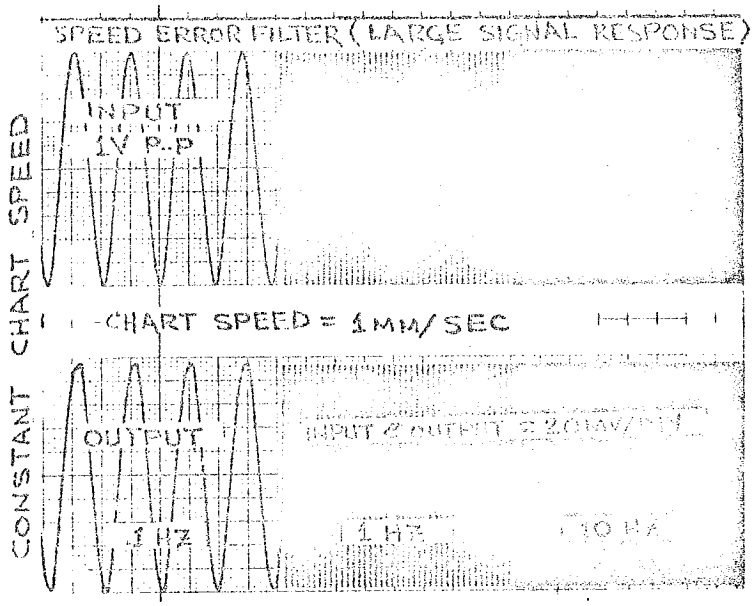
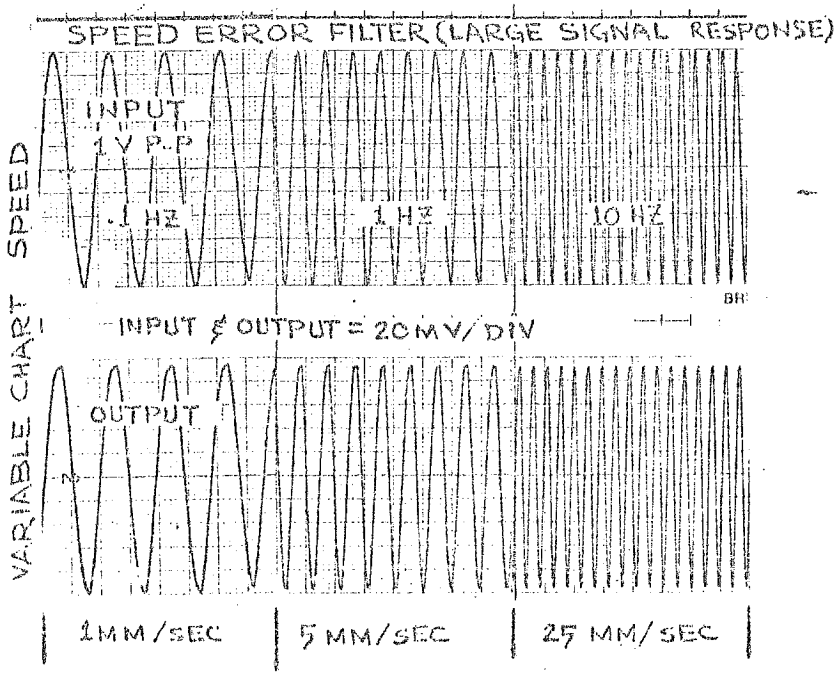
FIG 4 "SPEED ERROR FILTER"
LARGE SIGNAL RESPONSE
(INPUT GREATER THAN WINDOW)



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TEST INSTRUCTIONS FOR SPEED ERROR FILTER (SEF)

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APPROVED BY: R L Olson DATE 5/30/78

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