

REV NO. 0

P3K-AL-0389-A01

TITLE

TEST INSTRUCTIONS FOR BACKUP OVERSPEED TRIP TEST CIRCUIT  
BOARD 1TM2-D001

CONT ON SHEET 2 SH NO. 1

FIRST MADE FOR EHC MARK II (ASS'Y DRAWING 117D9946 G1)

REVISIONS

# I. CIRCUIT DESCRIPTION

CIRCUIT BOARD REV. 1

This circuit performs the operations necessary for the testing of the backup overspeed trip system.

The board contains 6 latching and 3 nonlatching 24 VDC relays.

# II. CIRCUIT SPECIFICATIONS

The circuit consists of three identical interconnected parts; thus to specify its logic function it is sufficient to compile a truth table for one of these parts and apply it to all three, in three series of tests.

Table I gives for each test series the actual pin numbers that correspond to the "given pin names". These are simply the headings of Table II, which specifies the logic function of the circuit.

During the tests 24 VDC should be connected to pin 38 and 24 VDC ground to pin 40. In Table II 1 means 24 VDC and 0 means OV.

TABLE I

GIVEN PIN NAMES	TEST 1	TEST 2	TEST 3
A	KL1*1 25	KL2-115	KL3-424
B	KL4*4 21	KL5-1 22	KL6-1 14
C	32	2	28
D	4	36	5
E	16	27	26
F	18	20	17
G	27	26	16
H	20	17	18
I	26	16	27
J	17	18	20
K	RESET 19	19	19

273-2

273-12

273-71

273-138

273-221

273-227

PRINTS TO

MADE BY J. Polacek Sept. 16, 1977

APPROVALS

Steam Turbine

DIV OR DEPT.

P3K-AL-0389-A01

ISSUED

Sept 16, 1977

Schenectady, N.Y.

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SH NO. 1

## II. CIRCUIT SPECIFICATIONS (continued)

TABLE II

### INPUTS AT PINS

### CORRECT OUTPUTS AT PINS

A B E G I K

C D F H J

0 0 0 0 0 0

0 0 0 0 0

1 0 0 0 0 0

1 0 0 0 0

0 0 0 0 0 0

1 0 0 0 0

0 0 0 1 1 0

1 0 0 0 0

0 0 0 0 0 0

1 0 0 0 0

0 0 0 0 0 1

0 0 0 0 0

0 0 0 0 0 0

0 0 0 0 0

0 1 0 0 0 0

0 1 0 0 0

0 0 0 0 0 0

0 1 0 0 0

0 0 0 1 1 0

0 1 0 0 0

0 0 0 0 0 0

0 1 0 0 0

0 0 0 0 0 1

0 0 0 0 0

0 0 0 0 0 0

0 0 0 0 0

0 0 1 0 0 0

0 0 1 0 0

0 0 1 1 1 0

0 0 1 0 0

0 0 0 0 0 0

0 0 0 0 0

The following two items should be checked separately:

a. Continuity between pins 9 and 19.

b. Appearance of a voltage at pins 32, 4, 2, 36, 28, and 5 when 24 VDC is applied to pin 23. This voltage is 24 VDC at no load, but is dropping when loaded according to the load resistance (68.1 Ohms internal resistance at each pin).

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REV. NO. 0

CONT ON SHEET -- SH NO. 3

P3K-AL-0389-A01

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TEST INSTRUCTIONS FOR BACKUP OVERSPEED TRIP TEST CIRCUIT  
BOARD 1TM2-D001

CONT ON SHEET -- SH NO. 3

FIRST MADE FOR EHC MARK II (ASS'Y DRAWING 117D9946-G1)

REVISIONS

PREPARED BY

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DATE

*2/21/74*

D. Economou  
EHC DESIGN ENGINEERING

APPROVED BY

*P.C. Callan*

DATE

*9-6-77*

P.C. Callan - MANAGER  
EHC DESIGN ENGINEERING

TEST PROCEDURE

REVIEWED BY

*R. Debertolis*

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*4/6/77*

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EHC TEST ENGINEER

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MADE BY  
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