REV NO. Ø1	TITLE
P3K-AL-0707-A01	TEST SPECIFICATION FOR THRUST BEARING WEAR DETECTOR TEST LOGIC (1TM2-S201)
CONT ON SHEET 1A SH NO. 1	FIRST MADE FOR EHC MARK IIA

REVISIONS

1 KPAulisi SEP 8 1982 chgs made

I. CIRCUIT DESCRIPTION

This circuit board is designed to provide the Sequential Logic that is necessary for testing of the Thrust Bearing Wear Detector. There are two redundant circuits on this board; one to test the Upper Thrust Bearing Wear Detector and one to test the Lower Thrust Bearing Wear Detector.

The circuit board is identified as follows:

TBWD Test Logic -- 1TM2-S201 Schematic - 145D2479
Assembly - 186C8150 G1

II. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

V1: +24 ± 4.0% VDC at 200 mA max.

B. Operating Signal Levels

Inputs +24 VDC ± 4.0%.

C. Output Loads

1. R1: Pins 18, 20, 22, 24 - IL Lamp 40 mA at 28 VDC
   Equivalent Load - 700Ω ± 10% at 1 Watt

2. R2: Pins 26, 28, 30, 32 - 24 VDC K-Relay -- Coil Resistance 472Ω ± 10% at 2 Watts

III. CIRCUIT OPERATION

A. TBWD Test Circuit

Attach required loads to Pins 18, 20, 22, 24, 26, 28, 30 and 32. As shown in Figure 1.

B. Power Supply

NOTE: This board is to be tested over the full range of power supply tolerances.

PRINTS TO
273-314
273-5
~~273-2~~
273-12²
273-71
273-138
~~273-221~~
~~273-227~~

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ISSUED MAY 25 1982		Schenectady, N.Y. LOCATION	CONT ON SHEET 1A SH NO. 1

REV NO. 1

P3K-AL-0707-A01
CONT ON SHEET 2 SH NO. 1A

TITLE
TEST SPECIFICATION FOR THRUST BEARING WEAR DETECTOR TEST LOGIC (1TM2-S201)

FIRST MADE FOR .EHC MARK IIA

REVISIONS

SEP 8 1982 O.J.Aulisi new art added

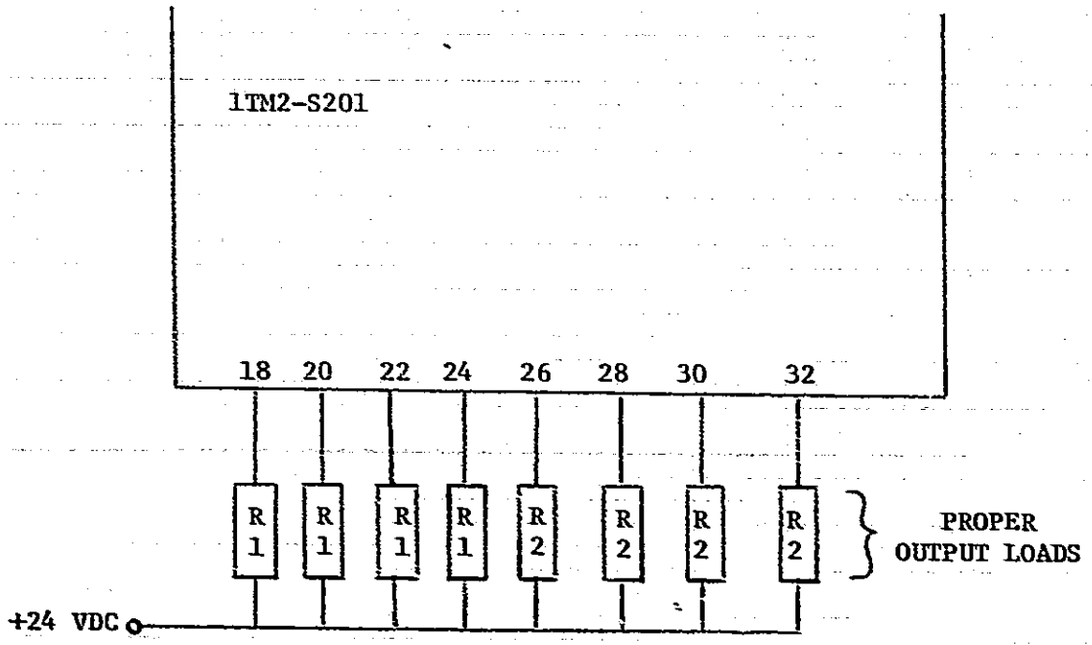

FIGURE 1 - LOAD CONFIGURATION DIAGRAM

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CONT ON SHEET 2 SH NO. 1A

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III. CIRCUIT OPERATION (continued)

B. Power Supply (continued)

1. Connect +24 VDC to Pin 38.
2. Connect 24 VDC common to Pin 40.
3. Note that DS1 (GN) is lit.
4. Measure +5 VDC ± 5.0% between TP2 (+) and TP1 (-).
5. **Measure +24 VDC ± 5.0% at output Pins 18, 20, 22, 24, 26, 28, 30 and 32. These measurements represent the initial power-up state of the board as it will be in the EHC cabinet.**

C. Timer Test

1. **Momentarily apply +24 VDC to Pin 3.**
2. Measure the duration of a TTL high level pulse (approx. 3.5 to 5 VDC) at TP50. This pulse should last 3 seconds ± 10% from the time the +24 VDC signal is removed from Pin 3.
3. Momentarily apply +24 VDC to Pin 7.
4. Measure the duration of a TTL high level pulse at TP51. This pulse should last 3 seconds ± 10% from the time the +24 VDC signal is removed from Pin 12.

D. Logic Truth Table

The following truth table should be used to perform a functional test of the circuit board logic. Input signals that are indicated as being at logic level "0" do not have to be tied to +24 VDC common.

Logic Level Definition

1 - +24 VDC ± 5.0%

0 - +24 VDC Common

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TEST SPECIFICATION FOR THRUST BEARING WEAR DETECTOR TEST LOGIC (1TM2-S201)
FIRST MADE FOR EHC MARK IIA

	INPUT PIN NUMBERS						OUTPUT PIN NUMBERS							
STEP #	3	15	5	7	13	9	28	24	22	32	26	18	20	30
1	0	0	0	0	0	0	1	1	1	1	1	1	1	1
2	0	1	0	0	0	0	0	1	1	1	1	1	1	1
3	0	1	1	0	0	0	0	1	0	0	1	1	1	1
* 4	1	1	1	0	0	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	0	0	1	0	1	1	1	1	1
6	0	0	1	0	0	0	**	1	0	1	1	1	1	1
7	0	0	0	0	0	0	1	1	1	1	1	1	1	1
8	0	0	0	0	1	0	1	1	1	1	0	1	1	1
9	0	0	0	0	1	1	1	1	1	1	0	1	0	0
*10	0	0	0	1	1	1	1	1	1	1	0	0	0	0
11	0	0	0	1	0	1	1	1	1	1	0	1	0	1
12	0	0	0	0	0	1	1	1	1	1	***	1	0	1
13	0	0	0	0	0	0	1	1	1	1	1	1	1	1

** NOTE: Pin 28 will attain a high logic level 3 seconds ± 10% after +24 VDC is removed from Pin 3.

*** NOTE: Pin 26 will attain a high logic level 3 seconds ± 10% after +24 VDC is removed from Pin 7.

* NOTE: Care should be taken when applying +24 VDC to Pins 3 and 7 so that the SE555 timer is not falsely triggered.

E. Lamp Test

1. Apply +24 VDC to Pin 11.

2. Measure logic level "0" at Pins 18, 20, 22 and 24.

REVISIONS

1	J.Aulisi SEP 8 1982	NO CHG. THIS SHT.

PRINTS TO

GENERAL ELECTRIC

REV NO. Ø1	P3K-AL-0707-A01 CONT ON SHEET -- SH NO. 4
P3K-AL-0707-A01 CONT ON SHEET -- SH NO. 4	TITLE TEST SPECIFICATION FOR THRUST BEARING WEAR DETECTOR TEST LOGIC (1TM2-S201)
	FIRST MADE FOR EHC MARK IIA

REVISIONS

1	PAulisi SEP 8 1982	NO CHG. THIS SHT.

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