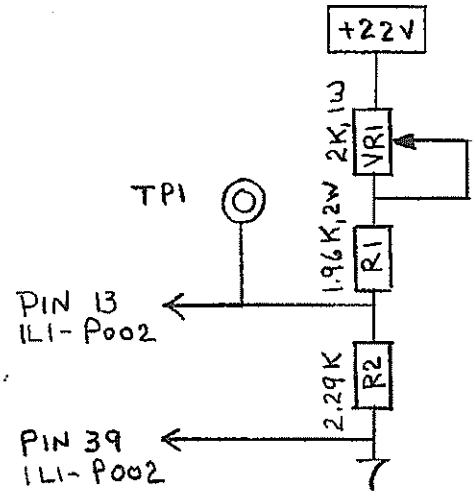


FIGURE 1

NOTE: 1. Resistor R2
1W, 1%

2. Adjust VR1 for 11 VDC at TP1, prior to connection to board 1L1-P002

9.1.0 SCOPE

This document establishes the performance requirement and recommended test for the 6.9KV Power Electronics Gating Module identified as:

DS5220PEG

This specification will check the output tolerances based on a known input.

9.2.0 Test Equipment and Documentation

9.2.1 Standard Equipment Required

The following instrumentation is needed:

(a) 2 channel oscilliscope $\geq$100 MHZ badnwidth.

(b) 0-2 Amp AC ammeter.

(c) A signal generator capable of delivering a pulse train consisting of square pulses of variable width and 22.22 KHZ frequency. The pulse train period shall be 16.67 MS.

9.2.2 Special Equipment Required

(a) AC Source:

This module is designed to operate with a voltage stabilizing transformer input. It is preferred that such a source (rated 250 VA or greater) be used to test this module.

If a standard transformer is used, it should not droop more than 2%.

$$\left[\text{Droop} = \left(\frac{V_{NL}-V_{FL}}{V_{NL}}\right)(100\%)\right]$$

The transformer must have an output of 240V, 60HZ with center tap.

9.3.0 Pin Connections

(a) AC Power:

L1 to AC1
L2 to AC2
Center tap to TB1-1
Ground all four terminals of TB1

| | | | | | | |
|---|---|---|---|---|---|---|
| REV. 1 | REV. 4 | REV. 7 | PRINTS TO DL119 BHC | ENGINEER JLH | GENERAL ELECTRIC SALEM, VA. U.S.A. | POWER ELECTRONICS GATING MODULE |
| REV. 2 | REV. 5 | ISSUED 3-27-84 | | | | DS5220PEG |
| REV. 3 | REV. 6 | MADE BY J. W. Hylton | | | | CONT. ON SH. 9AB SH. NO. 9AA |

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9.3.0 Pin Connections (continued)

(b) Ribbon Header (JA):

Gate input signal to JA1
Gate input common to JA4
Overvoltage input signal to JA10
Overvoltage common to JA8
JA8 and JA10 should be shorted together and to COM when not in use.

(c) Gate Output:

Connect gate pulse transformer loads to Plug JE. Positive gate current will flow out of JE-2 and return thru JE-1. Do not ground the load circuit externally.

(d) Overvoltage Relay Contacts:

Connect ohmmeter to JD1 and JD2. Polarity is unimportant.

9.4.0 Setup and Initial Loading

(a) Connect as shown on the test elem. (Fig. 1)

**********
*        *
*  CAUTION ! !  *
*        *
**********

C1 is charged to 170 volts DC upon application of power. When power is removed, the cap requires two minutes to discharge to 50 volts and approximately ten minutes to discharge completely. The danger area encompasses the entire module including the HPTP card. Before handling, make sure that C1 is discharged. C1 may be discharged in ≈ two seconds by shorting with a 500Ω resistor.

9.5.0

9.5.1 Gate Command Signal

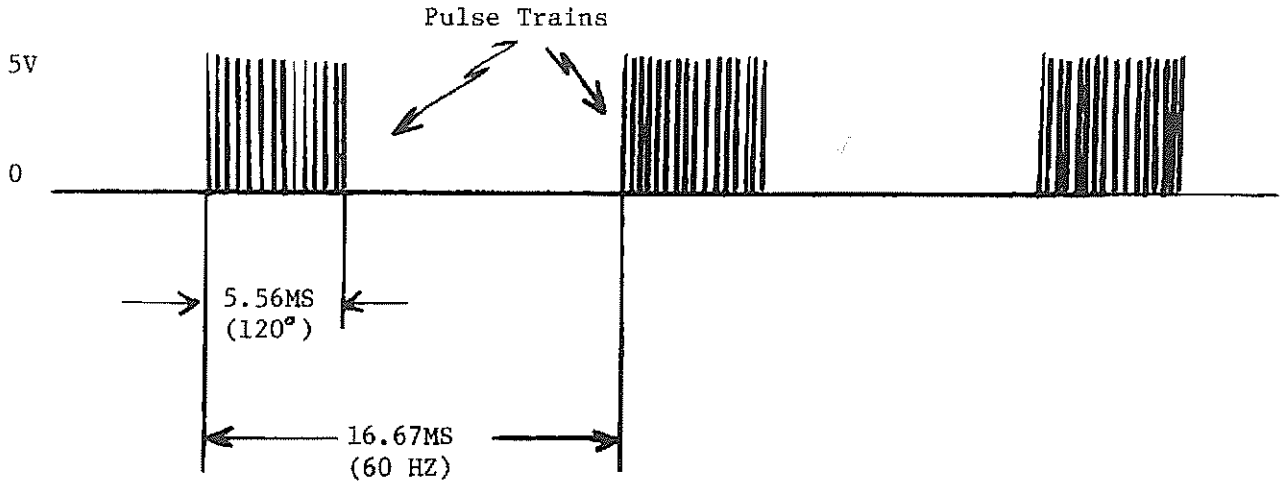


Fig. 9-2 Input Pulse Train

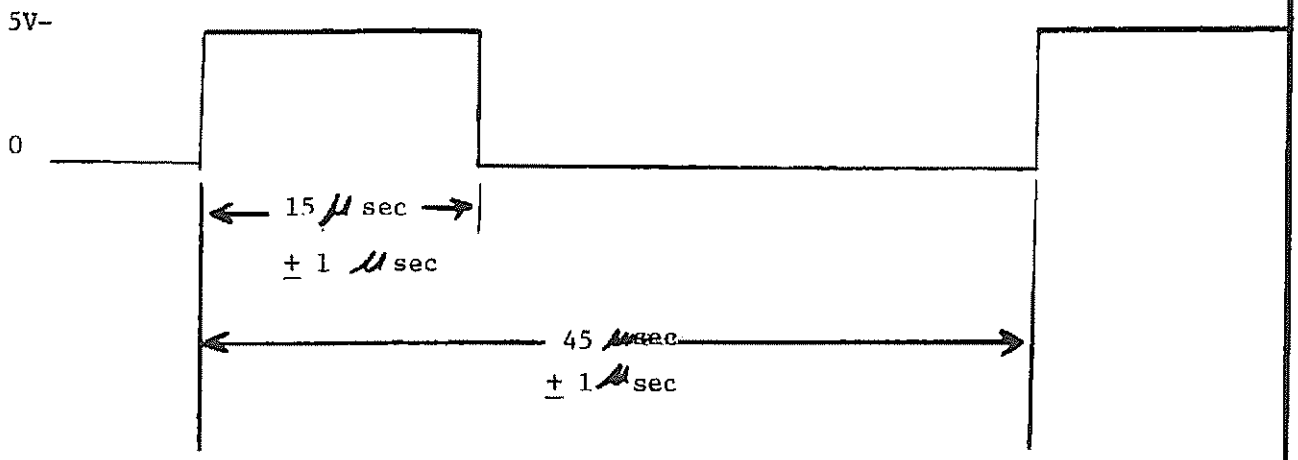


Fig. 9-3 Input Pulse

| | | | | | | |
|---|---|---|---|---|---|---|
| REV. 1 | REV. 4 | REV. 7 | PRINTS TO DL119 BMA | ENGINEER | GENERAL ELECTRIC | POWER ELECTRONICS GATING MODULE |
| REV. 2 | REV. 5 | ISSUED 3-27-84 | | | | |
| REV. 3 | REV. 6 | MADE BY J.W. Hylton | | | SALEM, VA. U.S.A. | DS5220PEG |
| | | | | | | CONT. ON SH. 9AD SH. NO. 9AC |

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9.5.2

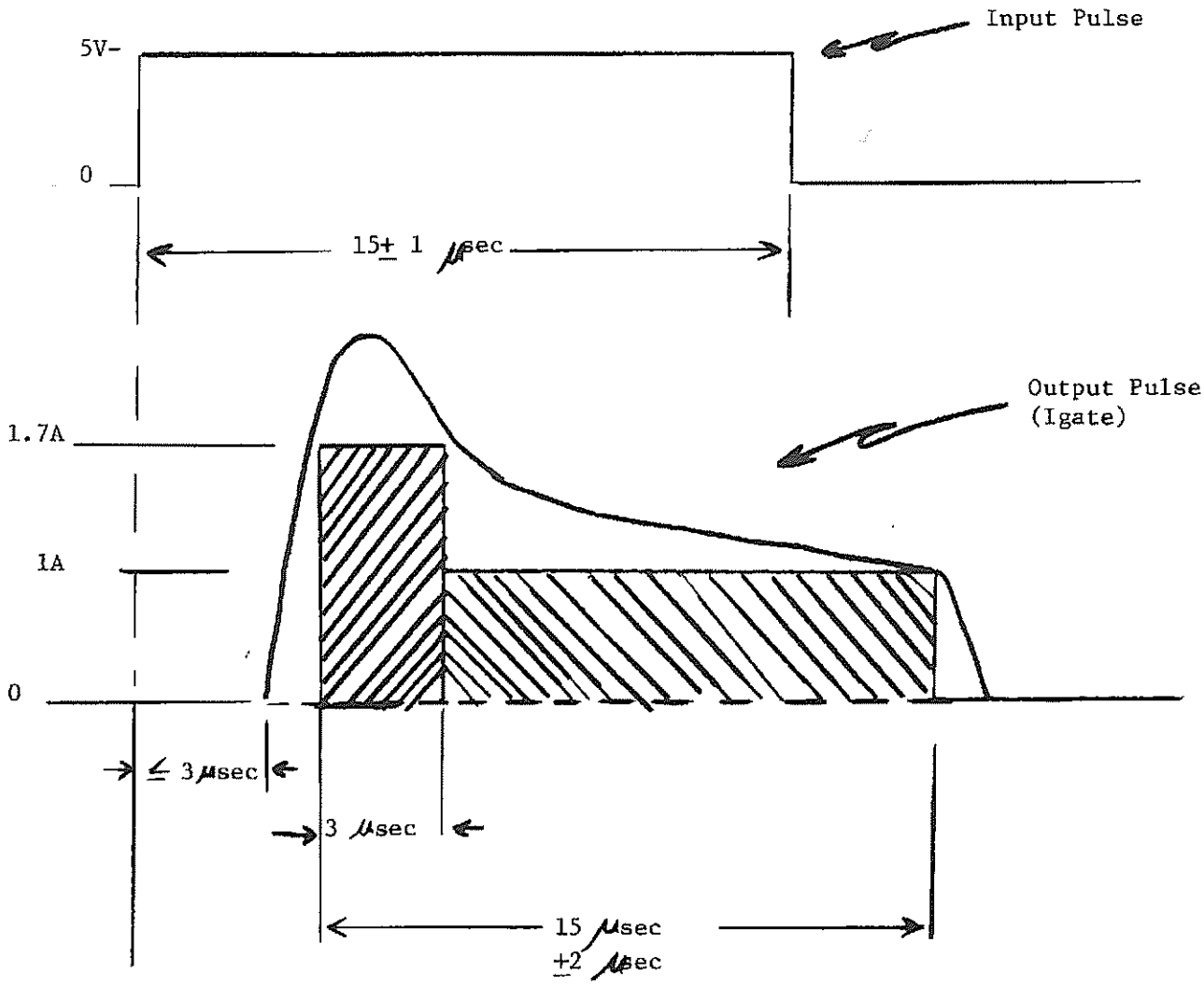


Fig. 9-4 Normal Gate Input and Output

| | | | | | | |
|---|---|---|---|---|---|---|
| REV. 1 | REV. 4 | REV. 7 | PRINTS TO DL119 | ENGINEER | GENERAL ELECTRIC SALEM, VA. U.S.A. | POWER ELECTRONICS GATING MODULE |
| REV. 2 | REV. 5 | ISSUED 3-27-84 | | | | DS5220PEG |
| REV. 3 | REV. 6 | MADE BY J. W. Hylton | | | | CONT. ON SH. 9AE SH. NO. 9AD |

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9.5.3 Overvoltage Command Signal

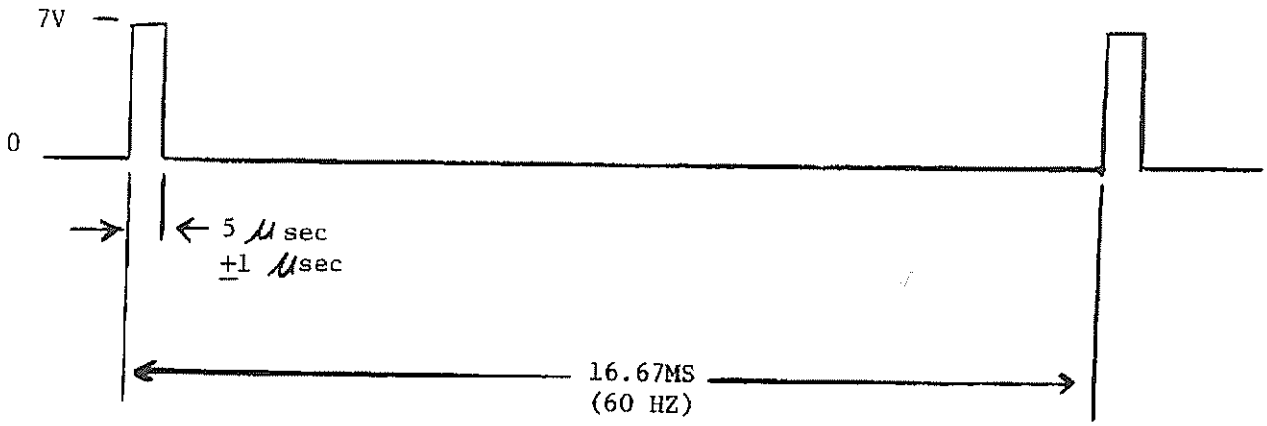


Fig. 9-5 OV Input

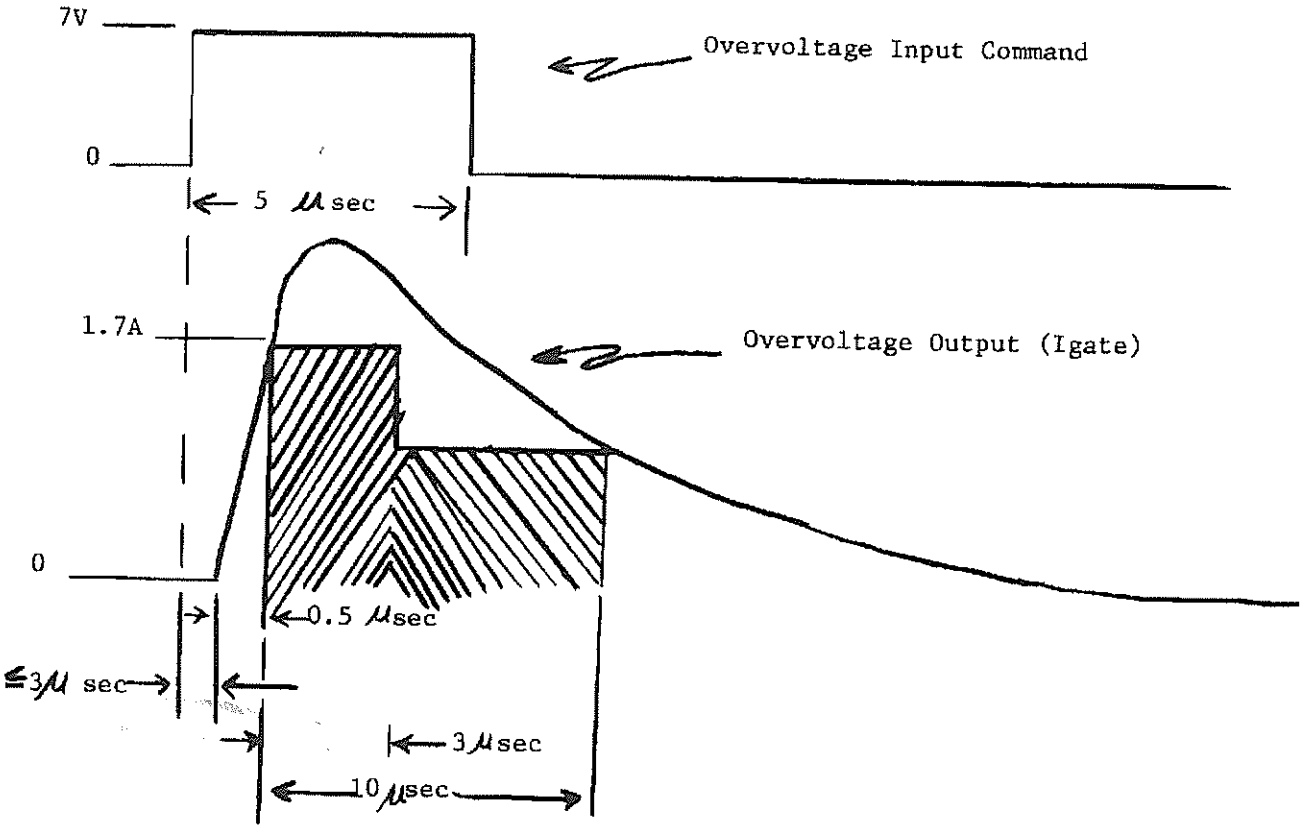


Fig. 9-6 OV I/O

| | | | | | | |
|---|---|---|---|---|---|---|
| REV. 1 | REV. 4 | REV. 7 | PRINTS TO DL119 | ENGINEER | GENERAL ELECTRIC | POWER ELECTRONICS GATING MODULE |
| REV. 2 | REV. 5 | ISSUED 3-27-84 | | | | |
| REV. 3 | REV. 6 | MADE BY J. W. Hylton | | | SALEM, VA. U.S.A. | DS5220PEG |
| | | | | | | CONT. ON SH. 9AF SH. NO. 9AE |

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9.6.0 Test Procedure

9.6.1 Preliminary Inspection

The element shall be inspected prior to application of power to verify that it is assembled according to assembly drawing.

9.6.2 Initial Checks

(a) Remove fuses FU1 and FU2

(b) Apply AC input power

(c) AC input current should be ≤ 0.2A

(d) All LED's should be off

(e) Voltage regulator levels:

All voltages referenced to COM (TPS)

| Regulator | TP | Limits From | Limits To |
|---|---|---|---|
| P15 | 4 | +14.9V | +15.1V |
| N15 | 6 | -14.6V | -15.4V |
| PR10 | 7 | +9.97V | +10.03V |

(f) O.V. Alarm Relay (K1) Contacts, JD1-JD2 should be open

(g) Remove AC power

(h) Replace FU1 and FU2

(i) Apply AC input power

(j) AC input current should be ≤ 0.2A

(k) LED's:

OV Fire (CR50) - off
Fire (CR51) - off
IMOK (CR52) - On

(l) OV Relay, K1

JD1-JD2 should be less than 1Ω.

9.6.4 Output Gate Check

(a) Apply input gate command signal pulse train as shown in Figures 2 and 3.

(b) Output pulse (Igate) as measured with current probe shall be outside the shaded area shown in Figure 4.

(c) LED's:

OV Fire (CR50) - off
Fire (CR51) - on
IMOK (CR52) - on

(d) There shall be no current glitches of $\geq$ 4MA between pulse trains.

(e) Remove input gate command signal.

9.6.5 Overvoltage Gate Check

(a) Apply the overvoltage command signal as specified in paragraph 9.3.0 (B) and Figure 5.

(b) Output (Igate) shall be as shown in Fugure 6.

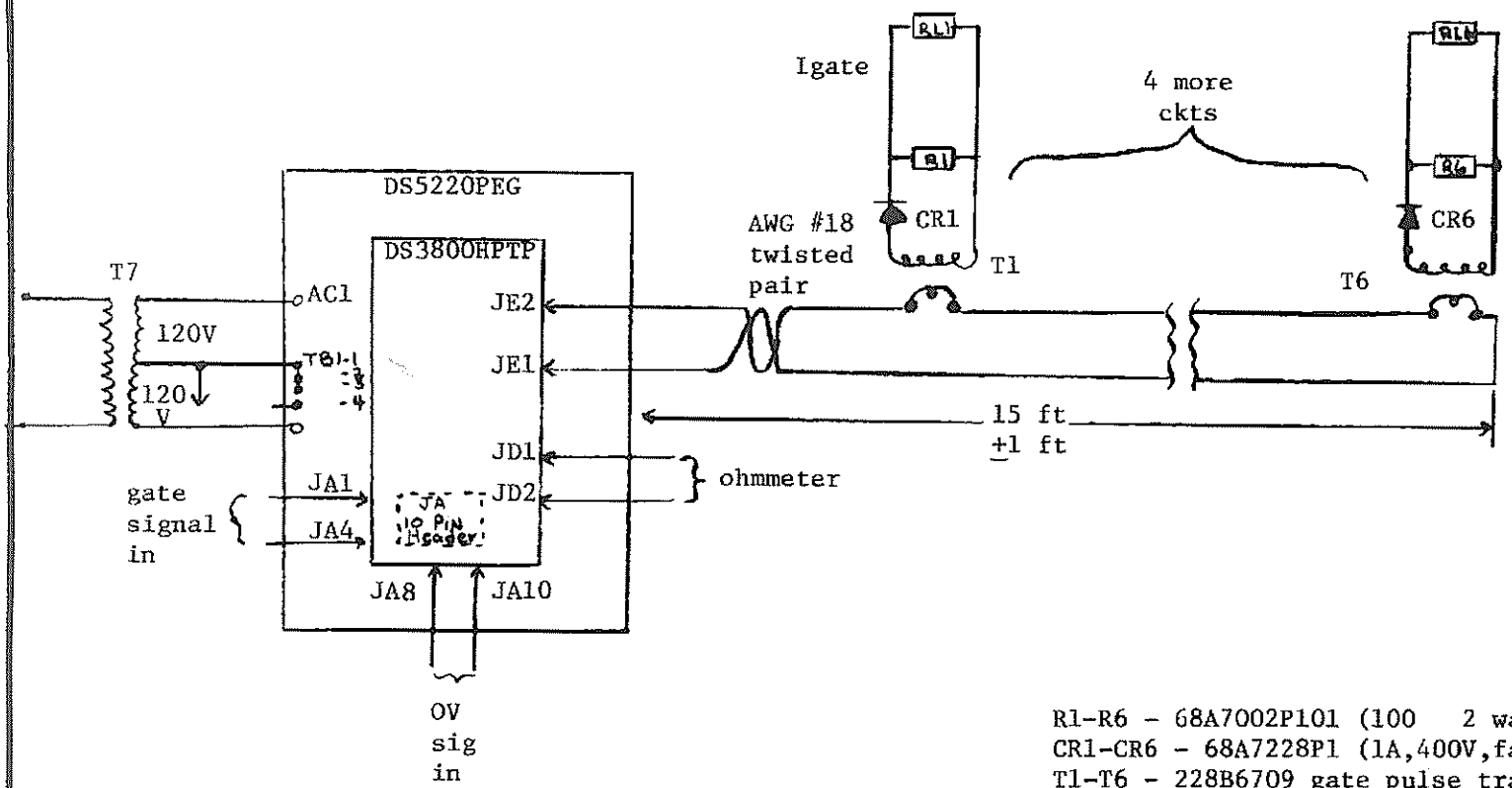
(c) LED's:

"OV Fire" (CR50) - on
"Fire" (CR51) - off
IMOK (CR52) - on

(d) Remove the overvoltage command signal (CR50) "OV Fire" shall remain on.

(e) Press pushbutton SW1 (reset). CR50 shall go off and remain off.

END OF TEST




R1-R6 - 68A7002P101 (100 2 watt)
CR1-CR6 - 68A7228P1 (1A,400V,fast rec)
T1-T6 - 228B6709 gate pulse transformer
T7 - voltage stabilizing transformer,250VA or greater
RL1-RL6 - 15Ω ±0.1 (non inductive) @ 6 watts

Note: This can be a parallel string of 2W resistors trimmed to 15Ω (hot) or a single 15Ω non-inductive stick. Check hot resistance by measuring volts and amps while dissipating 6 watts. (This is normal 120° conduction)

POWER ELECTRONICS GATING MODULE
DS5220PEG CONT. ON SH. FL SH. NO. 9AH
GENERAL ELECTRIC SALEM, VA. U.S.A.
ENGINEER
PRINTS TO DL119
ISSUED 9-27-84
MADE BY J. W. Hylton
REV. 1 REV. 2 REV. 3 REV. 4 REV. 5 REV. 6 REV. 7
DSD 0151 (09-76)