REV NO. 5

TITLE
TEST INSTRUCTIONS TO TBWD POS. IND. 1TM1-A001
(ASSEMBLY DRAWING 117D9105 G1)
FIRST MADE FOR EHC MARK II

ACTIVE FOR P1
BY RC DATE 2/10/97

P3K-AL-0426-A01
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REVISIONS

I. SCOPE

This instruction outlines the test specifications for circuit board 1TM1-A001 (Reference Drawing 117D9105).

II. CIRCUIT DESCRIPTION

The Thrust Bearing Wear Detector Position Indicator Demodulator is an electronic circuit which transforms the output of an LVDT into a DC current suitable for driving a milliammeter.

The circuit operates as follows: The LVDT secondary output voltages are first individually amplitude demodulated and then electronically summed to produce a DC voltage which is proportional to the magnitude of the LVDT differential output voltage, and polarized to indicate the direction of LVDT core position. Extensive filtration is then applied to eliminate 400 HZ ripple from the DC voltage.

In the circuit, Amplitude Demodulation is performed by two half wave rectifier stages, IC1 and IC2. One stage, IC1, produces a positive half wave rectified wave form while the other, IC2, produces a negative one, as illustrated in figure 1.

The operational amplifiers which perform the half wave rectification operate in two distinct states. When diodes CR6 and CR8 are conducting (CR5 and CR7 cut off), the half wave rectifier output votlages are determined by the feedback resistance ($R_F = R_9 = R_{10}$), the input resistance ($R_I = R_3 = R_4 = R_5 = R_6$) and the input capacitance ($C = C_5 = C_6$):

$$\frac{E_{OUT}\ (PEAK)}{E_{IN}\ (PEAK)} = \frac{R_F}{2R_I\left[1 + \frac{R_I\ C\ S}{2}\right]} = 1.327 \angle -45^\circ \quad \text{at 400 HZ}$$

During the "off" state, when diodes CR5 and CR7 are conducting (CR6 and CR8 cut off), resistors R11 and R12 are used to clamp the output voltages at zero volts.

The outputs of the two half wave rectifiers are then filtered, to extract their DC components ($\frac{1}{\pi}$ time their peak value), and electronically added to a variable offset bias, established by VR1, R13, R14 and R17, which compensates for LVDT mechanical offsets of upto $\pm$ 0.3 inches. The filtration and signal summing is done with a single operation amplifier, IC3.

The output of the summer and filter stage, IC3, is then scaled and filtered to produce a low ripple, calibrated DC voltage suitable for high resolution measurements. Two stages of range adjustment facilitate calibration to within $\pm$ 0.001 volts over the $\pm$ 10 volt range. One range adjustment is a voltage divider consisting of R20 and VR2. The second range adjustment is a variable gain operational amplifier, IC4, which also

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273-12
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II. CIRCUIT DESCRIPTION (continued)

serves as an additional filter for 400 HZ ripple:

$$\frac{E_{OUT\ (IC4)}}{E_{IN}} = \frac{(R24 + VR3)}{2\ R_{22}\ (1 + \frac{R_{22}}{2}\ C_9\ S)} \approx \frac{2.5}{1 + 0.025\ S}$$

Current to drive a ± 500 uA panel meter is derived from the range adjust and filter stage output voltage by a large, adjustable resistance (R25 and VR4) which is placed in series with the meter.

III. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

1. Power Supply 1 (Pin 37): +22.000 ± 0.002 VDC at 40 ma (approx.)

2. Power Supply 2 (Pin 41): -22.000 ± 0.002 VDC at 40 ma (approx.)

B. Operating Signal Levels

1. Input 1 (Positive Direction Sensing LVDT Output) (Pin 12): 0 to 5 VRMS at 400 HZ. NOTE: LVDT 5TM1-S002-LT1 produces 1.0 VRMS at -0.3 inches, 2.1 VRMS at Null and 3.8 VRMS at +0.3 inches.

2. Input 2 (Negative Direction Sensing LVDT Output) (Pin 14): 0 to 5 VRMS at 400 HZ. NOTE: LVDT 5TM1-S002-LT1 Produces 3.8 VRM at -0.3 inches, 2.1 VRMS at null and 1.0 VRMS at +0.3 inches.

C. Output Loads

1. Load 1 (Pin 32): 10K Ohm ± 1%

2. Load 2 (Pin 36): 40 Ohm ± 1% (simulates uA meter)

D. Individual Stage Performance Specifications

1. Power Supply (CR1, 2, 3, & 4)

a. V_{TP1}: +15.7 ± 1.0 VDC ✓

b. V_{TP2}: -15.7 ± 1.0 VDC ✓

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III. CIRCUIT SPECIFICATIONS (continued)

D. (continued)

2. Voltage Divider Network for Zero Adjust (R13, R14, R17, VR1, TP5).

VR1 POSITION	VOLTAGE AT TP5
CCW	-3.414 ± 1.389 VDC
CW	3.414 ± 1.389 VDC

3. Positive Half Wave Rectifier Stage (IC1, R3, R4, R7, R9, R12, C6, CR5, CR6, TP3, TP50).

a. Transfer Function

$$\frac{TP50}{TP3} = \frac{-G1}{1 + T_1 S}$$

Where: Gain (G1) = 1.877 ± 0.038 Volts/Volt
Noise Suppression Lag Time Constant (T1) = 402 ± 24 usec
Noise Suppression Lag Break Point (F1) = 397 ± 24 Hz

b. AC to DC Conversion

$$\frac{TP50}{TP3} = 0.598 \pm 0.012 \text{ VDC/VRMS at 400 HZ}$$

c. Saturation Limits (TP50)

± 11.5 VDC (minimum)

4. Negative Half Wave Rectifier Stage (IC2, R5, R6, R8, R10, R11, C5, CR7, CR8, TP4, TP51).

a. Transfer Function

$$\frac{TP51}{TP4} = \frac{-G2}{1 + T_2 S}$$

Where: Gain (G2) = 1.877 ± 0.038 Volts/Volt
Noise Suppression Lag Time Constant (T2) = 402 ± 24 usec
Noise Suppression Lag Break Point (F2) = 397 ± 24 Hz

b. AC to DC Conversion

$$\frac{TP51}{TP4} = -0.598 \pm 0.012 \text{ VDC/VRMS at 400 HZ}$$

c. Saturation Limits (TP51)

± 11.5 VDC (minimum)

III. CIRCUIT SPECIFICATIONS (continued)

D. (continued)

5. Summer and Filter Stage (IC3)

a. Transfer Function for Positive Half Wave Rectifier Stage Output (R15, R19, C8, TP50, TP52)

$$\frac{TP52}{TP50} = \frac{-G3}{1 + T_3 S}$$

Where: Gain (G3) = 10.002 ± 0.200 Volts/Volt
Noise Suppression Lag Time Constant (T3) = 0.182 ± 0.020 SEC.
Noise Suppression Lag Break Point (F3) = 0.884 ± 0.097 HZ

b. Transfer Function for Negative Half Wave Rectifier Stage Output (R16, R19, C8, TP51, TP52)

$$\frac{TP52}{TP51} = \frac{-G4}{1 + T4 S}$$

Where: Gain (G4) = 10.002 ± 0.200 Volts/Volt
Noise Suppression Lag Time Constant (T4) = 0.182 ± 0.020 SEC.
Noise Suppression Lag Break Point (F4) = 0.884 ± 0.097 HZ

c. Transfer Function for Zero Adjust Bias (R17, R19, C8, TP5, TP52)

$$\frac{TP52}{TP5} = \frac{-G5}{1 + T_5 S}$$

Where: Gain (G5) = 1.000 ± 0.020 Volts/Volt
Noise Suppression Lag Time Constant (T5) = 0.182 ± 0.020 SEC.
Noise Suppression Lag Break Point (F5) = 0.884 ± 0.097 HZ

d. Saturation Limits (TP52)
± 11 VDC (minimum)

6. Voltage Divider Network for Coarse Range Adjust (VR2, R20, R21, R22, TP52, TP6) (Voltage at TP52 set to -4.000 VDC)

VR2 POSITION	VOLTAGE AT TP6
CCW	-1.591 ± 0.106 VDC
CW	-4.000 ± 0.000 VDC

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III. CIRCUIT SPECIFICATIONS (continued)

D. (continued)

7. Range Adjsut and Filter Stage (IC4)

a. Acceptable Offset at TP7: ± 1.0 mv DC (zero input)

b. Transfer Function for Coarse Range
Adjust Output (R21, R22, R24, VR3, TP6, TP7)
(VR3 full CCW)

$$\frac{TP7}{TP6} = \frac{-G6}{1 + T_6 S}$$

Where: Gain (G6) = 2.435 ± 0.049 Volts/Volt
Noise Suppression Lag Time Constant (T6) = 25.0 ± 2.7 msec.
Noise Suppression Lag Break Point (F6) = 6.45 ± 0.71 HZ

c. Transfer Function for Coarse Range
Adjust Output (R21, R22, R24, VR3, TP6, TP7)
(VR3 full CW)

$$\frac{TP7}{TP6} = \frac{-G7}{1 + T_7 S}$$

Where: Gain (G7) = 2.636 ± 0.071 Volts/Volt
Noise Suppression Lag Time Constant (T7) = 25.0 ± 2.7 msec.
Noise Suppression Lag Break Point (F7) = 6.45 ± 0.71 HZ

d. Saturation Limits (TP7)

± 11 VDC (minimum)

8. Voltage Divider Network for Meter Range Adjust (R25, VR4, Specified Load, TP7, Pin 36)
(Voltage at TP7 set to +10.000 VDC)

VR4 POSITION	VOLTAGE AT PIN 36
CCW	0.016 ± 0.001 VDC
CW	0.027 ± 0.001 VDC

IV. SET POINTS

A. Adjustment of VR1

This potentiometer is used to compensate for a small mechanical offset in LVDT core position and/or any imbalance in the two half wave rectifier stages. VR1 should be factory adjusted to produce zero volts

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IV. SET POINTS (continued)

A. (continued)

at TP52 when TP3 and TP4 are both grounded.

B. Adjustment of VR2

This potentiometer is used to achieve proper scaling of the DC voltage for rated LVDT core travel. VR2 should be adjusted to produce -4.000 VDC at TP6 when the LVDT core is at +0.100 inches.

C. Adjustment of VR3

VR3 is provided as a fine adjustment on the DC voltage representing LVDT core position. VR3 should be adjusted to produce 10.00 VDC at TP7 when the LVDT core is at +0.100 inches.

D. Adjustment of VR4

This variable resistor is used to set the panel meter range. VR4 should be set to produce 0.020 VDC at Pin 36 for 10.000 VDC at TP7. .5ma on ampmeter

+100
~2.46

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REVISIONS

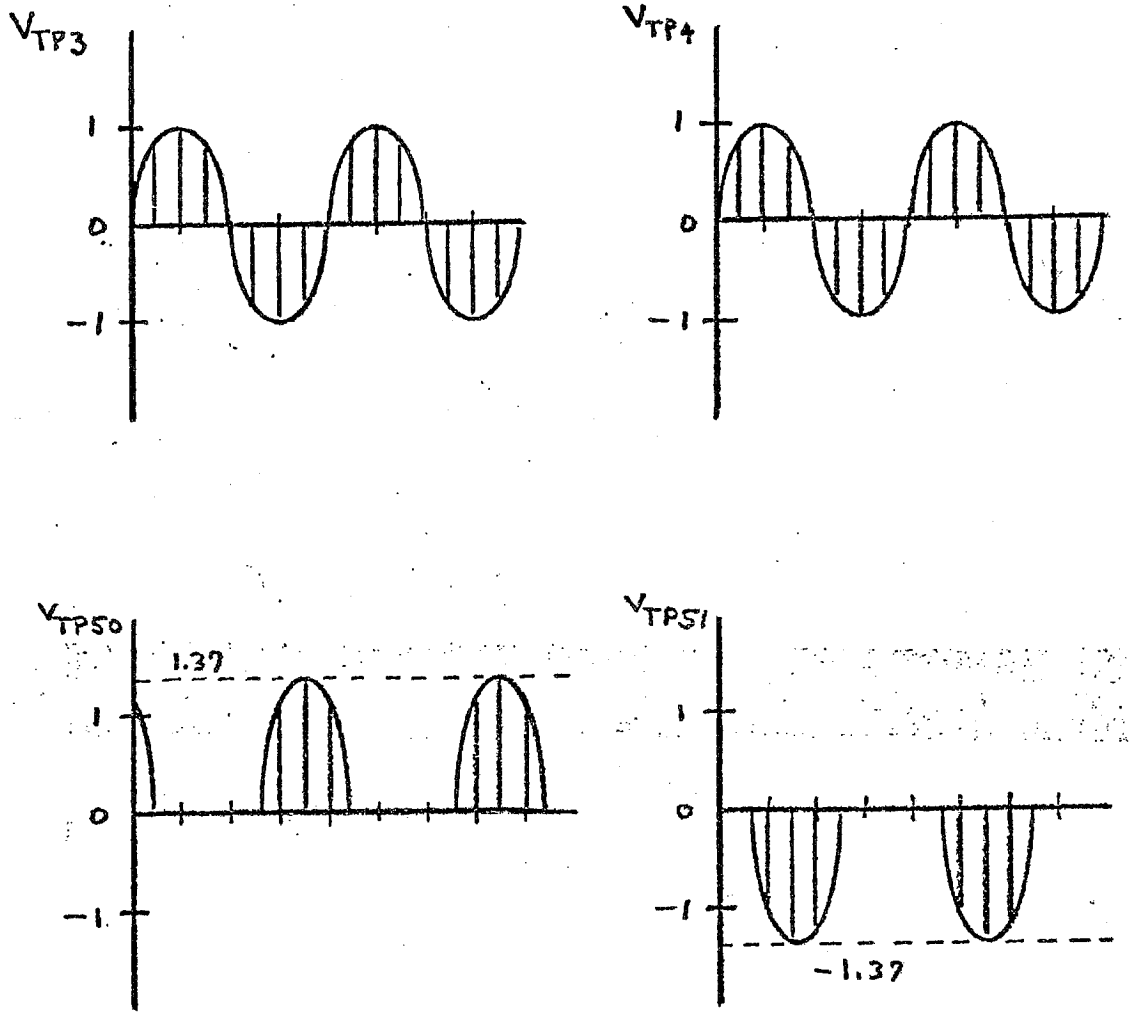

FIGURE 1 DEMODULATOR WAVE FORMS

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REVISIONS

SPECIFICATION PREPARED BY R. S. Gordon DATE 8-26-74
R.S. Gordon
EHC DESIGN ENGINEERING

APPROVED BY P C Callan DATE 9-12-77
P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE REVIEWED BY R. W. Debertolis DATE 9-9-77
R. Debertolis
EHC TEST ENGINEER

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