REVISIONS

I. CIRCUIT DESCRIPTION

The purpose of the Load Limit/Load Set Runback Circuit is to impose operating limits upon the flow reference signal of the controlling valve set due to plant and turbine operating conditions and to reposition the load set motor in accordance with these limits.

The load limit consists of a variable-rate load setback limit circuit and a hand-set load limit circuit. The variable-rate load setback limit circuit has simultaneously switched input signals of a load setback limit applied to the limit amplifier and a load setback rate applied to the intergrator. There are four separate load setback limits with their four associated load setback rates. These limits and rates are adjustable on the LL & LSR printed circuit board. These four load setback limits and the four load setback rates are each gated in such fashion that should more than one input occur at the same time, then the lowest limit and the fastest load setback rate will prevail.

The gated load setback limit input signal is summed with an adjustable opening bias to provide the appropriate signal voltage level for a limit signal. This summing operation is accomplished with the operational amplifier connected as an amplifier, which is referred to as the limit amplifier.

The operational amplifier connected as an intergrator has initial conditions established by an input bias that keeps the operational amplifier in negative saturation, while the feedback capacitor is charged to the flow reference signal of the controlling valve set.

The output signal of the intergrator is gated with the output of the limit amplifier in a high value gate. This gated output is the load limit signal. Operation of this combination is such that when a load setback rate is applied to the integrator and a load setback limit is applied to the limit amplifier, the integrator will integrate down from the initial flow reference condition to the load setback limit established at the output of the limit amplifier at the prescribed rate. The load setback limit will then prevail as the load limit signal as the operational amplifier of the integrator will again go into negative saturation.

This load limit signal is used to operate a voltage comparator (pin 28) and provide a signal to the load runback circuit, but it requires a power stage to supply the necessary current for the output low value gate.

The load limit power stage output signal is gated with the pressure limiter signal and the controlling valve amplifier signal in a low value gate to establish the flow reference signal for the controlling valves.(pin 16)

This LL & LSR Circuit is designed to drive either two, three, or four valve position loops whose individual input impedance is 20 kilohms.

273-2
273-12
273-71
273-13
273-22
273-22

PRINTS TO

CIRCUIT DESCRIPTION (continued)

The load limit signal is summed with an input signal from the Loading Rates and Load Set Limits Circuit in an operational amplifier connected as an amplifier. This amplifier is referred to as the runback amplifier. The runback amplifier output signal is used to operate two voltage comparators (Pins 29, 30).

The hand-set load limit potentiometer that is mounted on the turbine control panel provides an input signal to the limit amplifier. This potentiometer signal is diode gated with the load setback limit input signals such that the lowest value will prevail. A differential voltage comparator compares the potentiometer signal with the load setback limit signal (pins 18&20). Another voltage comparator is driven by the hand-set load limit potentiometer only (pin 21).

II. CIRCUIT SPECIFICATIONS

A. EXTERNAL CONNECTION REQUIREMENTS

A1. Power Supplies

1. Power Supply 1 (Pin 37):
   +22.000 ± 0.002 VDC at 130 MA (approx) Pin 39 Com
2. Power Supply 2 (Pin 41):
   - 22.000 ± 0.002 VDC at 140 MA (approx)

A2. Operating Signal Levels

S1A 1. Input 1 (Pin 19; load limit setting):
   0.1 to + 10 V (approx.) (Controlled by a 5 K load limit potentiometer connected between pins 26 and 36)

S1 2. Input 2 (Pin 31; load setback rate bias): +22V (switched to pin 11).
S2 3. Input 3 (Pin 35; load setback rate #1): +22V (switched to pin 11).
S3 4. Input 4 (Pin 34; load setback rate #2): +22V (switched to pin 11).
S4 5. Input 5 (Pin 33; load setback rate #3): +22V (switched to pin 11).
S5 6. Input 6 (Pin 32; load setback rate #4): +22V (switched to pin 11).
S6 7. Input 7 (Pin 22; load setback limit #1): +22V (switched to pin 11).
S7 8. Input 8 (Pin 23; load setback limit #2): +22V (switched to pin 11).
S8 9. Input 9 (Pin 24; load setback limit #3): +22V (switched to pin 11).
S9 10. Input 10(Pin 25; load setback limit #4): +22V (switched to pin 11).
S10 11. Input 11(Pin 27; loading rates & load set load set limit signal):
P5#3 0 to -10 V.

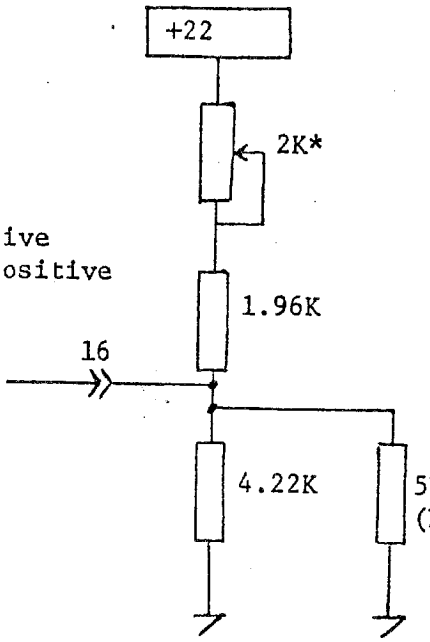
A3. Output Loads

1. Load 1 (Pin 16):
   Low value gate voltage divider--load configuration as per figure 1.

11 to 31 and to GND.

TITLE
TEST INSTRUCTION FOR LOAD LIMIT LOAD
SET RUNBACK CIRCUIT BOARD 1L1-H001
ASS'Y DRAWING 117D6694 G-1
FIRST MADE FOR EHC MARK II

REVISIONS



*adjusted to +10.0V when IC1 in negative saturation and IC2 in positive saturation

Values = 1%

FIGURE 1

2 Load 2 (Pin 28): 4.75 M Ohms (Voltage comparator)
3 Load 3 (Pin 18): 4.75 M Ohms (Voltage comparator)
4 Load 4 (Pin 20): 4.75 M Ohms (Voltage comparator)
5 Load 5 (Pin 21): 4.75 M Ohms (Voltage comparator)
6 Load 6 (Pin 29): 4.75 M Ohms (Voltage comparator)
7 Load 7 (Pin 30): 4.75 M Ohms (Voltage comparator)
8 Load 8 (Pins 26-36) 5K ± 1% (Hand set load limit pot)

B. INDIVIDUAL STAGE PERFORMANCE SPECIFICATIONS

1. Power supply (CR 1,2,3, and 4, R1 and 2)
   a. TP1: +15.7± 1.0 VDC
   b. TP2: -15.7± 1.0 VDC
2. Limit Amplifier (IC2)
   (With IC1 driven into negative saturation) ← S1 closed -13.7V
   a. Acceptable offset at TP6, (zero inputs): ± 1.0 m VDC
      (adjustable through VR51-adjustment point should be at least two turns away from either pot ends).
   b. Transfer function for load limit signal (R20, R21, R23, C5)

$$\frac{TP6}{TP7} = \frac{-G1}{1+T1 \cdot S}$$

Jumper pin 11 to pin 31 - set. on IC1 ground TP3 & TP7; Adjust R51 for Zero at TP6.

PRINTS TO

MADE BY J.Polacek Sept. 19, 1977
ISSUED SEP 20 1977
APPROVALS
Steam Turbine DIV OR DEPT.
Schenectady, N.Y. LOCATION
P3K-AL-0393-A01
CONT ON SHEET 4 SH NO. 3

FF-803-WA (4-71) PRINTED IN U.S.A.
CODE IDENT NO

where Gain (G1) = 1.002 + 0.020 volts/volt

Noise Suppression Lag Time Constant (T1) = 1.70 ± 0.19 msec
Noise Suppression breakpoint (F1) = 95 ± 11 HZ

c. Transfer function for valve opening bias (R19, R23)

$$\frac{7.1}{10.00}\,\frac{TP6}{TP3} = -G2$$

where Gain (G2) = 1.000 ± 0.020 volts/volt

d. Saturation limits (TP4): 14.9
± 13 VDC (minimum)

CONNECT 50K RESISTOR FROM TP6 TO TP50

3. Integrator Amplifier (IC1)
(With IC2 driven into negative saturation) TP4

a. Acceptable offset rate at TP6: ± 1.0 m VDC/sec (adjustable through VR50 - adjustment point should be at least two turns aways from either pot ends).

b. Transfer function for bias signal
(R5, R6, C1, C3)

$$\frac{TP6}{TP14} = \frac{-G3}{S(1+T3\cdot S)}$$

where Gain (G3) = 0.503 + 0.030 volts/volt
Noise Suppressions Lag Time Constant (T3) = 1.70 ± 0.19 msec
Noise Suppressions Breakpoint (F3) = 95 ± 11 HZ

c. Transfer function for load limit rate signal (R7, R8, C1, C4)

$$\frac{TP6}{TP13} = \frac{-G4}{S(1+T4.S)}$$

where Grain (G4) = 0.101 ± 0.006 volts/volt/sec
Noise Suppression Lag Time Constant (T4) = 1.89 ± 0.21 msec
Noise Suppression Lag Time Constant (F4) = 86 ± 10 HZ

d. Saturation limits (TP10):
Positive; 13.216 ± 0.293 Volts
Negative;-13.216 ± 0.293 Volts

4. Load Runback Amplifier (IC3)

a. Acceptable offset at TP12 (zero inputs): ± 1.0 mVDC
(Adjustable through VR52 - adjustment point should be at least two turns away from either pot end)

b. Transfer function for load limit signal
(R27, R29)

$$\frac{TP12}{TP9} = -G5$$

where Gain (G5) = 1.000 ± 0.020 volts/volt

c. Transfer function for loading rates and load set limit input signal (VR7, R26, R28, R29)

$$\frac{TP12}{TP16} = \frac{-G6}{(1+T6 \cdot S)}$$

C.1 VR7 Fully CW

Gain (G6): 1.243 ± 0.025 volts/volt
Noise suppression Lag Time Constant (T6): 1.18 ± 0.13 msec
Noise Suppression Lag Time Constant (F6): 137 ± 15 HZ

C.2 VR7 Fully CCW
Gain (G6) = 0.829 ± 0.042 volts/volt
Noise suppression Lag Time Constant (T6): 1.57 ± 0.20 msec
Noise suppression Lag Time Constant (F6): 103 ± 13 HZ

d. Saturation limits (TP12)
± 13VDC (minimum)

5. Voltage divider for integrator bias signal input. (Pin 31 connected to Pin 11)
Voltage at TP14: 5.554 ± 0.131 V

6. Voltage dividers for load setbacks and load limit rate inputs (VR2,3,4,5 fully CCW and VR53, 54, 55, 56 fully CW)
   a. Resistance between each of pins 22, 23, 24, 25, 32, 33, 34 and 35 and ground:
   10 K Ohms ± 10%
   b. Voltage at TP7 and Pin 18 with any one of pins 22, 23, 24, 25 or 19 connected to pin 11: 21.410 ± 0.464.
   c. Voltage at TP13 with any one of pins 32, 33, 34 or 35 connected to pin 11: 21.410 ± 0.464

7. Voltage divider for Load Limit Potentiometer (5K 1% resistor connected between pins 26 and 36).

VR6 fully CW - Voltage at TP15: 9.243 ± 0.253V
VR6 fully CCW - Voltage at TP15: 11.195 ± 0.110 V

11.468V

8. VR1 ?

NO SET POINTS

GENERAL ELECTRIC

P3K-AL-0393-A01
CONT ON SHEET SH NO 6

REV NO. 0	TITLE TEST INSTRUCTION FOR LOAD LIMIT LOAD SET RUNBACK CIRCUIT BOARD 1L1-H001 ASS'Y DRAWING 117D6694 G-1
P3K-AL-0393-A01	
CONT ON SHEET SH NO. 6	FIRST MADE FOR EHC MARK II

REVISIONS

PREPARED BY D. Economou DATE 11/26/73

D. Economou
EHC DESIGN ENGINEERING

APPROVED BY P C Callan DATE 9-6-77

P. C. Callan - Manager
EHC DESIGN ENGINEERING

TEST PROCEDURE
REVIEWED BY: R. Debertolis DATE 9/6/77

R. Debertolis
EHC TEST ENGINEER

PRINTS TO

MADE BY J.Polacek Sept. 19, 1977	APPROVALS	Steam Turbine DIV OR DEPT.	P3K-AL-0393-A01
ISSUED SEP 20 1977		Schenectady, N.Y. LOCATION	CONT ON SHEET SH NO. 6

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