GENERAL ELECTRIC

224X449AA

CONT ON SHEET 2 SH NO. 1

REV NO. 01

224X449AA

CONT ON SHEET 2 SH NO. 1

TITLE AF-3124 INVERTER CARD
ENGINEERING SPEC. & TEST INSTRUCTIONS

FIRST MADE FOR 193X476AAG01 & ABG01

REVISIONS

1.0 SCOPE

The following covers the performance capabilities and the test instructions for the 193X476AAG01 Inverter Card. This card is designed to be a standard part of the AF-400X Inverter, and performs the following functions:

1.01 Determines the inverter commutation interval and provides commutation pulse and inverter blanking signals from a six times fundamental frequency input.

1.02 Detects commutation current and regulates the peak commutation current by providing an initial pulse signal suitably placed within the commutation interval.

1.03 Generates an inverter firing pulse train.

1.04 Produces a firing signal supply which is delayed on control power energization to allow for control circuit settling.

1.05 Provides control undervoltage detection and inverter shutdown logic, including fault indication.

1.06 Provides commutation overcurrent detection and inverter shutdown logic, including fault indication.

1.07 Provides selectable inverter overfrequency detection and inverter shutdown logic, including fault indication and readout.

1.08 Provides inverter shoot-through fault detection and inverter shutdown logic, including fault indication and readout.

1.09 Provides inverter shutdown logic for a d.c. link overvoltage condition detected and indicated on another card.

2.0 PERFORMANCE CAPABILITIES

All cards shall be capable of the following performance while exposed to the conditions of section 4.0. In these specifications, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt, when 20 volts control power is applied to the card.

2.01 Inputs/Outputs

Tabs 14, 15, 20 & 28 are logic inputs. Logic sources connected to these tabs must each be capable of sinking 1 ma.

Tabs 17, 19, 26, 27, 29, 30, 31 & 32 are logic outputs, capable of sinking 2 ma in their low logic states. All of these tabs are capable of sourcing 1 ma in their high logic states.

Tab 10 is an analog output which is capable of supplying up to 40 ma at over 16 volts for firing signal supply.

Add ABG01 5/31/83

AW(BW)
5B(8)M
5D(CD)
5E(3)BK
5R(2)BW
5P(1)BW

PRINTS TO

MADE BY H. O. Loberg 2/8/80

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224X449AA

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GENERAL ELECTRIC

224X449AA

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224X449AA

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TITLE AF-3124 INVERTER CARD
ENGINEERING SPEC. & TEST INSTRUCTIONS

FIRST MADE FOR 193X476AAG01 & ABG01

REVISIONS

2.01 (Continued)

Tabs 4, 5, 9, 11, 12, 13 & 21 are analog inputs.

2.02 Commutation Interval Control

The inverter commutation interval is determined by the outputs at tabs 17, 19, and 26, which are in turn determined by the inputs at tabs 9 and 20. With no commutation current feedback inputs at tabs 9, the outputs at tabs 17, 19 and 26 are (for 460V) determined by the width of the $\overline{OP}$ pulse input at tab 20, as shown by the dotted lines in Fig. 1. The outputs at tab 17 will directly and inversely follow the tab 20 signal. The CP tab 19 pulse will go high 12.5 $\pm$ 1 μsec. after 20 pulse goes low. The CP pulse width will be 12.5 $\pm$ 1 μsec. The IP tab 26 pulse will occur at the time that tab 17 goes low, and will be 12.5 $\pm$ 1 μsec. wide.

With commutation current feedback input at tab 9, the outputs at tabs 17, 19, and 26 are determined by the magnitude of the commutation current input signal, as shown by the solid lines in Fig. 1. The tabs 17, and 26 outputs are determined by the commutation current regulator when the peak voltage at input tab 9 exceeds approximately 11 volts, as explained in section 2.03. Below this peak voltage input, the tabs 17 and 26 outputs are determined by a time period which is selected to equal one-half of the oscillation period of the inverter commutation circuit. This time period begins with the start of the CP tab 19 pulse and ends with the ending of the tab 17 pulse and the initiation of the tab 20 pulse. This time period is from 17 to 23 μsec when the 460V jumper is not connected, for low voltage inverters having nominal 40 usec. long commutation oscillations. When the 460V jumper is connected, the time period is 34 to 46 usec, for high voltage inverters having nominal 80 usec. long commutation oscillations.

NOTE - 193X476ABG01 Card
The voltage jumper notation is changed from 460V to "A" and from 230V to "B". The 100kVA (and 75kVA) 460V Inverter uses asymmetrical main SCRs with a commutati pulse base width of 40usec. (same as for 230V), and the voltage jumper should be in position "B".

5/31/83 Add ABG01

AW(BW)
5B(8)M
5D(CD)
5E(3)E
5R(2)E
5P(1)E
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224X449AA

CONT ON SHEET 3 SH NO. 2

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REVISIONS

Jumper Connections	IPA TAB 28 Input frequency
1. 75 Hz	68 to 83 Hz
2. 110 Hz	99 to 125 Hz
3. 165 Hz	149 to 182 Hz
4. 275 Hz	248 to 303 Hz
5. 410 Hz	369 to 451 Hz

3.09 Inverter Fault Shutdown

Apply an adjustable voltage to LCS tab 4 to simulate an inverter shoot-through fault. When the tab 4 input voltage reaches a level between 10.3 and 10.9 volts, an inverter fault shutdown should occur, producing the following results:

a) Turns on IOC light LED-4.
b) Causes $\overline{\text{IFT}}$ tab 30 to go low and IFL tab 32 to go high after 4 to 7 millisec.
c) Causes a pulse train to appear at $\overline{\text{IFP}}$ tab 31 which should consist of 10 to 12 usec. low pulses and 32 to 38 usec. high periods. This pulse train should persist as long as the voltage at tab 4 exceeds the trip level, but should disappear when the tab 4 voltage is decreased below the trip level.

The fault latch and light should be reset by momentarily disconnecting $\overline{\text{RST}}$ tab 14 from +20V after removing the tab 4 voltage.

3.10 Link Overvoltage Shutdown

If the $\overline{\text{LOV}}$ tab 15 is disconnected from +20V, to simulate a d.c. link overvoltage trip as detected on another card, a shutdown should occur, producing the following results:

a) Causes $\overline{\text{IFT}}$ tab 30 to change from a high to a low state.
b) After a time delay of 4 to 7 millisec. causes IFL tab 32 to change from a low to a high state, and causes one or two low going pulses to appear at $\overline{\text{IFP}}$ tab 31.

4.0 OPERATING AND TEST CONDITIONS

This card should be capable of operating within the performance specified in section 2.0 and pass all tests specified in section 3.0 while exposed to the following conditions:

4.01 DC Supply Voltage
+19.8 to +20.2 volts from tab 1 to tab 2.

4.02 Ambient Temperature
0 to +75°C.

1 | Chg IPA Tab 28 (125HZ) 3/4/83

AW(BW)
5D(CD)
5E(A&S)
5J(BW)
5B(8)M
5P(1)BW
5R(2)BW

PRINTS TO

3.07 Commutation Overcurrent Shutdown

Apply an adjustable voltage to CF tab 9, to simulate a commutation current. When this voltage reaches a level between 18.0 ± .5 volts, a commutation overcurrent shutdown should occur, producing the following results:

a) Turns on COC light LED-2 and causes $\overline{\text{IFT}}$ tab 30 to change from a high to a low state.
b) After a time delay of 4 to 7 millisec. causes IFL tab 32 to change from a low to a high state, and causes one or two low going pulses to appear at $\overline{\text{IFP}}$ tab 31.

The fault latches and lights should be reset by momentarily disconnecting $\overline{\text{RST}}$ tab 14 from +20 V after reducing the tab 9 voltage.

3.08 Inverter Overfrequency Shutdown

Connect an adjustable frequency, square wave voltage to IPA tab 28. The frequency should be variable from 60 to 450 Hz, with the high and low periods being exactly equal in time. The high voltage level should be from 14 to 20 volts.

There are five overfrequency trip points which are selectable by means of a card jumper. In each case, when the overfrequency trip level is reached, an over frequency shutdown should occur, producing the following results:

a) Turns on the IOF light LED-3.
b) Causes $\overline{\text{IOF}}$ tab 29 to change from a high state to a low.

After each overfrequency trip, the fault latch and light should be reset by momentarily disconnecting $\overline{\text{RST}}$ tab 14 from +20V.

The IPA tab 28 input frequency which should produce an overfrequency shutdown for each of the five jumper connections is given in the following table:

AW (BW
5B (8)
5D (CD
5E (3)
5R (2)
5P (1)
PRINTS

GENERAL ELECTRIC

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FIRST MADE FOR 193X476AAG01

REVISIONS

3.05 Delayed Firing Supply

Connect a 1K, 2 watt pot, with all resistance in, from DFS tab 10 to common, and connect a 1.8K, ½ W resistor from tab 10 to +20 volts.

When +20 volt power is applied to this card, output tab 10 should stay below 1.5 volts relative to common for .4 to 1.3 sec. after power is applied before going to its high state. In its high state with 1K output loading, the tab 10 voltage should be from 17.3 to 18.25 volts.

If the 1K pot is adjusted to reduce the loading resistance, the tab 10 output current should increase up to at least 40 ma when the tab 10 output voltage is still 16.0 volts or above. As the loading resistance is decreased further, the tab 10 output current will be limited such that when tab 10 is shorted to common, its output current will be between 45 and 110 ma. 92.6 A control undervoltage trip should occur during this test and the $\overline{RST}$ tab 14 will have to be momentarily disconnected from +20 V to reset the fault lights.

3.06 Control Undervoltage Shutdown

With a fixed 9.0 volt input at tab 5, decrease the +20 volt control supply voltage applied to tab 1 at a 1 second time constant rate. When this voltage reaches a level between 18.2 and 17.8 volts, a control undervoltage shutdown should occur, producing the following results:

a) Turns on CUV light LED - 1 and causes $\overline{IFT}$ tab 30 to change from a high to a low state.
b) After a time delay of 4 to 7 millisec, ~~turns on IOC light LED - 4;~~ DOES NOT DO THIS SEE 2.01 causes IFL tab 32 to change from a low to a high state, and causes one or two low going pulses to appear at $\overline{IFP}$ tab 31.

The fault latches and lights should be reset by momentarily disconnecting $\overline{RST}$ tab 14 from + 20V, after returning tab 1 to +20V.

Slowly reduce the +20 volt control power at tab 1 from the undervoltage trip level down to zero volts. The voltage at DFS tab 10 should remain below 2 volts over this whole control undervoltage range, with a 1K ohm resistor connected between DFS tab 10 and common.

Chg 306 b) 6/10/80

AW(BV
5B(8)
5D(CD
5E(3)
5R(2)
5P(1)E
PRINTS

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Change the voltage jumper to the 460 volts, position "A" for AB cards. The IBL pulse will now go low 34 ±6usec after the CP pulse goes high.

The initial pulse, IP, at tab 26, is triggered by the trailing edge of the IBL pulse. The IP pulse will go high when IBL goes low. The IP pulse width will be 12.5 ± 1 usec.

3.03 Commutation Current Regulator

With the voltage jumper connected for 460 volts, position "A" & the CF voltage equal zero, reduce the LVF voltage from 10 volts to 5.5 volts. The IBL pulse width should increase such that the IP pulse goes high 78 ± 16 usec after the CP pulse goes high.

Let LVF = 10 volts. As the CF, tab 9, voltage is increased from 0 to 4.0 volts, there should be no change in the IP pulse delay.

Apply 10.0 volts to CF, tab 9. The IP pulse should now go high 58 ± 10 usec. after CP pulse goes high.

Change the voltage jumper to 230 volts, position "B", With LVF=10V and CF = 10.0 volts the IP pulse should go high 29 ± 5 usec after the CP pulse goes high.

3.04 Initial Pulse and Inverter Pulse Train

The IP output at tab 26 should go high at the time when IBL tab 17 output goes low at the end of its pulse, as shown in Fig. 1. The tab 26 pulse should be from 12.5 ± 1 usec. wide.

The TR output at tab 27 should be a pulse train as shown in Fig. 1, synchronized with the initial pulse of tab 26. The high pulses should be from 95 to 11.5usec. wide with the low periods between pulses being from 31 to 36 usec. wide.
For the ABG01 card: Pulse width 8 to 10usec, with low periods from 19 to 23usec.

Gen'l chgs 5/31/83

AW(BW
5B(8)
5D(CD)
5E(3)B
5R(2)B
5P(1)B
PRINTS T

2.11 Fault Reset

All fault shutdowns described in sections 2.06 through 2.09 are maintained by logic latches. A momentary low input to $\overline{RST}$ tab 14 will reset all fault latches, lights and readouts to their off state.

2.12 Power Supply Requirements

The 20 volt power supply requirements for this card will be 100 ma ± 15%, (neglecting the delayed firing power supplied to other cards).

3.0 TEST INSTRUCTIONS

In these instructions, a "high" logic state refers to 18 to 20 volts and a "low" logic state refers to 0 to 1 volt, when 20 volts control power is applied to the card. A fixed 9.0 volt control level is connected to CRZ tab 5. The oscillator signal which is low for about 35 usec, and high for about 5 milliseconds, is applied to $\overline{OP}$ tab 20. Applying control power to this card, it will be necessary to momentarily disconnect $\overline{RST}$ tab 14 from +20V to reset any fault lights which have latched on. Connect $\overline{RST}$ and LQV to +20V.

3.01 On-card 13 Volt Power Supply

The on-card 13 volt nominal power supply can be measured by checking the voltage at Z1 with a meter having a minimum input impedance of 10 megohms. The voltage at Z1 should be 13.1 ± .65 volts.

3.02 Commutation Pulse, Inverter Blanking Pulse and Initial Pulse

Connect the voltage jumper for 230 volts, position "B" for AB cards, set tab 21 LVF = 10 volts & tab 9, CF = 0 volts.

The commutation pulse CP at tab 19 is triggered by the oscillator pulse $\overline{OP}$ applied at tab 20. CP will go high 12.5 ± 1 usec after $\overline{OP}$ goes low. The CP pulse width will be 12.5 ± 1 usec.

The inverter blanking pulse IBL at tab 17 is also triggered by the $\overline{OP}$ pulse. When $\overline{OP}$ goes low, IBL will go high. The width of the IBL pulse is variable with the minimum width equal the width of the $\overline{OP}$ pulse. With the input conditions as specified, IBL will go low when $\overline{OP}$ goes high.

REVISIONS

Chg 3.0 5/31/83

Chg 3.0 & 3.02 6/10/80

Chg 3.0

AW(BW)
5B(8)M
5D(CD)
5E(3)B
5R(2)B

PRINTS T

GENERAL ELECTRIC

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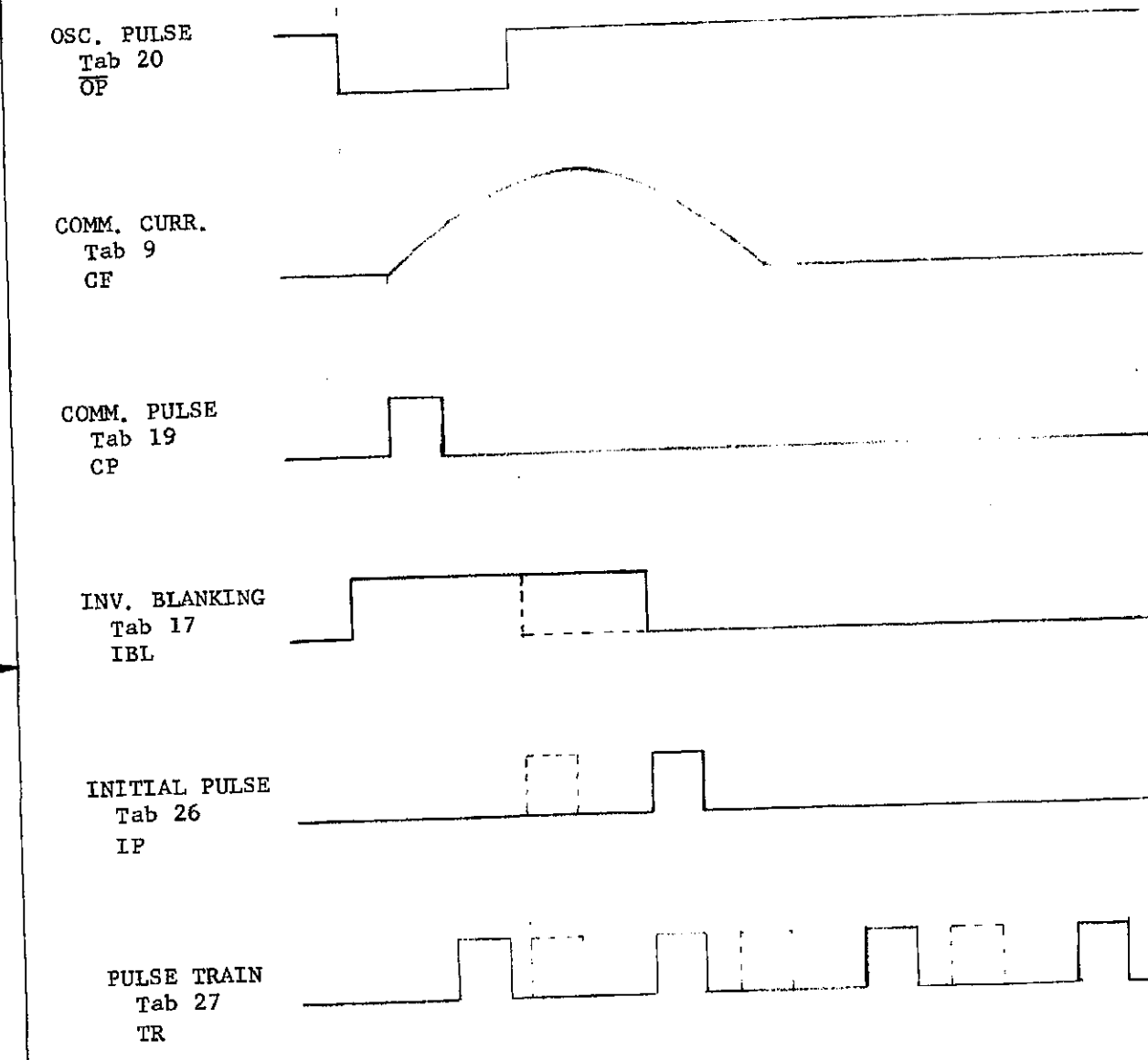
REV NO. 0
224X449AA
CONT ON SHEET 7 SH NO. 6

TITLE AF-3124 INVERTER CARD
ENGINEERING SPEC. & TEST INSTRUCTIONS

FIRST MADE FOR 193X476AAG01

REVISIONS



RELATIVE WAVESHAPES FOR 460V OPERATION

Figure 1

AW (BW
5B (8)
5D (CD)
5D (3)
5R (2)
5P (1)
PRINTS

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ISSUED 2/11/80

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REV NO. X1
224X449AA
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ENGINEERING SPEC. & TEST INSTRUCTIONS

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REVISIONS

2.08 Inverter Overfrequency Shutdown

An overfrequency trip is produced when the inverter frequency input signal at IPA tab 28 reaches the values given in the following table.

Jumper Connection	75Hz	110Hz	165Hz	275Hz	400Hz
Trip Frequency ±10%	75Hz	110Hz	165Hz	275Hz	400Hz

An overfrequency trip results in the following action:

1) The IOF fault light will turn on.
2) The $\overline{\text{IOF}}$ tab 29 will go to the low state.

2.09 Inverter Fault Shutdown

An inverter fault trip is produced when the DC link current signal at LCS tab 4 reaches 10.5 volts ± 3%, and results in the following action:

1) The IOC fault light turns on.
2) $\overline{\text{IFT}}$ tab 30 will go low and the IFL tab 32 will go high.
3) A pulse train appears at $\overline{\text{IFP}}$ tab 31, remaining as long as the tab 10 voltage exceeds 10.5 volts ± 3%. This pulse train consists of 10 to 12 usec. low pulses and 32 to 38 usec. high periods.

2.10 DC Link Overvoltage Shutdown

A d.c. link overvoltage condition is detected and indicated on another cards. A logic signal from this trip is applied to $\overline{\text{LOV}}$ tab 15 and results in the following action:

1) $\overline{\text{IFT}}$ tab 30 will go to the low state.
2) After a time delay of 4 to 7 millisec, IFL tab 32 will go high and one or two low going pulses will appear at $\overline{\text{IFP}}$ tab 31.

A Chg 2.09 5/31/83

AW(
5B(
5D(
5E(
5R(2
5P(1
PRIN

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REVISIONS

2.06 Control Undervoltage Shutdown

With a fixed 9.0 volt ±5% input at CRZ tab 5 (from the power supply card zener), a control undervoltage trip will occur if the voltage between tabs 1 and 2 decreases to 18.0 ± 1.1V or below. This will result in the following action:

1) The CUV fault light will turn on and $\overline{\text{IFT}}$ tab 30 will go low.
2) After a time delay of 3 to 5 millisec., IFL tab 32 will go high and a 40 usec. min. train of low going pulses will appear at $\overline{\text{IFP}}$ tab 31.
3) DFS tab 10 will remain in a high state until the pulse train disappears at tab 31, after which tab 10 will go low.

A control undervoltage trip is also initiated if the DFS tab 10 is loaded so that its output voltage decreases to 14.2 ± 1.1 V or below. This will result in the same shutdown action as with a +20 V undervoltage except that DFS tab 10 is not caused to go low.

The firing signal supply at DFS tab 10 will be maintained below 2 volts for control power levels from the undervoltage trip level down to zero volts. This prevents any SCR firing due to control logic misoperation at low control voltages.

2.07 Commutation Overcurrent Shutdown

A commutation overcurrent trip is produced when a commutation current input signal at tab 9 reaches 18.3 volts ±4%, and results in the following action:

1) The COC fault light will turn on and $\overline{\text{IFT}}$ tab 30 will go low.
2) After a time delay of 3 to 5 millisec., IFL tab 32 will go high and one or two low going pulses will appear at $\overline{\text{IFP}}$ tab 31.

AW(BW)
5B(8)M
5D(CD)
5E(3)BK
5R(2)BW
5P(1)BW
PRINTS TO

2.03 Commutation Current Regulation

When the commutation current peak input voltage at tab 9 exceeds 11.2 volts ± 7%, the tab 17 pulse width is lengthened by the peak voltage regulator to produce a later initiation of the IP tab 26 pulse. This reduces the commutation pump-up capabilities of the inverter to limit the commutation current magnitude. For stable operation, the gain of the peak voltage regulator is such that the peak input voltage at tab 9 must increase from 1.6 to 2.0 volts, to 13.0 volts ± 7%, to cause the IP tab 26 pulse to move from the middle of the commutation current pulse to the end. Since the commutation pump-up capabilities of the inverter increase with increasing d.c. link voltage, a feedback of this voltage into LVF tab 21 acts as a positive feedback to increase regulator gain.

The tab 21 input voltage will be 10 volts at zero d.c. link voltage and approximately 5.5V at rated voltage. The performance of the commutation current regulator will vary somewhat depending on inverter rating and commutation component tolerances, but will try to regulate the peak commutation current inputs at tab 9 to 12.0 volts ± 10% over a 10 to 1 inverter frequency range.

2.04 Inverter Firing Pulse Train

The TR tab 27 provides a 24 kilohertz ± 6% synchronized pulse train for inverter firing modulation. The high going pulses are 9.7 to 11.1 usec. wide with alternate low periods of 31 to 36 usec. The initial pulse at tab 26 is used to synchronize the pulse train. The ABG01 card: 34kHz ±6% pulse train. Pulse width 8.25-9.4usec, low periods are 19 to 23usec. wide.

2.05 Delayed Firing Signal Supply

The DFS output at tab 10 is a controlled source of firing signal supply. When +20 volt power is applied to the driver cards, tab 10 will remain in the low state so that firing signals are not inadvertently generated during the short period when the control is settling down. After .4 to 1.3 seconds, tab 10 will go high. Tab 10 can supply up to 40 ma at 16 volts or more. If tab 10 is shorted to common either directly or indirectly, the current is limited to a max of 110 ma.

Add ABG01 to 2.04 5/31/83

AW(BW)
5B(8)
5D(CD)
5E(3)
5R(2)
5P(1)
PRINTS

GENERAL ELECTRIC

224X449AA
CONT ON SHEET FL SH NO. 12

REV NO. 0

224X449AA

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AF-3124 INVERTER CARD
ENGINEERING SPEC. & TEST INSTRUCTIONS

FIRST MADE FOR 193X476AAG01

REVISIONS

4.03 Humidity

24 hours in 90% relative humidity at 40°C.

4.04 Voltage to Ground

600 volts.

AW(BW)
5B(8)
5D(CD)
5E(3)B
5R(2)
5P(1)E
PRINTS

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