g GE Industrial Systems	**Functional Testing Specification**
Renewal Services ***Louisville,KY***	**LOU–GED-IC3600QEAA**

Test Procedure for an IC3600QEAA Card

DOCUMENT REVISION STATUS: Determined by the last entry in the "REV" and "DATE" column

REV.	DESCRIPTION	SIGNATURE	REV. DATE
A	Initial release, Re-write of Salem procedure.	D. Laemmle	03/20/03
B			
C			

PREPARED BY	REVIEWED BY	REVIEWED BY	QUALITY APPROVAL
D. Laemmle			Robert Dwall
DATE	**DATE**	**DATE**	**DATE**
03/20/03			03/20/03

Functional test procedure for a Card

1. SCOPE

1.1 This is a functional testing procedure for a Card.

2. STANDARDS OF QUALITY

2.1 Refer to the current revision of the IPC-A-610 standard for workmanship standards.

3. APPLICABLE DOCUMENTS

3.1 The following document(s) shall form part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue shall apply.
3.1.1

4. ENGINEERING REQUIREMENTS

4.1 Equipment Cleaning
- **4.1.1** Equipment should be clean and free of debris prior to applying power unless performing an initial check. Refer to the local documented procedures for cleaning guidelines.

4.2 Equipment Inspection
- **4.2.1** Equipment should be visually inspected for any defects prior to applying power. This inspection should include the following as a minimum:
  - **4.2.1.1** Wires broken or cracked
  - **4.2.1.2** Terminal strips / connectors broken or cracked
  - **4.2.1.3** Loose wires
  - **4.2.1.4** Components visually damaged
  - **4.2.1.5** Capacitors leaking
  - **4.2.1.6** Solder joints damaged or cold
  - **4.2.1.7** Circuit board burned or de-laminated
  - **4.2.1.8** Printed wire runs burned or damaged

5. EQUIPMENT REQUIRED

5.1 The following equipment is required to perform the process requirements. Equipment may be substituted provided that all accuracy's and test ratios are equivalent or better.

Qty	Reference #	Description
1		Fluke 85 DMM (or Equivalent)
1		JRL VRD307 Precision Voltage Divider
1		QEAA Test Fixture (Salem)
1		Shielded Lead Set
1		2215 Tektronix Oscilloscope or equiv.
1		HP Digital voltmeter Model 3455 or equiv.
4		15v Power Supplies

6. TESTING PROCESS

6.1 Setup

6.1.1 The test fixture, precision voltage divider, and shielded test leads need to be requested from Salem, Va.

Note:

6.2 Testing Procedure

6.2.1 See attached

6.3 ***TEST COMPLETE ***

7. NOTES

9.0 QEAA TEST INSTRUCTIONS

A copy of this test can be obtained by logging onto the VAX and then typing the following command. QEAA.

9.1 SCOPE

This document describes the setup and test procedure for the IC3600QEAA.

The following PWB versions can be tested by this procedure.

9.2 TEST EQUIPMENT

	QTY
1. Wavetek Signal Generator Model 142	1
2. Digitec Volt/Current Sources Model 3110	5
3. HP Digital Voltmeter Model 3455	1
4. Precision Voltage Divider type JRL VDR307	1
5. Tektronix Oscilliscope Model 7603	1

9.3 POWER SUPPLY REQUIREMENTS

SUPPLY	NOM.	TOL.	PINS
P15A	+15.00V	+/- 5%	P15A
N15A	-15.00V	+/- 5%	N15A
ACOM (P15A,N15A,COM)			ACOM
P15A1	+15.00V	+/- 5%	P15A1
N15A1	-15.00V	+/- 5%	N15A1
ACOM1 (P15A1,N15A1,COM)			ACOM1

9.4 INITIAL SETUP

9.4.1 TEST SETUP DESCRIPTION

1. Connect PWB per setup drawing figure 1.

2. IC3600QEAA PWB's use Cmos IC which are extremely static sensitive therefore Ground all test equipment and use ground straps when handling the pwb.

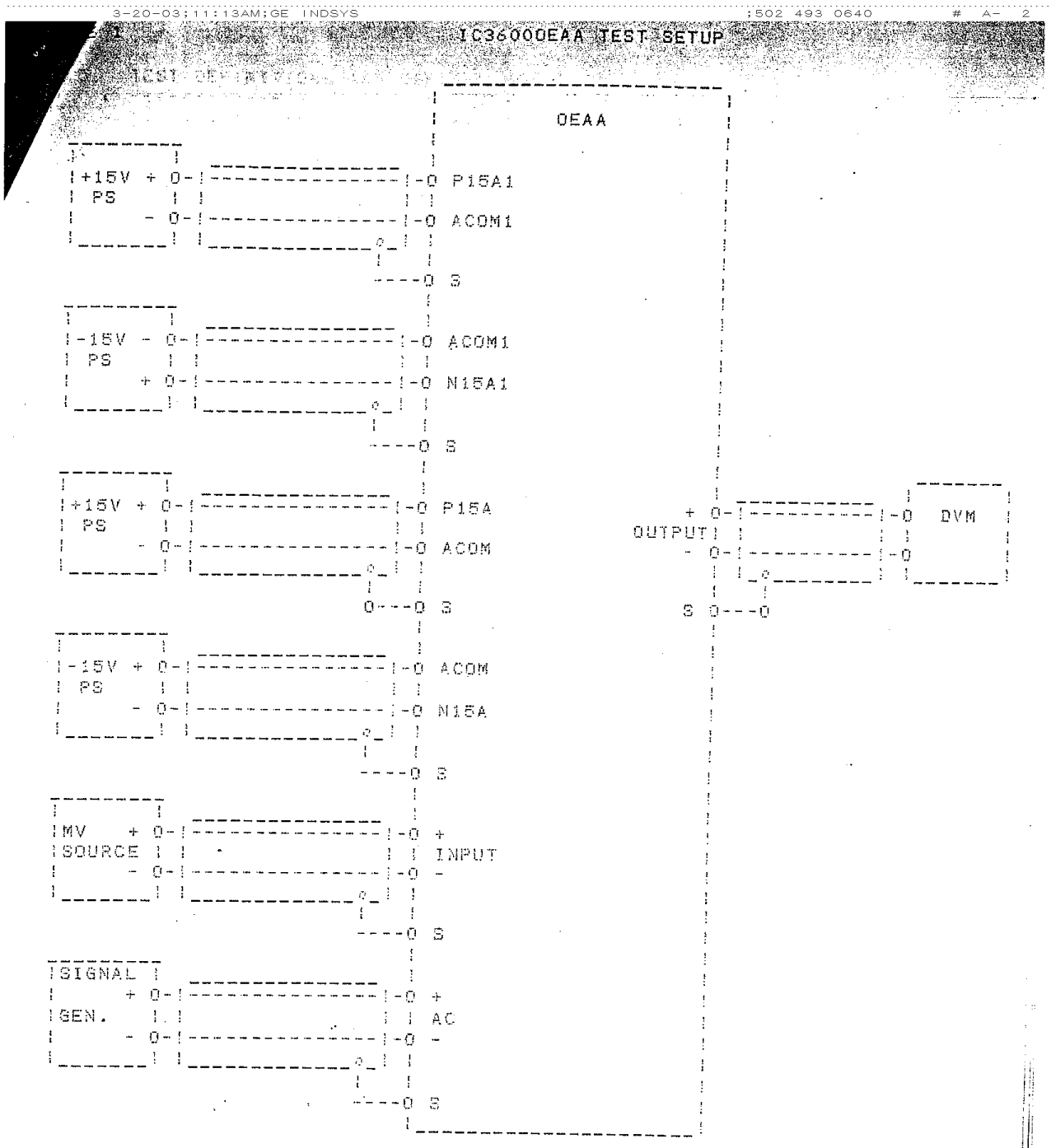
3. Before performing any adjustments, all IC3600QEAA PWB's to be tested must be stored in a warm up tray for a minimum of one hour prior to test.(And when the PWB's are not under power in test fixture.)

4. A group of PWB may be tested on a per test setup bases.

5. Plug in PWB and powerup for 5min. before testing.

ACTIVE FOR Test

BY Tom DATE 11-14-96



9.5 TEST DEFINITIONS AND SPECIAL NOTES

1. Digital logic input levels:
   Logic "0" 0 to +.7V (Low)
   Logic "1" +12.0 +/-1V (High)

2. Digital logic output levels:
   Logic "0" 0 to +.7V (Low)
   Logic "1" +12.0 +/-1V (High)

3. Unless otherwise specified, the following conditions apply throughout the test procedure.
   a. Voltages are positive DC.
   b. Any negative DC voltages are preceeded with a "-".
   c. Any AC voltages are RMS (.707 X peak).
   d. DC inputs should be within 2 millivolts of nominal.
   e. AC inputs should be within 10 millivolts of nominal.
   f. Inputs are to be floating unless a signal is specifically applied.
   g. Once an input is applied it should be left applied until specifically told to remove it.
   h. Any pot settings should be adjusted as close to nominal as possible. Not just to within tolerance.

9.6 TEST PROCEDURE

9.6.1 Digital Address Decoding

1. Switch SW7 on.

2. Toggle switches SW1-SW6 and verify the output from PIN 25 (PLUG 25) to ACOM as indicated in following table:
   Note: 1 = switch off, 0 = switch on

STEP	SW1	SW2	SW3	SW4	SW5	SW6	PIN 25
1	0	0	0	0	0	0	0
2	0	0	0	0	0	1	1
3	0	0	0	0	1	0	0
4	0	0	0	0	1	1	0
5	0	0	0	1	0	0	1
6	0	0	0	1	0	1	1
7	0	0	0	1	1	0	1
8	0	0	0	1	1	1	1
9	0	0	1	0	0	0	0
10	0	0	1	0	0	1	1
11	0	0	1	0	1	0	0
12	0	0	1	0	1	1	1
13	0	0	1	1	0	0	0
14	0	0	1	1	0	1	1

3-20-03;11:13AM;GE INDSYS ;502 493 0640 # A- 4

STEP	SW1	SW2	SW3	SW4	SW5	SW6	PIN 26
15	0	0	1	1	1	0	1
16	0	0	1	1	1	1	0
17	0	1	0	0	0	0	1
18	0	1	0	0	0	1	1
19	0	1	0	0	1	0	1
20	0	1	0	0	1	1	1
21	0	1	0	1	0	0	1
22	0	1	0	1	0	1	1
23	0	1	0	1	1	0	1
24	0	1	0	1	1	1	1
25	0	1	1	0	0	0	1
26	0	1	1	0	0	1	1
27	0	1	1	0	1	0	1
28	0	1	1	0	1	1	1
29	0	1	1	1	0	0	1
30	0	1	1	1	0	1	1
31	0	1	1	1	1	0	1
32	0	1	1	1	1	1	1
33	1	0	0	0	0	0	0
34	1	0	0	0	0	1	1
35	1	0	0	0	1	0	0
36	1	0	0	0	1	1	1
37	1	0	0	1	0	0	1
38	1	0	0	1	0	1	1
39	1	0	0	1	1	0	1
40	1	0	0	1	1	1	1
41	1	0	1	0	0	0	0
42	1	0	1	0	0	1	1
43	1	0	1	0	1	0	0
44	1	0	1	0	1	1	1
45	1	0	1	1	0	0	1
46	1	0	1	1	1	0	1
47	1	0	1	1	1	1	1
48	1	1	0	0	0	0	0
49	1	1	0	0	0	1	1
50	1	1	0	0	1	0	1
51	1	1	0	0	1	1	0
52	1	1	0	1	0	0	1
53	1	1	0	1	0	1	1
54	1	1	0	1	1	0	1
55	1	1	1	0	0	0	1
56	1	1	1	0	1	0	1
57	1	1	1	0	1	1	1
58	1	1	1	1	0	0	0
59	1	1	1	1	0	1	1
60	1	1	1	1	1	0	1
61	1	1	1	1	1	1	0
62	0	0	0	0	0	0	0
63	1	1	1	1	1	1	0

9.6.2 Amplifier Calibration

1. Plug in PWB and powerup for 5min. before testing and switch SW7 on.
2. Switch 3/4TIE on.
3. Switch G3 on.
4. Switch GTP4 on.
5. Adjust PWB pot. R1 until the voltage from TP6 to Acom equal 0.00 +/-.001vdc. (Pot. may need several adjustments before stabilizing)
6. Switch GTP4 off and GTP3 on.
7. Adjust PWB pot. R2 until the voltage from TP5 to Acom equal 0.00 +/-.001vdc. (Pot. may need several adjustments before stabilizing)
8. Switch GTP3 off.
9. Repeat steps 4 through 8.
10. Adjust PWB pot. R1 slightly until the voltage from TP5 to TP6 equal 0.00 +/-.001vdc. (Pot. may need several adjustments before stabilizing)
11. Set SW1-SW4 to "0" position.
12. Switch G15 on.
13. Switch G3 off.
14. Apply a 20VAC, P-P, 20Hz. sine wave signal from Input(+) to Acom (Not Input -).
15. Connect Oscilliscope from Output(+) to Output(-).
16. Adjust PWB pot. R4 for a minimum voltage from Output(+) to Output(-), using the oscilliscope. (Pot. may need several adjustments before stabilizing)
17. Verify that the voltage from Output(+) to Output(-) is less than 100mv P-P and that the waveform is undistorted.
18. Switch GTP5/6 on.
19. Adjust PWB pot. R5 slightly until the voltage from Output(+) to Output(-) equal 0.00 +/-.001vdc. (Pot. may need several adjustments before stabilizing)

20. Switch GTP5/6 off.

21. Switch 3/4TIE off.

22. Switch G15 off.

23. Disconnect signal generator.

9.6.3 Amplifier Gain Adjustment

1. Reconnect test setup per figure 2

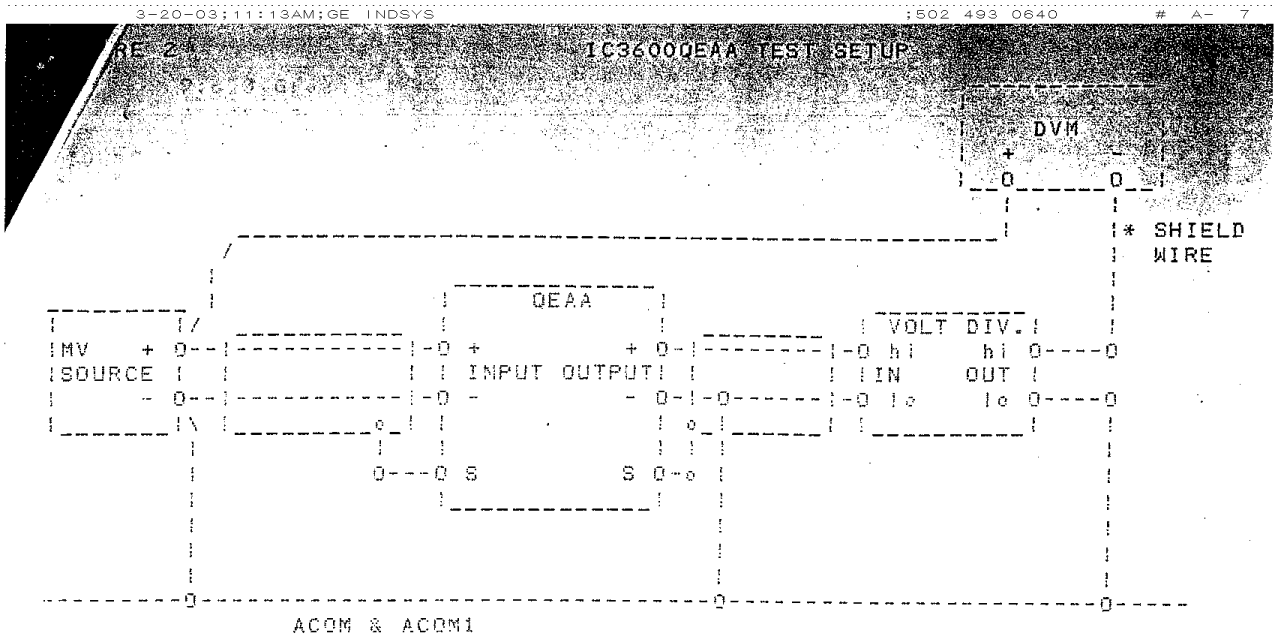
2. Plug in PWB and powerup for 5min. before testing.

3. Set the Precision Voltage Divider per the following table:
   Example: QEAA1 = card form 1, QEAA2 = card form 2, etc.

Form	Precision Volt. Divider Setting	Input 1 (+) to Acom	Input 2 (+) to Acom
1	.0027667	25mv +/-10uv	-25mv +/-10uv
2	.0032108	30mv +/-10uv	-30mv +/-10uv
3	.0047415	45mv +/-10uv	-45mv +/-10uv
4	.0053631	50mv +/-10uv	-50mv +/-10uv
5	.0068421	65mv +/-10uv	-65mv +/-10uv

4. Apply Input 1 voltage from Input(+) to Acom. (Note: Be sure to jumper Input - to Acom per figure 2.)

5. Adjust PWB pot. R3 until the voltage from Output voltage equal 0.000000 +/-.000008vdc. (Pot. may need several adjustments before stabilizing)



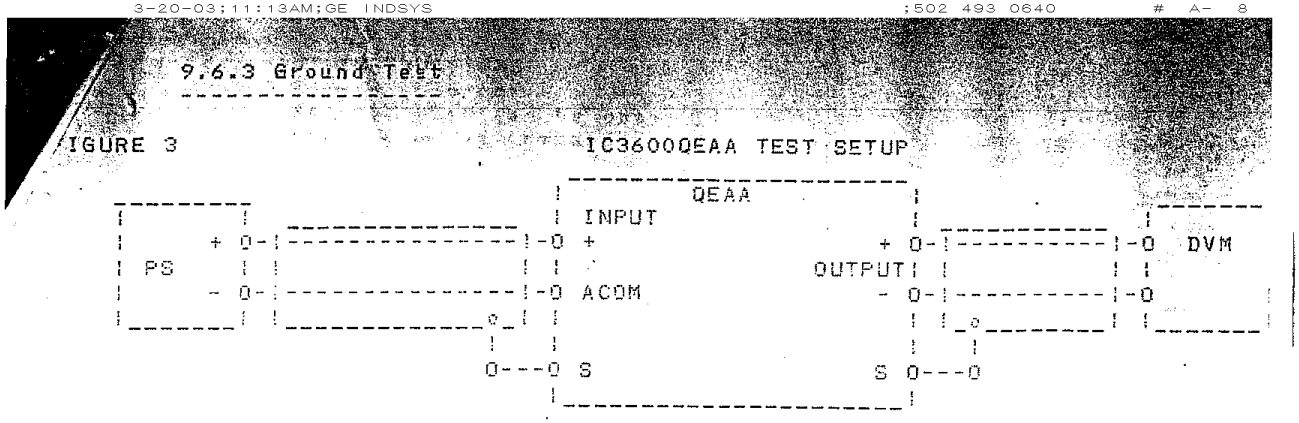
6. Apply Input 2 voltage from Input(+) to Acom and verify the Output voltage 0.000000 +/-.000008vdc. If not, it may take several iterations of Gain and Offset adjustment to get within specified limits. Refer to the following table for some examples:
   Note: R1 = offset, R3 = gain

Step	Meter Reading for Source Input Positive	Meter Reading for Source Input Negative	Condition	Action to Take First	Action to Take Second
1	+40uv	-40uv	Gain Too Low	Turn R3 CW	---
2	-40uv	+40uv	Gain Too High	Turn R3 CCW	---
3	-40uv	-40uv	Positive Offset	Turn R1 CCW	---
4	+40uv	+40uv	Negative Offset	Turn R1 CW	---
5	+40uv	-80uv	Gain Low Offset Error	Input Neg.,Adjust R1 to get Ex.1	Adjust R3
6	-80uv	+40uv	Gain High Offset Error	Input Pos.,Adjust R1 to get Ex.2	Adjust R3
7	+40uv	+80uv	Gain Error Positive Offset	Input Pos.,Adjust R1 to get Ex.2	Adjust R3
8	-40uv	-80uv	Gain Error Negative Offset	Input Pos.,Adjust R1 to get Ex.1	Adjust R3

3-20-03;11:13AM;GE INDSYS ;502 493 0640 # A- 8

9.6.3 Ground Test

IGURE 3 IC3600QEAA TEST SETUP



*** DO NOT EXCEED 14.5V OR IC1 MAY BE DAMAGED ***

1. Connect Test setup per figure 3.

2. Plug in PWB and powerup for 5min. before testing.

3. Switch 3/4TIE on and switch SW7 off.

4. Vary input voltage from Input(+) to Acom between +12vdc to -12vdc and verify Output(+) to Output(-) = 0.000v +/- 300mvdc.

5. Switch SW7 on and repeat step 3.

SEAL ALL POTS

END OF TEST

TEST INSTRUCTION REVISION STATUS

REV	INIT	DESCRIPTION OF CHANGE	DATE COMPLETE
0	SAJ	First made for IC3600QEAA	02/05/85
1	REV	Misc cleanup and clarification	02/08/88