g GE Energy	**Functional Testing Specification**
Parts & Repair Services ***Louisville, KY***	**LOU-GED-115D2220G2**

Test Procedure for a 115D2220G0002, frequency to voltage card

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DATE	**DATE**	**DATE**	**DATE**
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1. SCOPE

1.1 This is a functional testing procedure for a 115D2220G0002 (CB-FREQ TO VOLT CONV MK1).

2. STANDARDS OF QUALITY

2.1 Refer to the current revision of the IPC-A-610 standard for workmanship standards.

3. APPLICABLE DOCUMENTS

3.1 The following document(s) shall form part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue shall apply.
3.1.1 P3K-AL-0305-A01

4. ENGINEERING REQUIREMENTS

4.1 Equipment Cleaning
4.1.1 Equipment should be clean and free of debris prior to applying power unless performing an initial check. Refer to site specific SRA's for cleaning guidelines.
4.2 Equipment Inspection
4.2.1 Equipment should be visually inspected for any defects prior to applying power. This inspection should include the following as a minimum:
4.2.1.1 Wires - broken, cracked, or loosely connected
4.2.1.2 Terminal strips / connectors - broken or cracked
4.2.1.3 Components - visually damaged
4.2.1.4 Capacitors - bloated or leaking
4.2.1.5 Solder joints - damaged or cold
4.2.1.6 Circuit board - burned or de-laminated
4.2.1.7 Printed wire runs / Traces - burned or damaged

5. EQUIPMENT REQUIRED

5.1 The following equipment is required to perform the process requirements. Equipment may be substituted provided that all accuracy's and test ratios are equivalent or better.

Qty	Reference #	Description
1		Fluke 87 DMM (or Equivalent)
1		Oscilloscope
1		Fluke 5500A Calibrator
1		Dual Power Supply

6. Testing Process

6.1 Setup

6.1.1 Connect card as in figure 1.

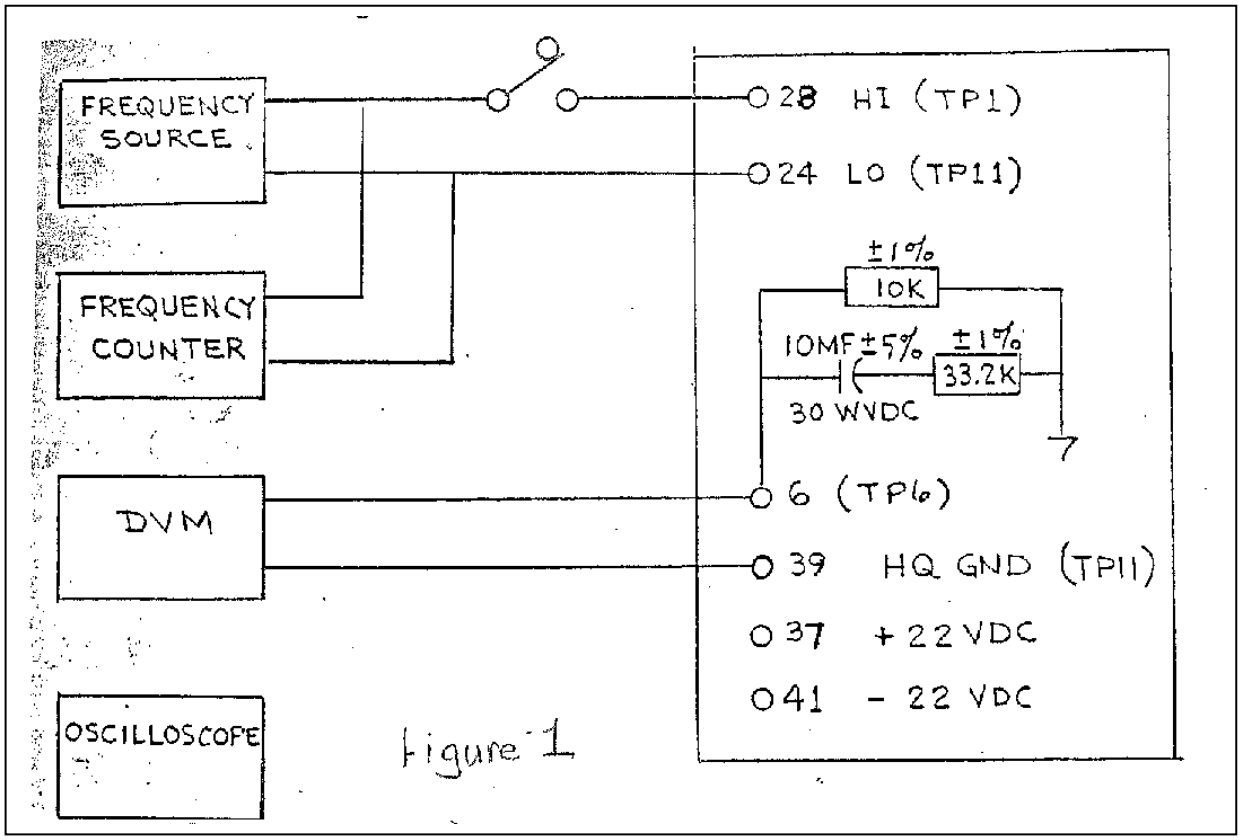

Figure 1

6.1.2 Set power supply for +22.000VDC +/- 2mVdc and connect to pin 37

6.1.3 Set power supply for -22.000VDC +/- 2mVdc and connect to pin 41

6.1.4 Common to pin 39

6.2 Testing Procedure

6.2.1 Apply power to card.

6.2.2 With no input to the card adjust VR51 for 0.00VDC +/- 1mV at TP6.

6.2.3 Verify the following voltages.

6.2.4 TP52- CR3 = +5.1vdc +/- .25v

6.2.5 TP55- CR4 = +9.0vdc +/- .09v

6.2.6 TP53- CR5 = +11.7vdc +/- .59v

6.2.7 Cathode of CR6 = +16.0vdc +/- .80v

6.2.8 TP54- CR7 = +12vdc +/- .60v

6.2.9 TP56- CR8 = -16.0vdc +/- .80v

(SETTING INPUT LEVEL TO BE DETECTED)

6.2.10 Adjust VR50 full CCW.

6.2.11 Apply a 480hz 20mvP/P sinewave signal (input signal) between pin 28 and pin 24.

6.2.12 Slowly adjust the amplitude of the applied signal until the converter just turns on (F/V output -1.0V) at TP6.

6.2.13 Verify input amplitude:

6.2.14 G1= 100mv +/- 25mvP/P

6.2.15 G2=200mv +/- 100mvP/P

6.2.16 Set input signal to 50mvP/P.

6.2.17 Observe, with a scope, the signal at TP2 and slowly adjust VR50 just until a stable square wave is obtained.

Note: A stable DC output voltage (TP6) from the F/V card will result when VR50 is properly adjusted.

Note: The primary purpose of VR50 is to adjust detection level to 50mvP/P.

(CHECKING AND RECORDING CRITICAL VALUES)

6.2.18 Set the input signal to approx. 2vP/P and exactly 4800hz +/- 1 hz.

6.2.19 Adjust VR1 full CW and verify the output DC voltage at TP6 is more negative or equal to -10.200v.

Example: -10.400v is acceptable and -10.100 is unacceptable.

6.2.20 Adjust VR1 full CCW and verify the DC voltage at TP6 is less negative or equal to -9.800v.

Example: An output voltage of -9.600 is acceptable and a voltage of -9.900 is unacceptable.

(CALIBRATING F/V OUTPUT VOLTAGE)

6.2.21 Adjust VR52 full CCW.

6.2.22 With the input signal set at exactly 4800hz +/- 1hz and approx. 2vP/P adjust the trimpot VR1, at TP6, until the voltage equals -10.000vdc +/- .001 volts.

6.2.23 Increase and decrease the input amplitude form 2vP/P to 20vP/P and verify the output DC voltage at TP6 doesn't change.

6.2.24 Adjust the following input frequencies and verify the DC output voltages at TP6.

6.2.25 6000hz = -12.500vdc +/- .002v

6.2.26 4800hz = -10.000vdc +/- .001v

6.2.27 2400hz = -5.000vdc +/- .002v

6.2.28 480hz = -1.000vdc +/- .002v

6.2.29 48hz = approx.. -0.10vdc

6.2.30 4.8hz = approx.. -.0.01vdc

6.2.31 Return the input frequency to 4800hz and verify TP6 is -10.000vdc +/- .001v.

6.2.32 Set a heat probe for 55 degrees C and apply the probe to the unijunction transistor Q3 for 30 sec.

6.2.33 Remove the probe and verify that the output voltage at TP6 returns to within +/- 3mv of the original -10.000vdc setting

(SETTING THE LOCK UP LEVEL)

6.2.34 Set VR52 full CCW.

6.2.35 Increase the input frequency slowly from 4800hz to 6000hz and verify the output voltage at TP6 increases linearly from -10.000vdc to -12.500vdc.

6.2.36 Verify the output voltage at TP6 doesn't decrease or fall off before reaching 6000hz

6.2.37 Adjust VR52 CW until the output voltage jumps from -12.5 to -13.3vdc.

6.2.38 After setting the lock up voltage at 6000hz with VR52, increase the input frequency from 6000hz to 10000hz and verify that the output voltage at TP6 doesn't change in the lock up region.

(OBSERVING THE OUTPUT FOR OSCILLATIONS AND CHECKING FOR RIPPLE)

6.2.39 Using a scope, vary the input frequency from 480hz to 10Khz and verify the ripple or noise riding on the DC output at TP6 doesn't exceed 10mvP/P.

6.2.40 Verify the following:

INPUT FREQ	OUTPUT VOLTS	AC RIPPLE	WAVEFORM
4.8	- .01	100 mV	
12	- .025	80 mV	
24	- .05	60 mV	
48	- .10	40 mV	
120	- .25	20 mV	
240	- .50	10 mV	
480	- 1.0	10 mV	

(CHECKING OPERATION OF IC4, UNIJUNCTION TIMING CIRCUIT AND LOCK UP TIME SETTING)

6.2.41 Return the input frequency 4800hz

6.2.42 Connect a scope in the duel channel chop mode and connect channel 1 to TP3 and channel 2 to TP5. Trigger externally at TP3.

6.2.43 Increase the input frequency to 6000hz and verify the waveform at TP5 disappears before the waveform at TP3 begins to skip.

Note: At frequency less than lock up the waveforms will be inverse of each other.

6.2.44 Verify while in lock up the waveform at TP3 will have a duty cycle of approx. 93.5%.
The leading edge of the pulse to the fall edge of the same pulse = approx. 156usec
The leading edge of the pulse to the leading edge of the next pulse = approx. 167usec
156usec divided by 167usec =93.5%

(CHECKING UNIJUNCTION TIMMING CAPACITOR)

6.2.45 Apply freeze spray the unijunction timing capacitor C6, being careful not to effect surrounding components.

6.2.46 With an input frequency of 4800hz verify the output voltage at TP6 remains constant at 10.000vdc +/- 25mvdc

6.3 ***TEST COMPLETE ***

7. Notes

7.1 None at this time.

8. Attachments

8.1 None at this time.