

## **GE Power Generation Engineering**

**PROCESS SPECIFICATION** 

Materials and Processes Engineering Schenectady, NY 12345

P3K-AL-0326-A01

TEST INSTRUCTIONS FOR POWER LOAD UNBALANCED LOGIC CIRCUIT BOARD

DOCUN	MENT REVISIO	N STATUS:	DETERMINED BY THE LAST ENTRY IN THE "REV" A	ND "DATE" COLUMN	
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A	YA00096	SPECIFICATION LISTED IN STEAM TURBINE/GENERATOR INDEX AS "INACTIVE" HAS BEEN FORMALLY REVISED AS "INACTIVE FOR NEW DESIGN". (PR BUDKA)		C.R. truppi	DEC 0 2 1991
		AS TNAC	INACTIVE FOR NEW DESIGN  AS OF 12/02/91		
		1991			

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PREPARED BY:	P.R.	BUDKA	
ORIG. ISSUE DATE:		-	

GENERAL % ELECTRIC P3K-AL-0326-A01 CONT ON SHEET SH NO. TITLE TEST INSTRUCTIONS FOR POWER LOAD UNBALANCE LOGIC CIRCUIT BOARD P3K-AL-0326-A01 CONT ON SHEET SH NO. FIRST MADE FOR REVISIONS CIRCUIT BOARD REVISION #1 I. SCOPE 1975 This instruction outlines the test specifications for circuit board 1PU2-A001 (Board Drawing 117D7745G1). €3 O. P. MAL JAN CIRCUIT DESCRIPTION II. This circuit board: Contains the necessary logic to provide +24V to action relays located throughout the EHC system wherever a PLU condition exists. (i.e. mechanical power exceeds electrical power by a set amount, and at least momentarily during the same period the rate of decrease of the electrical power exceeds a set amount). Inputs to FH & PC are also \* provided. Provides the means to test itself and the rest of the PLU circuits. Provides a path to activate a signalling lamp in case of loss of pressure signal (which represents mechanical power). Provides paths for lamp testing. Function (a) is initiated by a Volt. Com. (proportional part of unbalance) which shorts pins 34, 35 and another VC (rate part of unbalance) which applies 24V to pin 34. This voltage activates K3, which applies 24V to pin 34, (so that the action of the second VC is no longer necessary-hence the word mementarily above), as well as to pin 33. Besides, this 24V finds its way through NC contacts to pins 8, 9, 10, 11, 12  $^{13}$  and  $^{14}$  where the "action relays" (located elsewhere) and the inputs to FH & PC are connected. All relays except K3 remain de-energized. Function (b) is accomplished by applying 24V to pin 2. This provides power to the lamp connected on pin 3 and energizes relays K1, K2. These relays (1) interrupt the path to pins 8, 9, 10, 11, and 12; (2) apply 24V to pin 20, which causes a simulated PLU condition, which in turn is fed back as a 24V voltage to pin 35, and (3) connect relays K5, 6, 7, 8 coils to pin 35. The main function of these is to light lamp 1L2. Disconnecting 24V from pin 2 causes lamp 1L2 to go out. Any defect of the PLU circuits, including this one, will cause this lamp either not to light or to light and stay on after release of the test button. This function is performed in a fail safe manner in the sense that will never cause a valve closure, and with a high degree of redundancy. Function (c) is performed by applying 24V to pin 4, which lights the lamp

Function (c) is performed by applying 24V to pin 4, which lights the lamp connected to pin 5. Function (d) is performed by applying 24V to pin 6, which lights the lamps connected to pins 7, 3, 5.

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TITLE TEST INSTRUCTIONS FOR POWER LOAD UNBALANCE LOGIC CIRCUIT BOARD

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FIRST MADE FOR

REVISIONS

# 1975

#### CIRCUIT SPECIFICATIONS III.

1. Before the board is coated, each diode of the 8 diode pairs should be checked (e.g. using an ohmeter) both in the forward and reverse direction, to insure that redundancy is effective.

The rest of the tests can be conducted with the board coated as well as uncoated.

With ground connected at pin 40 and +24V connected to TP6, TP52-TP3, should form a closed circuit, TP8-TP55 should form a closed circuit, and TP55 should remain at 0.V. \*

The same conditions should exist with +24V connected to TP7 instead of TP6.

Connect permanently ground to pin 40 and +24V to pin 38. A +24V should appear between TP1 and TP2.

Connect permanently loads (e.g. standard 20 ma 28V miniature lamps) between ground and pins 3, 5, 7, 8, 9, 10, 11, 12, 13, 14, 20, 33 and

The logic and conduit continuity should be checked according to the following table:

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Steam Turbine

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GENERAL & ELECTRIC P3K-AL-0326-A01 SH NO. 🎒 CONT ON SHEET TITLE TEST INSTRUCTIONS FOR POWER LOAD UNBALANCE LOGIC CIRCUIT BOARD P3K-AL-0326-A01 4 FIRST MADE FOR 5 SH NO. CONT ON SHEET REVISIONS Follow Sequence Without \* \* 0: Discontinuities 0 N 0 0 0 8 0 +24V or lamp on (\*In this case 1 represents lower voltage for abnormal brightness indicating wrong resistor. INPUTS AT PINS 2 These states can occur during operation due to non (momentarily) or lamp off O 4 0 0 0 0 Ö 0 JAN 0 9 0 0 Ö 0 0 0 0 35 0 PLU Circuit Test + or H Signal Loss of Id1e Id1e PLU Condition Lamp occurred\*\* Test button released Simulated PLU Simulated PLU occur-Test button depressed tinguished Simulated PLU extinguished\*\* Simulated PLU not Test button depressed MEANING OF STATE because Test \* Pressure O. external circuit defects not exyet 0 0 ᅷ 0 0 0 0 0 0 0 <del>ا</del> Ċī 0 0 <u>بر</u> \* 0 0 0 0 0 0 0 0  $\infty$ 0 0 0 0 0 Q 0 0 0 0 0 0 0 0 LAMPS zero external circuit 0 10 O 0 0 (persistently). 0 0 due 0 0 0 0 0 0 0 O O Q 0 0 14 12 0 ç CORRECT OUTPUTS 0 0 0 20 0 0 0 68.1**,1** (ည (ည 0 O 0 0 0 52 response  $\circ$ 0 resistors 0 0 0 0 0 0 0 0 0 0 0 0 0 0 time **5** 0 0 0 0 O 0 0 1 0 0 Ó 0 0 Watch 0 0 0 O 0 0 O 0 0 0 0 0 + PRINTS TO APPROVALS P3K-AL-0326-A01 DIV OR D.Mone 1973 Steam Turbine 20, Mar. SH NO. 1373 CONT ON SHEET S LOCATION Schenectady, N.Y. CODE IDENT NO. FF-803-WA (11-72)

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P3K-AL-0326-A01

Test Instructions for Power Load Unbalance Logic Circuit Board

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6 SH NO. 5

FIRST MADE FOR

TEST INSTRUCTIONS 1PU2-A001

Assembly 117D7745

Schematic 115D2204

### PROCEDURE:

- 1. Refer to Table A for test circuit.
- 2. Measure +24 VDC from TP1 to TP2.
- 3. The chart which follows outlines the procedure for testing the relay logic of this circuit.

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P3K-AL-0326-A01 TEST INSTRUCTIONS FOR POWER LOAD UNBALANCE LOGIC CIRCUIT BOARD FIRST MADE FOR SH NO. CONT ON SHEET REVISIONS 1975  $\sim$ ដ 검 g t +24VDC PROCEDURE Check for 4 TP3, 4, 6, ţ, ď End 36 PRINTS TO APPROVALS DIV OR P3K-AL-0326-A01 Steam Turbine \_ DEPT.

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TEST INSTRUCTIONS FOR POWER LOAD UNBALANCE LOGIC

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CIRCUIT BOARD FIRST MADE FOR

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		Table A
Pin 35 6 7 2 3 5 4	SW3 up SW4 up SW5 up SW6 up SW7 up SW8 up SW8 up	
38 40	+24 VDC	
20 8 9 10 11 12 34 33	L1 12 L3 L4 L5 L6 L7	
6 7 2 3 5 4	L9 L10 L11 L12 L13 L14	

Switch commons are wired to +24 VDC. NOTE:

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+>		Bugg  HC TEST ENGINE	<b>C</b> R	DATE: _	2/21/72	30
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