REVISIONS

TEST INSTRUCTIONS 1L1-G001

Assembly 115D2291

Schematic 115D2289

use this set for Test.
HPE 4/14/89

PROCEDURE:

1. Refer to Fig. A for test circuit.
2. Refer to Fig. B for equipment list and setup instructions.

NOTE: All settings and specifications are ±1MV unless otherwise specified.

All setpoints must not be closer than 2 turns from either end of setpoint pot.

Before Plugging Board In:

3. Adjust VR2 CW. Adjust VR5 CCW.
4. ALL SWITCHES DOWN.

Plug Board In:

5. Check test supply voltages for +22.00VDC at Pin 37 and -22.00 VDC at Pin 41.

PRINTS TO

6. Check ckt. bd. supply voltages at TP1 and TP2 for +15.7 and -15.7 VDC (Tol. = ±1.0VDC).

7. S2 up - ground TP9.

8. Adj. VS1 and VS2 for 0.00VDC at pins 27 and 26 (TP7 and TP6).

9. Adjust offset (VR50) of IC 1 for 0 VDC at pin 33. (TP3)

10. Adj. offset (VR51) of IC 2 for 0 VDC at pin 29. (TP10)

11. Adj. VS1 for 10.00 VDC at pin 27. (TP7)

12. Check saturation voltage of IC 1. (> -13.00 VDC at TP4)

13. Check saturation voltage of IC 2. (> -12.00 VDC at TP10)

14. Adj. VS1 for -10.00 VDC at pin 27. (TP7) S1 up. clear

15. Check saturation voltage of IC 1. (> +13.00 VDC at TP4)

16. Check saturation voltage of IC 2. (> +12.00 VDC at TP10) S1 down.

17. Adj. VR2 CCW.

18. Check range of VR3 at TP3.

CW	CCW
-1.275 / 1.531 VDC	-1.308 / 1.572 VDC
~~11.355/11.819 VDC~~	~~6.309/7.216 VDC~~

19. Adj. VR2 CW (Final Setting)

20. Check range of VR3 at TP3.

CW	CCW
11.355/11.819 VDC	6.309/7.216 VDC

21. Adj. VR3 at TP3 for +10.000 VDC (Final Setting).

22.- Adj. VS1 for -1.000VDC at pin 27 (TP7).

23.- Check TP3 for +4.900 to 5.100VDC.

24.- Adj. VS1 for 0.00VDC.
Adj. VS2 for -1.000VDC at pin 26 (TP6).

25.- Check the range of VR1 at TP3.

CW	CCW
+3.680/3.830VDC	1.189/1.305

26.- Adj. VS2 for 0.00 VDC.

27.- S2 down.

28.- Check TP5 for +9.940 to 10.158 VDC.

29.- Remove VS2 from pin 26.
Connect VS2 to TP5.
Adj. VS2 for +1.000 at TP5.

30.- S3 up.

31.- Check TP3 for -1.960 to 2.040 VDC. (Wait for C3 to charge)

32.- Adj. VS2 for 0.00VDC.
Remove VS2 from TP5.
S2 up.

33.- Remove the ground from TP9.

34.- Check range of VR4 at TP9.

CW	CCW
-10.462/10.682VDC	-9.408/9.784VDC

35.- Adj. VR4 for -10.000VDC at TP9.

36.- Check TP3 for +9.980 to 10.020 VDC.

37.- Adj. VR4 for +10.000 at TP3.

38.- Check TP10 for +10.000VDC.

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TEST INSTRUCTIONS FOR INTERCEPT VALVE AMPLIFIER

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39.— Check the range of VR5 at pin 31.

CW	CCW
> 80 MV	< 25 MV

40.— Adj. VR5 for +40 MVDC at pin 31.

41.— Adj. VS1 for +2.000VDc at pin 27 (TP7).

42.— Adj. VR4 for 0.00VDC at TP3 (Final Setting).

43.— Ground TP9
S3 down - open

44.— Adj. VR1 CW.

45.— Disconnect VS1 and VS2.

Table 1 is a summary procedure for measuring the noise suppression lag of each amplifier input filter circuit. Each row on the table provides data to enable testing of one input filter.

Repeast steps 46 thru 51 for each row on the table.

46. Connect the FUNCTION GENERATOR to the APPLY INPUT pin. 27
(Mode - sine wave, offset = 0 unless specified otherwise).

47. Connect the SCOPE to the MONITOR OUTPUT test point. 3

48. Set the FUNCTION GENERATOR to the frequency specified under INPUT FREQ. and to the amplitude specified under INPUT AMPLITUDE.

49. Measure the output at the MEASURE OUTPUT pin. 33

50. The acceptable output amplitude must be in the range specified under OUTPUT AMPLITUDE.

51. Monitor the output signal to assure that no distortion occurs in the amplifier.

52.— Connect VS1 to pin 27.
Adj. VS1 for 0.00VDC at pin27 (TP7)

53.— Connect VS2 to pin 26.
Adj. VS2 for 0.00VDC at pin 26 (TP6).

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54. The noise suppression lag time constant of the closing bias input will be measured by applying a step input voltage and measuring the amplifier response with a plotter.

    Use S2 to apply a step from 0V to +10.0VDC (at TP5). The acceptable response at TP3 is as shown in Figure 1.

55. Adj. VS2 for -10.000VDC at pin 26 (TP6).

56. Adj. VS1 for +7.000VDC at pin 27 (TP7).

57. Remove the ground from TP9.

58. S2 up.

59. Adj. VR1 for 0.00VDC at TP3. (Final Setting)

60. End of Test.

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P3K-AL-0373-A01

TEST INSTRUCTIONS FOR INTERCEPT VALVE AMPLIFIER

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TABLE 1

DC Gain has been checked in previous step SDC 4-14-81

APPLY INPUT	INPUT FREQ.	INPUT AMPLITUDE	MONITOR OUTPUT	MEASURE OUTPUT	OUTPUT AMPLITUDE			
PIN	HZ	VOLTS RMS	TP	PIN	VOLTS RMS	A VDC	V/V	fo HZ
27	104	1.0	3	33	3.28/3.81	5		105 ±12
26	143	1.0	3	33	2.47/2.86		3.76	144 ±16

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MADE BY

ISSUED

APPROVALS

Steam Turbine DIV OR DEPT.

Schenectady LOCATION

P3K-AL-0373-A01

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CODE IDENT NO.

FF-803-WB (6-74)
PRINTED IN U.S.A.

REV NO.

P3K-AL-0373-A01

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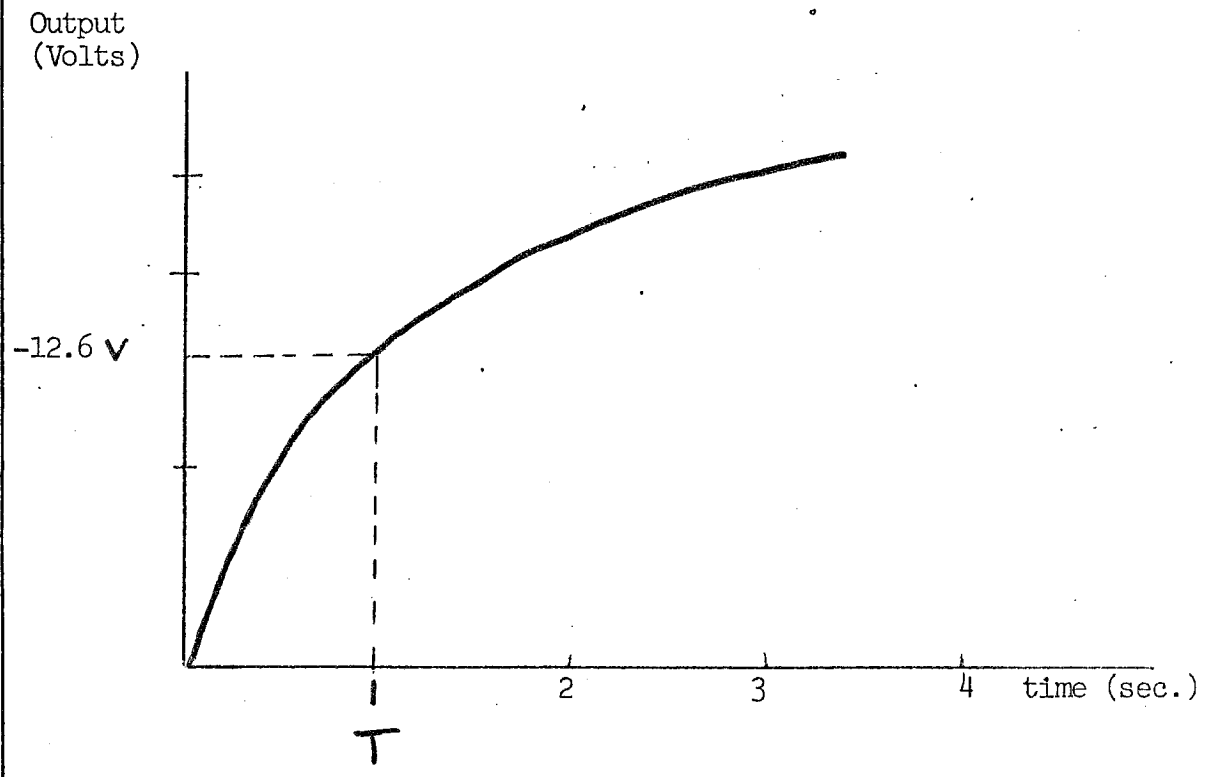
FIGURE 1



The time constant is the time required for the output to rise to 63% of its final value; in this case -12.6 VDC.

For acceptance, the time constant must be between 750 and 1120 MS.

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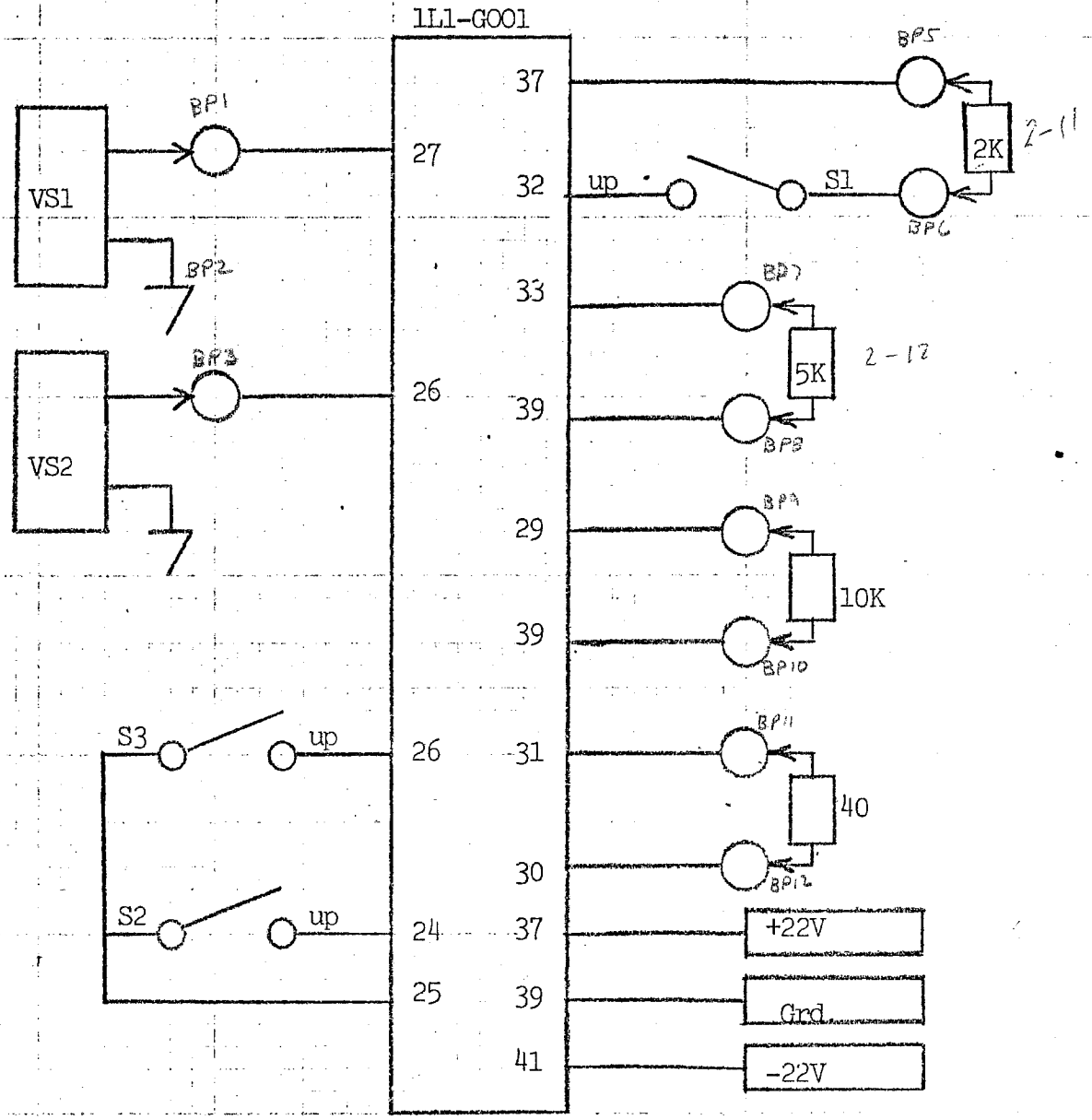

FIGURE A

PRINTS TO

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P3K-AL-0373-AO1 | TEST INSTRUCTIONS FOR INTERCEPT VALVE AMPLIFIER

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EQUIPMENT NEEDED

A. DVM 5 digit AC/DC SD7005A

B. VS1, VS2 DC power supply HP6112A

C. Function generator HP3300A

D. Frequency counter SD6150

E. Scope TEK R5103N

F. XY plotter Honeywell 530

SETUP INSTRUCTIONS

1. All loads to be applied to the ckt, under test are ±1% tolerance.

2. All signals are measured and applied with respect to Pin 39.

FIGURE B

PRINTS TO

REV NO.	TITLE
P3K-AL-0373-A01 CONT ON SHEET --- SH NO. 15	TEST INSTRUCTIONS FOR INTERCEPT VALVE AMPLIFIER 1L1-G001 (ASS'Y DRAWING 115D2291 G-1) FIRST MADE FOR EHC MARK II (LOAD CONTROL UNIT)

REVISIONS

PREPARED BY D. Economou DATE 7/26/73
D. Economou
EHC DESIGN ENGINEERING

APPROVED BY _____ DATE _____
P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE
PREPARED BY _____ DATE _____
C. Bugg
EHC TEST ENGINEER

TEST PROCEDURE
REVIEWED BY _____ DATE _____
D. Economou
EHC DESIGN ENGINEERING

PRINTS TO