

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	D.F.BEHRINGER SH 2 P 2,1. BOARD PI FULLY COUNTER CLOCKWISE WAS BOARD PI FULLY CLOCKWISE. SH 3 P 5,1,1. BOARD PI FULLY CLOCKWISE WAS BOARD PI FULLY COUNTER CLOCKWISE.	9/10/86	DFB
B	D. Lison CN91-4177 SHEETS 2 THRU 5 RETYPED WITH CHANGES. ORIGINALS MARKED PERMANENT COPY.	9/1/03/01	FHH

DIST TO	170	14E
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ORIGINALLY FURNISHED, EXCEPT WITH WRITTEN PERMISSION FROM GE NAVAL & DRIVE TURBINE SYSTEMS DEPARTMENT.

## 1.0 SET-UP

- 1.1 Check that the board has all proper JG2 components and jumpers.
- 1.2 Check that the board has all the required modifications and deviations, if any.
- 1.3 Check that plug-in devices IC3 and IC4 are properly assembled.
- 1.4 Connect the test circuit shown in Figure 1.

## 2.0 POWER CHECK

- 2.1 Run test P1 fully counterclockwise, run test P2 and test P3 fully counterclockwise, run board P1 fully counterclockwise, apply power and verify that applied voltage, voltage regulator outputs and current drains are as specified.

## 3.0 PILOT VALVE LVDT CHANNEL

### 3.1 Excitation and Bias

- 3.1.1 Adjust test P2 to get at TP3 the value specified.
- 3.1.2 Observe the waveform between PIN 29 (+) and PIN 31 (-). Check that it is a noise free sine wave, that it has the peak-to-peak voltage specified, that it has the frequency specified and that it has the AC voltage specified.
- 3.1.3 Check that the AC voltage between PIN 30 (+) and PIN 31 (-) is at the value specified.

### 3.2 Gain

- 3.2.1 Adjust test P2 to get between PIN 30 (+) and PIN 31 (-) the AC voltage computed as specified.
- 3.2.2 Adjust board P2 to get at TP3 the value specified.



DEPT N&amp;DTS LOC FITCHBURG

SIZE

**A**

CAGE CODE

**03502**

TEST INSTRUCTION FOR:  
125D458AD

DRAWN DE BEHRINGER, 84-03-29

ISSUED SEE SHEET 1

SCALE

**NONE**

165A855AC

REV **B**

SHEET

**2**

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#### 4.0 OPERATOR LVDT CHANNEL

##### 4.1 Excitation and Bias

- 4.1.1 Adjust test P3 to get at TP4 the value specified.
- 4.1.2 Observe the waveform between PIN 26 (+) and PIN 28 (-). Check that it is a noise free sine wave, that it has the peak-to-peak voltage specified, that it has the frequency specified and that it has the AC voltage specified.
- 4.1.3 Check that the AC voltage between PIN 27 (+) and PIN 28 (-) is at the value specified.

##### 4.2 Gain

- 4.2.1 Adjust test P3 to get between PIN 27 (+) and PIN 28 (-) the AC voltage computed as specified.
- 4.2.2 Adjust board P3 to get at TP4 the value specified.

#### 5.0 SERVO AMPLIFIER

##### 5.1 Off Current

- 5.1.1 Run test P1 fully counterclockwise, run test P2 and test P3 fully clockwise and run board P1 fully clockwise. Check that A3 current drain is as specified.

##### 5.2 Lift Setpoint Channel Gain

- 5.2.1 Adjust test P1 to get at TP2 the value specified. Adjust board P1, test P2 and test P3 to get the A3 current drain specified. Recheck TP2. Trim all devices to satisfy both requirements.
- 5.2.2 Adjust test P1 to get the A3 current drain specified. Check that TP2 is at the value specified.



DEPT N&amp;DTS LOC FITCHBURG

SIZE  
A

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03502

TEST INSTRUCTION FOR:  
125D458AD

DRAWN DF BEHRINGER, 84-03-29

ISSUED SEE SHEET 1

SCALE NONE

165A855AC

REV B

SHEET

3

## PROPRIETARY INFORMATION

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### 5.3 Pilot Valve LVDT Channel Gain

5.3.1 Adjust test P2 to get at TP3 the value specified. Adjust board P1, test P1 and test P3 to get the A3 current drain specified.

5.3.2 Adjust test P2 to get the A3 current drain specified. Check that TP3 is at the value specified.

### 5.4 Operator LVDT Channel Gain

5.4.1 Adjust test P3 to get at TP4 the value specified. Adjust board P1, test P1 and test P2 to get the A3 current drain specified.

5.4.2 Adjust test P3 to get the A3 current drain specified. Check that TP4 is at the value specified.

### 5.5 Bias

5.5.1 Run board P1 fully counterclockwise. Adjust test P1, test P2 and test P3 to get the A3 current drain specified. Check that TP6 is at the value specified.

5.5.2 Run board P1 fully clockwise. Adjust test P1, test P2 and test P3 to get the A3 current drain specified. Check that TP6 is at the value specified.

5.5.3 Adjust test P2 to get at TP3 the value specified.

5.5.4 Adjust test P3 to get at TP4 the value specified.

5.5.5 Adjust test P1 to get at TP2 the value specified.

5.5.6 Adjust board P1 to get the A3 current drain specified.

### 5.6 Non-Linear Input Circuit

5.6.1 CR7 Off Check

5.6.1.1 Adjust test P1 to get at TP2 the value specified.



SIZE

CAGE CODE

A

03502

TEST INSTRUCTION FOR:  
125D458AD

DEPT N&amp;DTS LOC FITCHBURG

DRAWN DF BEHRINGER, 84-03-29

ISSUED SEE SHEET 1

SCALE NONE

165A855AC

REV B

SHEET

4

SIZE <b>A</b>	165A855AC	SHEET 5	REV <b>B</b>
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- 5.6.1.2 Adjust test P2 and test P3 to get the A3 current drain specified.
- 5.6.1.3 Check that CR7 anode is at the value specified.
- 5.6.1.4 Adjust test P1 to get at TP2 the value specified.
- 5.6.1.5 Adjust test P2 and test P3 to get the A3 current drain specified.
- 5.6.1.6 Check that CR7 anode is at the value specified.

5.6.2 Gain Check


- 5.6.2.1 Adjust test P1 to get at TP2 the value specified.
- 5.6.2.2 Adjust test P2 to get at TP3 the value specified.
- 5.6.2.3 Adjust test P3 to get the A3 current drain specified.
- 5.6.2.4 Adjust test P1 to get at TP2 the value specified.
- 5.6.2.5 Adjust test P2 to get the A3 current drain specified.
- 5.6.2.6 Check that TP3 is at the value specified.

6.0 NOISE CHECK

- 6.1 Check with an oscilloscope that the noise between TP9 and TP8 does not exceed the specified value.

**NOTE:** Neither TP9 nor TP8 are at signal common. Do not connect either one to signal common.

- 6.2 Check with an oscilloscope that the noise amplitude and noise beat at TP3 and TP4 do not exceed the values specified.
- 6.3 Check with an oscilloscope that the noise at TP5 and TP6 do not exceed the value listed.

	SIZE <b>A</b>	CAGE CODE <b>03502</b>	<b>TEST INSTRUCTION FOR: 125D458AD</b>			
DEPT <b>N&amp;DTS</b> LOC <b>FITCHBURG</b>						
DRAWN <b>DF BEHRINGER, 84-03-29</b>						
ISSUED <b>SEE SHEET 1</b>	SCALE <b>NONE</b>	165A855AC	REV <b>B</b>	SHEET	5	

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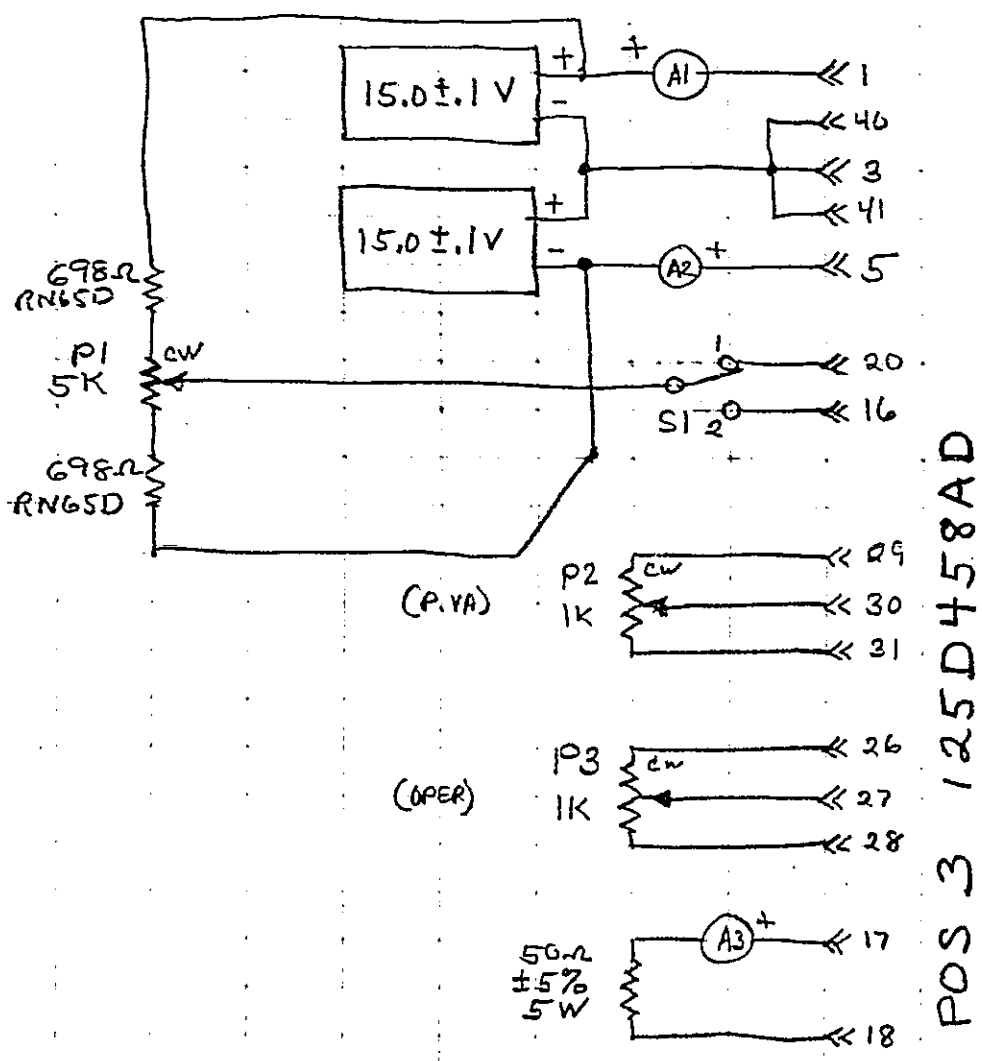


FIGURE 1. -- TEST CIRCUIT

POS 3 125D458AD

13G 14E