

REV  
NO.

TITLE

TEST INSTRUCTIONS OP/DFG AMP  
CIRCUIT BOARD 117D9929 G-1  
FIRST MADE FOR

P3K-AL-0220

CONT ON SHEET

2

SH NO.

1

GENERAL

*See next page for test.*

This board is a direct replacement for OP/DFG Amp Bd. 948D881 G-4, and is always used with the VPU preamplifier function board.

A. POWER SUPPLIES

$$V_{TP1} = 15.7 \pm 1 \text{ VDC}$$

$$V_{TP2} = -15.7 \pm 1 \text{ VDC}$$

B. PREAMPLIFIER (IC1)

Using a setup similar to that in figure 1, verify the following:

ACTIVE FOR TEST  
BY *form* DATE *6-3-96*

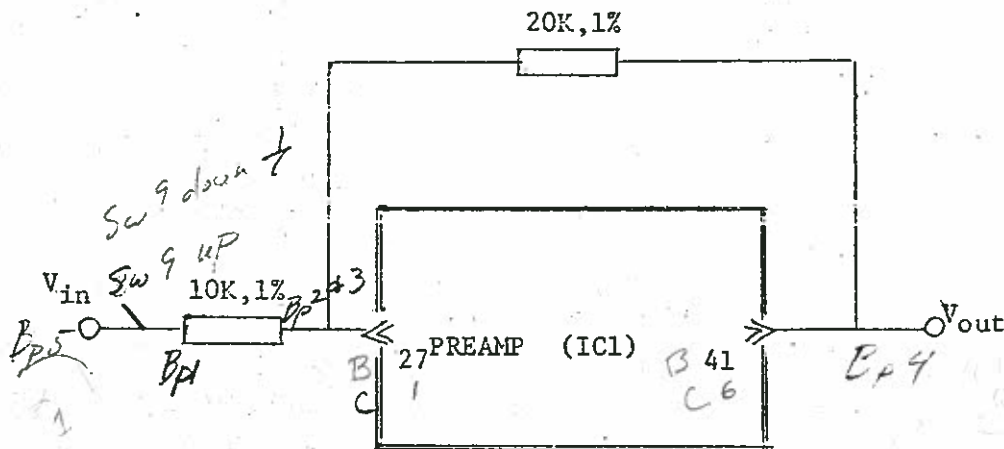


FIGURE 1

1. Null IC1 (VR1)

$$2. -2.05 < \frac{V_{out}}{V_{in}} < -1.95$$

$$3. |V_{out}| < 9.2 \text{ VDC}$$

*GAIN = 2 with 3V or less input*

$$|V_{in}| < 3 \text{ VDC}$$

*clamp before 9.2V*

C. FEEDBACK AMPLIFIER (IC2)

1. Null IC2 (VR2)

$$2. 2.95 < V_{TP6} < 3.05 \text{ (VR3 CW),}$$

$$(0 \leq V_{TP5} < 3 \text{ VDC})$$

*GAIN OF 3 ± .05*

$$2 \text{ V} = 6 \text{ V out}$$

VERIFIED

ET-273

273-2

273-12

273-13

273-17

273-71

PRINTS TO

MADE BY  
D.Mone Oct. 8, 1974

ISSUED  
OCT 8 1974

APPROVALS

Steam Turbine

Schenectady, N.Y.

DIV OR  
DEPT

LOCATION

P3K-AL-0220

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## REVISIONS

1. Connect test circuit as shown in Fig. A.
2. Check test supply voltage (Tol.  $\pm 1$  MV)
3. ~~S3~~ down S9 common (PIN 27)  
S4 down S10 pin 1 common
4. Check ckt. card supply voltages at TP1 and TP2 for +15.7 VDC and -15.7 VDC (Tol.  $\pm 1.0$  V)

## CHECK OP AMP

5. Adj. VR1 for 0 VDC at TP4.
6. ~~S3~~ up S9 to VS1 (PIN 27)
7. Adj. VS1 for -0.100 VDC at BP1. BP5 AT PS 1
8. Check TP4 for +2.50 VDC (Tol.  $\pm 100$  MV)
9. Adj. VS1 for -1.000 VDC
10. Check TP4 volts for ~~+2.500~~ <sup>2.2 to 2.9</sup> to +9.500 VDC
11. Adj. VS1 for +1.000 VDC.
12. Check TP4 volts for ~~-7.900~~ <sup>-7.79 to -8.61</sup> to -9.500 VDC. Per E.A.

## CHECK DFG DRIVING AMP

13. Adj. VR2 for 0 VDC at TP6.
14. ~~S4~~ up S10
15. Adj. VS2 for +5.00 VDC at TP5. BP7
16. Adj. VR3 for +5.00 VDC at TP6.

## FINAL ZERO ADJUST CHECK

17. ~~S3~~ down S9 common 27 TO COM  
S4 down S10 pin 1 to common
18. Make a final trim with VR1 for 0 VDC at TP4.
19. Make a final trim with VR2 for 0 VDC at TP6.
20. Apply red locking solution to VR1 and VR2. RTV
21. End of Test.

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SH NO. 2

P3K-AL-0220

TITLE

Test Instructions OP/DFG AMP  
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SH NO. 3

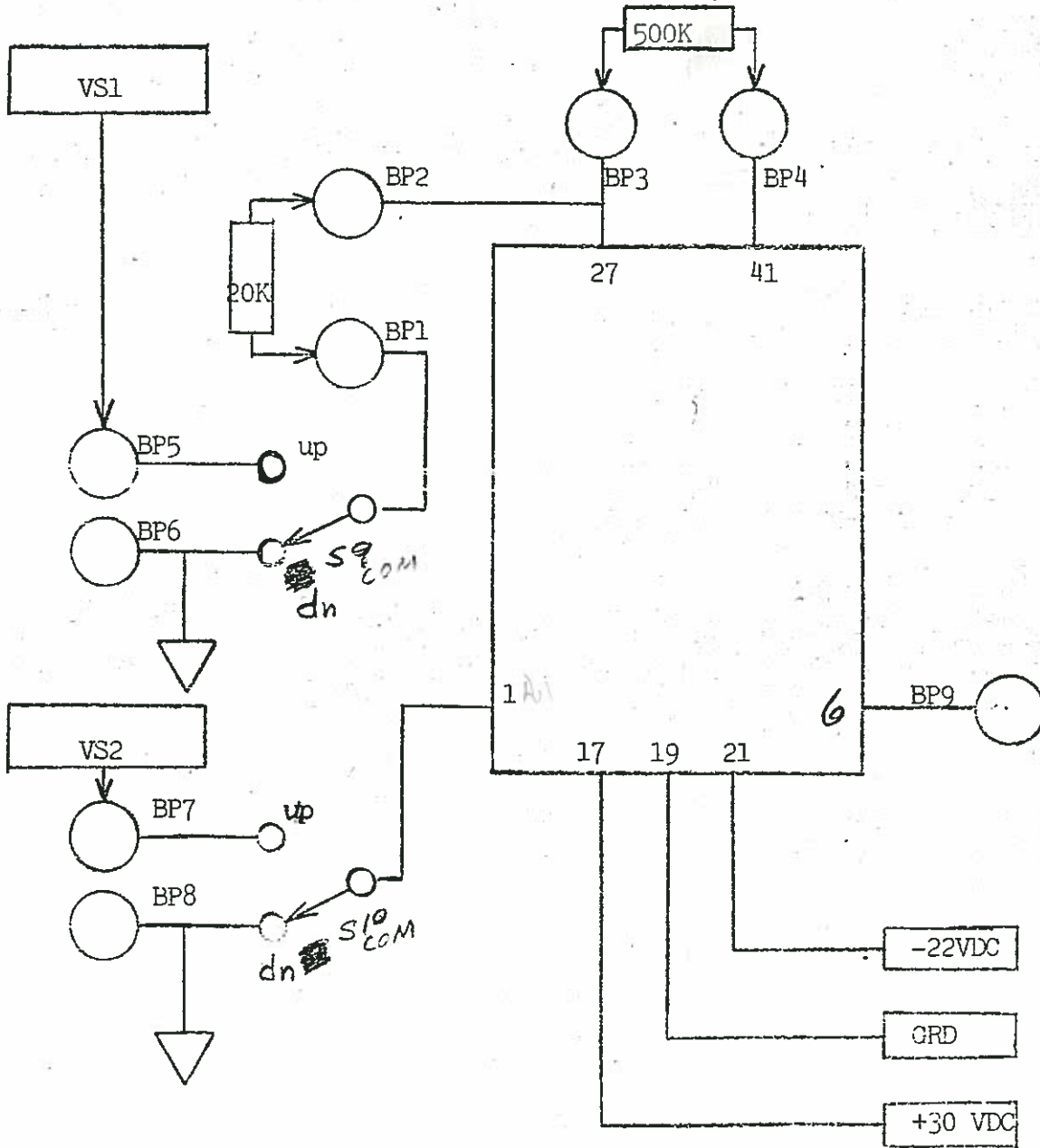
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REVISIONS

FIGURE 1

*FIG 1A*

*Patch Bnd 8-1  
1/16/84 PGB*



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PRINTS TO

P3K-AL-0220

CONT ON SHEET ---

SH NO. 4

TITLE

TEST INSTRUCTIONS OP/DFG AMP  
CIRCUIT BOARD 117D9929 G-1, G-2  
FIRST MADE FOR

REVISIONS

PREPARED BY

*S. S. Abelson*

DATE

5/24/74

S.S. Abelson  
EHC DESIGN ENGINEERING

APPROVED BY

*F.C. Callan*

DATE

10-4-74

F.C. Callan - MANAGER  
EHC DESIGN ENGINEERING

APPROVED BY

*C. Bugg*

DATE

5/28/74

C. Bugg  
EHC TEST ENGINEER

VERIFIED: \_\_\_\_\_

PRINTS T

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ISSUED OCT 8 1974

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Schenectady, N.Y.

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SH NO. 4

## Data Sheet

[illegible]