TITLE
TEST INSTRUCTIONS FOR CONTROL VALVE AMPLIFIER 1L1-E005
(ASS'Y DWG 118D1367 G1)
FIRST MADE FOR EHC MARK II (LOAD CONTROL UNIT)

REVISIONS
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I. SCOPE

This instruction outlines the test specifications for circuit board 1L1-E005. (Ass'y Dwg. 118D1367 G1, G2 & G3: for reference use schematic 125D3687).

NOTE: The Group 1 & 2 boards have been replaced on all BWR units. Ref. ECN T351-679.

II. CIRCUIT DESCRIPTIONS

Board 1L1-E005 is used on those turbines that have starting and loading on the control valves, do not require stage pressure feedback and have standby transfer at the input to the CVA.

The purpose of the Control Valve Amplifier (CVA) circuit is to combine all the necessary control functions to produce a single controlvvalve flow reference signal. This board includes three operational amplifiers that perform the following functions:

1. A control valve amplifier that sums a modified speed error, load reference and rotor-shell warming signal, along with either the isolated grid or load reference test signal. The output of CVA is applied to a voltage follower power stage to provide the necessary output current.

2. An isolation amplifier that operates as a voltage follower with a voltage follower power stage at its output. This circuit is switched in during standby operation only.

3. A CV matching amplifier that sums the speed error signal with the load reference signal to obtain a CV flow reference signal for the standby unit.

This board has input signals of speed error, load reference and standby. It also has relayed input signals of rotor-shell warming, isolated grid operation and load reference testing.

The speed error signal is further modified by the control valve regulation potentiometer that is mounted on the CVA printed circuit board to maintain the appropriate speed versus load relationship shown in Figure 1.

Logic relays switch out the speed error, load reference, isolated grid bias and load reference test bias signals, in the standby mode. The isolate grid bias signal is set for a 12% reduction in E_L at the CVA output. The load reference test bias is set for a 10% reduction in E_L at the CVA output.

The modified speed error signal is summed with the load reference signal to develop a control valve flow reference signal for normal operation. A ceiling limit resistor is incorporated at the output of the CVA to limit the CVAamplifier in the opening direction.

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273-5
~~273-2~~
273-12
273-71
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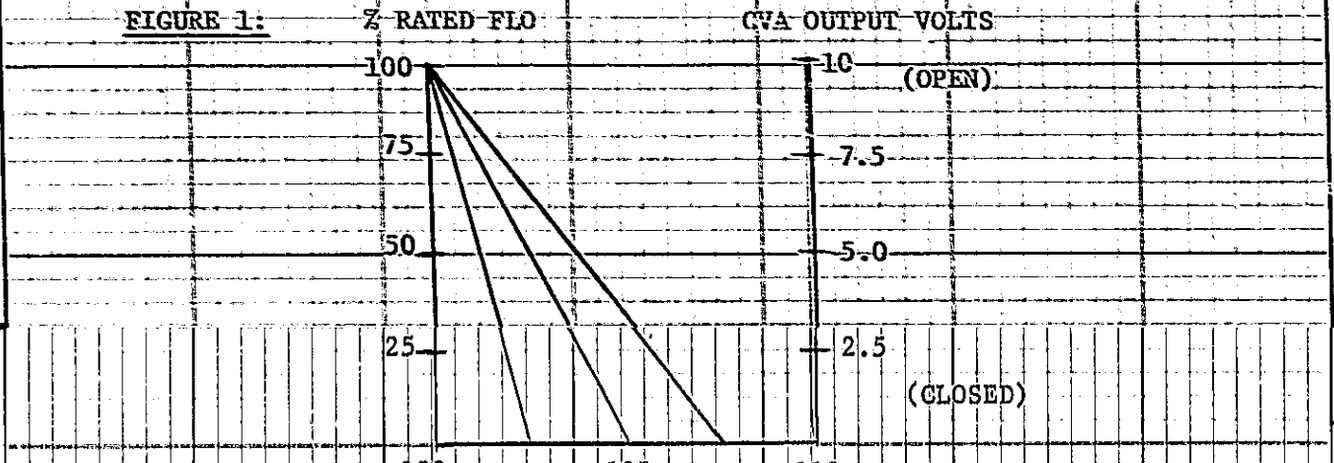
II. CIRCUIT DESCRIPTIONS (continued)

During the shell warming mode of operation, a control valve opening bias provided by relay action opens the control valves 100%. This bias is summed with the modified speed error signal and load reference signal to provide speed control during the warming mode. This bias is removed by pushbutton selection to the off mode.

The CV matching amplifier has speed error and load reference signals as inputs. The output signal is applied to a standby matching meter, plant communications, and to the standby circuits. A voltage follower called isolation amplifier is switched in during standby only.

FIGURE 1:



III. CIRCUIT SPECIFICATIONS

A. Power Supply Requirements

1. Power Supply 1: +22.000 ± 0.002 VDC
(Pin 37) at 275 MA (Approximately)

2. Power Supply 2: +22.000 ± 0.002 VDC
(Pin 41 at 100 MA (Approximately)

B. Operating Signal Levels

1. Input 1 (Speed Error Signal): ± 10.000 VDC
(Pin 4) (0 volts at speed, 1 volt/% speed error)

2. Input 2 (Load Reference Signal): 0 to -10 VDC
(Pin 11) (0 volts at no load, -10 volts at full load)

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III. CIRCUIT SPECIFICATIONS (continued)

B. (continued)

3. Input 4 (Valve Opening Bias): 0 to -22 VDC
(Pin 23) (0 volts at 0 pressure, 10 volts at rated pressure)

4. Input 5 (Isolated Grid Bias): +22 VDC (controlled by customer relay)
(Pin 3)

5. Input 6 (Load Reference Test Bias): +22 VDC (applied during test only)
(Pin 7)

C. Output Loads

1. Load 1: 5K Ohm ± 1% (Max. load)
(Pin 34)

2. Load 2: 200K Ohm ± 1%
(Pin 30)

3. Load 3: 40 Ohm ± 1% (simulates MA Meter)
(Pin 28)

4. Load 4: 100K Ohm ± 1%
(switched between Pins 21 and 40)

D. Individual Stage Performance Specifications

1. Power Supply (CR1, 2, 3 & 4)

a. TP1: +15.7 ± 1.0 VDC
b. TP2: -15.7 ± 1.0 VDC

2. Control Valve Amplifier (IC2)

a. Acceptable Offset at TP16.
(zero input): ± 1.0 MVDC
b. Transfer function for shell warming bias
(R37, R38, R7, C8, TP9, TP16)

$$\frac{TP16}{TP9} = \frac{-G1}{1 + T_1 S}$$

Where: Gain (G1) = 1.000 ± 0120 volts/volt
Noise suppression lag time constant (T1) = 1.38 ± 0.15 msec.
Noise suppression breakpoint (F1) = 117 + 13 HZ

c. Transfer function for load reference signal (R24, R23, R26, R7, C4)

$$\frac{TP16}{TP3} = \frac{-G2}{1 + T_2 S}$$

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III. CIRCUIT SPECIFICATIONS (continued)

D. (continued)

2. (continued)

c. Where: Gain (G2) = -1.000 ± 0.020 volts/volt
Noise suppression lag time constant (T2) = 2.02 ± 0.22 msec.
Noise suppression breakpoint (F2) = 79.8 ± 8.80 HZ

d. Transfer function for standby signal (R27,R28,R29,R7,C5)

$$\frac{TP16}{TP6} = \frac{-G3}{1 + T_3 S}$$

Where: Gain (G3) = -1.000 ± 0.020 volts/volt
Noise suppression lag time constant (T3) = 2.02 ± 0.22 msec.
Noise suppression breakpoint (F3) = 79.8 ± 8.80 HZ.

e. Transfer function for CV regulation modified speed error signal (R21, R22, R23, R7, C3)

$$\frac{TP16}{TP4} = \frac{-G4}{1 + T_4 S}$$

Where: Gain (G4) = -4.00 ± 0.080 volts/volt
Noise suppression lagetime constant (T4) = 1.42 ± 0.16 msec.
Noise suppression breakpoint (F4) = 113.60 ± 12.50 HZ

f. Transfer function for rotor-shell warming signal (R37, R38, R7, C8)

$$\frac{TP16}{TP9} = \frac{-G5}{1 + T_5 S}$$

Where: Gain (G5) = -1.000 ± 0.020 volts/volt
Noise suppression lag time constant (T5) = 1.38 ± 0.15 msec.
Noise suppression breakpoint (F5) = 117.05 ± 12.86 HZ

g. Transfer function for isolated grid bias signal (R33,R34,R7,C7)

$$\frac{TP16}{TP8} = \frac{-G6}{1 + T_6 S}$$

Where: Gain (G6) = -1.000 ± 0.020 volts/volt
Noise suppression lag time constant (T6) = 1.38 ± 0.15 msec.
Noise suppression breakpoint (F6) = 117.05 ± 12.86 HZ

h. Transfer function for load reference test bias signal (R30,R31, R7, C6)

$$\frac{TP16}{TP7} = \frac{-G7}{1 + T_7 S}$$

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III. CIRCUIT SPECIFICATIONS (continued)

D. (continued)

2. (continued)

h. Where: Gain (G7) = -1.000 ± 0.020 volts/volt
Noise suppression lag time constant (T7) 1.38 ± 0.15 msec.
Noise suppression breakpoint (F7) 117.05 ± 12.86 HZ

3. CV Matching Amplifier (IC3)

a. Acceptable offset at TP17 (zero input) ± 100 MVDC

b. Transfer function for load reference signal (min. gain) (VR3, R16, R17, R14, C1)

$$\frac{TP17}{TP3} = \frac{-G8}{1 + T_8 S}$$

Where: Gain (G8) = -0.854 ± 0.029 volts/volt
Noise suppression lag time constant (T8) = 1.52 ± 0.18 msec.
Noise suppression breakpoint (F8) = 106.0 ± 12.70 HZ.

c. Transfer function for load reference signal (max. gain) (R16, R17, R14, VR1 CW, C1)

$$\frac{TP17}{TP3} = \frac{-G9}{1 + T_9 S}$$

Where: Gain (G9) = -1.184 ± 0.040 volts/volt
Noise suppression lag time constant (T9) = 1.32 ± 0.15 msec
Noise suppression breakpoint (F9) 121.9 ± 13.40 HZ

d. Transfer function for CV regulation modified speed error signal (min. gain) (R19, R20, R14, C2)

$$\frac{TP17}{TP4} = \frac{-G10}{1 + T_{10} S}$$

Where: Gain (G10) = -3.767 ± 0.075 volts/volt
Noise suppression lag time constant (T10) = 1.65 ± 0.18 msec.
Noise suppression breakpoint (F10) 97.54 ± 10.72 HZ

e. Transfer function for CV regulation modified speed error signal (max. gain) (R14, VR1, R19, R20, C2)

$$\frac{TP17}{TP4} = \frac{-G11}{1 + T_{11} S}$$

Where: Gain (G11) = -4.434 ± 0.089 volts/volt
Noise suppression lag time constant (T11) = 1.65 ± 0.18 msec.
Noise suppression breakpoint (F11) 97.54 ± 10.72 HZ.

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III. CIRCUIT SPECIFICATIONS (continued)

D. (continued)

4. Isolation amplifier (IC1)

a. acceptable offset at TP13 (zero input) ± 1.0 MVDC

b. Transfer function for islation amplifier output (TP13, TP16)

$$\frac{TP13}{TP16} = G12$$

Where: Gain (G12) = 1.000 volts/volt

c. Saturation limits (10K Ohm effective load) = ± 12.0 VDC (Min.)

5. Voltage divider network for speed error signal (VR5, VR4, R18) 15K Ohm load off VR5 wiper.

VR5 Position	VR4 Position	Voltage at TP4
CCW	CW	-10.000 VDC
CW	CW	-3.168 ± 0.239
CW	CCW	-3.580 ± 0.289

6. For Group 1 & 2 Only

Voltage divider network for load reference test bias (R32, VR6)
Apply +22 VDC to Pin 7.

VR6 Position	Voltage at TP7
CW	+1.720 VDC ± 0.172
CCW	0

7. For Group 1 & 2 Only

Voltage divider network for isolated grid bias (R35, VR7)
Apply +22 VDC to Pin 3.

VR7 Position	Voltage at TP8
CW	+2.290 VDC ± 0.223
CCW	0

8. For Group 3 Boards

Voltage divider network for load reference test bias (R32, VR6)
Apply +13.1 VDC to Pin 7.

VR6 Position	Voltage at TP7
CW	+1.720 VDC ± 0.172
CCW	0

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III. CIRCUIT SPECIFICATIONS (continued)

D. (continued)

9. For Group 3 Boards

a. Voltage divider network for isolated grid bias (R35, VR7) Apply +10.1 VDC to pin 3.

VR7 Position	Voltage at TP8
CW	+2.290 VDC ± 0.223
CCW	0

b. Check resistor (10.2K) R41 at pin 2 by adding a 10.2K resistor in series. Read +11 VDC at pin 2.

10. Voltage divider network for CV amp ceiling limit (R5, R6 and an external load of 100K Ohms)

+11.970 VDC ± 0.109

11. Voltage divider network for isolation amp ceiling limit (R5, R6 and an external load of 100K Ohms)

+11.224 VDC ± 0.110

IV. SETPOINTS

A. Adjustment of VR5 and VR4 (Pin 14 not to be grounded)

These two (2) potentiometers are used to establish the CV regulation limits for the speed error signal.

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IV. SET POINTS (continued)

A. (continued)

VR4 should be adjusted to permit a CV regulation range of 2.5 - 7.5% which corresponds to the full CCW and full CW position of VR5.

To implement this, set VR5 full CW and adjust VR4 to produce a DC gain of +1.333 volts/volt, between TP4 and TP5. This sets the 7.5% regulation point. The 2.5% regulation point is fixed by the rest of the circuit.

B. Adjustment of VR2

This potentiometer sets the current drive for a milliammeter. Set VR2 to produce full scale deflection of meter for +10000 VDC at TP17.

C. Adjustment of VR3

This potentiometer sets the 4:1 signal ratio between load reference and speed error to obtain proper regulation.

D. Adjustment of VR1

This potentiometer varies the gain of IC3 to obtain +10 V at TP17.

E. Adjustment of VR6

Set this potentiometer to obtain a 10% reduction in E_L at TP16.

F. Adjustment of VR7

Set this potentiometer to obtain a 12% reduction in E_L at TP16.

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J.D. 7-7-82

APPROVED BY P C Callan DATE 9-12-77
P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE
REVIEWED BY R. W. Debertolis DATE 9-9-77
R. Debertolis
EHC TEST ENGINEER

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