General Description:

The low value gate is essentially a summing junction to give acceleration error (actual acceleration minus acceleration reference) when accelerating, and speed error (actual speed minus speed reference) when at speed. It is called a low value gate because it takes the signal (acceleration error or speed error) corresponding to the lowest valve position for its output. The more positive signal will call for the lowest valve position.

There are two identical low value gate boards. One is called the primary and the other the back-up low value gate. Each board receives the same inputs; a separate speed signal, however, it supplied each gate from the two power amplifier and magacycler boards. In actual operation the outputs of the two gates will be tied together through two diodes (CR3). The input potentiometers on the back-up gate will be set such that CR3 (on the back-up gate) will be reverse biased under normal operation (when the primary gate is controlling). If the primary low value gate malfunctions for some reason (upon failure of an amplifier or loss of the primary speed signal, for example), its output will go negative to cut off the output diode (CR3). The corresponding diode on the back-up gate will then be forward biased, thus bringing the back-up low value gate into control. Since each board will be tested separately, the operation will be described without the outputs tied together.

The inputs to the board are the speed signal, speed reference, wobbulator signal, and acceleration reference. The speed reference and speed signal are summed by the speed amplifier, whereas acceleration reference and actual acceleration are summed by the acceleration amplifier. The wobbulator signal is added via the speed amplifier to give a slow variation in speed about 3000 RPM whenever that speed is called for. The speed reference and speed signal are summed directly by the speed operational amplifier to give speed error. The acceleration operational amplifier is used to differentiate the speed signal (to give acceleration) and sum this with the acceleration reference. The amplifier circuit also integrates both signals; thus, the output is the resultant of a positive-going ramp (from the acceleration input) and a negative-going ramp (from the acceleration reference input) which cancel exactly when the turbine is accelerating at the rate called for.

When the turbine is at speed, the output of the speed amplifier (speed error) will be zero since the speed reference and actual speed will be matched. The acceleration amplifier will be in negative saturation (since turbine acceleration is 0). If a higher speed is then called for, the speed error will go negative, thus driving the speed amplifier into negative saturation. This negative signal calls for the valves to open further, and the turbine will start to accelerate. At this time, the output of the acceleration amplifier will rise since the two inputs (acceleration and acceleration reference) are now more closely matched. With the speed amplifier in negative saturation (-7 volts CR1 will be reverse biased and CR2 will be forward biased to bring the acceleration amplifier into control. The turbine will then accelerate at the rate called for by the reference. The output of the acceleration amplifier will stay slightly negative to keep the valves opening slowly (to keep the turbine accelerating). When the turbine reaches the speed called for by the speed reference,

REVISIONS
1 V. Schnable JUN 4 1986 NO CHG. THIS SHT.

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the speed amplifier will come out of negative saturation toward 0 volts. This reverse biases CR2 and forward biases CR1 to bring the speed amplifier back into control. The card output will then hold constant at 0 volts until another speed is selected. The transistor circuit at the output of the amplifiers is used for current amplification to drive the external load. Its base to emitter drop may be neglected.

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1 V. Schneible JUN 4 1984 NO CHG. THIS SHT.

PRINTS TO

CIRCUIT BOARD TEST FOR LOW VALUE GATE

FIRST MADE FOR 872D432-G1 & G2

REVISIONS

1	D. Schmidle JUN 4 1968	NO CHG. THIS SHT.

1. Speed Circuit Checks

NOTE: Set the zero offset of op amps 1 & 2 to 0.000.

Select the proper patchboard needed to properly test this board, or wire up one according to wiring diagram appearing at the end of these instructions.

2. Using th Wayne Kerr bridge measure and record the value of C1 and C2 on all the L.V.G. boards to be tested, on their respective test data sheet; label the value of C with dymo label tape on the board next to capacitor C1 and C2.

3. Plug the board under test into PCR2.

4. Jumper BP2, BP3, BP5, BP6, to BP10. This grounds all unused inputs for the moment.

5. Adjust pot 1 for approximately +10 volts at BP11.

6. Jumper BP11 to BP4; this will apply a large positive bias on the acceleration circuit while checking out the speed amplifier portion. Check TP4 to insure that op 2 is in negative saturation. ~~(-6.8 to -7.2 V)~~ -8.7 ± .2 also place a jumper across C1 (shorting it out).

7. With an external power supply, apply to BP1 -0.5000V.

8. Monitor BP7 with the dvm and adjust R1 for +2.500V at BP7.

9. Remove the applied voltage from BP1 and remove the ground from BP2, and ground BP1.

10. Apply -20.00V to BP2; with dvm at BP7 adjust R13 for +1.000V.

11. Remove the applied voltage to BP2 and remove the ground from BP3, and ground BP2.

12. Apply -1.000V to BP3 while checking with the dvm at BP7 for +1.00V±.1 out.

13. Remove the applied signal to BP3 and ground BP3.

14. Remove the ground from BP6 and apply -0.100V to BP6; adjust R17 for +2.000V at BP7.

15. Remove the applied voltage from BP6, remove the jumper from BP11 to BP4 and jumper BP11 to BP6. This now will drive the speed amplifier into negative saturation while checking out the acceleration circuit.

16. Apply with an external power supply -1.000V into BP4 and adjust R8 for +1.00 out at BP7. With DVM check that voltage is present at BP8 & BP9, (+1.000V ±.1

17. Remove the applied voltage from BP4 and remove the ground from BP5 & ground

TITLE

CIRCUIT BOARD TEST FOR LOW VALUE GATE

FIRST MADE FOR 872D432-G1 & G2

17. (Continued)
BP4.

18a. For G1 type boards: R14 should be a 2 meg pot and R15 a 9.09 meg resistor. Apply -20.00V to BP5 and adjust R14 for .200V at BP7.

18b. For G2 type boards, R14 should be a 10K resistor and R15 a 95.3K resistor. In this case apply -1.000V to BP5 and adjust R14 for +1.000V at BP7.

19. Remove the applied voltage from BP5 and ground BP5.

20. Remove the ground from BP1 and jumper C2, then apply +0.333V to BP1 and read at BP7 +1.000V.

21. Remove the jumper from C2; the output at BP7 should decay from 1.0V to 0.0 in approx. 1 sec.

22. Remove the jumper from C1.

23. Remove test leads, stamp board with test stamp and sign off in test log book.

TEST COMPLETE

REJECTIONS

If voltages as stated are not attainable, or if any adjustments cannot be reached, the board should be rejected and Control Engineering notified.

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1	D. DeNora JUN 4 1971	CHANGES MADE

PRINTS TO

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CONT ON SHEET 7 SH NO. 6

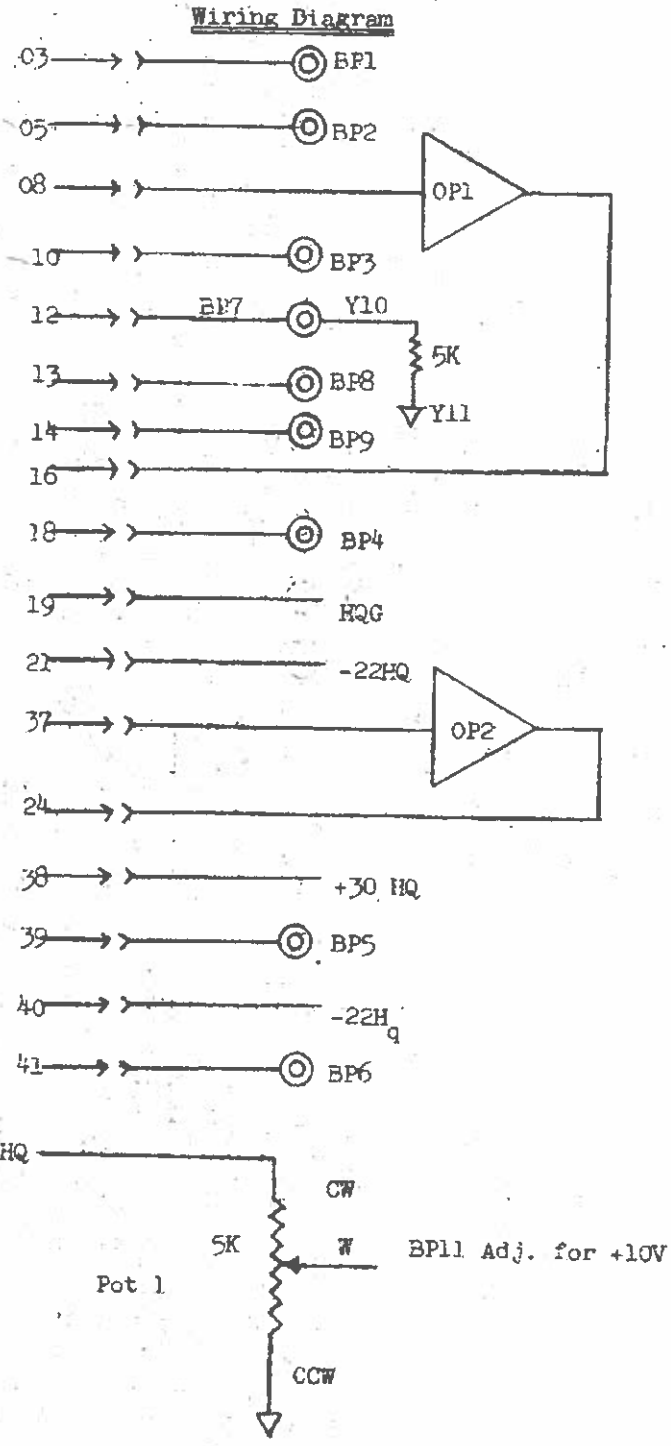
TITLE

CIRCUIT BOARD TEST FOR LOW VALUE GATE

FIRST MADE FOR 872D432-G1 & G2

PCB2

Wiring Diagram



REVISIONS

1 W. Schmidle JUN 4 1980 NO CHG. THIS SHT.

PRINTS TO

MADE BY D.DeNora Jan. 18,1971

ISSUED JAN 18 1971

APPROVALS

Steam Turbine DIV OR DEPT.

Schenectady, N.Y. LOCATION

P3K-AL-0108-A01

CONT ON SHEET 7 SH NO. 6

CODE IDENT NO. 11770

PE-803-NA (1-70) PRINTED IN U.S.A.

Data Sheet

Job # _____
Serial # _____
Date _____
Data Sheet for _____ 872D432G0003
Test Procedure _____ P3K-AL-0108-A01

Burn-in Start _____
Burn-in Stop _____
Technician _____

Test Procedure Step	Nominal	Lower Limit	Pre-Burn in Results	Post Burn in Results	Upper Limit	Pot Values If applicable CW	Pot Values If applicable CCW	Pass/Fail
6	8.75VDC	8.5VDC			9.0VDC	-	-	
8	2.5VDC	-			-			
10	1.0VDC	-			-			
12	1.0VDC	-			-	-	-	
14	2.0VDC	-			-			
16	1.0VDC	-			-			
18	1.0VDC	-			-			
20	-1.0VDC	-			-	-	-	

1/9/2012
CW