REV NO.	TITLE
277A3677 CONT ON SHEET 2 SH NO. 1	TEST SPECIFICATIONS FIRST MADE FOR IC3600AMLG1

REVISIONS

1.0 SCOPE

THIS DOCUMENT ESTABLISHES THE PERFORMANCE REQUIREMENTS AND RECOMMENDED TESTS FOR THE ANALOG MULTIPLIER/DIVIDER CARD AMLG.

2.0 TEST EQUIPMENT REQUIRED

1. ± 15 VOLT POWER SUPPLIES, ± .2 VOLTS 60MA MAX. CURRENT.
2. 2 DIGITEC 3110 PRECISION VOLTAGE SOURCES OR EQUIVALENT 0 TO +10 VOLT ADJUSTABILITY TO ± 1.0MV.
3. DANA 5900 DIGITAL VOLTMETER OR EQUIVALENT 5 PLACE ACCURACY.
4. SEVEN 1KΩ 1/2 WATT RESISTORS, 68A7030P100E.

3.0 TEST CONNECTIONS AND LOADING

1. POWER SUPPLIES

   CONNECT +15 VOLTS ± .2 VOLTS TO PIN 27, ACOM TO PIN 2.

   CONNECT -15 VOLTS ± .2 VOLTS TO PIN 29, ACOM TO PIN 2.

2. LOADS

   1. CONNECT 2KΩ (TWO 1KΩ RESISTORS IN SERIES, 68A7030P100E) BETWEEN AOUT (24) AND ACOM (2).
   2. CONNECT 2KΩ BETWEEN BOUT (3) AND ACOM (2).
   3. CONNECT 2KΩ BETWEEN COUT (10) AND ACOM (2).
   4. CONNECT A 1KΩ RESISTOR BETWEEN HOUT (46) AND ACOM (2, 50).

4.0 MULTIPLIER TESTS

THIS CARD CONTAINS THREE IDENTICAL MULTIPLIER CIRCUITS. REFER TO THE TABLE BELOW FOR PIN NUMBERS DURING THE REMAINING TESTS. PERFORM THE FOLLOWING TESTS ON CIRCUIT A, REPEAT THE TESTS FOR CIRCUITS B AND C PER THE TABLE.

INPUT	CIRCUIT A		CIRCUIT B	CIRCUIT C
X1	AX1 (23)	×2	BX1 (9)	CX1 (17)
X2	AX2 (22)	-1	BX2 (8)	CX2 (16)
Y1	AY1 (21)		BY1 (7)	CY1 (15)
Y2	AY2 (20)	2	BY2 (6)	CY2 (14)
Z1	AZ1 (25)		BZ1 (4)	CZ1 (11)
Z2	AZ2 (19)		BZ2 (5)	CZ2 (12)
OUT	AOUT (24)		BOUT (3)	COUT (10)

2520

PRINTS TO

MADE BY	APPROVALS		
R. E. GRUBBS	RES	DRIVE SYSTEMS (DIV OR DEPT.)	277A3677
ISSUED 2/13/77		SALEM, VA. U.S.A. (LOCATION)	CONT ON SHEET 2 SH NO. 1

CODE IDENT NO.

A- 25→24
B 4→3
C 11→10

MULTIPLICATION MODE

1. TIE Z1 TO OUT. 25, 4, 11 → 24, 3, 10

TIE Z2, X2, AND Y2 TO ACOM.

CONNECT ONE VARIABLE VOLTAGE SOURCE TO X1 AND THE OTHER TO Y1.

VARIFY THE FOLLOWING OUTPUTS PER THE INPUTS LISTED BELOW (ALL INPUTS SHOULD BE SET TO ± 1MV ACCURACY) FOR ALL THREE CIRCUITS.

A
19, 20, 22 ↑ TO COM
B
5, 6, 8 ↑ TO COM
C
12, 14, 16 ↑ TO COM

X1	Y1	OUT
0V	0V	± 15MV
0V	+10V	+ 35MV
+1V	+10V	± 40MV
+10V	+10V	+ 65MV
+10V	+1V	± 40MV
+10V	0V	+ 35MV
+10V	-10V	+ 60MV
-10V	-10V	± 50MV
-10V	+10V	+ 60MV

2. LEAVE Z1 CONNECTED TO OUT. REMOVE X1 AND Y1 FROM VARIABLE VOLTAGE AND TIE X1 AND Y1 TO ACOM. CONNECT THE VARIABLE VOLTAGE SOURCES TO X2 AND Y2. VARIFY THE OUTPUTS PER THE TABLE ABOVE FOR ALL 3 CIRCUITS. Z2 TO ACOM (INPUTS SET ± 1MV).

3. REMOVE ALL INPUT CONNECTIONS.

DIVISION MODE

20, 6, 14 → 22-8-16, 21-7-15, 25-4-11

1. TIE Y2 TO OUT. TIE X2, Y1, AND Z1 TO ACOM. CONNECT THE VARIABLE VOLTAGE SOURCES TO X1 (23) AND Z2 (19). VARIFY THE FOLLOWING OUTPUTS PER THE INPUTS LISTED BELOW (ALL INPUTS SHOULD BE SET TO ± 1MV ACCURACY) FOR ALL THREE CIRCUITS.

Z2	X1	OUT
0V	+10V	0V ± 35MV
+1V	+10V	+1V ± 40MV
+10V	+10V	+10V ± 50MV
+1V	+1V	+10V ± 150MV
-1V	+1V	-10V ± 150MV
-1V	+10V	-1V ± 50MV

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3LL VN

PRINTS TO

DIVISION MODE (CONTINUED)

2. TIE Z2 TO ACOM, LEAVE Y2 CONNECTED TO OUT. CONNECT X1 AND Z1 TO VARIABLE VOLTAGE SOURCES. VARIFY THE OUTPUTS PER THE TABLE ON SHEET 2 ON ALL THREE CIRCUITS, EXCEPT THAT THE POLARITY OF THE OUTPUTS IS REVERSED. (INPUTS SET ± 1MV).

5.0 ANALOG MEMORY TEST

TIE READB (40) TO ACOM.(2)

TIE READA (39) TO P15. (27)

CONNECT A +10.0 VOLT SIGNAL ± 2MV TO AMIN (33). VERIFY THAT HOUT (46) IS +10.0 VOLTS ± 25MV. LEAVE THE 10 VOLT SIGNAL CONNECTED FOR two MINUTE AND THEN OPEN THE P15 VOLT CONNECTION TO READA. RECORD THE VOLTAGE ON HOUT (46), IT SHOULD BE +10 VOLTS ± 25MV. WAIT 5 MINUTES AND RECORD THE VOLTAGE ON HOUT AGAIN. THE VOLTAGE SHOULD NOT HAVE DRIFTED MORE THAN ± 17.5MV.

END OF TEST