TEST SETUP FOR LOAD LIMIT P.C. BOARD

FIRST MADE FOR 872D490 G-2 & G-3 Rev PL MJB 4-19-84

REVISIONS

Oct 4,72 10 41 yrs Neg Returned

GENERAL DESCRIPTION

The function of this board is to limit the signal to the valve position loops if a load limit is called for. The board has an operational amplifier. The operational amplifier then feeds a transistor amplifier (used only for current amplification.)

An input bias feeds the amplifier to keep its output at approximately +5 volts when the other inputs are at their non-limiting values.

Load may be limited either by turning the load limit potentiometer on the control panel or via a relay contact closing. Turning the load limit potentiometer applies an output to the load limiting amplifier to decrease its output, thereby limiting the signal to the valve position loops. A biasing network allows the customer to set the voltage at TP8, which becomes an input to the amplifier when the contact closes. Assuming that the load limit potentiometer is turned all the way to ground potential (0 volts input), the customer may limit load by energizing the relay to close the contact mentioned above. This applies the pre-selected bias to decrease the amplifier output and limits the valve position signal. With the other load limiting input at 0 volts, diode ~~CR8~~ CR1 will be reverse biased and a voltage comparator will activate to energize a relay which locks in the customer-selected bias. Thus, the selected bias can be removed only by de-activating the voltage comparator. This is done by turning the load limit potentiometer until ~~CR8~~ CR1 becomes forward biased. At this time VC1 will turn off to de-energize the relay which causes the appropriate contact to open and lock out the customer bias input. The load limit potentiometer may then be turned back to zero to remove the limiting bias.

ET-273
273-2
273-12
273-13
273-13
273-7T
PRINTS TO

1. Connect board as per Figure 2. ~~Jumper BP3 To TP4.~~
2. Open SW3, SW4, ~~and~~ SW5, and SW6.
3. Plug in board and ground TP9, ~~SW3, SW5 dn,~~ ~~SW6d~~ Pot 8 CW, Jumper BP3 To TP4.
4. Adjust R31 for ~~+5.20V~~ +5.10VDC at ~~TP5~~. ~~R31~~ TP5 of R
5. ~~Close SW2 and~~ SW4 dn, The voltage at TP5 should drop to 0V ± .05.
6. Open ~~SW3 and~~ SW4.
7. The voltage at TP5 should return to ~~+5.20V.~~ +5.10VDC.
8. Remove ground from TP9. ~~Ground TP8.~~ ~~(S5d)~~ ~~OPEN SW3~~ Ground TP8 (SW5d). ~~SW5d~~ ~~SW5d~~
9. ~~Close SW5 and~~ turn Load Limit pot (#8) fully ~~CW.~~ CCW. The voltage at TP5 should be ~~+5.20V~~ +5.10V 0V
10. Turn Pot 8 fully ~~CW~~ CCW and adjust R30 for ~~0V~~ at TP5.
11. Turn Pot 8 fully ~~CCW~~ CW
12. Remove ground from (S5d) TP8 and adjust R26 for 3.0V at TP5.
13. Turn Pot 8 fully CCW. The voltage at TP5 should be 0 V.
14. Adjust Pot 8 for 2.5V at TP5; close ~~SW3~~ S3d and ~~SW4.~~ S4d
15. The voltage at TP5 should be 0 V. Adjust Pot 8 from it full CW to it full CCW limit. The voltage at TP5 should not change in value from the allowable deadband of ±.05V.
16. Turn Pot 8 fully CW. Open SW3 and SW4 and SW5; output at TP5 should be ~~5.20V.~~ +5.10 VDC.
17. ~~Adjust R31 for +5.00V at TP4.~~ Hook up memory type oscilloscope to read voltage at TP5. ~~S4d~~ S6d
18. ~~Close SW4.~~ The oscilloscope trace should be the same as shown Figure 1.
19. Open ~~SW4;~~ S6 S5d; adjust ~~R30~~ R26 for ~~4V~~ 0.0V at ~~TP5.~~ TP5 - OPEN SW5 ~~Close SW5~~
20. a. Close ~~SW5~~ S5d and observe that the oscilloscope trace is the same as Figure 1. SAME
    b. Adjust R26 for 3.0VDC at TP5. c. Open all switches. VTP5 should be +5.10VDC.
21. End of test.

PRINTS TO

GENERAL ELECTRIC

P24B-AL-4837

CONT ON SHEET 4 SH NO. 3

REV NO. 1

P24B-AL-4837

CONT ON SHEET 4 SH NO. 3

TITLE

TEST SETUP FOR LOAD LIMIT P.C. BOARD

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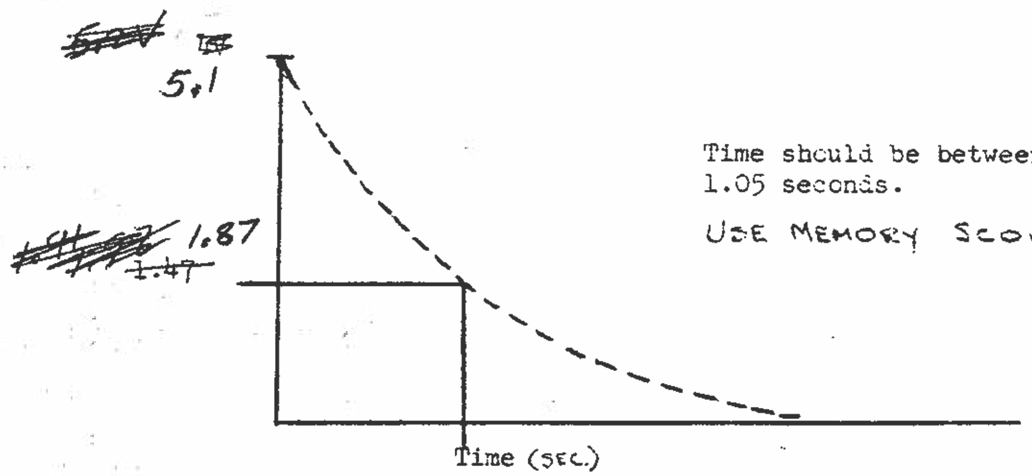
1 [illegible]

FIGURE 1



Time should be between .7 and 1.05 seconds.

USE MEMORY SCOPE

SAME

PRINTS TO

MADE BY R.J.Dickenson Apr. 5, 1968

APPROVALS

ISSUED Oct 4, 1972

LST DIV OR DEPT.

Schenectady LOCATION

P24B-AL-4837

CONT ON SHEET 4 SH NO. 3

GENERAL ELECTRIC

REV NO. | TITLE | CONT ON SHEET 5 | SH NO 4

CONT ON SHEET | SH NO. | FIRST MADE FOR

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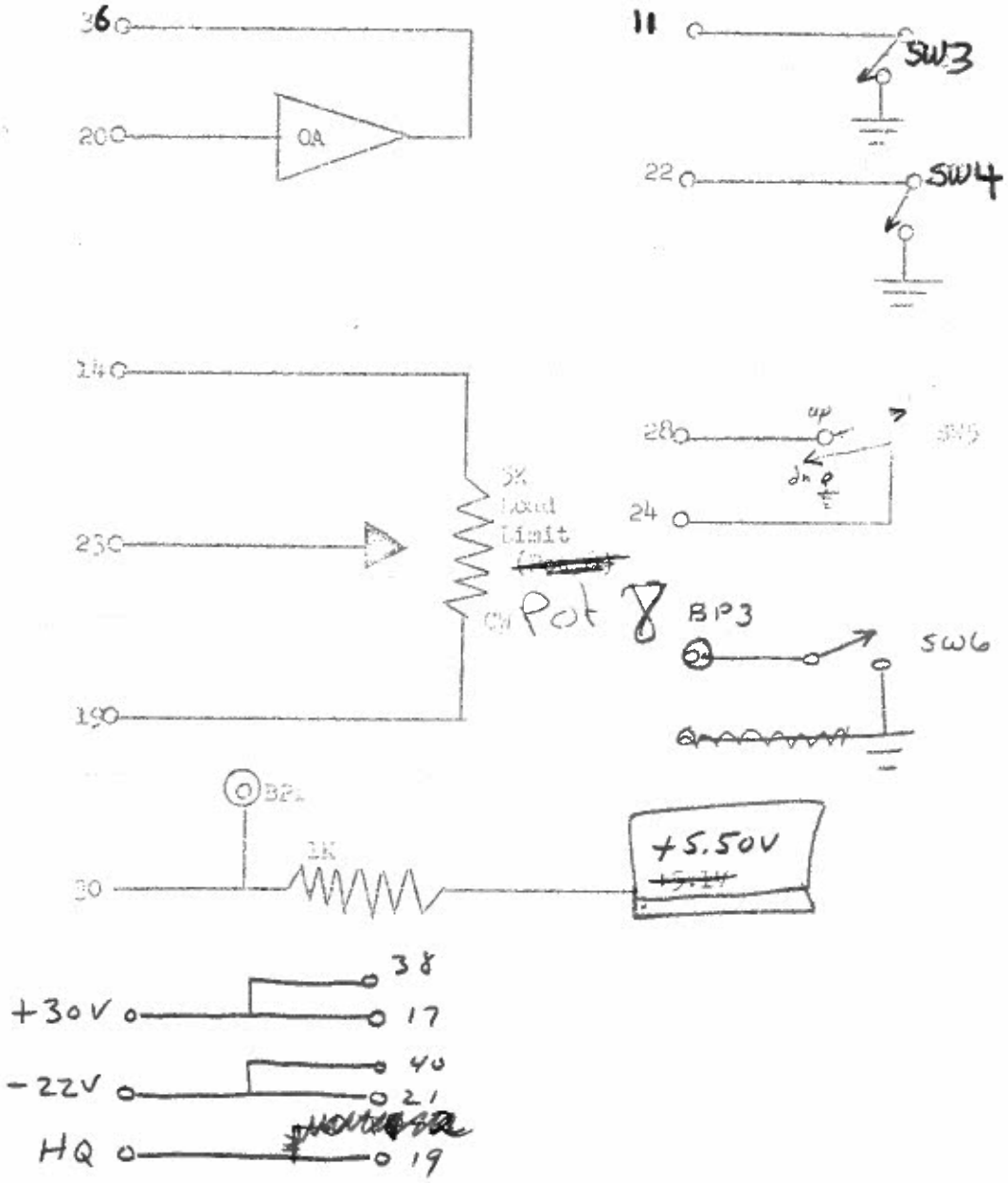
FIGURE 1



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TITLE

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TEST SETUP FOR LOAD LIMIT P.C. BOARD

FIRST MADE FOR

REVISIONS

Prepared By R D [illegible] Date 8-14-72

Reviewed By [illegible] Date

Control Engineering

Approved By [illegible] Date 8/16/72

CR Bugg/RJ Dell'Orfano

SAME

PRINTS TO

MADE BY R. Debertolis July 28, 1972

ISSUED Aug 4, 1972

APPROVALS

DW OR DEPT. LST

LOCATION Schenectady

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