QUALITY STANDING INSTRUCTION
GE FANUC AUTOMATION

QSI: 3.7.3.0066
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TITLE: **Series Six HSCA 1 Printed Wiring Assembly Test**
For: 44A717584-G01

REVISION RECORD

REVISION	DATE	AFFECTED PAGES	APPROVED	ORIGINATOR
0	04/27/84	Original	Richard H. Aust	M.A. Roy
1	2/27/03	1,2,3,4	Greg Faust	Rick Swisher

NATURE OF LAST CHANGE

PAGE #	SECTION NAME	BRIEF SUMMARY OF CHANGE
1	Purpose, Scope, Reference, General	Removed Reference to Temperature Cycle or T/C
2, 3, 4	Procedure	Removed Reference to Temperature Cycle or T/C

STAKEHOLDERS: **All Series Six HSCA Test Operators**

Note: Hardcopies are uncontrolled and are for reference only.
The electronic master is on the data storage location specified in QSI 1.4.0.2.

1.0 PURPOSE

This instruction specifies the testing the SERIES SIX HSCA Printed Wiring Assembly.

2.0 SCOPE

This instruction pertains to the Series Six High Speed Counter and related test hardware.

3.0 REFERENCES

3.1 44C723118	High Speed Counter Test Hardware
3.2 44A717584-G01	HSCA Printed Wiring Assembly
3.3 44C720514	HSCA 1 Elementary
3.4 HSC Factory Test Operation	

4.0 RESPONSIBILITY

Quality Control (Q.C.) shall keep this document up to date, initiate corrective action to insure process control and keep records adequate to allow process control. Test records shall be maintained to ensure product reliability and consistency.

5.0 GENERAL

In addition to a description of the test system, Table 1. Abbreviations defines various abbreviations used in this Standing Instruction.

TABLE 1. ABBREVIATIONS

ABBREVIATION	DEFINITION
CCMA	Communications Control Module
CPU	Central Processor Unit
HSC	High Speed Counter
I/O	Input / Output
JP	Jumper
LED	Light Emitting Diode
PDT	Program Development Terminal
PR	I/O Receiver
PWA	Printed Wiring Assembly
S.I.	Standing Instruction
T/C	Temperature Cycle
TP	Test Program
UUT	Unit Under Test

17-53 Locked up LED Info on

5.0 GENERAL (continued)

The High Speed Counter Test Program (TP019) consists of seventeen individual tests which run consecutively, simultaneously exercising four UUT. The operator controls the test via the HSCA RESET/STOP/START switch on the monitor upright. The monitor rack consists of support hardware (PWA); two of these PWA are predominately used by the test person. One PWA is in slot 2, it is an AC output PWA. If an AC power fault occurs, output point 8 (bottom neon) is latched ON and the output PWA in the monitor rack FLASH their lamps SYNCHRONOUSLY. The other PWA, the primary one used by the test person, is a High Density output module in slot 3. Each Group of 8 LED's (Group 1, 2, 3 and 4) is for one UUT.

When a LED is ON, there is a fault in the UUT. The Group LED number correlates directly to a UUT number; i.e. Group 1 is for UUT 1. The UUT rack houses the UUT; going left to right, as UUT 1, UUT 2, UUT 3 and UUT 4. The remainder of the PWA in the monitor rack, except the Thermocouple PWA which is optional, is used in testing the UUT. The heart of those PWA is the HSCT1 PWA in slot 6.

The CPU for the test is a Model 6000. The CPU has a CCMA PWA that dumps Failure Data (First Fail or Real Time Failure Data) to either a VT100 or a printer via the J2 port of the CCMA. The Failure Data is a user option and is not required in order to run the test. Setting the HSCA RESET/STOP/START switch to STOP causes the CCMA to dump First Fail Data. Setting the switch to START allows Failure Data to be dumped to a VT100 or a printer in Real Time. Refer to Appendix A for Failure Data format.

The I/O chain consists of just one UUT rack. The UUT rack holds a maximum of four UUT. On the AC hazard box is a switch labeled UUT DC. This switch controls the DC power (= 30 VDC) to the UUT edge connector. Associated with this connector is a HSC Plug that attaches to JP4 on the UUT.

6.0 PROCEDURE

6.1 Verify the CPU is loaded with the HSCA Test Program, TP019. If not, load the

HSCA Test Program into the CPU.

6.2 The I/O chain must be OK before starting test. (PR1 are not UUT).

6.3 SET the UUT DC switch to OFF. SET unit under test rack Logic Power switch to OFF.

6.4 SET HSCA jumpers and dip switch to Test Configuration per Table 1.

***** NOTE *****

THE SHIP CONFIGURATION IS NOT THE SAME AS THE Test CONFIGURATION. FIVE JUMPERS JP4 AND JP6-JP9 NEED CONFIGURING AFTER ACCEPTABLE TEST.

TABLE 1. HSCA JUMPER AND DIP SWITCH

CONFIGURATION FOR Test

JUMPER		DIP SWITCH	
JP1	1 + 2	U69A - SW 1	OPEN
JP2	1 + 2	SW 2	OPEN
JP3	1 + 2	SW 3	OPEN
JP4	HSC Plug (White wire to JP4 Pin 1)	SW 4	CLOSED
JP5	1 + 2		
JP6	No connection		
JP7	No connection		
JP8	No connection		
JP9	No connection		
JP10	1 + 2		
JP11	1 + 2		
JP12	1 + 2		
JP13	1 + 2		

6.5 Load HSCA PWA in UUT rack STARTING AT THE LEFT SIDE. Install the first PWA then the edge connector and the HSC Plug (WHITE WIRE GOES TO JP4 PIN 1), before preceding to the next UUT to the right. This is done because the room between the UUT may not allow the operator to connect the HSC Plug. There are a maximum of four UUT in the I/O UUT rack.

6.6 SET the UUT rack Logic Power switch to "ON". SET the UUT DC switch to ON.

6.7 SET the CPU RUN/STOP keyswitch to the RUN position.

6.0 Procedure (continued)

6.8 SET the RESET/STOP/START switch, on the monitor rack, labeled HSCA to the RESET position. To insure proper fault indication, check the operation of the lamps

in the I/O support rack. LED's that ore ON are as follow: slot 9 (High Density Output), 1 to 16 and 23 to 32. Slot 8 (High Density Input), 15 to 32. Slot 5 and 4 (Reed Relay Output) all ON. Slot 3 (High Density Output), 1 to 32. Slot 2 (AC Output) all neon's ON. Slot 1 (AC Input), only input 7 while switch is in RESET position. Check this operation before starting test and again after test. Additionally, LED's 1, 2 and 4 on the HSC PWA are turned ON and LED 3 on each HSC PWA BLINKS for about 20 seconds and then goes OFF. You do not have to wait for the LED 3 to stop blinking before setting the switch to the START position.

6.9 SET the HSCA RESET/STOP/START switch to the START position. The tests run in a sequential order. Test 1 runs after Test 17.

6.10 Log any failures indicated by the High Density PWA in slot 3. Definition of the failure LED indication is in Appendix A.

6.11 When a printer is utilized, connect the printer to CCMA port J2 and SET the RESET/STOP/START switch to STOP. The test halts when the current step has been executed and dumps first fail data. If no failure data occurred, no failure data occurred, no failure data is printed. THERE IS A FIVE SECOND DELAY BETWEEN EACH LINE PRINTED.

6.12 The test status is recorded at the time of the first failure being detected for each UUT. The test restarts from the current test/step position when the switch is returned directly to the START position from the STOP position.

6.13 When the HSC Test has been successfully completed, SET the HSCA RESET/STOP/START switch to RESET. Verify the UUT LED's 1, 2 and 4 are ON while LED 3 BLINKS. THE TEST PERSON HAS ABOUT 25 SECONDS FROM THE TIME THE SWITCH IS PUT IN RESET TO VERIFY UUT LED'S.

6.14 SET RESET/STOP/START switch to STOP.

6.15 SET the UUT DC switch to OFF and SET Logic Power to OFF.

6.16 REMOVE THE HSC PLUG FROM JP4 BEFORE REMOVING THE EDGE CONNECTOR; then remove the edge connector. Remove the HSCA PWA from UUT rack starting at the right and work to the left.

6.17 SET Jumpers and Dip Switch per Table 2. HSCA Ship Configuration.

Table 2. HSCA SHIP CONFIGURATION

JUMPER		DIP SWITCH	
JP1	1 + 2	U69A - SW1	OPEN
JP2	1 + 2	SW2	OPEN
JP3	1 + 2	SW3	OPEN
JP4	1 + 2	SW4	CLOSED
JP5	1 + 2		
JP6	1 + 2		
JP7	1 + 2		
JP8	1 + 2		
JP9	1 + 2		
JP10	1 + 2		
JP11	1 + 2		
JP12	1 + 2		
JP13	1 + 2		

APPENDIX A

Table 3. FAILURE INDICATIONS

	LED	**1 -**	**UUT 1**	**Heartbeat Failure**
		2 -		**Power-up Bit Set**
G		**3 -**		**External Power Supply Failure**
R		**4 -**		**Error Code Error**
P		**5 -**		**Counting Error**
1		**6 -**		**Setup Data Error**
		7 -		**Output, Limit Switch Status Error**
	LED	**8 -**	UUT 1	**unused**
	LED	**9 -**	UUT 2	**Heartbeat Failure**
		10 -		**Power-up Bit Set**
G		**11 -**		**External Power Supply Failure**
R		**12 -**		**Error Code Error**
P		**13 -**		**Counting Error**
2		**14 -**		**Setup Data Error**
		15 -		**Output, Limit Switch Status Error**
	LED	**16 -**	UUT 2	**unused**
	LED	**17 -**	UUT 3	**Heartbeat Failure**
		18 -		**Power-up Bit Set**
G		**19 -**		**External Power Supply Failure**
R		**20 -**		**Error Code Error**
P		**21 -**		**Counting Error**
3		**22 -**		**Setup Data Error**
		23 -		**Output, Limit Switch Status Error**
	LED	**24 -**	UUT 3	**unused**
	LED	**25 -**	UUT 4	**Heartbeat Failure**
		26 -		**Power-up Bit Set**
G		**27 -**		**External Power Supply Failure**
R		**28 -**		**Error Code Error**
P		**29 -**		**Counting Error**
4		**30 -**		**Setup Data Error**
		31 -		**Output, Limit Switch Status Error**
	LED	**32 -**	UUT 4	**unused**

APPENDIX A

Table 4. CCMA STATUS MESSAGE FORMAT

TIM = XXXXX TEM = +XX UUT = X TST = XXX STP = XX COD = XXXX LC = X I1 = XXXXXX XX 01 = XXXXXX XX
where: TIM - Test run time in minutes. TEM - Oven temperature in Deg C. UUT - Unit under test. TST - Individual test number. STP - Test step number. COD - Test code being executed. LC - Loop counter (gives board mode). I1 - Input from HSCA. Consists of 3 status bytes (XXXXXX) and the board condition byte (XX). O1 - Output to HSCA. Consists of 3 data bytes (XXXXXX) and the command byte (XX).

NOTE: For more information concerning input from and output to the HSCA, consult the "HSC USER's GUIDE".

EXAMPLE OF STATUS MESSAGE

TIM = 00000 TEM = +03 UUT = 4 TST = 001 STP = 15 COD = 0068 LC = 1 I1 = 000017 8B 01 = 101001 02

APPENDIX A

Table 5. HSCA TESTS

1	RESET BOARD, CHECK DEFAULT CONDITIONS, CLR PWR - UP BIT
2	ESTABLISH SERIES 6 CPU - HSCA CPU COMMUNICATIONS
3	SOFTWARE LIMIT SWITCH LOAD COMMANDS
4	LIMIT SWITCH STATUS CHANGES
5	COUNTING ACCURACY
6	BIDIRECTIONAL COUNTING - COUNTER MODE
7	COUNT ENABLE / DISABLE - COUNTER MODE
8	RESET COUNTER - COUNTER MODE
9	BIDIRECTIONAL COUNTING - ENCODER MODE
10	COUNT ENABLE / DISABLE - ENDODER MODE
11	OUTPUT STATUS CHANGES
12	OUTPUT LATCHES
13	HOME POSITION
14	COUNTER ROLLOVER
15	COUNTS / TIMEBASE
16	CYCLE LED's (30 SEC)
17	RETURN DATA COMMANDS