GE Power Generation Engineering

Materials and Processes Engineering
Schenectady, NY 12345

PROCESS SPECIFICATION

P3K-AL-0400-A01

TEST INSTRUCTIONS FOR POWER LOAD UNBALANCE CIRCUIT BOARD

DOCUMENT REVISION STATUS: DETERMINED BY THE LAST ENTRY IN THE "REV" AND "DATE" COLUMN

REV.	AN NO.	DESCRIPTION	SIGNATURE	REV. DATE
A	YA00096	SPECIFICATION LISTED IN STEAM TURBINE/GENERATOR INDEX AS "INACTIVE" HAS BEEN FORMALLY REVISED AS "INACTIVE FOR NEW DESIGN". (PR BUDKA)	C.R. Tripoli DEC 1991	

INACTIVE FOR NEW DESIGN

AS OF 12/02/91

PREPARED BY: P.R. BUDKA

ORIG. ISSUE DATE: --

TITLE
TEST INSTRUCTIONS FOR POWER LOAD UNBALANCE CIRCUIT BOARD 1PU1-B001, 115D2231 & 1PU1-B002, 169C4740 *

FIRST MADE FOR EHC MARK II

REVISION

① PAU MAR 30 1982 * Chg. made

BOARD REVISION #3,1PU1-B001
BOARD REVISION #0,1PU1-B002

I. CIRCUIT DESCRIPTION

This circuit board receives three AC current signals proportional to the generator phase currents. Each of these currents is rectified by a full wave rectifier with an adjustable load resistance so that a proper voltage signal is produced. The three voltage signals are summed and amplified by IC1, which is referred to as the total generator current amplifier, thus providing a voltage signal proportional to the total generator current (DC with 360 HZ AC ripple).

This signal is summed with the adjustable power pressure input signal, representing turbine mechanical power, by IC2 which is referred to as the proportional error amplifier. The output of IC2 is the proportional output of the board.

The output of the total generator current amplifier is also differential by IC3 which is connected as a differentiator and is referred to as the current rate amplifier. The output of IC3 is the rate output of the board.

The circuit board contains also an adjustable gain amplifier which is referred to as the watt signal amplifier, whose input is a voltage signal proportional to the generator power, and whose output is the watt signal output of the board.

II. CIRCUIT SPECIFICATIONS

A. Power Supply Requirement

1. Power Supply 1: +22.000 ± 0.002 VDC
   (Pin 37) at 50 ma (Approx.)

2. Power Supply 2: -22.000 ± 0.002 VDC
   (Pin 41) at 50 ma (Approx.)

B. Operating Signal Levels

1. Input 1 (Phase A Current Signal):

   (Pins 38 and 40) 0 to 3.88 ma RMS, 60 HZ
   (0 at 0 generator current, 3.88 ma at rated generator current)

2. Input 2 (Phase B Current Signal)

   (Pins 26 and 28) 0 to 3.88 ma RMS, 60 HZ, 120° phase angle with respect to input 1.
   (0 at 0 generator current, 3.88 ma at rated generator current)

273-5
273-314
~~273-2~~
273-125
273-71
273-138
~~273-221~~
~~273-227~~
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II. CIRCUIT SPECIFICATIONS (continued)

B. Operating Signal Levels (continued)

3. Input 3 (Phase C Current Signal)

(Pins 18 and 20) 0 to 3.88 ma RMS, 60 HZ, 120° phase angle with respect to input 2
(0 at 0 generator current, 3.88 ma at rated generator current)

4. Input 4 (Power Pressure Signal)

(Pin 23) 0 to +10.0 VDC
(0 at 0 pressure, +10.0 at rated pressure)

5. Input 5 (Watt Signal)

(Pin 13) 0 to +100 mv DC
(0 at 0 generator power, 100 mv at rated generator power)

C. Output Loads

1. Load 1: (Pin 30) 10K ohm ± 1%

2. Load 2: (Pin 12) 10K ohm ± 1%

3. Load 3: (Pin 22) 4.75M Ohm ± 1%

4. Load 4: (Pins 17 and 16) 1M Ohm ± 1% (Simulates Digital Meter)

D. Individual Stage Performance Specifications

1. Power Supply (CR1, 2, 3, and 4, R1 and R2)

a. TP1: +15.7 ± 1.0 VDC
b. TP2: -15.7 ± 1.0 VDC

2. Total Generator Current Amplifier (IC1):

a. Acceptable offset at TP5 (with zero inputs at TP7, 12 and 13): ± 1.0m VDC (Adjustable through VR50; adjustment point should be at least two turns away from either pot end).

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II. CIRCUIT SPECIFICATIONS (continued)

D. Individual Stage Performance Specifications (continued)

2. (continued)

b. Transfer Functions for Phase Current Signals (R9-17, R20, C1-3)

$$\frac{TP5}{TP13} = \frac{TP5}{TP12} = \frac{TP5}{TP7} = \frac{-G1}{1 + T_1 S}$$

Where: Gain (G1) = 0.333 ± 0.007 volts/volt
Noise Suppression lag time constant (T1) = 0.022 ± 0.002 msec.
Noise Suppression lag breakpoint (F1) = 7315 ± 804 HZ

c. Saturation Limits (TP5): ± 12 VDC (minimum)

3. Proportional Error Amplifier (IC2)

a. Acceptable offset at TP9 (with zero input at TP5 and TP10): ± 1.0m VDC

(Adjustable through VR51 - Adjustment point should be at least two turns away from either pot end).

b. Transfer Function for Total Generator Current Amplifier Output. (R22, R24)

$$\frac{TP9}{TP5} = -G_2$$

Where: Gain (G2) = 1.000 ± 0.020 volts/volt

c. High Gain Transfer Function for Power Pressure Signal (VR5 CW, R18, R19, R24 C4)

$$\frac{TP9}{TP10} = \frac{-G3}{1 + T_3 S}$$

Where: Gain (G3) = 1.050 ± 0.021 volts/volt
Noise Suppression lag time constant (T3) = 1.05 ± 0.06 msec
Noise Suppression lag breakpoint (F3) = 152 ± 10 HZ

d. Low Gain Transfer Function for Power Pressure Signal (VR5 CCW, R18, R19, R24, C4)

$$\frac{TP9}{TP10} = \frac{-G4}{1 + T_4 S}$$

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II. CIRCUIT SPECIFICATIONS (continued)

3. Proportional Error Amplifier (IC2) (continued)

d. (continued)

Where: Gain (G4) = 0.949 ± 0.027 volts/volt
Noise Suppression lag time constant (TP4) = 1.16 ± 0.08 msec
Noise Suppression lag breakpoint (F4) = 138 ± 9 HZ

e. Saturation limits (TP9): ± 12 VDC (minimum)

4. Current Rate Amplifier (IC3)

a. Acceptable offset at TP8 (with zero input at TP3): ± 1.0m VDC

(Adjustable through VR52 - Adjustment point should be at least two turns away from either pot end).

b. Transfer Function for Total Converter Current Amplifier Output:

$$\frac{TP8}{TP5} = \frac{-G5\ S}{1 + T5\ S}$$

Where: Gain (G5) = 0.020 ± 0.002 volt per volt/sec
Noise Suppression time constant (T5) = 19.95 ± 2.19 msec
Noise Suppression breakpoint (F5) = 8 ± 1 HZ

c. Transfer Function between TP3 and TP8:

$$\frac{TP8}{TP3} = -G6$$

Where: Gain (G6) = 1.000 ± 0.020 volts/volt

d. Saturation Limits (TP9): ± 12 VDC (minimum)

5. Watt Signal Amplifier (IC4):

a. Acceptable offset at TP6 (with zero input at TP4): ± 1.0m VDC

(Adjustable through VR53 - Adjustment point should be at least two turns away from eitherpot end).

b. High Transfer Function:
(VR2 CW, R28, R29, R30, C6):

$$\frac{TP6}{TP4} = \frac{-G7}{1 + T7\ S}$$

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II. CIRCUIT SPECIFICATIONS (continued)

5. Watt Signal Amplifier (IC4) (continued):

b. (continued)

* Where: Gain (G7) = { 24.9 ± .5, 1PU1-B001; 30.1 ± .65, 1PU1-B002 }

Noise Suppression lag breakpoint (F7) = { 156 ± 9 HZ, 1PU1-B001; 188 ± 13 HZ, 1PU1-B002 }

c. Low Transfer Function
(VR2 CCW, R28, R29, R30, C6):

$$\frac{TP6}{TP4} = \frac{-G8}{1 + T8\ S}$$

* Where: Gain (G8) = { 9.4 ± .72, 1PU1-B001; 10.0 ± .9, 1PU1-B002 }

d. Saturation limits (TP6): ± 12 VDC (minimum)

6. Phase A Current Input Rectifier

A 3.88 VRMS, 60 HZ AC current from an isolated current source forced through pins 38 and 40 should produce a full-wave-rectified voltage at TP13 with a peak value of: 7.770 ± 0.078 volts (when VR6 fully CCW) and: 31.162 ± 1.345 volts (when VR6 fully CW). VR6 should be set so that the DC component of TP5 voltage with TP12 and TP7 grounded is: -3.333 ± 0.001 volts. The voltage between pins 38 and 40 should be a sinewave with a peak not exceeding TP13 voltage peak by more than 2 volts.

7. Phase B Current Input Rectifier

A 3.88 VRMS, 60 HZ AC current from an isolated current source forced through pins 26 and 28 should produce a full-wave-rectified voltage at TP12 with a peak value of: 7.770 ± 0.078 volts (when VR4 fully CCW), and: 31.162 ± 1.345 volts (when VR4 fully CW). VR4 should be set so that the DC component of TP5 voltage with TP13 and TP7 grounded is: -3.333 ± 0.001 volts. The voltage between pins 26 and 28 should be a sinewave with a peak not exceeding TP12 voltage peak by more than 2 volts.

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II. CIRCUIT SPECIFICATIONS (continued)

8. Phase C Current Input Rectifier

A 3.88 VRMS, 60 HZ AC current from an isolated current source forced through pins 18 and 20 should produce a full-wave-rectified voltage at TP7 with a peak value of: 7.770 ± 0.078 volts (when VR3 fully CCW), and: 31.162 ± 1.345 volts (when VR3 fully CW). VR3 should be set so that the DC component of TP5 voltage with TP13 and TP12 grounded is: -3.333 ± 0.001 volts. The voltage between pins 18 and 20 should be a sinewave with a peak not exceeding TP7 voltage peak by more than 2 volts.

9. Total Current Amplifier with Input Rectifiers

With VR6, VR4 and VR3 set as specified in the sections 6, 7, and 8, a symmetrical three phase 60 HZ current system with a 3.88 ma RMS should produce at TP5 the following voltage: DC component: -10.000 ± 0.003 volts, Ripple: 360 HZ and higher (6th and higher harmonics) Total voltage: Between -9.065 volts and -10.475 volts

10. Continuity

a. With same current inputs as in section 9 and connections between pins 15, 25, 33, and 32 the voltage at TP5 should be: ± 0.001 volts.

b. The following points have permanent continuity:

1. TP10 and pin 23
2. TP11 and pins 1, 14, 16, 32, and 39
3. TP9 and pin 30
4. TP8 and pin 12
5. TP6 and pin 22

c. Resistance between pins 17 and 22:

2000 ± 200 ohms	(VR1 CCW)
1 ohm (maximum)	(VR1 CW)

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SSA 3/22/82

PREPARED BY D. Economou DATE 4/25/74

D. Economou
EHC DESIGN ENGINEERING

REVIEWED BY P C Callan DATE 9-12-77

P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE
REVIEWED BY R. W. Debertolis DATE 9-9-77

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EHC TEST ENGINEER

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