GENERAL & ELECTRIC 2 7 8 A 3 0 7 L CONT ON SHEET TITLE TEST INSTRUCTIONS CONT ON SHEET FIRST MADE FOR 1572K17G700 REVISIONS STANDING INSTRUCTIONS FOR PRINTED CIRCUIT BOARD 1572K17G700 ECCENTRICITY PEAK-TO-PEAK/ SPEED VALVE AND ECCENTRICITY AMPLIFIER FOR T.S.I. DL13 3EL1 1RA2 Distribution Copies: 4QA3 1 QC Engineering 4EK1_ 1 QC Test 1 Engineering PRINTS TO MADE BY W. Lunsford 790813 DRIVE SYSTEMS 2 7 8 A 3 O 7 WLL SALEM, VA 8/13/19 CONT ON SHEET LOCATION CODE IDENT NO. FF-803 WF (11-77)

FF-803-WF (2-83-M) PRINTED IN U.S.A.

-5-**8**3

|5|83

SALEM, VIRGINIA

+

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CODE IDENT NO.

SH NO. -

LOCATION CONT ON SHEET 3

278A3071

CONT	ON	SHEET	4
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3 SH NO.

REVISIONS

BuggiRP CB

3.

TITLE

TEST INSTRUCTION

278A3071

CONT ON SHEET 4 / SH NO.

FIRST MADE FOR 1572K17G700G701

ELECTRICAL TEST

APPLY + 15VDC.

CLOSE SW2 AND PLACE SW1 DOWN. VERIFY THAT VOLTAGE AT TERM L WITH RESPECT TO TERM N IS - 4.7 + 001 VDC. OPEN SW2OFF

(NOTE: INTEGRATOR CAUSES VERY SLOW VOLTAGE SHIFTS AT PIN E C. SO ALLOW TIME TO STABALIZE) TO A Y TAKE 10 MIY, TO PROP

ADJUST R1802

PIN E OUTPUT

CCW CW 1.25 + .2VDC $3.80 \pm .2$ VDC

SET

2.0 + .010 VDC

(NOTE INITIAL SET POINT CAN BE MADE BY SETTING THE VOLTAGE AT ANODE OF CR1801 to 3.5VDC WITH RESPECT TO COMMON.THEN READJUST R1802 SOWLY TO MEET .005VDC TOLERANCE)

VERIFY CHART

E+, N-

R+, P-

M+, P-

T+, V-

 $2.0 \pm .010$ VDC $8.0 \pm .4$ MVDC $.2 \pm .02$ MADC $1.0 \pm .01$ MADC

CLOSE SW 2 PUT SW 1 UP. VERIFY THAT VOLTAGE AT TERM 2 WITH RESPECT TO TERM. N IS +3.8 + .01VDC. ALTERNATLY FLIP SW 1 UP AND DOWN APPROX. EVERY 5 SEC. THE VOLUMN AT E SHOULD LEVEL OFF AT 10.2 + .2VDC.

VERIFY CHART

E +, N-R +, P -M+, P− 10.0 + .1VDC 40 + .4MVDC 1, 0 + .02MADC 5.0 + .06MADC

DL13

3EL1 1RA2

4QA3

4EK1

PRINTS TO

E.A. POST 12.5.83

+

12/5/83

DRIVES SYSTEM

SALEM, VIRGINIA

278A3071

LOCATION CONT ON SHEET

3 SH NO.

CODE IDENT NO

FF-803-WF (2-83-M) PRINTED IN U.S.A.

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CONT ON SHEET

FL, SH NO. 4

REVISIONS

12/5/83

NV.

TITLE
TEST INSTRUCTION

278A3071

CONT ON SHEET FL. SH NO.

FIRST MADE FOR

1572K17G700G701

MAY TAKE 10-15 MIN

E. OPEN SW2 AND ALLOW TERM E TO GO TO 2.0VDC

CONNECT TERM S TO TERM N.

CLOSE SW2 AND TOGGLE SW1 UP AND DOWN APPROXIMATELY EVERY 5 SEC.

VOLTAGE AT TERM E TO TERM N SHOULD NOT INCREASE MORE THAN .5VDC

ABOVE 2.0 VDC.

REMOVE JUMPER TO TERMS.

- F. PUT SW. 1 UP (CONNECT 3.8 VDC TO TERM L)
 SET R1822 FOR 2.0 ± .005 VDC AT ORANGE
 TEST JACK WITH BLACK JACK COMMON.
- G. PUT SWI DOWN.

 SET R1825 FOR 10.0 + .005VDC AT ORANGE JACK.

 (COM. TO BLACK JACK)

 REPEAT STEPS F AND G UNTIL LIMITS ARE MET FOR BOTH POSITIONS OF SW 1.
- H. PUT SW. 1 UP. ORANGE JACK SHOULD BE AT 2.0 VDC AND SHOULD NOT CHANGE FOR ANY OF THE FOLLOWING CONNECTIONS.
 - 1. TERM S TIED TO COM. (PIN N)
 - 2. TERM K TIED TO COM.
 - 3. TERM S AND K TIED TO COM.
- J. REMOVE JUMPER FROM S AND K AND CHECK FOLLOWING POINTS FOR CONTINUITY.

TERM C TO H

SHORTED

TERM A TO H

OPEN

TERM F TO H

OPEN

K. CONNECT TERM K TO COMMON

TERM C TO H

OPEN

TERM A TO H

SHORTED

TERM F TO H

STORES OPEN

L. CONNECTED TERM S AND TERM K TO COMMON

TERM C TO H

OPEN

TERM A TO H

SHORTED

TERM F TO H

SHORTED

PUT RTV ON ALL POTS.

REMOVE ALL POWER

PRINTS TO

DL13

3EL1

1RA2

4QA3

4 EK 1

E.A.POST APPROVALS DIV OR DIV OR

185UED 12-5-83

REU 12/5/8

DRIVES SYSTEMS
SALEM, VIRGINIA

-- DIV OR

LOCATION

278A3071

CONT ON SHEET FI. SH NO.

MADE BY

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