REV NO.	TITLE
304A8436	Test Instructions
CONT ON SHEET 2 SH NO. 1	FIRST MADE FOR 304A8434

REVISIONS

1 REVISED 8-1-83 CBG

I. TEST INSTRUCTIONS 304A8436

REF ELEM 158C2448

II. SCOPE

THE FOLLOWING DESCRIBES THE SETUP AND TEST PROCEDURE FOR THE PWB 304A8434.

III. SPECIAL TEST EQUIPMENT

NONE

IV. POWER SUPPLY REQUIREMENTS

P15	PINS 1-2
N15	PINS 5-6
ACOM	PINS 3-4

ALL POWER SUPPLIES SHOULD BE WITHIN +/- 10%.

V. INITIAL SETUP

1. PRESET POTS AS FOLLOWS:

R1 (CNTR)	FULLY CCW
R2 (RADIUS)	FULLY CW
R4 (VCAL)	FULLY CCW
R5 (ICAL)	FULLY CW
R6 (COFF)	FULLY CW

2. SET BERG JUMPERS AS FOLLOWS:

BJ1	"I"
BJ2	"HI"

VI. DAUGHTER BOARD

NONE

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1 REVISED CA 8-1-83

VII. ELECTRICAL TEST

NOTE: UNLESS OTHERWISE SPECIFIED, ALL INPUTS AND MEASUREMENTS ARE WITH RESPECT TO ACOM (3-4).

A. CIN CHANNEL TEST

1. JUMPER PHASE1 (13-14), PHASE2 (11-12), AND PHASE3 (15-16) TO ACOM THEN APPLY -10.00 +/- .01 VDC AT CIN (29-30).
2. VERIFY +6.30 +/- .54 VDC AT TP4 AND -2.48 +/- .26 VDC AT TP21.
3. ADJUST R5 FOR -2.00 +/- .01 VDC AT TP21.
4. VERIFY -3.92 +/- .20 VDC AT TP5.
5. REMOVE TEST VOLTAGE FROM CIN AND JUMPERS FROM ALL PHASE INPUTS.

B. PHASE INPUT CHANNEL TEST

1. JUMPER CIN (29-30) TO ACOM AND APPLY +10.00 +/- .01 VDC AT PHASE1 (13-14), PHASE2 (11-12), AND PHASE3 (15-16) INPUTS.
2. VERIFY -5.1 +/- .2 VDC AT TP18 AND +1.0 +/- .2 VDC AT TP6.
3. ADJUST R4 FOR +2.00 +/- .01 VDC AT TP6.
4. VERIFY +3.92 +/- .34 VDC AT TP11.
5. APPLY +15.10 +/- .01 VDC AT CIN (29-30) THEN VERIFY +2.0 +/- .3 VDC AT TP10.
6. ADJUST R3 FOR +1.00 +/- .05 VDC AT TP9.
7. CHANGE BJ2 FROM "HI" TO "LO" AND VERIFY +.5 +/- .1 VDC AT TP10.
8. REMOVE TEST VOLTAGES FROM ALL INPUTS APPLIED IN THIS SECTION.

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C. CIN CHANNEL RECTIFIER TEST

1. APPLY A 10.00 20V P-to-P +/- .01 VOLT PEAK 10 HZ SINE WAVE AT CIN(29-30) THEN VERIFY A NEGATIVE 3.8 +/- .6 VOLT PEAK FULL WAVE RECTIFIED SINE WAVE TP5. (SIGNAL WILL DIFFER SOMEWHAT FROM THE IDEAL FULL WAVE SIGNAL DUE TO FILTERING ON THE CIRCUIT.)

2. CHANGE THE FREQUENCY OF THE INPUT TO 100 HZ AND VERIFY THE OUTPUT AT TP5 IS NOW NEGATIVE 2.7 +/- .2 VDC WITH ABOUT .5 VOLTS 200HZ RIPPLE.

3. REMOVE INPUT FROM CIN (29-30).

D. PHASE VOLTAGE CHANNEL RECTIFIER TEST

1. JUMPER PHASE2 (11-12) AND PHASE3 (15-16) TO ACOM AND APPLY A 10.00 +/- .01 VOLT PEAK 10 HZ SINE WAVE AT PHASE1 (13-14) THEN VERIFY A FULL WAVE RECTIFIED POSITIVE 3.9 +/- .6 VOLTS PEAK SINE WAVE AT TP11.

2. CHANGE THE INPUT FREQUENCY TO 100 HZ AND VERIFY THE OUTPUT AT TP11 IS NOW POSITIVE 2.7 +/- .2 VDC WITH ABOUT .5 VOLTS 200 HZ RIPPLE.

3. REMOVE TEST VOLTAGE FROM PHASE1 INPUT AND REMOVE JUMPER BETWEEN PHASE2 AND PHASE3.

E. FINAL STAGE TESTS

NOTE: THIS TESTING INVOLVES A CIRCUIT CONTAINING A PURE INTEGRATOR WHICH IS FORMED BY C3 ON U7. WITH C3 ACTIVE THE OUTPUT OF U7 WILL TEND TO INTEGRATE ANY INPUT FROM U3 OR TP9 AND AS A RESULT WILL RAMP TO N15 OR SOME POSITIVE VALUE. THE INTEGRATOR WILL BE TESTED AND THEN TO MAKE IT EASIER TO DO THE REMAINING TESTS A SHORT WILL BE PLACED ON C3 TO TURN U7 INTO AN INVERTING AMPLIFIER WITH A GAIN OF ABOUT 4.5.

1. JUMPER PHASE1 (13-14), PHASE2 (11-12), PHASE3 (15-16), AND CIN (29-30) TO P15. ALSO JUMPER ACROSS R50 (BJ2 IN "LO"). THIS SHOULD BRING TP10 TO 0 VOLTS SO THAT IT WILL NOT AFFECT FURTHER TESTS.

2. SHORT C3 AND VERIFY THAT TP2 IS 0 +/- .2 VDC. (TP2 WILL TEND TO RAMP WITHOUT THE SHORT.) LEAVE C3 SHORTED.

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3. APPLY +5.20 +/-.05 VDC AT TP9 AND ADJUST R3 FOR +1.00 +/- .01 VDC AT JUNCTION OF R53 AND R54. (THIS POINT SHOULD ALREADY BE NEAR ONE VOLT. IF IT ISN'T, CHECK R3 AND R53 FOR CORRECT VALUES.) THEN VERIFY -4.52 +/- .15 VDC AT TP2.

4. WITH 5 VOLTS STILL ON TP9, REMOVE THE SHORT ACROSS C3 AND VERIFY TP2 BEGINS TO RAMP TOWARD THE NEGATIVE BUSS AT A RATE OF 5 VOLTS EVERY 10 +/- 2 SECONDS.

5. REMOVE THE INPUT FROM TP9, SHORT C3, AND CHECK THAT TP2 IS ONCE AGAIN NEAR 0 VOLTS.

6. APPLY -5.20 +/- .05 VDC AT TP9 AND VERIFY THE OUTPUT AT TP2 GOES TO +4.52 +/- .15 VDC WITH NO DELAY.

7. REMOVE THE SHORT ACROSS C3 AND VERIFY TP2 GOES UP IN VOLTAGE BY ABOUT ONE DIODE DROP (.3-.6 VDC). THE OUTPUT SHOULD NOT RAMP ONCE IT HAS SETTLED.

8. VERIFY THAT TP3 IS AT THE SAME VOLTAGE AS TP2 +/- .2 VDC BUT WITH THE OPPOSITE POLARITY.

9. REPLACE THE SHORT ACROSS C3 AND LEAVE IT ON FOR THE REMAINDER OF THE TESTS IN THIS SECTION. U5 WITH OUTPUT AT TP16 IS WORKING AS A COMPARATOR. WHILE MONITORING TP16 WITH A METER, VARY THE VOLTAGE OF THE INPUT TO TP9. OBSERVE THAT TP16 SWITCHES FROM THE POSITIVE BUSS TO THE NEGATIVE BUSS (WITHIN 3.0V) WHEN THE VOLTAGE ON TP2 PASSES THROUGH +.15 +/- .05 VDC. ABOVE .15V TP16 SHOULD BE POSITIVE AND BELOW .15V TP16 SHOULD BE NEGATIVE.

10. VERIFY THAT WHEN TP16 IS NEGATIVE, THE VOLTAGE ON TP12 SHOULD BE WITHIN ONE VOLT OF TP16 AND WHEN TP16 IS MADE TO GO POSITIVE, TP12 HAS AN EXPONENTIAL RISE PASSING THROUGH ZERO VOLTS AFTER 10 +/- 2 SECONDS. WHEN TP16 AGAIN GOES NEGATIVE, TP12 SHOULD FOLLOW WITH NO DELAY.

11. OBSERVE TP12 AND TP17. ALLOW TP12 TO RAMP UP AS IN STEP 10 ABOVE AND VERIFY TP17 GOES FROM THE POSITIVE BUSS TO THE NEGATIVE BUSS (WITHIN 3.0V) WHEN THE VOLTAGE ON TP12 PASSES THROUGH ZERO.

12. WITH TP17 REMAINING NEGATIVE, VERIFY THAT TP8 IS WITHIN 2.5 VOLTS OF TP17.

13. WITH TP17 ONCE AGAIN POSITIVE, TP8 SHOULD BE WITHIN ONE VOLT OF TP3.

14. REMOVE ALL INPUTS AND JUMPERS APPLIED IN THIS SECTION.

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1 REVISED CG 8-1-93

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1 REVISED 8/1/83 CRG

F. FINAL CALIBRATION

1. SET POTS AND BERG JUMPERS AS FOLLOWS:
   - R1 FULLY CCW
   - R3 FULLY CW
   - R6 FULLY CCW
   - BJ1 "D"
   - BJ2 "HI"

2. APPLY 8.5 +/- .1 VRMS (60 HZ) AT CIN (29-30) AND ADJUST R5 FOR -2.50 +/- .01 VDC AT TP5. THEN REMOVE INPUT ON CIN.

3. APPLY 3 PHASE 17.0 +/- .1 VRMS LINE TO NEUTRAL (60 HZ) TO INPUTS AS FOLLOWS:
   - PHASE 1 PINS 13-14
   - PHASE 2 PINS 11-12
   - PHASE 3 PINS 15-16
   - NEUTRAL PINS 3-4

4. ADJUST R4 FOR 5.66 +/- .05 VRMS AT TP6.

5. ADJUST R1 FOR -3.25 +/- .01 VDC AT TP5.

6. ADJUST R2 FOR +4.00 +/- .01 VDC AT TP11.

7. REMOVE 3 PHASE INPUTS APPLIED IN THIS SECTION.

G. FINAL STAGE COMPONENT VERIFICATION

1. VERIFY THE FOLLOWING COMPONENTS ARE THE CORRECT VALUE.
   - C4 10MFD
   - C6 1.0MFD
   - C7 .15MFD
   - R60 82.5K
   - R61 562K
   - R63 562K

END OF TEST

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