9.1.0 SCOPE

THIS DOCUMENT ESTABLISHES THE PERFORMANCE REQUIREMENT AND RECOMMENDED TESTS FOR THE DC EXCAVATOR REFERENCE PWB IDENTIFIED AS:

DS3800HERA.

9.2.0 TEST EQUIPMENT AND DOCUMENTATION

9.2.1 STANDARD EQUIPMENT REQUIRED:

TEST EQUIPMENT SHALL BE PROVIDED WHICH MEETS THE REQUIREMENTS AND ACCURACIES PRESCRIBED IN THIS SPECIFICATION. ALL TEST EQUIPMENT IS DEFINED BY QUALITY CONTROL STANDARD _____ EXCEPT AS NOTED IN SECTION 9.2.2.

9.2.2 SPECIAL EQUIPMENT REQUIRED:

9.2.2.1 1 MHZ ± 10 KHZ SQUARE WAVE SIGNAL SOURCE
SIGNAL LEVEL: 4.5V AT 2MA
RISE AND FALL TIME $< 1\mu S$.

9.2.2.2 VARIABLE FREQUENCY SINE WAVE GENERATOR ADJUSTABLE FROM 30 HZ TO 75 HZ
SIGNAL LEVEL: 4.0V RMS AT 2MA

9.3.0 POWER SUPPLY REQUIREMENTS AND PIN CONNECTIONS

THE FOLLOWING REGULATED INPUT VOLTAGE SOURCES ARE REQUIRED TO TEST THIS PRODUCT ELEMENT.

REV. 1	REV. 4	REV. 7	PRINTS TO DL100 PRI	ENGINEER DCM	GENERAL ELECTRIC DRIVE SYSTEMS DEPT SALEM, VA. U.S.A.	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV 23, 1977				DS3800HERA CONT. ON SH. 9BA SH. NO. 9AA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/11/77				

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NOMINAL VOLTAGE[1]	MAXIMUM CURRENT[2] (AMPS)	MIN. ADJ. RANGE	% REG.	MAXIMUM VOLTAGE[3] (VDC)	PIN (S)[4]
P28	NOT USED				
P15	0.1	10%	± 5%	+18.0	PA5, PB5
N15	0.1	10%	± 5%	-18.0	PA7, PB7
P5	1.0	10%	± 5%	+7.0	PA3, PA45, PA77, PB3, PB45, PB77
ACOM	0.2	-	-	-	PA9, PB9
DCOM	1.0	-	-	-	PA1, PA43, PA79, PB1, PB43, PB79
P28	NOT USED				
P15	NOT USED				
N15	NOT USED				

NOTES:

1. NOMINAL VOLTAGE USED UNLESS OTHERWISE SPECIFIED.
2. ELEMENTS REQUIRING MORE THAN THE MAXIMUM VALUE MAY SUFFER DAMAGE.
3. VOLTAGES ABOVE MAXIMUM VOLTAGE MAY IMPAIR ELEMENT LIFE.
4. CONNECT ALL DCOM PINS TOGETHER FIRST, THEN WIRE TO ACOM. ANALOG SIGNAL POWER SUPPLIES, OSCILLOSCOPES, AND VOLTMETERS SHOULD CONNECT TO ACOM FOR THE MOST ACCURATE READINGS.

THE MAXIMUM POWER DISSIPATION OF THIS PRODUCT ELEMENT DURING TEST IS:

8.0 WATTS

REV. 1	REV. 4	REV. 7	PRINTS TO DL108 PRI	ENGINEER DEM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV 23, 1977			DRIVE SYSTEMS DEPT SALEM, VA. U.S.A.	DS3800HERA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/12/77				DIVISION SH. 9CA SH. NO. 99A

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9.4.0 SETUP AND INITIAL LOADING

9.4.1 CONNECTIONS

9.4.1.1 WIRES:

FROM	TO	SHEET
ACOMX (PA15)	ACOM (PA9)	4CA

9.4.1.2 COMPONENTS:

NONE

9.4.1.3 SWITCHES, FROM A (NORMALLY OPEN CONTACTS) ONLY:

NONE

9.4.1.4 OP AMP SUMMING JUNCTIONS - TERMINATE AT JUNCTION BOX (SHORT WIRE)

NONE

9.4.1.5 SPECIAL

NONE

9.4.2 ELEMENT LOADS

NONE

9.4.3 DAUGHTER BOARD

9.4.3.1 COMPONENT MATERIAL LIST REQUIRED FOR MODIFICATION:

NONE REQUIRED

9.4.3.2 CIRCUIT DIAGRAM AS MODIFIED:

NO MODIFICATIONS REQUIRED.

REV. 1	REV. 4	REV. 7	PRINTS TO DL108 PRI	ENGINEER DEM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED Nov 23, 1977			DRIVE SYSTEMS DEPT	DS3800HERA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/11/77			SALEM, VA. U.S.A.	PRINT SH. 9DA SH. NO. 9CA

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9.4.3 DAUGHTER BOARD (CONTINUED)

9.4.3.3 SET POTS AS FOLLOWS:

R1, -.1 ± .04V
R2, -.27 ± .04V
R3, -.58 ± .04V
R4, -1.21 ± .04V
R5, -2.46 ± .04V
R6, -4.96 ± .04V
R7, -7.46 ± .04V
R8, -10.06 ± .04V

9.5.0 SIGNAL LEVELS

9.5.1 TTL INPUT SIGNALS

UNLESS OTHERWISE SPECIFIED, THE FOLLOWING INPUT DATA LEVELS SHALL BE APPLIED TO THE ELEMENT AT TTL INPUTS:

LOGIC "0" LEVEL = 0.4 ± 0.4VDC
LOGIC "1" LEVEL = 2.2 ± 0.2VDC

THE SIGNAL SOURCE FOR THESE LOGIC LEVELS SHALL BE CAPABLE OF SINKING 10 MA IN THE LOGIC "0" STATE AND SOURCING 0.8MA IN THE LOGIC "1" STATE.

THE RISE AND FALL TIME OF THE SIGNALS SHALL BE LESS THAN 100 AND MORE THAN 3 NANOSECONDS. THE TTL INPUT SIGNALS SHALL BE APPLIED AT A RATE WITHIN A RANGE OF DC TO 1 KHZ, EXCEPT AS NOTED FOR TIME DELAYS.

9.5.2 PROCESS OUTPUT LEVELS

THE FOLLOWING PROCESS OUTPUT LEVELS ARE USED IN TEST TABLES ON SHEETS 9GA-9MA.

LEVEL	VOLTAGE	LEVEL	VOLTAGE
A	+10.2 ± .2V	J	- .10 ± .05V
B	+5.04 ± .05V	K	- .27 ± .05V
C	+2.54 ± .05V	L	- .58 ± .05V
D	+1.29 ± .05V	M	- 1.21 ± .05V
E	+.66 ± .05V	N	- 2.46 ± .05V
F	+.35 ± .05V	P	- 4.96 ± .05V
G	+.20 ± .05V	Q	- 7.46 ± .05V
H	+.00 ± .05V	R	-10.06 ± .05V

9.5.3 TTL OUTPUT LEVELS

UNLESS OTHERWISE SPECIFIED, THE FOLLOWING OUTPUT DATA LEVELS SHALL BE VERIFIED:

LOGIC "0" LEVEL = 0.0 TO 2.0VDC

LOGIC "1" LEVEL = 2.0 TO 5.0VDC

AN "X" = DON'T CARE OR NOT BEING TESTED

NOTES:

1. CHARACTERS WITHIN QUOTATION (") MARKS ARE USED IN THE TEST VECTOR TABLE OF SECTION 9.6.3.

9.6.0 TEST PROCEDURE

9.6.1 PRELIMINARY INSPECTION

THE ELEMENT SHALL BE INSPECTED PRIOR TO APPLICATION OF POWER TO VERIFY THAT IT IS ASSEMBLED ACCORDING TO THE ASSEMBLY DRAWING.

9.6.2 DIGITAL TESTS

DIGITAL TESTS ARE COVERED BY _____.

9.6.3 HYBRID TESTS

9.6.3.1 A/D AND ASSOCIATED CIRCUITRY TEST

THE CHART BELOW DEFINES INPUT SIGNAL LEVELS TO BE APPLIED PER TABLES ON SHEETS 9GA-9MA

LEVEL	VOLTS	INPUT NAME (PIN)
A	+10.2 ± .1V	IDC (PA14)
B	+5.04 ± .04V	VDC (PA13)
C	+2.54 ± .04V	IAC (PA12)
D	+1.29 ± .04V	VAC (PA11)
E	+ .66 ± .04V	REFO (PA10)
F	+ .35 ± .04V	SP1 (PA8)
G	+ .20 ± .04V	SP2 (PA6)
H	.00 ± .04V	IAC2 (PA)
Z	NO CONNECTION	AS SPECIFIED IN TEST TABLES

INPUTS SPECIFIED IN THE ABOVE CHART SHOULD BE . . . . . .

APPLIED ONLY DURING BIT TIMES THEY ARE REQUIRED. DURING ALL OTHER BIT TIMES THE INPUTS SHOULD BE CONNECTED TO +10VDC.

APPLY INPUTS AND VERIFY OUTPUTS PER TABLES ON SHEETS 9GA-9MA.

REV. 1	REV. 4	REV. 7	PRINTS TO DL100 PRI	ENGINEER DEM	GENERAL ELECTRIC DRIVE SYSTEMS DEPT SALEM, VA. U.S.A.	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV 23, 1977				DS3800HERA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/11/77				CONT. ON SH. 9GA SH. NO. 9FA

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9.6.3.1.1 INPUTS/OUTPUTS

NOTE NO.	MNEMONIC	SH. NO.	PIN NO.	TEST TERM.	BIT TIME			SUB ROUTINE A-1			SUB ROUTINE A-2			SUB ROUTINE A-3		
						1	2	A	B	C	A	B	C	A	B	C
	OBDPR0	4AA	PA61		1	0	0	1	0	0	0	X	0	1	X	0
	OBDPR1	4AA	PA62		1	0	0	1	0	1	1	X	1	0	X	0
	OBDPR2	4AA	PA63		1	1	1	1	0	X	1	X	X	1	X	X
	OBDPR3	4AA	PA64		1	0	0	1	0	X	1	1	X	1	1	X
	OBDPR4	4AA	PA65		1	0	0	X	0	X	X	1	X	X	1	X
	OBDPR5	4AA	PA66		1	1	1	X	0	X	X	1	X	X	1	X
	OBDPR6	4AA	PA67		1	1	1	X	0	0	X	1	X	X	1	X
	OBDPR7	4AA	PA68		1	0	0	X	0	0	X	1	X	X	0	X
	OBBIN	4AA	PA17		1	1	1									
	OBCMRS	4AA	PA2		1	1	1									
	OBCMWS	4AA	PA4		1	1	0									
	OBAPR0	4BA	PA18		1	1	1									
	OBAPR1	4BA	PA19		1	1	1									
	OBAPR3	4BA	PA48		1	0	0									
	OBAPR8	4BA	PA53		1	0	0									
	OBAPR9	4BA	PA54		1	0	0									
	OSELECT	4BA	PA25		1	0	0									
	OMUXWR	4BA	TA6		ø	X	X									
	OADCONV	4BA	TA23		ø	X	X									
	HLD	4HA	TA22		ø	X	X									
	AVAL	4HA	TA24		ø	X	X	A			B			C		
	OCONVTP	4JA	TA17		1	X	X									
2	IDC1	4HA	PA14		1	X	X	A								
2	VFB	4HA	PA13		1	X	X				B					
2	IAC	4HA	PA12		1	X	X							C		
	(U58-9)	4HA	TA						A			B			C	
	MO	4GA	TA8						0			1			0	
	M1	4GA	TA1						0			0			1	
	M2	4GA	TA13						0			0			0	
	M3	4GA	TA9						0			0			0	

NOTES: 1. SEE TABLE 9.6.3.1.6 FOR INPUTS AND OUTPUTS ASSOCIATED WITH SUB ROUTINE A- .

2. APPLY THIS INPUT FOR EACH BIT TIME OF ITS ASSOCIATED SUB-ROUTINE. ALL OTHER BIT TIMES THIS INPUT SHOULD BE AT +10VDC.

REV. 1	REV. 4	REV. 7	PRINTS TO DL100 PR1	ENGINEER DEM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV. 23 1977			DRIVE SYSTEMS DEPT	DS3800HERA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/11/77			SALEM, VA. U.S.A.	CONT. ON SH. 9HA SH. NO. 9GA

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9.6.3.1.2 INPUTS/OUTPUTS

NOTE NO.	MNEMONIC	SH. NO.	PIN NO.	TEST TERM. NO.	BIT TIME: SUB ROUTINE A-4			SUB ROUTINE A-5			SUB ROUTINE A-6			SUB ROUTINE A-7		
					A	B	C	A	B	C	A	B	C	A	B	C
	OBDPR0	4AA	PA61		0	X	1	1	X	1	0	X	1	1	X	1
	OBDPR1	4AA	PA62		0	X	1	1	X	1	1	X	1	0	X	1
	OBDPR2	4AA	PA63		1	X	X	0	X	X	0	X	X	0	X	X
	OBDPR3	4AA	PA64		1	1	X	1	1	X	1	1	X	1	0	X
	OBDPR4	4AA	PA65		X	1	X	X	1	X	X	0	X	X	1	X
	OBDPR5	4AA	PA66		X	1	X	X	0	X	X	1	X	X	1	X
	OBDPR6	4AA	PA67		X	0	X	X	1	X	X	1	X	X	1	X
	OBDPR7	4AA	PA68		X	1	X	X	1	X	X	1	X	X	1	X
	ODBIN	4AA	PA17													
	OBCMRS	4AA	PA2													
	OBCMWS	4AA	PA4													
	OBAPR0	4BA	PA18													
	OBAPR1	4BA	PA19													
	OBAPR3	4BA	PA48													
	OBAPR8	4BA	PA53													
	OBAPR9	4BA	PA54													
	OSELECT	4BA	PA25													
	OMUXWR	4BA	TA6													
	OADCONV	4BA	TA23													
	HLD	4HA	TA22													
	AVAL	4HA	TA24			D			E			F			G	
	OCONVTP	4JA	TA17													
2	VAC	4HA	PA11		D											
2	REFO	4HA	PA10					E								
2	SP1	4HA	PA8								F					
2	SP2	4HA	PA6											G		
	(U58-9)	4HA	TA			D			E			F			G	
	MO	4GA	TA8			1			0			1			0	
	M1	4GA	TA1			1			0			0			1	
	M2	4GA	TA13			0			1			1			1	
	M3	4GA	TA9			0			0			0			0	

NOTES: 1. SEE TABLE 9.6.3.1.6 FOR INPUTS AND OUTPUTS ASSOCIATED WITH SUB ROUTINE A- .

2. APPLY THIS INPUT FOR EACH BIT TIME OF ITS ASSOCIATED SUB-ROUTINE ALL OTHER BIT TIMES THIS INPUT SHOULD BE AT +10VDC.

REV. 1	REV. 4	REV. 7	PRINTS TO DL100 PR1	ENGINEER DEM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV. 23, 1977			DRIVE SYSTEMS DEPT	DS3800HERA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/12/77			SALEM, VA. U.S.A.	CONT. ON SH. 9JA SH. NO. 9HA

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9.6.3.1.3 INPUTS/OUTPUTS

NOTE NO.	MNEMONIC	SH. NO.	PIN NO.	TEST TERM. NO.	BIT TIME: SUB ROUTINE A-8			SUB ROUTINE A-9			SUB ROUTINE A-10			SUB ROUTINE A-11		
					A	B	C	A	B	C	A	B	C	A	B	C
	QBDPR0	4AA	PA61		0	X	1	1	X	0	0	X	0	1	X	0
	QBDPR1	4AA	PA62		0	X	1	1	X	0	1	X	0	0	X	0
	QBDPR2	4AA	PA63		0	X	X	1	X	X	1	X	X	1	X	X
	QBDPR3	4AA	PA64		1	1	X	0	0	X	0	1	X	0	1	X
	QBDPR4	4AA	PA65		X	1	X	X	0	X	X	0	X	X	1	X
	QBDPR5	4AA	PA66		X	1	X	X	0	X	X	0	X	X	0	X
	QBDPR6	4AA	PA67		X	1	X	X	0	X	X	0	X	X	0	X
	QBDPR7	4AA	PA68		X	1	X	X	0	X	X	0	X	X	0	X
	QDBIN	4AA	PA17													
	QBCMRS	4AA	PA2													
	QBCMWS	4AA	PA4													
	QBAPR0	4BA	PA18													
	QBAPR1	4BA	PA19													
	QBAPR3	4BA	PA48													
	QBAPR8	4BA	PA53													
	QBAPR9	4BA	PA54													
	QSELECT	4BA	PA25													
	QMUXWR	4BA	TA6													
	QADCONV	4BA	TA23													
	HLD	4HA	TA22													
	AVAL	4HA	TA24			H			J			K			L	
	QCONVTP	4JA	TA17													
2	IAC2	4HA	PA		H											
	(U58-9)	4HA	TA			H			J			K			L	
	M0	4GA	TA8			1			0			1			0	
	M1	4GA	TA1			1			0			0			1	
	M2	4GA	TA13			1			0			0			0	
	M3	4GA	TA9			0			1			1			1	

NOTES: 1. SEE TABLE 9.6.3.1.6 FOR INPUT AND OUTPUTS ASSOCIATED WITH SUB ROUTINE A- .

2. APPLY THIS INPUT FOR EACH BIT TIME OF ITS ASSOCIATED SUB-ROUTINE ALL OTHER BIT TIMES THIS INPUT SHOULD BE AT +10VDC.

REV. 1	REV. 4	REV. 7	PRINTS TO DL109 PRI	ENGINEER DOM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED JUN 23,1977			DRIVE SYSTEMS DEPT	DS3800HERA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/12/77			SALEM, VA. U.S.A.	CONT ON SH. 9KA SH. NO. 9JA

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9.6.3.1.4 INPUTS/OUTPUTS

NOTE NO.	MNEMONIC	SH. NO.	PIN NO.	TEST TERM. NO.	BIT TIME: SUB ROUTINE A-12 A	A-12 B	A-12 C	SUB ROUTINE A-13 A	A-13 B	A-13 C	SUB ROUTINE A-14 A	A-14 B	A-14 C	SUB ROUTINE A-15 A	A-15 B	A-15 C
	OBDPR0	4AA	PA61		0	X	0	1	X	0	0	X	0	1	X	1
	OBDPR1	4AA	PA62		0	X	0	1	X	0	1	X	0	0	X	0
	OBDPR2	4AA	PA63		1	X	X	0	X	1	0	X	X	0	X	X
	OBDPR3	4AA	PA64		0	1	X	0	1	1	0	1	X	0	1	X
	OBDPR4	4AA	PA65		X	1	X	X	1	1	X	1	X	X	1	X
	OBDPR5	4AA	PA66		X	1	X	X	1	1	X	1	X	X	1	X
	OBDPR6	4AA	PA67		X	0	X	X	1	1	X	1	X	X	1	X
	OBDPR7	4AA	PA68		X	0	X	X	0	1	X	1	X	X	0	X
	ODBIN	4AA	PA17													
	OBCMRS	4AA	PA2													
	OBCMWS	4AA	PA4													
	OBAPR0	4BA	PA18													
	OBAPR1	4BA	PA19													
	OBAPR3	4BA	PA48													
	OBAPR8	4BA	PA53													
	OBAPR9	4BA	PA54													
	OSELECT	4BA	PA25													
	OMUXWR	4BA	TA6													
	OADCONV	4BA	TA23													
	HLD	4HA	TA22													
	AVAL	4HA	TA24		M			N			P			Q		
	OCONVTP	4JA	TA17													
	(U58-9)	4HA	TA		M			N			P			Q		
	M0	4GA	TA8		1			0			1			0		
	M1	4GA	TA1		1			0			0			1		
	M2	4GA	TA13		0			1			1			1		
	M3	4GA	TA9		1			1			1			1		

NOTES: 1. SEE TABLE 9.6.3.1.6 FOR INPUTS AND OUTPUTS ASSOCIATED WITH SUB ROUTINE A- .

REV. 1	REV. 4	REV. 7	PRINTS TO DL100 PR1	ENGINEER DSM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV 23,1977			DRIVE SYSTEMS DEPT SALEM, VA. U.S.A.	DS3800HERA CONT. ON SH. SLA SH. NO. SKA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/12/77				

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9.6.3.1.5 INPUTS/OUTPUTS

NOTE NO.	MNEMONIC	SH. NO.	PIN NO.	TEST TERM. NO.	BIT TIME: SUB ROUTINE A-16 A	B	C	3	4	5	6	7	8
	OBDPR0	4AA	PA61		0	1	1	1	1	X	X	X	0
	OBDPR1	4AA	PA62		0	1	0	1	1	X	X	X	0
	OBDPR2	4AA	PA63		0	1	X	1	1	X	X	X	0
	OBDPR3	4AA	PA64		0	1	X	1	1	X	X	X	0
	OBDPR4	4AA	PA65		X	1	X	1	X	X	X	X	0
	OBDPR5	4AA	PA66		X	1	X	1	X	X	X	X	0
	OBDPR6	4AA	PA67		X	1	0	1	X	X	X	X	0
	OBDPR7	4AA	PA68		X	1	1	1	X	X	X	X	0
	ODBIN	4AA	PA17					1	1	1	1	0	0
	OBCMRS	4AA	PA2					1	1	1	1	1	0
	OBCMWS	4AA	PA4					0	1	0	0	1	1
	OBAPR0	4BA	PA18					1	1	0	0	0	0
	OBAPR1	4BA	PA19					1	1	1	1	1	
	OBAPR3	4BA	PA48					0	0	0	0	0	0
	OBAPR8	4BA	PA53					0	0	0	0	0	0
	OBAPR9	4BA	PA54					0	0	0	0	0	0
	OSELECT	4BA	PA25					0	0	0	0	0	0
	QMUXWR	4BA	TA6					0	1	1	1	1	1
	QADCONV	4BA	TA23					1	1	1	1	1	1
	HLD	4HA	TA11					X	0	1	1	1	1
	AVAL	4HA	TA24			R		X	A	A	A	A	A
	QCONVTP	4JA	TA17					Z	Z	0	Z	Z	Z
	(U58-9)	4HA	TA			R			A	A	A	A	A
	M0	4GA	TA8			1			0				
	M1	4GA	TA1			1			0				
	M2	4GA	TA13			1			0				
	M3	4GA	TA9			1			0				

NOTES: 1. SEE TABLE 9.6.3.1.6 FOR INPUTS AND OUTPUTS ASSOCIATED WITH SUB ROUTINE A- .

REV. 1	REV. 4	REV. 7	PRINTS TO DL109 PRI	ENGINEER DBM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV. 23, 1977			DRIVE SYSTEMS DEPT SALEM, VA. U.S.A.	D S 3 8 0 0 H E R A
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/12/77				CONT. ON SH. SMA SH. NO. 9LA

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9.6.3.1.6 INPUTS/OUTPUTS

SUB ROUTINE A-____

NOTE NO.	MNEMONIC	SH. NO.	PIN NO.	TEST TERM. NO.	BIT TIME 1	2	3	4		5			
	OBDPR0	4AA	PA61		1	SEE	X	X	ø	X	SEE	X	SEE
	OBDPR1	4AA	PA62		1		X	X	ø	X		X	
	OBDPR2	4AA	PA63		1		X	X	ø	X		X	
	OBDPR3	4AA	PA64		1	NOTE	X	X	ø	X	NOTE	X	NOTE
	OBDPR4	4AA	PA65		1		X	X	ø	X		X	
	OBDPR5	4AA	PA66		1		X	X	ø	X		X	
	OBDPR6	4AA	PA67		1	1	X	X	ø	X	2	X	3
	OBDPR7	4AA	PA68		1		X	X	ø	X		X	
	ODBIN	4AA	PA17		1	1	1	1		0	0	0	0
	OBCMRS	4AA	PA2		1	1	1	1		1	0	1	0
	OBCMWS	4AA	PA4		1	0	1	0	1	1	1	1	1
	OBAPR0	4BA	PA18		1	1	1	0	0	0	0	1	1
	OBAPR1	4BA	PA19		1	1	1	1	1	1	1	0	0
	OBAPR3	4BA	PA48		1	0	0	0	0	0	0	0	0
	OBAPR8	4BA	PA53		1	0	0	0	0	0	0	0	0
	OBAPR9	4BA	PA54		1	0	0	0	0	0	0	0	0
	OSELECT	4BA	PA25		1	0	0	0	0	0	0	0	0
	OMUXWR	4BA	TA6		ø	0	1	1	1	1	1	1	1
	OADCONV	4BA	TA23		ø	1	1	0	1	1	1	1	1
	HLD	4HA	TA22		ø	X	0	1	1	1	1	1	1
	AVAL	4HA	TA24		ø	X	SEE NOTE 2						
	OCONVTP	4JA	TA17		1	Z	Z	Z	Z	Z	Z	Z	Z
	(U58-9)	4HA	TA			SEE NOTE 2							
	M0	4GA	TA8			NOTE 2							
	M1	4GA	TA1										
	M2	4GA	TA13										
	M3	4GA	TA9										

NOTES: 1. APPLY THESE INPUTS PER COLUMN "A" OF ASSOCIATED TEST TIME.

2. VERIFY THESE OUTPUTS PER COLUMN "B" OF ASSOCIATED TEST TIME. (SEE SECTION 9.5.2)

3. VERIFY THESE OUTPUTS PER COLUMN "C" OF ASSOCIATED TEST TIME.

REV. 1	REV. 4	REV. 7	PRINTS TO DL100 ARI	ENGINEER DEM	GENERAL ELECTRIC	TEST SPECIFICATIONS DIGITAL INTERFACE
REV. 2	REV. 5	ISSUED NOV 23 1977			DRIVE SYSTEMS DEPT SALEM, VA. U.S.A.	DS3800HERA CONT. ON SH. SNA SH. NO. SNA
REV. 3	REV. 6	MADE BY D.E. MOREHART 7/12/77				

DSD 0151 (09-76)

CARS

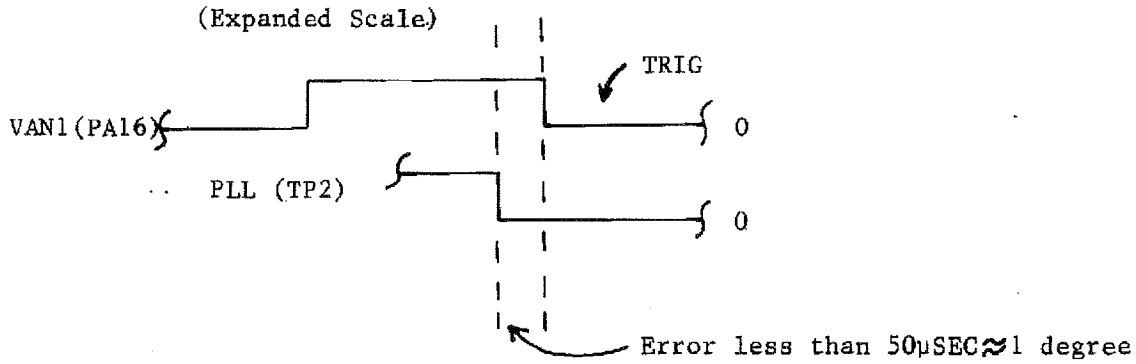
9.6.4 ANALOG TESTS

9.6.4.1 Phase Lock Loop Test

1. Connect a 1 MHZ 4.5V square wave (as defined in Section 9.2.2.1) to 02 (PA41).
2. Apply a 13.2 ± .2V peak to peak 60 HZ sine wave between VAN1 (PA16) and ACOM.
3. Observe a 5 ± 1VDC 60HZ square wave at PB60 (VAN0).
4. CR1 should be on at this time.
5. Verify that the wave shape at 0IR7 (PB80) is balanced between high and low states within 120 microseconds.
6. Set the VAN1 (PA16) signal to 55 HZ ± .1. Adjust R15 for 2.5 ± .01VDC at VCO (TP4).
7. Connect TB11 to DCOM.
8. CR1 should go OFF.
9. Disconnect TB11 from DCOM.
10. Observe that VCO (TB25) is 2.5 ± .01VDC.
11. Adjust the frequency of the input between VAN1 (PA16) and ACOM to 40 ± 1 HZ. CR1 should be on.
12. Re-adjust the input frequency to 75 ± 1 HZ. CR1 should be ON.
13. Re-adjust the input frequency to 60 ± 1 HZ.
14. Remove input from VAN1 (PA16) and apply to VAN2 (PA22). PLL light should be OFF.
15. Tie REF2 (PB56) to DCOM. PLL light should be ON.
16. Remove signal from REF2 (PB56) and VAN2 (PA22) from DCOM.
17. Tie OREFEN (PB70) to DCOM. Adjust R6 for 60 ± 1 HZ square wave at REFOSC (PB61). Should be switching to 5 ± 1VDC.

9.6.4.1 Phase Lock Loop Test (Continued)

18. Apply REFOSC (PB61) signal to VAN1 (PA16). Verify the following signals:



9.7.0 TEMPERATURE TESTS

This element shall be tested at room ambient only for production tests.

END OF TEST