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P3K-AL-0330-A01

TEST INSTRUCTIONS FOR SPEED CONTROL LOGIC

CONT ON SHEET SH NO.

EHC MARK II (SPEED CONTROL UNIT) FIRST MADE FOR

REV. #1

REVISION

I. SCOPE

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This instruction outlines the specifications for testing the Speed Control Logic board 1S2-A001.

CIRCUIT BOARD 117D7318.

II. CIRCUIT DESCRIPTION

The speed control logic is designed to incorporate the following features:

- When the power to the EHC control system is initially turned on, the unit will be in a TRIPPED condition. The speed reference will be in CLOSE VLAVES mode.
- The EHC Speed Control System must be RESET in order to activate the speed reference switches on the operating control panel. Note that the power for the switching bus is routed through the Plant Communication (PC) Circuitry. The speed reference will remain in the CLOSE VALVES mode when the system is RESET.
- Selecting anyone of the following SPEED SET switches on the operating control panel will seal in the selected circuit and drop out the previous mode.
 - CLOSE VALVES а.
 - LOW SPEED HOLD
 - MEDIUM SPEED HOLD
 - d. HIGH SPEED HOLD
 - RATED SPEED HOLD

There is no mandatory sequence of selection; the system can be in only one speed hold at a time. The speed reference logic will normally be in the CLOSE VALVES mode when the EHC system is TRIPPED or RESET. The purpose for the SPEED set logic is to switch the selected speed reference signal, to both LVG's and also to turn on the corresponding indicating light on the control panel.

4. When a new speed hold is selected which would call for an increase in speed, the acceleration amplifier of the primary LVG will normally come out of saturation and provide a constant rate of acceleration until the desired speed is reached. If the acceleration amplifier failed to come out of saturation, the turbine would accelerate up to the desired speed hold at an uncontrolled rate. This is referred to as a slingshot start. Therefore, whenever an increasing speed hold is selected, the speed control logic activates the antislingshot start circuit. When the speed hold switch is selected, a pulse is sent to the time delay relay K12 and to relay K10 which seals in the circuit. If the acceleration amplifier of the PRIMARY LVG, fails to come out

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Steam Turbine

Schenectady, N.Y.

P3K-AL-0330-A01

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TEST INSTRUCTIONS FOR SPEED CONTROL LOGIC

FIRST MADE FOR EHC MARK II (SPEED CONTROL UNIT)

CIRCUIT DESCRIPTION (continued)

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(continued)

of saturation before the time delay relay (K12) picks-up, the speed control logic will switch back to CLOSE VALVES. The antislingshot circuit is activated at all speed holds including OVERSPEED TEST. In otherwords, the antislingshot circuit is activated whenever the turbine is commanded to accelerate, and is disarmed when the turbine is commanded to decelerate.

- 5. The OVERSPEED TEST is possible only when the turbine is running at rated speed, and the circuit breaker is open (turbine not synchronized to the line). The overspeed circuit does not seal-in, and the button must be held down in order to increase turbine speed. The antislingshot circuit is automatically energized whenever the overspeed test is performed.
- When the circuit breaker is closed and the turbine is synchronized to the line, the RATED SPEED set will be sealed in. Note that all speed set circuits including the overspeed test are disarmed (locked-out) as soon as the breaker is closed.
- When the control system is at rated speed, all of the speed logic relays are de-energized except one (K9). If this relay should malfunction while the turbine is on line, it would probably go undetected since its loss would not affect the loaded turbine. However, when the unit is taken off line, this relay will be required to operate the RATED SPEED circuit, and the loss of K9 would automatically cause the control logic to revert back to the CLOSE VALVES mode.
- On tripping of the emergency trip system, the logic is de-energized and the CLOSE VALVES circuit is activated through an alternate +24 V source.
- When the HIGH SPEED HOLD mode is selected, the relay logic switches the wobbulator circuit to both the primary and back-up LVG's.
- 10. The relay logic prevents the primary LVG from being removed prior to the turbine being synchronized to the line. Since the primary LVG contains the only acceleration amplifier, it cannot be removed as long as the speed control system is in an operating mode which might call for the acceleration amplifier. If the LVG is pulled before the circuit breaker is closed, the speed control logic will return to the CLOSE VALVES mode.
- 11. Upon decrease of the speed reference, the unit will coast down to the new speed hold with valves closed. The valves will reopen when the new set speed is reached; there is no decelerating rate limit in the EHC speed control system.

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TEST INSTRUCTIONS FOR SPEED CONTROL LOGIC

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FIRST MADE FOR EHC MARK II (SPEED CONTROL UNIT)

II. CIRCUIT DESCRIPTION (continued)

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- The power to the Speed Reference switching bus is routed through the PC circuitry in order to control the Speed Hold circuits from either the operating control panel (MANUAL), or by the customers via REMOTE OPERATION. Relays are provided in the PC circuit to accomodate both operating modes. However, the LOW SPEED HOLD cannot be operated remotely.
- The LAMP TEST diodes and resistors are included on the relay logic 13. cards. These logic circuits permit all the lamps to be tested while the EHC system is in operation. A momentary pushbutton switch labeled LAMP TEST is located on the operating panel for checking the lamps.

III. CIRCUIT SPECIFICATIONS

- Before the board is coated, each diode of the 26 pairs should be checked (using an ohmmeter) both in the forward and reverse direction to insure that redundancy is effective.
- 2. All functional tests shown in the Logic Testing Table can be made with the board coated as well as uncoated.
- The symbols used on the Logic Testing Table are as follows:

TABLE SYMBOLS

- 0 = No Voltage applied or absence of voltage at output pins and test points or light off.
- 1 = +24 VDC applied to PWR input pins or presence of +24V at output pins and test points or light on.
- M = +24 VDC momentarily applied.
- P = +24 VDC pulse to pickup relay K10 and seal in time delay relay circuit.
- $H = Hold + 24 \ VDC \ (> 10 \ Sec.)$ on momentary input to insure that time delay relay K12 will not retime.

Apply +24V to pin 38 (TP11) and common to pin 40 (TP10) for all steps in the Logic Testing Table.

Before applying +24V to circuit board, perform the following continuity Checks:

> Continuity: Pins 35 to 36 Pins 31 to 34 Open, Ckt: Pins 31 to 32

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P3K-AL-0330-A01

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