1. TURN ON THE PRO 350 (ON-OFF SW. IN UPPER LEFT CORNER, ON=1, OFF=0)
THE COMPUTER SHOULD BE LEFT 'ON' AT ALL TIMES.
THE PRO 350 DOES A HARDWARE CHECK, THEN LOADS OPERATING SYSTEM, THIS TAKES APPROX. 1 MINUTE.
THE MAIN MENU IS NOW DISPLAYED, MOVE THE CURSOR TO DMC COMMUNICATOR 1 AND HIT RETURN OR DO. THE HELP MENU IS NOW DISPLAYED AND A MESSAGE "DMCTASK RUNNING" AND THE TIME.
PUSH PF1 KEY TO SET BAUD RATE TO 1200.
PUSH F17 KEY TO CLEAR SCREEN.

2. SET BERG JUMPERS PER ELEMENTARY.
CONNECT POWER TO UNIT UNDER TEST.
CONNECT CRT TO PLC/DMC CARD RS-232 CONN. (A NULL MODEM IS REQUIRED BETWEEN RIBBON CABLE AND PROCESSOR BOARD.)

3. APPLY POWER -- CHECK POWER UP ROUTINE (TEST SOFTWARE NOT LOADED YET)

PLC	DMC
DMC SELF TEST	DMC SELF TEST
PROM CSUM -- OK	PROM CSUM -- OK
BASE RAM -- OK	BASE RAM – OK
<INITIALIZED>	<INITIALIZED>
SYSTEM RAM - OK	SYSTEM RAM - OK
APP CSUM - NEW	APP CSUM - NEW
SELF TEST DONE	SELF TEST DONE

4. HIT RETURN UNTIL THE FOLLOWING IS DISPLAYED:
DMC MONITOR
REV. 3.16 4/07/87 (REV. AND/OR DATE MAY DIFFER)
SYS ID = DEFAULT
*>
ENTER PASSWORD (P) GE2
IF PLC/DMC BOTTOM LED TEST IS ON, TURN CONTROLLER OFF, AS FOLLOWS:
FOR PLC, TYPE (0) THEN (C) THEN (Y) THEN (Q).
FOR DMC, TYPE (0) THEN (C) THEN (OFF) THEN (Q).

5. CHECK MEMORY MAP (B) THEN (T) THEN RETURN
REFER TO LOCAL CONTROLLER MEMORY MAP MASTER & ELEMENTARY TO DETERMINE & VERIFY MEMORY MAP.
EXAMPLE: 00000 =RAM
02000 = NONE
04000 = RAM (RAMA)
0C800 = NONE
20000 = EEPROM
28000 = NONE
8E000 = RAM (HRMB)
90000 = NONE
F8000 = PROM (PLC/DMC)
COMMAND COMPLETE

TYPE Q TO EXIT THE B MODE OR ANY OF THE OTHER MODES.

NOTES: RAMA, EEPA, & PLC/DMC ARE ON 'L' BUS.
HRNB IS MAPPED INTO THE MEMORY USING 'E' BUS.
THIS REQUIRES A RIBBON CABLE BETWEEN PLC/DMC AND HPHB.
THIS IS CABLE SOMETIMES GIVES US PROBLEMS.
IF THE HRMB DOES NOT MAP CHECK THAT PIN 37 IS TIED TO COMMON.

6. TO LOAD USERS PROGRAM FROM PRO 350 HARD DISK
PUSH F17 KEY TO CLEAR SCREEN.
PUSH HELP KEY.
PUSH PF4 KEY TO SET BAUD RATE TO 9600.
PUSH F17 KEY TO CLEAR SCREEN.
PUSH HELP KEY.
RESET THE PROCESSOR BOARD (TEMPORARILY JUMPER TP1 TO TP2)
PUSH F19 KEY TO START LOADING PROCEDURE.
WHEN "TRANSMIT FILE TO DMC" MENU COMES UP, TYPE DMC, PLC OR CSF. (WHICHEVER IS WANTED) AFTER FILENAME THEN PUSH RETURN.
AFTER A FEW SECONDS ODSERVE THE COUNTER ON SCREEN COUNTING UP, AFTER LOAD IS COMPLETE, COUNTER WILL STOP AND FILE CLOSED, LAST WRITE QSTAT ( ) = 1 1, VAX NO ERRORS, SYSTEM RESTART, AND ANOTHER SELF TEST WILL BE DISPLAYED.
HIT RETURN UNTIL PROMPT *> IS DISPLAYED.
NOTE:
TO DETERMINE IF MEMORY BOARD IS LOADED WITH SOFTWARE FOR A DMCA OF PLC_ HITTING THE RETURN KEY AFTER SELF TEST WILL DISPLAY ONE OF THE FOLLOWING MESSAGES ON CRT PRECEEDING THE *>. (REV. NUMBER AND DATE MAY CHANGE.)

DMCA	PLC
DMC MONITOR	DMC MONITOR
REV. 3.4 4/21/85	REV. 2.7 4/20/85
SYS ID = VERSION _0	SYS ID = VERSION _0

IF SYS ID = DEFAULT, THE TEST PROGRAM WAS NOT LOADED, NEED TO RE-LOAD.
ENTER A NEW PASSWORD (P) PS2.
TURN CONTROLLER ON, AS FOLLOWS:
FOR PLC, TYPE (0) THEN (C) THEN (Y) THEN (Q),
FOR DMC, TYPE (0) THEN (C) THEN (ON) THEN (Q).
IF JOB HAS PCLA TURN I/O CHANNELS 2 AND 3 ON.
IF JOB HAS HXCA TURN I/O CHANNEL 16 ON.
TO TURN CHANNELS ON OR OFF, TYPE 0 THEN ONLINE STAT 0> WILL BE DISPLAYED, TYPE I THEN CHANNEL ? WILL BE DISPLAYED, TYPE THE CHANNEL NUMBER DESIRED, THEN RETURN THEN CHAN, STATUS IS GIVEN THEN MODIFY? WILL BE DISPLAYED, ANSWER Y TO CHANGE OR N NOT TO CHANGE.

NOTE: IF LOADING PROCEDURE IS ABORTED, PUSH EXIT KEY, POWER DOWN UUT, SELECT DMC COMMUNICATOR 1, THEN F17, THEN POWER UP UUT, THEN F19 TO GO THROUGH LOADING PROCEDURE AGAIN. IF SYSTEM LOCKS UP, DO A CONTROL C TO GET BACK TO MAIN MENU AND START OVER AGAIN.

EXAMPLE TO DISPLAY CHANNEL I/O STATUS

```
>ENTER  (0)  RETURN
0>  ENTER (D) RETURN
CONTROLLER  = ON
OUTPUT      = ON
INITIAL     = ON
HMHA        = ON
EEP_SEG     = ON
CO_PRO      = ON
HXCA        = ON
MONITOR     = ON
CHANNEL 02  = ON
CHANNEL 03  = ON
CHANNEL 0F  = ON
CHANNEL 16  = ON
```

7. TEST ALL CARDS CONTAINING EEPROM.
BE SURE CONTROLLER IS TURNED ON.
>ENTER (U) RETURN (SELECT USER PROG. WHICH HAS QC TESTS)
SELECT EEPA TEST FROM MENU
THE STARTING ADDRESS MUST BE ENTERED (THE MSB IS THE SEGMENT)
THE CBL BLOCK MULTIPLIES THE ADDRESS ENTERED BY 16 TO GET THE TOTAL ADDRESSS SEGMENT & BASE. EX: YOU ENTER 2000 WHICH IS SEGMENT 2, BASE 0000. THE AMOUNT OF MEMORY TO BE TESTED IS THE SECOND ENTRY.
EACH SEGMENT MAY CONSIST OF UP TO 64K OF MEMORY.
SEE HUMA/HUMB/HUMC SECTION OF TEST INSTURTIONS FOR ADDITION INFO, ON BERG SETTINGS AND SPECIAL MEMORY MAP SITUATIONS.
THE FOLLOWING MAP IS FOR A 32K EEPA CARD WHICH IS A HUMA USING 2K x 8 EEPROM CHIPS.

	QUAD "A"	QUAD "B"	QUAD "C"	QUAD "D"
START ADDRESS	2000	2200	2400	2600
MEM TO BE TESTED	1FFF	1FFF	1FFF	1FFF
CHIP 1 EVEN ADD	2000 U23 OFFE	2200 U27 OFFE	2400 U31 OFFE	2600 U35 OFFE
CHIP 1 ODD ADD	2000 U25 OFFF	2200 U29 OFFF	2400 U33 OFFF	2600 U37 OFFF
CHIP 3 EVEN ADD	2100 U24 OFFE	2300 U28 OFFE	2500 U32 OFFE	2700 U36 OFFE
CHIP 4 ODD ADD	2100 U26 OFFF 2101	2300 U30 OFFF 2301	2500 U34 OFFF 2501	2700 U38 OFFF

THE FOLLOWING EXAMPLE MAP IS FOR A 64K x 8 EEPROM MMAB MEMORY BOARD WHICH IS A HUMA BOARD WITH 8K x 8 RAM CHIPS IN QUADS A & B AND 8K x 8 EEPROM CHIPS IN QUADS C & D.

	QUAD "A"	QUAD "B"	QUAD "C"	QUAD"D"
START ADDRESS	----------	----------	2000	2800
MEM TO BE TESTED	----------	----------	3FFF	3FFF
CHIP 1	DO A MEMORY MAP ONLY		2000 U31	2800 U35
EVEN ADD			3FFE	3FFE
	FOR QUADS A AND B			
CHIP 2			2000 U33	2800 U37
ODD ADD			3FFF	3FFF
START ADDRESS	----------	----------	2400	2C00
MEM TO BE TESTED	----------	----------	3FFF	3FFF
CHIP 3			2400 U32	2C00 U36
EVEN ADD			3FFE	3FFE
CHIP 4			2400 U34	2C00 U38
ODD ADD			3FFF	3FFF

OTHER STARTING ADDRESSES MAY APPLY, BUT ONLY 16K (3FFF) SHOULD BE TESTED AT A TIME TO SPEED UP THE ISOLATION OF A BAD CHIP. OTHER BOARDS MAY HAVE EEPROM IN DIFFERENT QUADS, BUT SAME PROCEDURE SHOULD BE USED.

NOTE: REMEMBER TO 'T' STAMP THE LABEL ON BACK OF CARD.

8. SAVE PROGRAM ON EEPROM (EEPA) OR (OTHER MEMORY BOARD)

```
>ENTER (X) RETURN
XFER SYSTEM
X> ENTER (S) RETURN
SAVE EE PROM
BASE SYSTEM ? ENTER (Y) RETURN          (Y=YES  N=NO)
---WORKING---
COMMAND COMPLETE
X>
```

REPEAT THIS PROCEDURE A SECOND TIME IT SHOULD ONLY TAKE A SECOND IF THE ORIGINAL SAVE WAS GOOD. THE PROGRAM ONLY WRITES TO EEPROM LOCATIONS THAT DO NOT MATCH RAM.

9. VERIFY SYSTEM LOADS FROM EEPA ON POWER UP
TURN POWER OFF AND BACK ON
CRT SHOULD BE AS FOLLOWS : (TEST SOFTWARE NOW LOADED)

PLC	DMC	CSF
DMC SELF TEST	SELF TEST DONE	DMC SELF TEST
PROM CSUM – OK		PROM CSUM – OK
BASE RAM – OK		BASE RAM – OK
<RESTORED>		8087 CHECK – OK
SYSTEM RAM – OK		SYSTEM RAM – OK
APP CSUM -- OK		APP CSUM – OK
SELF TEST DONE		CSF INIT – OK
		SELF TEST DONE

HIT RETURN UNTIL CRT DISPLAYS THIS TYPE MESSAGE:
(THIS IS A GENERAL EXAMPLE, REV. AND DATE MAY CHANGE)

DMC MONITOR
REV. 2.8 7/16/86
SYS ID = VERSION _ 0
*>

10. To test DMC I/O
Locate the proper test instructions per table of contents.

11. To test Stick I/O
Call user program & connect Unit Under Test(UUT) connectors to MEM DMC I/O test module JHB(34 pin) & JJB(26 pin) with ribbon cables.
HPBC on UUT must be in decode mode
Select card type to be tested HLIA, HLOA,NDAC, & NADA
UUT 34 Pin connector should have pins 2,4,6,8,10,12,16,18,20 & 27 tied together and to DCOM.
UUT 26 pin connector should have pins 2,4,6,8,12,19,21,23 & 25 tied together and to DCOM.

12. To test Local I/O
Call user program & connect UUT connectors to MEM DMC I/O test module JKA(34 pin) & JCA(26 pin) with ribbon cables.
HPBC on UUT must be in buffer mode
Select card type to be tested HLIA, HLOA, NDAC, & NADA
UUT 34 pin connector should have pins 1,2,3,5,7,9,11,13,15,17,19 21,23,25,27,29,31 & 34 tied together and to DCOM.
UUT 26 pin connector should have pins 1,2,3,5,7,9,11,13,15,17, & tied together & to DCOM.

13. Test of HRMB/HPBC shared memory between DMC module and Control Signal Highway (CSH).
Connect Highway Test Module (HTM) to CSH slave module (TM2 modified)
HTM Transmit to CSH slave HXLA JT1 (4th from top)
HTM Receive to CSH slave HXLA JT0 (top)
Connect maintenance cable from HTM to slave.
Connect CSH slave connectors JF & JJ to UUT HPBC/D connectors with ribbon cables.
Connect cable from E-bus connector on processor board to connector on HRMB (This must be done to map the RAM on HRMB board)
HPBC input lines must be terminated with NTEA card.
Be sure enable switch on HPBC/D is enabled.
Be sure 48 pin ribbon cable is connected between the HLSC card and HLSD card on the CSH module.
This test will verify E bus & CSH can read and write to HRMB 256 bytes of memory. (or whatever length you enter)
UUT 34 pin connector should have pins 1,2,3,5,7,9,11,13,15,17,19,21 23,25,27,29,31 & 34 tied together and to DCOM.
UUT 26 pin connector should have pins 1,2,3,5,7,9,11,13,15, & 17 tied together and to DCOM.

E BUS ADDRESS		HTM	HPBD
BASE	OFFSET	GROUP	GROUP
8E00	0000	00	0-1
	0002	01	0-1
	0004	02	0-1
	0008	04	0-1
	0010	08	0-1

0020	10	0-1
0040	20	2-3
0080	40	4-5
00F0	78	6-7
00FE	7F	6-7

HTM setup to output to DMC

	Outut data switched
Select STA-5, Page-off	F E D C B A 9 8 7 6 5 4 3 2 1 0
group-desired group per chart	1 1 1 1 1 0 1 0 1 1 0 0 1 1 1 0
HEX EQUALS	F A C E

Input/output mode-simulate, test control mode-repeat, select-output page-off.

When ready to input to DMC, push test on the HTM to input a single input to DMC. Each time test is pushed (if in 'single' mode) the bottom red LED on the HLSC card in the slave module should blink. If in the 'repeat' mode the input will cycle from the HTM automatically over and over and the bottom LED on the HLSC card will follow this cycle.

At the terminal:

> Enter B for breakpoint	CRT responds B>
Enter B for base	CRT responds base?
Enter 8E00 RETURN	CRT responds >
Enter D for display	CRT responds offset?
Enter the offset from chart, RETURN	CRT responds length?
Enter 256, REURN	CRT responds format (W,A,B)?
Enter W for word	CRT displays no. bytes selected

When you answer length?, the first group shown should read FACE, the value input to DMC from HTM. Any lines of memory locations containing all zeros will be replaced by an * on the CRT.

HTM setup to input to HTM

Input/output mode-simulate, test control-repeat, select-input, page-off group-desired group per chart.

At the terminal:

Enter RETURN the Q	CRT responds >
Enter B for breakpoint	CRT responds B>
Enter M for modify	CRT responds offset?
Enter offset from chart	CRT responds 8E00 : (offset no.) =XX XX = low order byte sent from HTM

Enter two digits (one byte) HEX value to be sent to HTM, when RETURN is pushed this value should be output from DMC to the HTM and XX HEX should be displayed on 'data and address display' on HTM as low order byte. Do a RETURN and enter a second entry, this will then appear as the high order byte on the HTM. Data bytes are in memory in the following order.

Low order byte		High order byte	
1100	1110	1111	1010
C	E	F	A

LEDs on HTM

FEDC BA98 7654 3210
1111 1111 1111 1111 = FFFF HEX

14. Test of 8087/80287 co-processor on PLC_/DMC_ daughter board.
Call user program and select CO_P test. Controller must be on.
This routine will exercise the co-processor to perform some
Arithmetic functions.

15. Test of PCLA (HMHA base board) (Control Party Line (CPL) master)
Perform test only if UUT contains PCLA
Put J15 and J16 in 'out' position.
Call user program and select PCLA.
Conn. Chan A of PCLA to PAAA (HSHA) slot 1A of MEM Local Controller I/O test module and Chan B of PCLA to PAAA slot 1D of MEM Local Controller I/O test module.
Controller must be on as well as channel 2 & 3.
The test is go/no go type.
NOTE: Set the WAIT times for DMCA to 20 and DMCC to 40 as follows:
Type M for 'Modify'mode, then another M for modify?, then type WAIT, the present WAIT time wil be displayed, then value, type in the desired value.
It is best to set CPL scan time to 0 ms when doing the PCLA test from the user monitor. (Call S then M then CPL then 0)

16. Test of PXCA (HXCA base board) (C bus master)
Perform test only if UUT contains HXCA

NOTE: HXCA MUST BE STRAPPED FOR ADDRESS 6000 TO PERFORM TEST.
AFTER TESTING HXCA , RE-ADDRESS PER ELEMENTARY .

J2	J3	J4	J5	J6	
.	.	.	.	.	T
.	l	l	.	.	
l	.	.	l	l	F
F	E	D	C	B	

Call user program and select HXCA
Conn. ribbon cable from HXCA JA UUT to HXRA JA in SEM Local Controller 'C' bus test module.
The test is go/no go type.

NOTE: CHANNEL 16 MUST BE ON. CHECK THAT PIN 4 ON THE HXCA GOES TO PIN 4 OF THE PROCESSOR CARD.

17. Test of HXMA (Local Controller/Series 6 shared memory 32 bytes)
HXMA contains 2-- 32 x 8 memories
The memory is accessed by L bus I/O from the Local Controller and
F bus from the HXRA/DXRA (series 6 I interface) .
L bus Inputs & F bus outputs access one 32 x 8 memory and
L bus outputs & f bus inputs access the other 32 x 8 memory.

Connect twisted ribbon cable between HXRA(JA) & DS3815PXCA (HXCA & prom)
If UUT is a DMC, a PXCA can be borrowed and temporarily inserted in any
'L' bus slot. (Pin 4 of PXCA slot must be wired to PLC_ pin 4 to allow
PXCA to work correctly (a temporary jumper may be added).
NOTE: Channel 16 & controller must be on for this test.
C_BUS scan set to 100ms
Switch on HXRA must be in the active position.
HXMA F-BUS starting address must be F-F for proper operation
of the communication. (FAB-5=F FAB-6=F)
Bottom light on HXRA must be blinking to indicate proper C_bus
communication.
Enter (U) on keyboard & Select HLOA test from menu.
Enter address 8000.
Select display test (D).
Enter 1010101010101010, Return.
Enter (N) return to exit without clearing data.
Enter EX, return (to exit user monitor program)
Select Display 'D' mode. CRT responds 'DISPLAY?'
Enter Ix01, return CRT should read HLIA =-21846.
Enter (M) for modify, CRT reads 'modify ?'
Enter Ox01 , CRT reads VALUE ? Enter 21845 , Return .
CRT reads D >, Enter (Q) to exit .
Enter (U) to select user program.
Select HLOA test, address 8000.
Select display test (D). Enter (0), return (An output is done prior to
an input to freeze the data for the input (read) function.
Select HLIA test , address 8000.
Data should read 0101010101010101.
Exit program , select HLOA test
and repeat above procedure for the following addresses.

NOTE : Address 8000 thur 803c are examples only , if HXMA is
addressed for 8000 , the address's are valid . Refer to
elementary for correct address .

	(D) DISPLAY	(M) MODIFY
8000	IX01	OX01
8004	IX02	OX02
8008	IX03	OX03
800C	IX04	OX04
8010	IX05	OX05
8014	IX06	OX06
8018	IX07	OX07
801C	IX08	OX08
8020	IX09	OX09
8024	IX10	OX10
8028	IX11	OX11
802C	IX12	OX12
8030	IX13	OX13
8034	IX14	OX14
8038	IX15	OX15

18. HSPC & HPCA

Connect test tach box to HSPC JA connector. The 3 jumpers on the HSPC must be set to 'SIN' position for the test tach. Reset to elementary position upon completion of this test. Turn knob on test box CW check that count up led is on & ST-0 thru ST-3 Leds are on. Turn knob on test box CCW. Check that count down Led is on & ST-0 thru ST-3 Leds are on. Put switch on HPCA to test position (up) check that Leds are counting. Put switch to normal position on HPCA. Check Leds g,d,e,f, on HPCA count up & down as knob on tach box is turned. Use the DISPLAY of the I/O address of the HPCA and verify 4 LED's agree with the most signifigant byte of the word displayed.

19. HXPC/D test ----------

Digital I/O is checked utilizing a wrap around cable and test is called from the USER MONITOR. If test fails HLOA,HLIA, or HDRA test may be used to further isolate faults. Card address to use is Base-address + 6H (card is mapped at 9000H use 9006 for input & output address. Interupts and counters are not checked.

20. HIOD TEST ----------

Connect special test harness to JA, JB & JC connectors. Select USER MONITOR HIOD test. Select loop test (GO/NO GO) for module level test. For final test or diagnostics use the discrete input & output options available.

21. NCVA TEST ----------

Card has 8 identical circuits, inputs at JA connector and outputs connected to NADA. Test as NADA(refer to NADA test) , Input current to appropiate JA conn. pins, read output volts from NADA. Inputs of 4 to 20 mil-amps will output 2 to 10 volts, test at mid-range.

22. HPRB/HPRC TEST ----------

Call HPRC test from USER MONITOR and input I/O address. Input test frequency of approx. 1khz at vrms to JA connector, verify with counter. The value measured by counter should match that displayed by test program. More than 1 input can be exercised at a time if signal generator being used is capable. Make sure terminal is running at 9600.

CKT	JA CONNECTIONS	
	INPUT	COM
1	JA-1	JA-2
2	JA-3	JA-4
3	JA-5	JA-6
4	JA-7	JA-8

23. HRTA TEST ---------- (ONLY WORKS WITH DMCA AT PRESENT)
Call HRTA test from USER MONITOR and input address. Select frequency and channel to be output and verify output with counter. For base clock frequency pin 4 must be tied to pin 8.

24. HAIA/HAIC TEST ----------
Call HAIA test from USER MONITOR and input address. Connect cable between JA & JB and run digital I/O check. Use special test to control or display back plane pins. Use analog section to control mux(internal & external) and perform A/D conversion and display results. Type in the 8 bits of the control word. Ex: 0100 0011 would select chan. 4 and input #3 (PA21)
Control word format:

MSB	LSB	
xxxx	xxxx	MSB control selects Chan 0-15(PA16,19,18,21-24 2,4,13,15,8,17,10,12) to be A/D converted
		LSB control determines the state of 1PA0-1PA3 (PA39,41,49,47) which are used by multiplexer cards such as NAIA or NTCF.

25. NAIA, NAIB, NAIE TEST ----------
NAIA/NAIE TEST (4-20ma = 2 to 10 volts out)
Use special NAIX/NTCF test fixture
Input 1.5v to box and connect ribbon cable between box & NAI_
Use HAIA test for mux control & A/D converting
Expect 7.5 volts to be displayed by HAIA test
Exercise all 16 inputs by switches on test box & HAIA control
Repeat with –1.5 volts in and –7.5 volts out

NAIB TEST (+/-10 volts in = +/-10volts out)
Input + & -7.5 volts and expect + & - 7.5 votls to be displayed with HAIA test.

26. NTCA, NTCB, NTCC, NTCD, NTCF, TEST

Use special NAIA/NTCF test fixture with user monitor HAIA test.
Input proper voltage per table below to test box.
(Input voltage times stated gain should = 7.5v read with HAIA test)
Select input to be tested via switches on test box
Exercise al 16 inputs by switches on test box & HAIA control

BOARD	GAIN	INPUT VOLTAGE
NTCA	361.4	20.8 MV
NTCB	304.1	24.7 MV
NTCC	271.1	27.7 MV
NTCD	199.9	37.6 MV
NTCF	216.3	34.7 MV

27. NVAA TEST ----------
4 Current driver circuits
Typically driven by NDAC
0-10 volts in = 4-20 ma out
Load all 4 output circuits with 500 ohms(IMOK led should be on)
Measure voltage across each load resistor
Value measured should be within 1% of the following computed values
Volts across resistors = .004*RL + .0016*Vin*RL where:
RL=load resistor value Vin=input voltage via NDAC

Example:
Load circuit with 511 ohm resistor & put +2 volts in from NDAC
Value to be measured = .004*511 + .0016*2*511
Value to be measured = 2.044 + 1.635 = 3.679

28. HCMA test ----------
The HCMA is tested utilizing a special loop back cable and PTCA, PTCB or PTCC software on the card. Any other configuration is not testable. The loop back cable must be connected between JA & JB. The test is go/nogo type. Enter the 'L' bus address of card and the test will run.

Printer or other output device may be verified by utilizing above test, but remove loop back cable from JA to JB on HCMA and connect device to be tested to JA.
use "Modify" utility to set HCMA baud rate("Baud1") to match baud rate of device under test.
When test is performed printer should print "ABCDEF123", and monitor will indicate test failure(due to open loop).
After test is complete reset "Baud1" to 4800 and verify by modify/ display utility.

29. NRTA/NPSL test
The NRTA/B card is tested using the HAIA Analog user monitor test and DMC test box 1. Test box switches resistors across each of the 8 circuits on the board as follows. * It takes 20 minutes for card to warm up.

JA21—1----{ R }----JA20
JA19---1

To perform test, set appropiate switch on test box and type in control word. Control word will echo on monitor and 7.5volt ouput will be displayed. Repeat for each circuit.

NOTE: Z in the control word should reflect the jumper on NRTA, if it is low, Z should be "0", if it is high, Z should be "1". If two NRTA outputs are tied together, the high/low jumpers must be set different on each card to avoid confliction.

CKT#	HAIA CONTROL WORD CHAN CKT
0 JA21, JA19--------JA20	XXXX Z000
1 JA22, JA23--------JA24	XXXX Z001
2 JA18, JA16--------JA17	XXXX Z010
3 JA14, JA13--------JA15	XXXX Z011
4 JA12, JA10--------JA11	XXXX Z100
5 JA7, JA9--------JA8	XXXX Z101
6 JA5, JA6--------JA4	XXXX Z110
7 JA2, JA3--------JA1	XXXX Z111

EXAMPLE: channel 12, circuit 1, with NTRA jumper high------1100 1001

30. LCFBUS TESTABLE INPUT CARDS

HLIA	5vdc 16 bit non-isolated
HLIC	5vdc 8 bit isolated
HDRA	JA 16 bit output (5v) , JB 16 bit input
HSCA	115VAC/105VDC 8 bit isolated
HSCB	125VDC 8 bit isolated
HSCC	28VDC 16 bit non-isolated
HSCD	105VDC 16 bit non-isolated (JA17 must br tied to DCOM)
HSCE	105VDC/28VDC 8 bit non-isolated
HSCH	28 VDC non-isolated
NADA/B	Analog to digital 8 channels +/-12.5 volts

HLIA, HLIC, HSCA, HSCB, HSCC, HSCD, HSCE, HSCH

A. Select USER MONITOR (U) and HLIA test. Connect the input test box to card under test. Apply the appropriate signal for the card under test to the test box. (Refer to card backsheets and module wiring to provide proper test signal inputs to card) Open and close switches on test box and verify CRT readout tracks the changes. For 8 bit cards use the LSBs on the HLIA display. The MSBs should be '0' if no other card is connected to that address.

B. If UUT has HLIA and HLOA, connect the special test harness between HLIA-JA and HLOA-JA . Select USER MONITOR (U) and HDRA test. Enter HLOA address for output address and HLIA address for input address. Use ripple or display to test both cards at the same time.

C. If card is not directly on 'F' bus ie: connected to DMC via 'C' bus or 'CPL' link the following technique can be used. The input can be displayed by using the display 'D' command. Example: Assume an HLIA card on 'C' bus addressed at 6002, use display. I6002B (B for HEX format) IF the displayed value were CF72 (1100 1111 0111 0010) would be the binary pattern that should also be present on that card.

31. HSCA, HSCB and HSCE test (8 circuits, inputs on JA2, 4, 6, 8, 10 ,12, 14, 16)
Apply appropriate input voltage to appropriate pins on card under test per list at beginning of step 30. Connect COM pin 17 of front edge connector and to DCOM on module. Check for correct output and proper LED is on.

32. HSCC, HSCD and HSCH test (16 circuits, inputs on JA1 through JA16
Apply appropriate input voltage to appropriate pins on card under test
per list at beginning of step 30. connect COM to pin 17 of front edge
connector and to DCOM on module. Check for correct output and proper
LED is on.

33. NADA/B----------

A. Select USER MONITOR (U) and NADA test. Connect power supply to NADA
JA (see * below) input voltages (+/-12.5 volts) to the 8 channels
and check for the same voltages being read when the NADA test is run.

*NADA channel :	0N-JA1	channel	1N-JA3	channel	2N-JA3	channel	3N-JA7
	0P-JA2		1P-JA4		2P-JA6		3P-JA8
	4N-JA9		5N-JA11		6N-JA13		7N-JA15
	4P-JA10		5P-JA12		6P-JA14		7P-JA16

B. NDAC to NADA, See special note in output section to test UUT which
contains NDAC and NADA cards.

C. If card is not directly on 'F' bus ie: connected to DMC via 'C' bus or 'CPL' link, the following technique can be used. The output can be displayed using the display 'D' command. The format of the output is as follows:

```
                I                 I
               XIXXX  XXXX  XXXX IXXXX
Sign bit       I                 I LSBs not used
               I                 I
```

Using the C (counts) mode for display, the conversion to volts can be made as follows:

$$\text{Input volts} = \frac{\text{Counts displayed}}{16} * .00488 \text{ volts} * \frac{1}{.8}$$

The division by 16 is to account for the 4 LSBs not being used in the returned word format. The .8 factor is to account for the gain of .8 from input to A/D converter on the card.

Example: NADA card on 'C' bus with starting address at 6000. Use display 'D' of .I6000C and get 16393 (0100 0000 1001 0000) Convert to volts as follows:

$$\text{Input volts} = \frac{16393}{16} * .00488 * \frac{1}{.8} = 1024.5 * .00488 * 1.25 = 6.249\text{v}$$

If card is NABD the above information applies to the +/-12.5 volts jumper setting. If the jumper is set for +/- 10 volts operation, the .00488 number changes to .0039.

34. HDRA/C ----------

A. R-bus test: Connect a ribbon cable from HDRA JA to HDRA JB
Select USER MONITOR (U) and HDRA test. Enter HDRA address for input and output address. Ripple or display test can be run, then verify correct inputs and outputs.

B. Manual mode test: Place a 'TEST' HDRA card in slot 1G of 'TEST MEM' with J1 set to the 'R' position. Connect a 34 pin cable from JA of 'TEST' HDRA to JB of HDRA in UUT. Call up HLOA test from USER MONITOR at address 4010 and do the display test, set in different bit patterns to exercise the HDRA outputs.

The following table shows bit position to output pin relationship and input to output relationships.

F E D C	B A 9 8	7 6 5 4	3 2 1 0	
57 58 59 60	53 54 55 56	48 47 50 52	76 74 72 70	
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	= 1 HDRA output
1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	= 0 HDRA ouput

The output pins may be looked at with DVM or if HDRA output drive into logic circuits the inputs to HDRA may be changed to set up permissives for the logic circuits.

35. LCFBUS TESTABLE OUTPUT CARDS

HLOA—5VDC 16 bit non-isolated
HLOB—5VDC 8 bit non-isolated
HLOC—5VDC16 bit non-isolated
HRRB—8 bit normally open reed relay isolated
HSDD—8 bit fused solenoid driver isolated
NDAC/D—digital to analog, 4 channels +/-10 volts

HLOA, HLOB, HLOC, HRRB, HSDD

A. Select USER MONITOR (U). Use HLOA for any 16 bit card. Use HRRB for 8 bit card. Run ripple test or display test and check that LED's correspond to data being input.

B. If two 8 bit cards are addressed to a word (16 bit), one low byte and one high byte, use the HLOA test.

C. If the module being tested has an HLOA (output) and an HLIA (input) connect the test harness between HLIA JA and HLOA JA. Select USER MONITOR HDRA test. Enter HLOA address for output address and HLIA address for input address. Ripple or display test can be used to test both cards simultaneously.

D. If the card is not directly on the 'F' bus ie: connected to DMC via 'C' or 'CPL' link the following technique can be used. The output can be controlled using the modify 'M' command to the address of the output to be monitored.
Example: Modify HLOA output addressed at 6000 on 'C' bus.
Do modify .06000B (b calls for HEX format)
Input desired output A261 (1010 0010 0110 0001)

36. HSDD test ----------
Use HRRB test. NOTE: Pin 18 on the HSDD should be tied to pin 56 on the processor board.

37. NDAC/D ----------

A. Select USER MONITOR (U) Select NDAC test. Connect voltmeter to first circuit and output voltage (Range +/-10 volts) Voltmeter should read the output voltage. Repeat at different voltages and for all 4 circuits.

TP1—COM—JA4
TP2—CKT#1—JA3
TP3—CKT#2—JA5-(JA8 COM)
TP4—CKT#3—JA7-(JA8 COM)
TP5—CKT#4—JA9-(JA10 COM)

When using the NADA in the unipolar mode, (J1A and J1B = +) only the operation of circuit #1 is affected. Using the NDAC test , when you ask for X number of volts out you will get one half of that value on circuit #1. Circuits # 2-4 still produce a 1 to 1 ratio.