g GE Energy	**Functional Testing Specification**
Parts & Repair Services ***Louisville, KY***	**LOU-GED-117D6635**

Test Procedure for a 117D6635G0001 and G0002 Low Value Gate Cards

DOCUMENT REVISION STATUS: Determined by the last entry in the "REV" and "DATE" column

REV.	DESCRIPTION	SIGNATURE	REV. DATE
A	Transferred from P3K-AL-03060A01 into shop's format	M. Starling	6/6/2013
B	Updated step 12 – remove ground for TP7 and step 13 first line to Leave S2 connected to Pot.	G. Chandler	6/24/2013
C			

PREPARED BY	REVIEWED BY	REVIEWED BY	QUALITY APPROVAL
M. Starling			Charlie Wade
DATE	**DATE**	**DATE**	**DATE**
6/62013			6/6/2013

1. SCOPE

1.1 This is a functional testing procedure for a 117D6635G0001 and G0002 Low Value Gate Cards

2. STANDARDS OF QUALITY

2.1 Refer to the current revision of the IPC-A-610 standard for workmanship standards.

3. APPLICABLE DOCUMENTS

3.1 The following document(s) shall form part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue shall apply.
- **3.1.1** Check board's electronic folder for more information
- **3.1.2** Reference P3K-AL-0306-A01 procedure

4. ENGINEERING REQUIREMENTS

4.1 Equipment Cleaning
- **4.1.1** Equipment should be clean and free of debris prior to applying power unless performing an initial check. Refer to site specific SRA's for cleaning guidelines.

4.2 Equipment Inspection
- **4.2.1** Equipment should be visually inspected for any defects prior to applying power. This inspection should include the following as a minimum:
  - **4.2.1.1** Wires - broken, cracked, or loosely connected
  - **4.2.1.2** Terminal strips / connectors - broken or cracked
  - **4.2.1.3** Components - visually damaged
  - **4.2.1.4** Capacitors - bloated or leaking
  - **4.2.1.5** Solder joints - damaged or cold
  - **4.2.1.6** Circuit board - burned or de-laminated
  - **4.2.1.7** Printed wire runs / Traces - burned or damaged

5. EQUIPMENT REQUIRED

5.1 The following equipment is required to perform the process requirements. Equipment may be substituted provided that all accuracy's and test ratios are equivalent or better.

Qty	Reference #	Description
1		Tektronix TDS2012B O-scope or equivalent
1		Fluke 189 Multimeter or equivalent
1		Dual output bench Power Supply for +22 / -22 VDC
1		H188973 +10/-10 VDC Precision Power Supply

6. Modifications/Upgrades

TEST INSTRUCTIONS / PROCEDURE P3K-AL-0306-A01 LOW VALUE GATE CARD (LVG)

(Refer to the LVG circuit board schematic while board is being tested)

- Connect LVG board as shown in test set-up.

1. **CHECK SUPPLY VOLTAGES**
   - Check that the supply voltage at TP1 is +15.700 ± 1.000V.
   - Check that the supply voltage at TP2 is -15.700 ± 1.000V.
   - Check that the supply ground at TP11 is zero Volts.
2. **BALANCE SPEED AMPLIFIER**
   - Open S7 (PIN 17) and close all other switches. (All inputs to speed and acceleration amplifier are now shorted and grounded, and amplifier output is disconnected from LVG configuration).
   - Balance speed amplifier IC1 by adjusting VR50 until the voltage at TP6 is zero volts, ± 1 mV. Check that the voltage at TP7 is approx. +2.000V.
3. **SET BIAS**
   - Check speed amplifier output bias voltage at PIN 14. Check that this voltage can be varied from approx. +2.500V (max. CW) to zero volts (max. CCW) by adjusting VR1. Set this voltage to +1.000V.
4. **BALANCE ACCELERATION AMPLIFIER**
   - Open S2 (PIN15). Close S7 (PIN 17). All other switches should remain closed. Jumper 5K potentiometer output to PIN 15 and set to +10.000V. (This signal will cause the speed amplifier to go into negative saturation). Jumper out (short) capacitor C7.
   - Balance acceleration amplifier IC2 by adjusting VR51 until the voltage at TP6 is zero volts ± 1 mV. Check that the voltage at TP4 is approx. +2.000V.
   - Remove the 5K potentiometer output from PIN 15 and the jumper from across C7.

5. **TEST SPEED AMPLIFER & SET GAINS**
   - Open S6 (PIN 25). Close S2 (PIN 15). All other switches should remain closed. Jumper 5K potentiometer output to PIN 25 and set to +10.000V. (This signal will cause the acceleration amplifier to go into negative saturation). Check voltage at TP4 to insure that the acceleration amplifier is in negative saturation. Check voltage at TP7 to insure speed amplifier is not saturated; this voltage should be approx. +2.000V.
   - Check that LVG output voltage at TP6 is 0.000V ± 1 mV.
   - Leave 5K potentiometer output connected to PIN 25 and set to +10.000V.
6. **SET SPEED SIGNAL GAIN**
   - Open S1 (PIN 26)
   - Apply a +.500V signal to PIN 26. Adjust VR4 until LVG output voltage at TP6 is -5.000V.
   - Remove +.500V signal and apply a -.500V signal to PIN 26. Check that the LVG output voltage at TP6 is +5.000V. Remove -.500V signal.
   - Leave 5K potentiometer output connected to PIN 25 and set to +10.000V.
7. **SET SPEED REFERENCE SIGNAL GAIN**
   - Open S2 (PIN 15). Close S1 (PIN 26). All other switches with the exception of S6 (PIN 25) should be closed.
   - Apply a +.900V signal to PIN 15. Adjust VR3 until LVG output voltage at TP6 is -10.000V.
   - Remove +.900V signal and apply a -.900V signal to PIN 15. Check that the LVG output voltage at TP6 is +10.000V. Remove -.900V signal.
   - Leave 5K potentiometer output connected to PIN 25 and set to +10.000V.

8. **SET SUPPLEMENTARY SPEED REFERENCE GAIN**
   - Open S3 (PIN 19). Close S2 (PIN 15). All other switches with the exception of S6 (PIN 25) should be closed.
   - Apply a +.900V signal to PIN 19. Adjust VR2 until LVG output voltage at TP6 is -1.500V.
   - Remove +.900V signal and apply a -.900 V signal to PIN 19. Check that the LVG output voltage at TP6 is +1.500 V. Remove -.900V signal.
   - Leave 5K potentiometer output connected to PIN 25 and set to +10.000V.
9. **CHECK WOBBULATOR GAIN**
   - Open S4 (PIN 12). Close S3 (PIN 19). All other switches with the exception of S6 (PIN 25) should be closed.
   - Apply a +8.960V signal to PIN 12. Check that the LVG output voltage at TP6 is -10.000V ± 0.200 V.
   - Remove +8.960V signal and apply a -8.960V signal to PIN 12. Check that the LVG output voltage at TP6 is +10.000V ± 0.200V. Remove -8.960V signal.
   - Remove 5K potentiometer output connected to PIN 25.
10. **TEST ACCELERATION AMPLIFIER**
    - Open S2 (PIN 15). Close S4 (PIN 12). Leave S6 open (PIN 25). All other switches should be closed. Place a jumper across capacitors C5, C6, and C7.
    - Jumper 5K potentiometer output to PIN 15 and set to +10.000V, forcing the speed amplifier to go into negative saturation. Check the voltage at TP7 to insure that the speed amplifier is in negative saturation.
    - Check the voltage at TP4 is approx. +2.000 V insuring that the acceleration amplifier is not saturated.
    - Check LVG output voltage at TP6; the output should be zero volts.

11. **CHECK ACCERERATION REFERENCE GAIN**
    - Apply a -5.000V signal to PIN 25 and check that the LVG output at TP6 is approx. +5.000 V.
    - Remove -5.000V signal and apply a +5.000V signal. Check that the LVG output voltage at TP6 is now approx. -5.000V.
12. **CHECK PRIMARY SPEED SIGNAL GAIN**
    - Open S1 (PIN 26). Close S6 (PIN 25). Leave S2 connected to pot (PIN 15). All other switches should be closed. Jumpers should still be across C5, C6, and C7.
    - Apply a -3.330V signal to PIN 26. Check that the LVG voltage at TP6 is approx. +10.000V.
    - Remove -3.330V signal and apply a +3.330V signal. Check that the LVG output voltage at TP6 is now approx. -10.000V.
    - Remove jumper from across C5 and observe the time required for the LVG output at TP6 to decay to zero volts. Should be approx. 3 seconds.
    - Remove +3.330V signal from PIN 26. Jumper C5 and R21.
    - Apply a -0.100V signal to PIN 26. Remove jumper from C7 and observe that the LVG output at TP6 integrates up to +10.000V in approx. 10 seconds.
    - Remove -0.100V signal from PIN 26. Remove Jumpers from C5 and R21.
13. **CHECK BACKUP SPEED SIGNAL GAIN**
    - Open S5 (PIN18). Close S1 (PIN26). Leave S2 connected to Pot (PIN 15). All other switches should be closed. Replace jumper across C7.
    - Apply a -3.330V signal to PIN 18. Check that the LVG voltage at TP6 is approx. +10.000V.
    - Remove -3.330V signal and apply a +3.330 V signal. Check that the LVG output voltage at TP6 is now approx. -10.000V.
    - Remove jumper from across C6 and observe the time required for the LVG output at TP6 to decay to zero volts. Should be approx. 3 seconds.
    - Remove +3.330V signal from PIN 18. Jumper C6 and R21.

- Apply a -0.100V signal to PIN 18. Remove jumper from C7 and observe that the LVG output at TP6 integrates up to +10.000V in approx. 10 seconds.
- Remove -0.100V signal from PIN 18. Remove Jumpers from C5, C6, C7 and R21.

14. **CHECK FREQUENCY COMPENSATION NETWORKS**

- Disconnect all leads to the test fixture, including power. (Recommend using a separate breakout fixture if testing multiple cards).
- Apply a 20Hz sine wave into PIN 15.
- Set amplitude to about 2.0VRMS at the C1, R24 junction.
- Using the frequency selection dial on frequency generator, raise the frequency until the C1, R24 junction equals about 1.41VRMS.
- The frequency should now read between 55Hz and 94Hz.
- Remove all leads.
- Apply a 6Hz sine wave into PIN 19.
- Set amplitude to about 2.0VRMS at the C2, R25 junction.
- Using the frequency selection dial on frequency generator, raise the frequency until the C2, R25 junction equals about 1.41VRMS.
- The frequency should now read between 9Hz and 14Hz.
- Remove all leads.
- Apply a 20Hz sine wave into PIN 12.
- Set amplitude to about 2.0 VRMS at the C3, R6 junction.
- Using the frequency selection dial on frequency generator, raise the frequency until the C3, R6 junction equals about 1.41VRMS.
- The frequency should now read between 59Hz and 90Hz.

15. Post Testing Burn-in Required _X_ Yes ___ No

Note: All MARK I, II, & III Turbine related cards require a post testing burn-in of 100 hours.

- Apply BUS or Operational power to the card for a period of 100 hours.
- Re-test card while warm using the above procedure.

16. ***TEST COMPLETE ***

7. Notes

7.1 See next page for test setup.

8. Attachments

8.1