

REV NO. 0

P3K-AL-0450-A01

CONT ON SHEET 2 SH NO. 1

TITLE

TEST INSTRUCTIONS FOR LOAD RATE/LOAD SET LIMIT LOGIC
CIRCUIT BOARD 1L2-E002 (ASSEMBLY DRAWING 118D1327 G1)
FIRST MADE FOR EHC MARK II

REVISIONS

I. SCOPE

This instruction outlines the test specifications for circuit board 1L2-E002 (BOARD ASSEMBLY DRAWING - 118D1327 G1) (SCHEMATIC - 117D9986)

II. CIRCUIT DESCRIPTION

This circuit depending on its input switching signals activates the appropriate analog to logic relays which in turn apply the suitable loading rate limits to the load reference amplifier.

The circuit is able to give five output commands:

1/2% Loading Rate: 24V at Pin 15

1% Loading Rate: 24V at Pin 14

3% Loading Rate: 24V at Pin 8

5 to 10% Loading Rate: 0V at Pin 20

Very High Loading Rate: 24V at Pin 32

The first four commands are selected through pushbuttons which apply momentarily 24V to pin 22, 5, 7, and 27. The first three pushbuttons are powered from the board itself (Pin 26). Depressing any pushbutton imposes the corresponding command and clears the previous one. The pushbuttons become inoperative and a 10% loading rate command is given in remote auto or remote operation modes (24V at Pin 28.)

When the main circuit breaker is open (24V at Pin 31) the very high loading rate command is given (24V at Pin 32) and the pushbuttons become inoperative. (A 10% rate command is simultaneously given but this is overridden by the very high rate command inside the analog circuit).

III. CIRCUIT SPECIFICATIONS

1. Before coating the board, each of the 34 diodes should be checked to insure that redundancy is effective.
2. Connect ground to pin 40 and +24 VDC to Pin 38. Connect 24V 20 MA lamps to pins 15, 14, 8, 20, 32, 28, 26, 2, 3, 4, 21, 23, 25.

The logic and path continuity should conform with the following table:

- 273-2
- 273-12
- 273-138
- 273-221
- 273-227
- 273-71
- PRINTS TO:

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0: OV or lamp off 1: 24V or lamp on 1*: reduced voltage due to the 68.1 ohms resistors								REVISIONS												
<div> <div>INPUTS AT PINS</div> <div> <div>22</div> <div>5</div> <div>7</div> <div>27</div> <div>28</div> <div>31</div> <div>9</div> <div>12</div> <div>6</div> <div>15</div> <div>14</div> <div>8</div> <div>20</div> <div>32</div> <div>26</div> <div>2</div> <div>3</div> <div>4</div> <div>21</div> <div>23</div> <div>25</div> </div> </div> <div>CORRECT OUTPUTS AT PINS</div>																				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0</

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TEST INSTRUCTION FOR LOAD RATE/LOAD
SET LIMIT LOGIC

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SH NO.

3

FIRST MADE FOR

MK II

REVISIONS

TEST INSTRUCTIONS

1L2-E002

Assembly
Schematic

118D1327
117D9986

PROCEDURE:

- A. Refer to P3K-AL-0494-A02 for test circuits, equipment list, and set up instructions.
- B. Table A provides the step by step procedure to follow in testing this circuit.
- C. Table B provides a step by step description of input voltages (to use as a troubleshooting aid).

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TEST INSTRUCTION FOR LOAD RATE/
LOAD SET LIMIT LOGIC

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ACTION	VOLTAGE AT PINS										REVISIONS
	2	3	4	5	7	8	14	15	20	21	
STEP 1 INIT COND											
STEP 2 APP P 6	B	B	B							B	
STEP 3 REM P 6											
STEP 4 APP P 9											
STEP 5 REM P 9											
STEP 6 APP P 12											
STEP 7 REM P 12											
STEP 8 APP P 38										B	
STEP 9 APP P 31										Ø	
STEP 10 REM P 31										B	
STEP 11 APP P 28										Ø	
STEP 12 REM P 28										B	
STEP 13 APP P 15	E				Ø	Ø			A	Ø	
STEP 14 REM P 15	E				Ø	Ø			A	Ø	
STEP 15 APP P 27	Ø				Ø	Ø			Ø	B	
STEP 16 REM P 27	Ø				Ø	Ø			Ø	B	
STEP 17 APP P 15											
STEP 18 REM P 15											
STEP 19 APP P 14											
STEP 20 REM P 14											
STEP 21 APP P 27											
STEP 22 REM P 27											
STEP 23 APP P 15											
STEP 24 REM P 15											
STEP 25 APP P 8											

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TITLE
TEST INSTRUCTION FOR LOAD RATE/
LOAD SET LIMIT LOGIC

FIRST MADE FOR MK II

ACTION	VOLTAGE AT PINS										REVISIONS
	2	3	4	5	7	8	14	15	20	21	
STEP 26 REM P 8											
STEP 27 APP P 27											
STEP 28 REM P 27											
STEP 29 APP P 14		E		C		Ø		Ø	A	Ø	
STEP 30 REM P 14		E		C		Ø		Ø	A	Ø	
STEP 31 APP P 27		Ø		Ø		Ø		Ø	Ø	B	
STEP 32 REM P 27		Ø		Ø		Ø		Ø	Ø	B	
STEP 33 APP P 14				C							
STEP 34 REM P 14				C							
STEP 35 APP P 15				Ø							
STEP 36 REM P 15				Ø							
STEP 37 APP P 27											
STEP 38 REM P 27											
STEP 39 APP P 14				C							
STEP 40 REM P 14				C							
STEP 41 APP P 8				Ø							
STEP 42 REM P 8				Ø							
STEP 43 APP P 27											
STEP 44 REM P 27											
STEP 45 APP P 8			E		C		Ø	Ø	A	Ø	
STEP 46 REM P 8			E		C		Ø	Ø	A	Ø	
STEP 47 APP P 27			Ø		Ø		Ø	Ø	Ø	B	
STEP 48 REM P 27			Ø		Ø		Ø	Ø	Ø	B	
STEP 49 APP P 8					C						
STEP 50 REM P 8					C						

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TITLE

TEST INSTRUCTION FOR LOAD RATE/
LOAD SET LIMIT LOGIC

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SH NO.

6

FIRST MADE FOR

MK II

ACTION

VOLTAGE AT PINS

REVISIONS

2	3	4	5	7	8	14	15	20	21
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STEP 31 APP P 15

STEP 52 REM P 15

STEP 53 APP P 27

STEP 54 REM P 27

STEP 55 APP P 8

STEP 56 REM P 8

STEP 57 APP P 14

STEP 58 REM P 14

STEP 59 APP P 27

STEP 60 REM P 27

STEP 61 REM P 38

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C

C

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TITLE
TEST INSTRUCTION FOR LOAD RATE/LOAD
SET LIMIT LOGIC

FIRST MADE FOR MK II

ACTION	VOLTAGE AT PINS										REVISIONS
	22	23	25	26	32						
STEP 1 INIT COND											
STEP 2 APP P 6		B	B								
STEP 3 REM P 6											
STEP 4 APP P 9			B								
STEP 5 REM P 9											
STEP 6 APP P 12		B									
STEP 7 REM P 12											
STEP 6 APP P 38				A							
STEP 9 APP P 31				Ø	C						
STEP 10 REM P 31				A	Ø						
STEP 11 APP P 28				Ø	C						
STEP 12 REM P 28				A	Ø						
STEP 13 APP P 15	C										
STEP 14 REM P 15	C										
STEP 15 APP P 27	Ø										
STEP 16 REM P 27	Ø										
STEP 17 APP P 15	C										
STEP 18 REM P 15	C										
STEP 19 APP P 14	Ø										
STEP 20 REM P 14	Ø										
STEP 21 APP P 27											
STEP 22 REM P 27											
STEP 23 APP P 15	C										
STEP 24 REM P 15	C										
STEP 25 APP P 8	Ø										

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TITLE
 TEST INSTRUCTION FOR LOAD RATE/LOAD
 SET LIMIT LOGIC
 FIRST MADE FOR MK II

ACTION	VOLTAGE AT PINS										REVISIONS
	22	23	25	26	32						
STEP 26 REM P 8	Ø										
STEP 27 APP P 27											
STEP 28 REM P 27											
STEP 29 APP P 14											
STEP 30 REM P 14											
STEP 31 APP P 27											
STEP 32 REM P 27											
STEP 33 APP P 14											
STEP 34 REM P 14											
STEP 35 APP P 15											
STEP 36 REM P 15											
STEP 37 APP P 27											
STEP 38 REM P 27											
STEP 39 APP P 14											
STEP 40 REM P 14											
STEP 41 APP P 8											
STEP 42 REM P 8											
STEP 43 APP P 27											
STEP 44 REM P 27											
STEP 45 APP P 8											
STEP 46 REM P 8											
STEP 47 APP P 27											
STEP 48 REM P 27											
STEP 49 APP P 8											
STEP 50 REM P 8											

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TEST INSTRUCTION FOR LOAD RATE/LOAD
SET LIMIT LOGIC

FIRST MADE FOR MK II

ACTION

VOLTAGE AT PINS

REVISIONS

22

23

25

26

32

STEP 51 APP P 15

STEP 52 REM P 15

STEP 53 APP P 27

STEP 54 REM P 27

STEP 55 APP P 8

STEP 56 REM P 8

STEP 57 APP P 14

STEP 58 REM P 14

STEP 59 APP P 27

STEP 60 REM P 27

STEP 61 REM P 38

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TITLE
TEST INSTRUCTION FOR LOAD RATE/LOAD
SET LIMIT LOGIC

FIRST MADE FOR MK II

ACTION	INPUT AT PINS										REVISIONS
	6	8	9	12	14	15	27	28	31	38	
STEP 1											
STEP 2 APP P 6	X										
STEP 3 REM P 6											
STEP 4 APP P 9			X								
STEP 5 REM P 9											
STEP 6 APP P 12				X							
STEP 7 REM P 12											
STEP 8 APP P 38										X	
STEP 9 APP P 31									X	X	
STEP 10 REM P 31										X	
STEP 11 APP P 28								X		X	
STEP 12 REM P 28										X	
STEP 13 APP P 15						X				X	
STEP 14 REM P 15										X	
STEP 15 APP P 27							X			X	
STEP 16 REM P 27										X	
STEP 17 APP P 15						X				X	
STEP 18 REM P 15										X	
STEP 19 APP P 14					X					X	
STEP 20 REM P 14										X	
STEP 21 APP P 27							X			X	
STEP 22 REM P 27										X	
STEP 23 APP P 15						X				X	
STEP 24 REM P 15										X	
STEP 25 APP P 8		X								X	
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TEST INSTRUCTION FOR LOAD RATE/LOAD
SET LIMIT LOGIC

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SH NO. 11

FIRST MADE FOR MK II

ACTION

INPUT AT PINS

REVISIONS

6	8	9	12	14	15	27	28	31	38
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STEP 26 REM P 8									X
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STEP 27 APP P 27						X			
------------------	--	--	--	--	--	---	--	--	--

STEP 28 REM P 27									X
------------------	--	--	--	--	--	--	--	--	---

STEP 29 APP P 14					X				X
------------------	--	--	--	--	---	--	--	--	---

STEP 30 REM P 14									X
------------------	--	--	--	--	--	--	--	--	---

STEP 31 APP P 27						X			X
------------------	--	--	--	--	--	---	--	--	---

STEP 32 REM P 27									X
------------------	--	--	--	--	--	--	--	--	---

STEP 33 APP P 14					X				X
------------------	--	--	--	--	---	--	--	--	---

STEP 34 REM P 14									X
------------------	--	--	--	--	--	--	--	--	---

STEP 35 APP P 15						X			X
------------------	--	--	--	--	--	---	--	--	---

STEP 36 REM P 15									X
------------------	--	--	--	--	--	--	--	--	---

STEP 37 APP P 27							X		X
------------------	--	--	--	--	--	--	---	--	---

STEP 38 REM P 27									X
------------------	--	--	--	--	--	--	--	--	---

STEP 39 APP P 14					X				X
------------------	--	--	--	--	---	--	--	--	---

STEP 40 REM P 14									X
------------------	--	--	--	--	--	--	--	--	---

STEP 41 APP P 8		X							X
-----------------	--	---	--	--	--	--	--	--	---

STEP 42 REM P 8									X
-----------------	--	--	--	--	--	--	--	--	---

STEP 43 APP P 27							X		X
------------------	--	--	--	--	--	--	---	--	---

STEP 44 REM P 27									X
------------------	--	--	--	--	--	--	--	--	---

STEP 45 APP P 8		X							X
-----------------	--	---	--	--	--	--	--	--	---

STEP 46 REM P 8									X
-----------------	--	--	--	--	--	--	--	--	---

STEP 47 APP P 27							X		X
------------------	--	--	--	--	--	--	---	--	---

STEP 48 REM P 27									X
------------------	--	--	--	--	--	--	--	--	---

STEP 49 APP P 8		X							X
-----------------	--	---	--	--	--	--	--	--	---

STEP 50 REM P 8									X
-----------------	--	--	--	--	--	--	--	--	---

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TITLE

TEST INSTRUCTION FOR LOAD RATE/LOAD
SET LIMIT LOGIC

FIRST MADE FOR MK II

ACTION

INPUT AT PINS

REVISIONS

6

8

9

12

14

15

27

28

31

38

STEP 51 APP P 15

X

STEP 52 REM P 15

STEP 53 APP P 27

X

STEP 54 REM P 27

STEP 55 APP P 8

x

STEP 56 REM P 8

STEP 57 APP P 14

x

STEP 58 REM P 14

STEP 59 APP P 27

X

STEP 60 REM P 27

STEP 61 REM P 38

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TITLE

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TEST INSTRUCTIONS FOR LOAD RATE/LOAD SET LIMIT LOGIC
CIRCUIT BOARD 1L2-E002 (ASSEMBLY DRAWING 118D1327 G1)
FIRST MADE FOR EHC MARK II

CONT ON SHEET — SH NO. 13

REVISIONS

PREPARED BY

M.J. Sindoni

DATE

4/24/75

M.J. Sindoni
EHC DESIGN ENGINEERING

APPROVED BY

P.C. Callan

DATE

5-22-76

P.C. Callan - MANAGER
EHC DESIGN ENGINEERING

TEST PROCEDURE

PREPARED BY

C. Bugg

DATE

5/20/76

C. Bugg
EHC TEST ENGINEER

TEST PROCEDURE

APPROVED BY

M.J. Sindoni

DATE

5/20/76

M.J. Sindoni
EHC DESIGN ENGINEERING

PRINTS TO

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