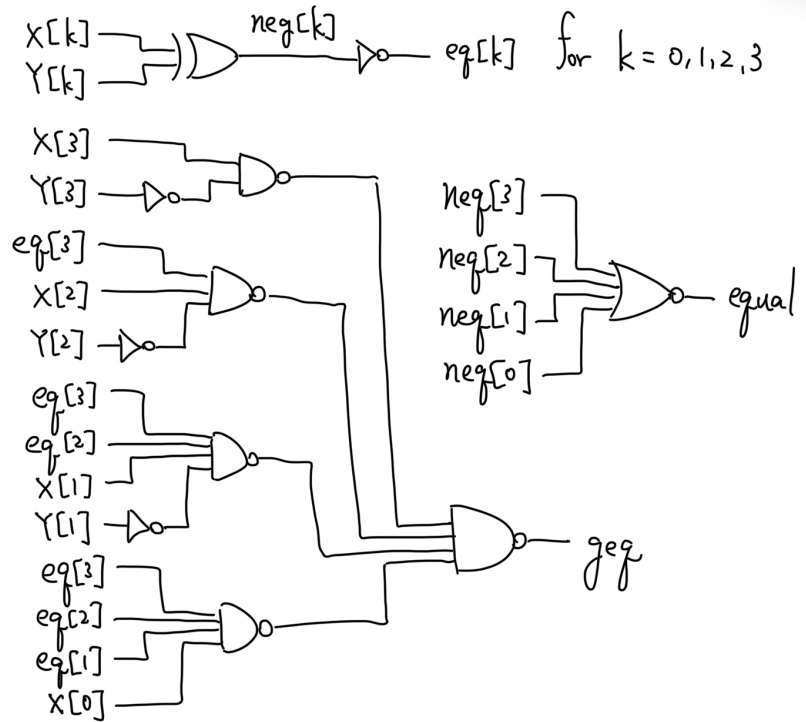# IC Design Homework 3
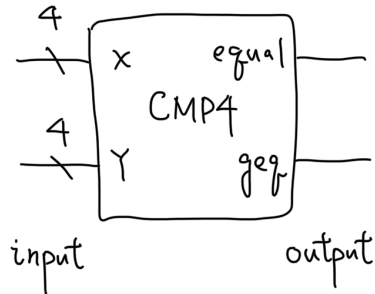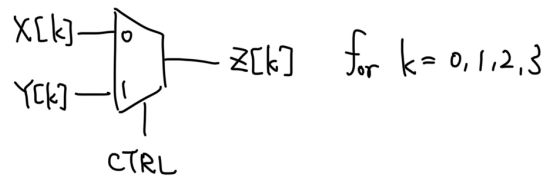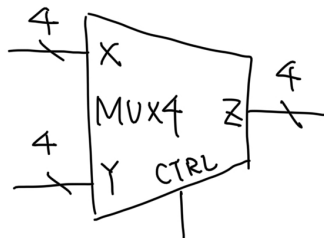
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1. Circuit Diagram.

(1) CMP4
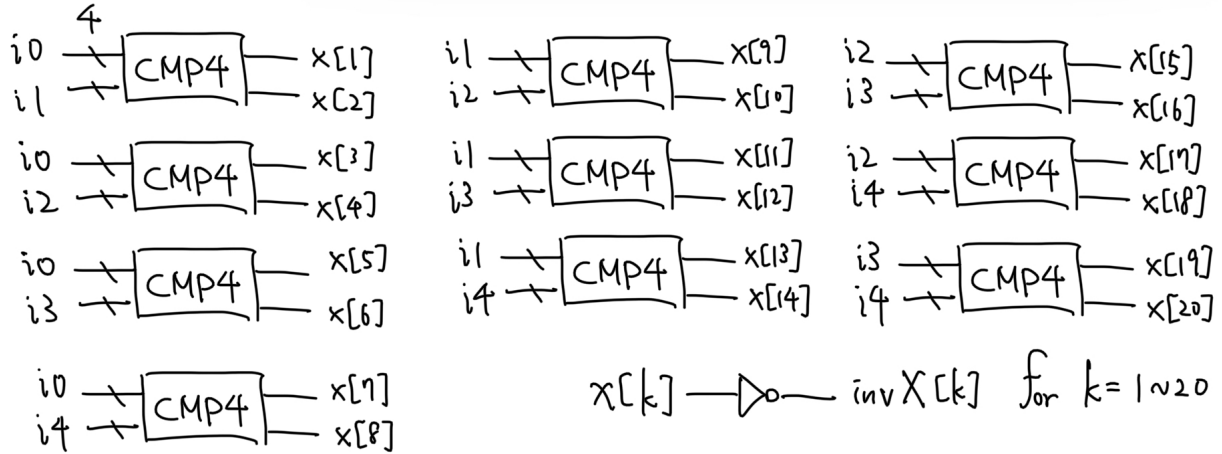

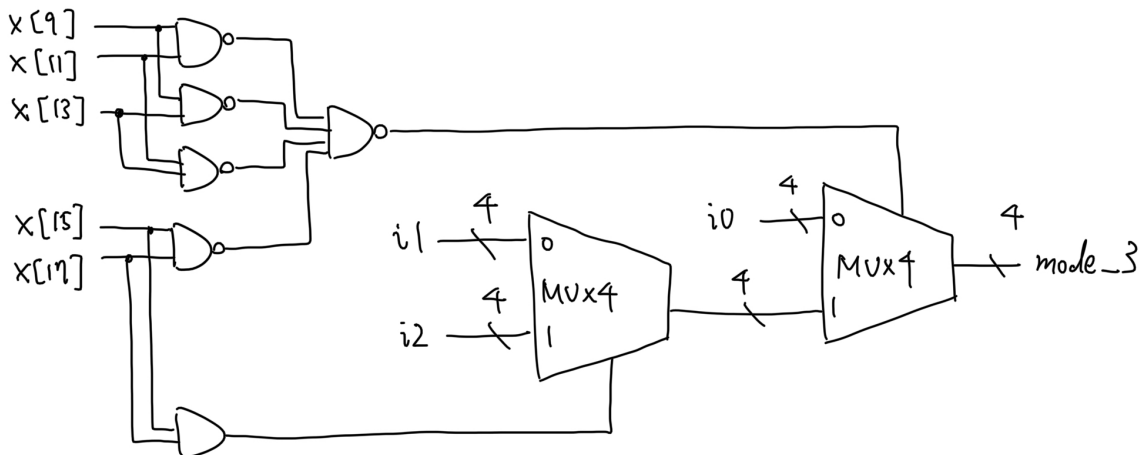(2) MUX4

(3) Pairwise compare the five inputs.

$$x[k] \longrightarrow\!\!\!\triangleright\!\!\circ\!\!\!- \text{inv } X[k] \quad \text{for } k=1\sim20$$

$x[1] = 1$	$i0 = i1$	$x[11] = 1$	$i1 = i3$
$x[2] = 1$	$i0 \geq i1$	$x[12] = 1$	$i1 \geq i3$
$x[3] = 1$	$i0 = i2$	$x[13] = 1$	$i1 = i4$
$x[4] = 1$	$i0 \geq i2$	$x[14] = 1$	$i1 \geq i4$
$x[5] = 1$	$i0 = i3$	$x[15] = 1$	$i2 = i3$
$x[6] = 1$	$i0 \geq i3$	$x[16] = 1$	$i2 \geq i3$
$x[7] = 1$	$i0 = i4$	$x[17] = 1$	$i2 = i4$
$x[8] = 1$	$i0 \geq i4$	$x[18] = 1$	$i2 \geq i4$
$x[9] = 1$	$i1 = i2$	$x[19] = 1$	$i3 = i4$
$x[10] = 1$	$i1 \geq i2$	$x[20] = 1$	$i3 \geq i4$

(4) Case i: more than three inputs are the same
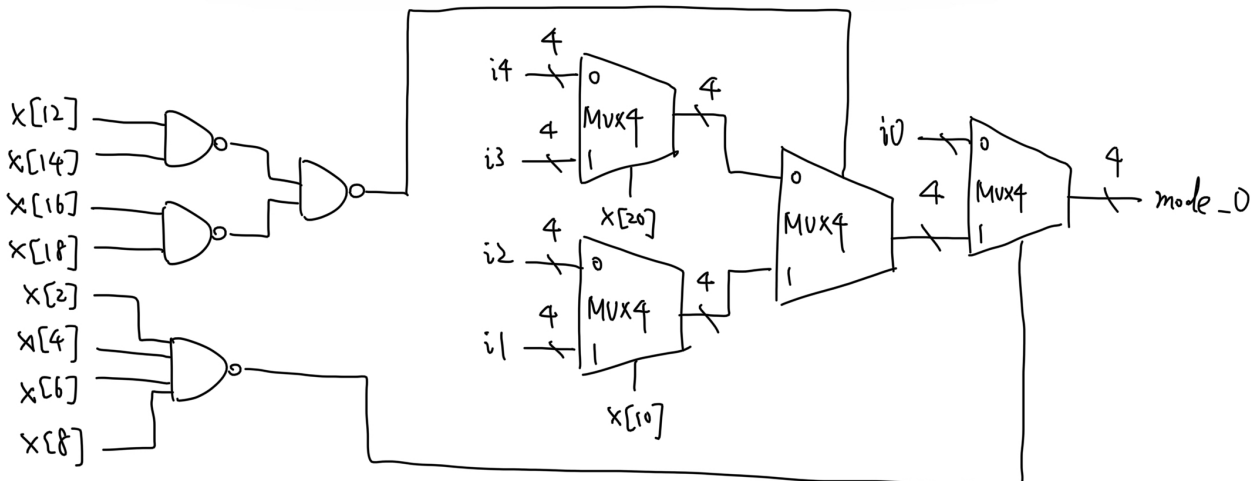   (e.g. 3,4,5,3,3; 0,2,2,0,2; 14,14,5,14,14; 1,1,1,1,1)

(5) Case ii: two but no more than three inputs are the same (e.g. 3,7,14,14,4; 10,10,1,1,7)
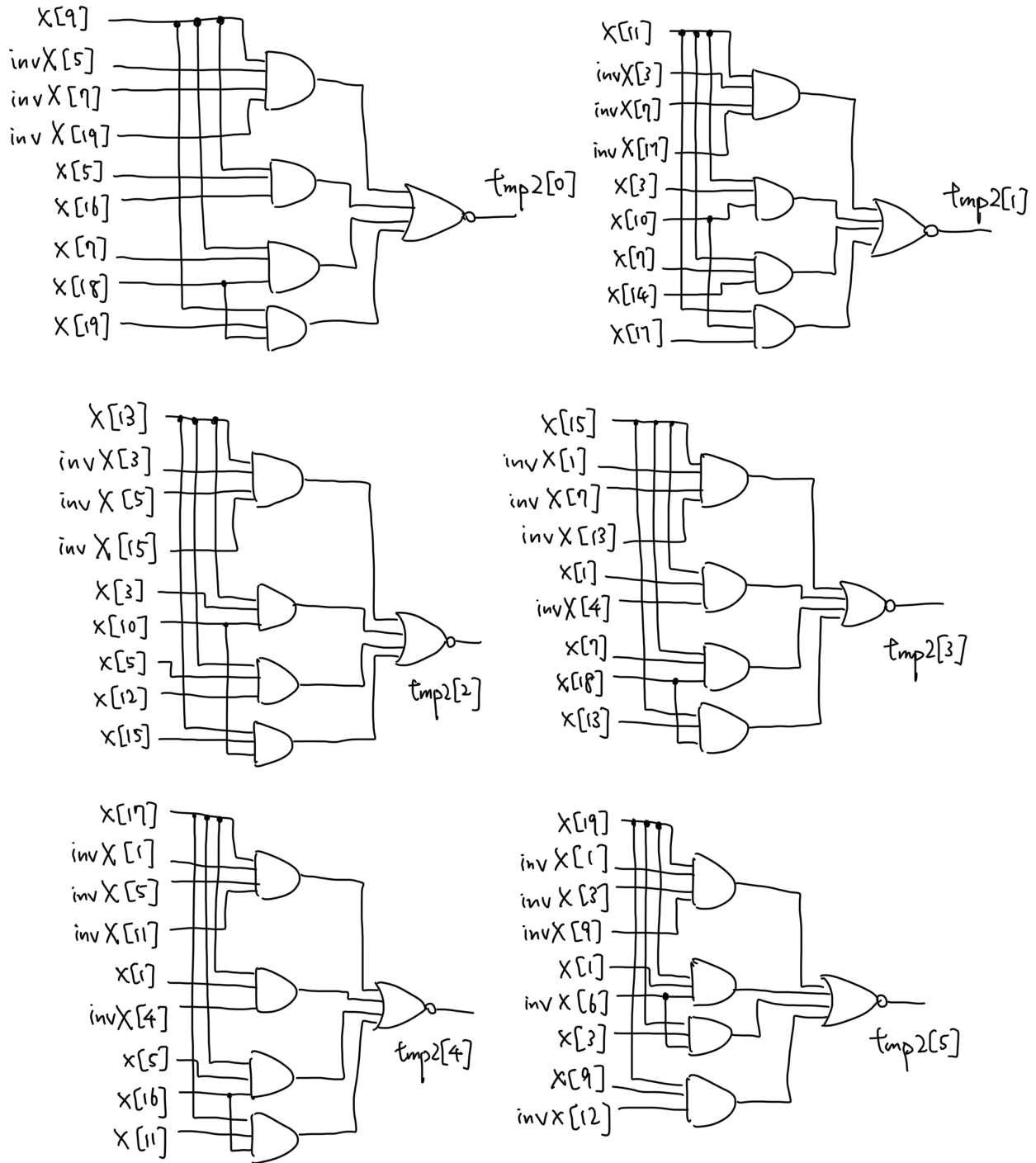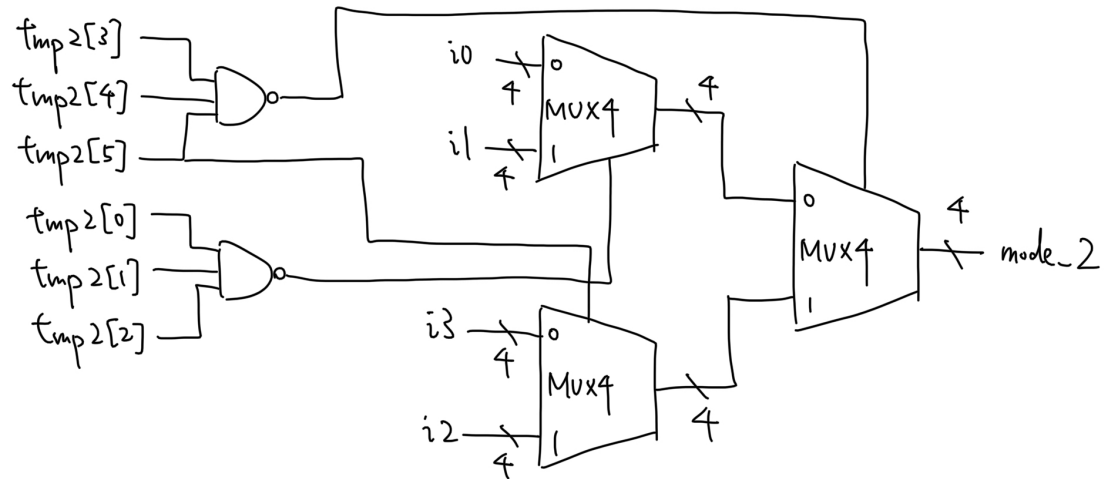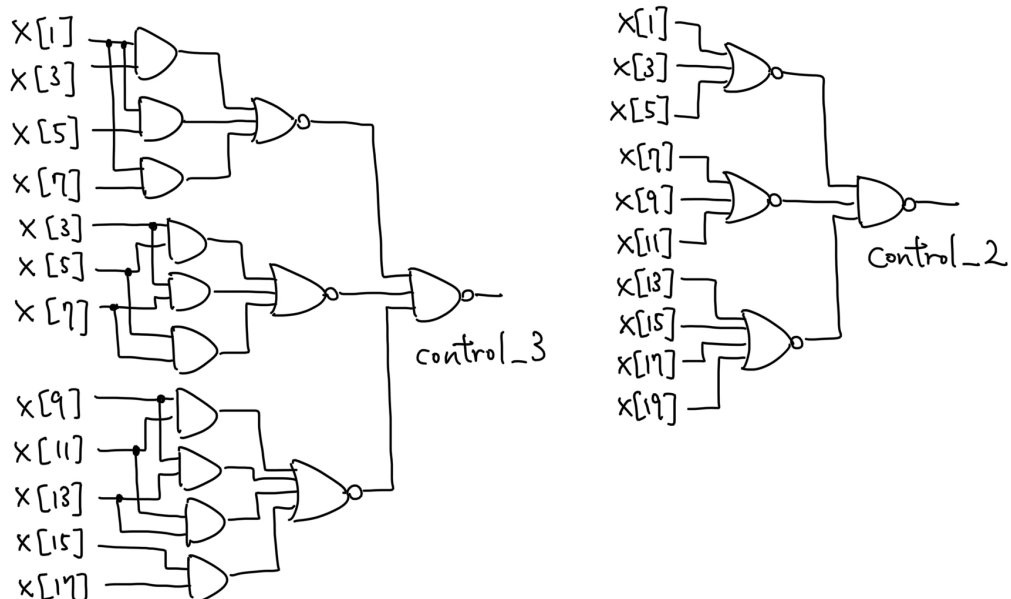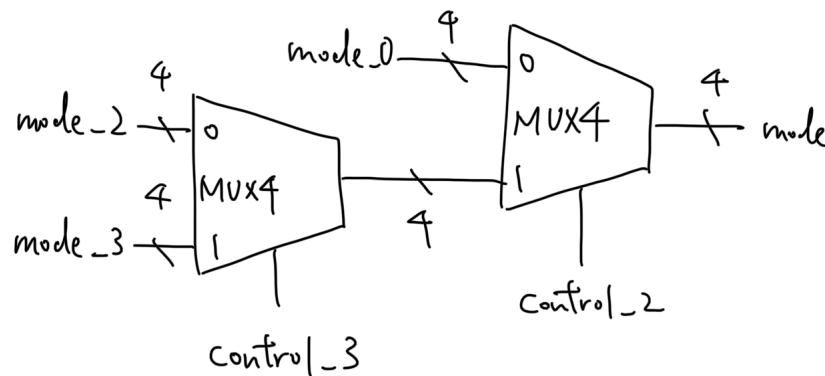
(6) Case iii: all five inputs are different (e.g. 10,5,4,7,3; 9;2;3;15;0)

(7) Generate control signals to determine which result (case i, ii or iii) should be the output.

(8) Output the result.

2. Discussion.

There are three cases:

i. At least three inputs are identical.
   If no more than three inputs among $i1$, $i2$, $i3$, $i4$ are identical, output $i0$.
   If $i2$, $i3$, $i4$ are the same, output $i2$.
   In all other situations, output $i1$.

ii. Two but no more than three inputs are identical.
   The condition for a pair of numbers to be the mode is that they have the same value, and other three numbers are different from one another, or there is a pair among the other three numbers but they are smaller. For example, the condition for $i3$, $i4$ to be the mode is: ($i3 = i4$ and $i0 \neq i1$ and $i0 \neq i2$ and $i1 \neq i2$) or ($i3 = i4$ and $i0 = i1$ and $i3 > i0$) or ($i3 = i4$ and $i0 = i2$ and $i3 > i2$) or ($i3 = i4$ and $i1 = i2$ and $i3 > i1$).

iii. All five inputs are different numbers. Just choose the largest input. For example, the condition for $i1$ to be the mode is: $i1 > i0$ and $i1 > i2$ and $i1 > i3$ $i1 > i4$.

When an input combination comes, calculate the output values for these three cases based on the logic circuit, and then use control signals (control_2 and control_3) to determine which case happens and output the corresponding result. If we don't handle these three cases separately, the control signals for multiplexers (for determining which of the five input numbers appears at output) are becoming more complex, hence leading to more stages of logic gates and lengthening the critical path.