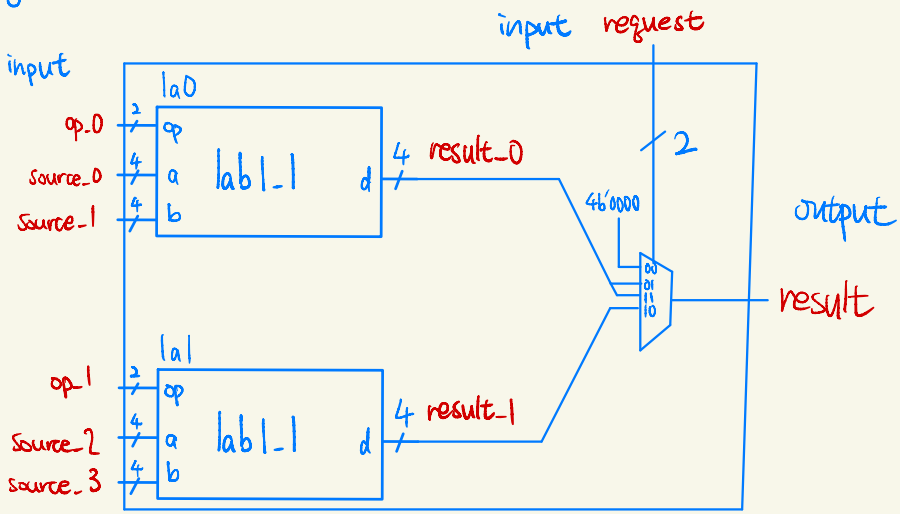
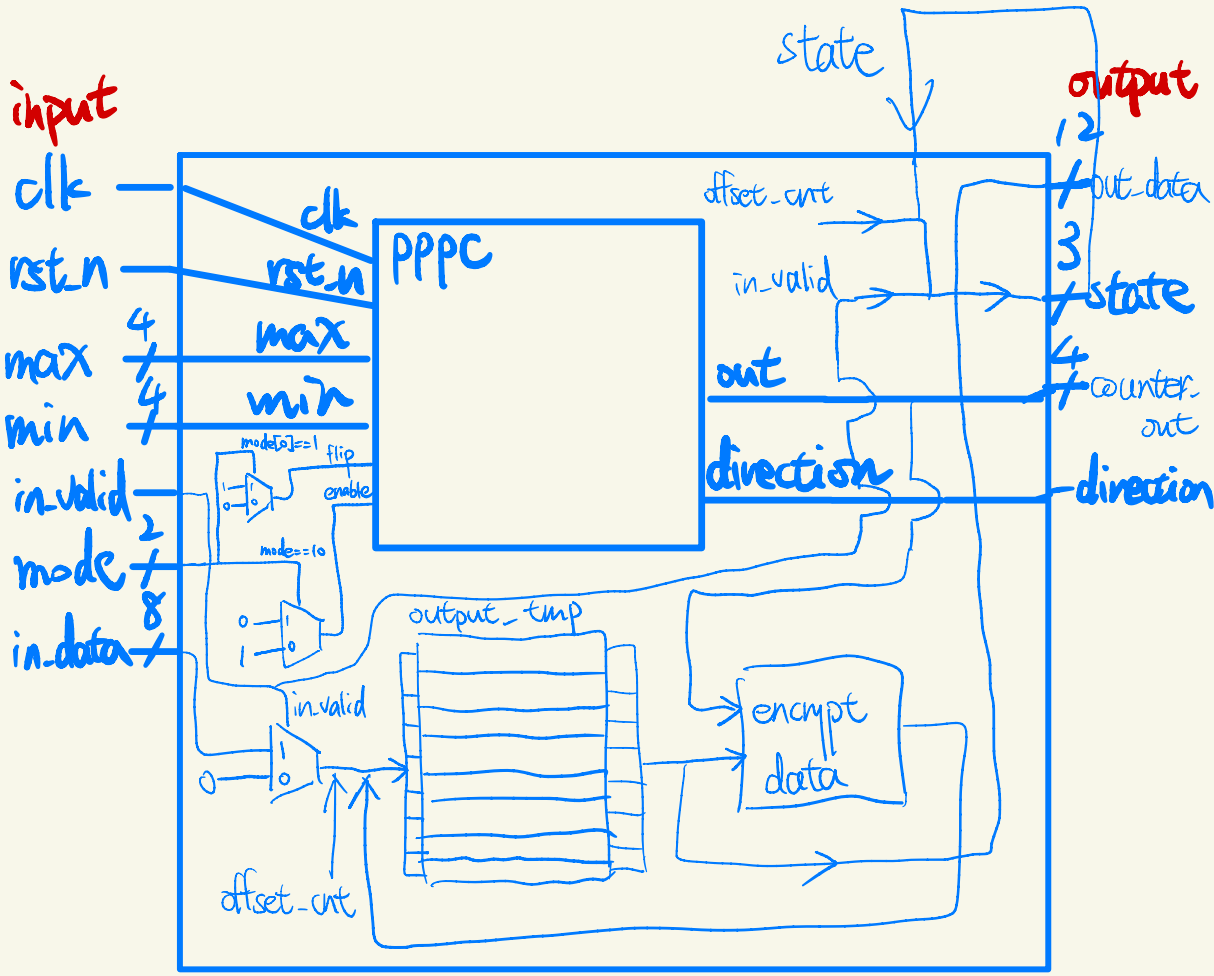
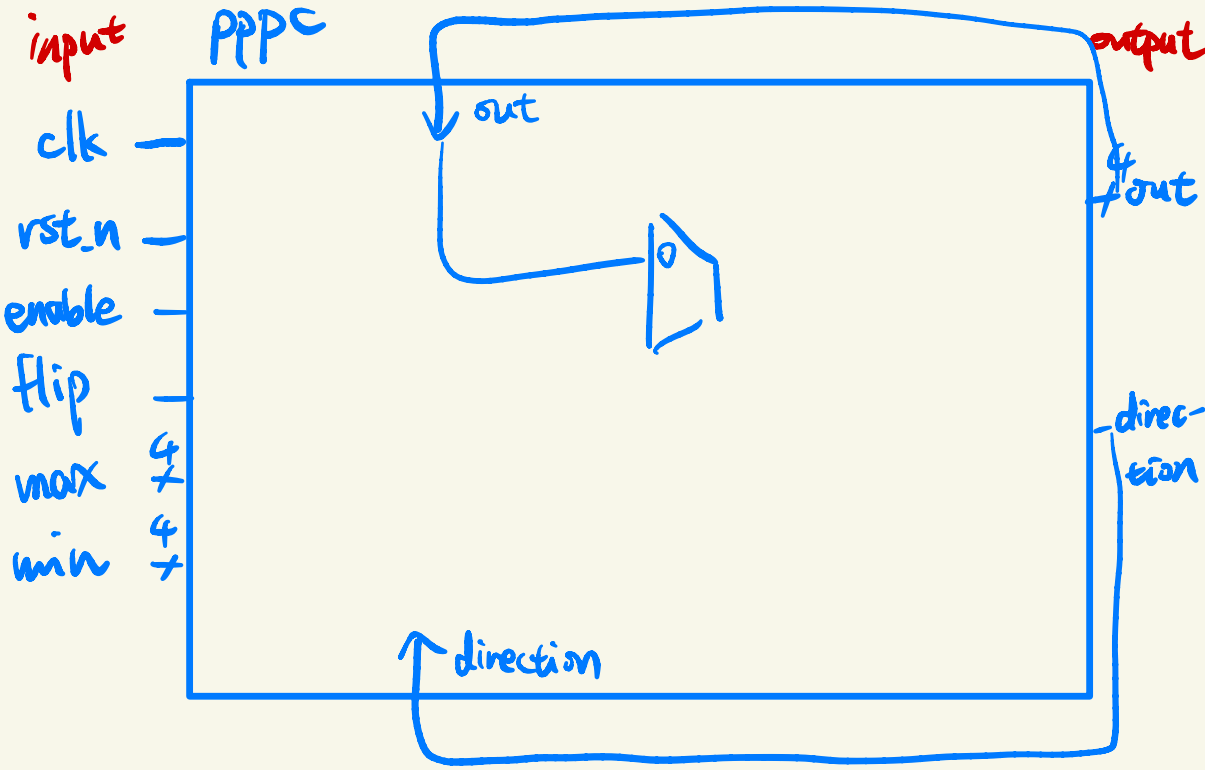
Lab 1

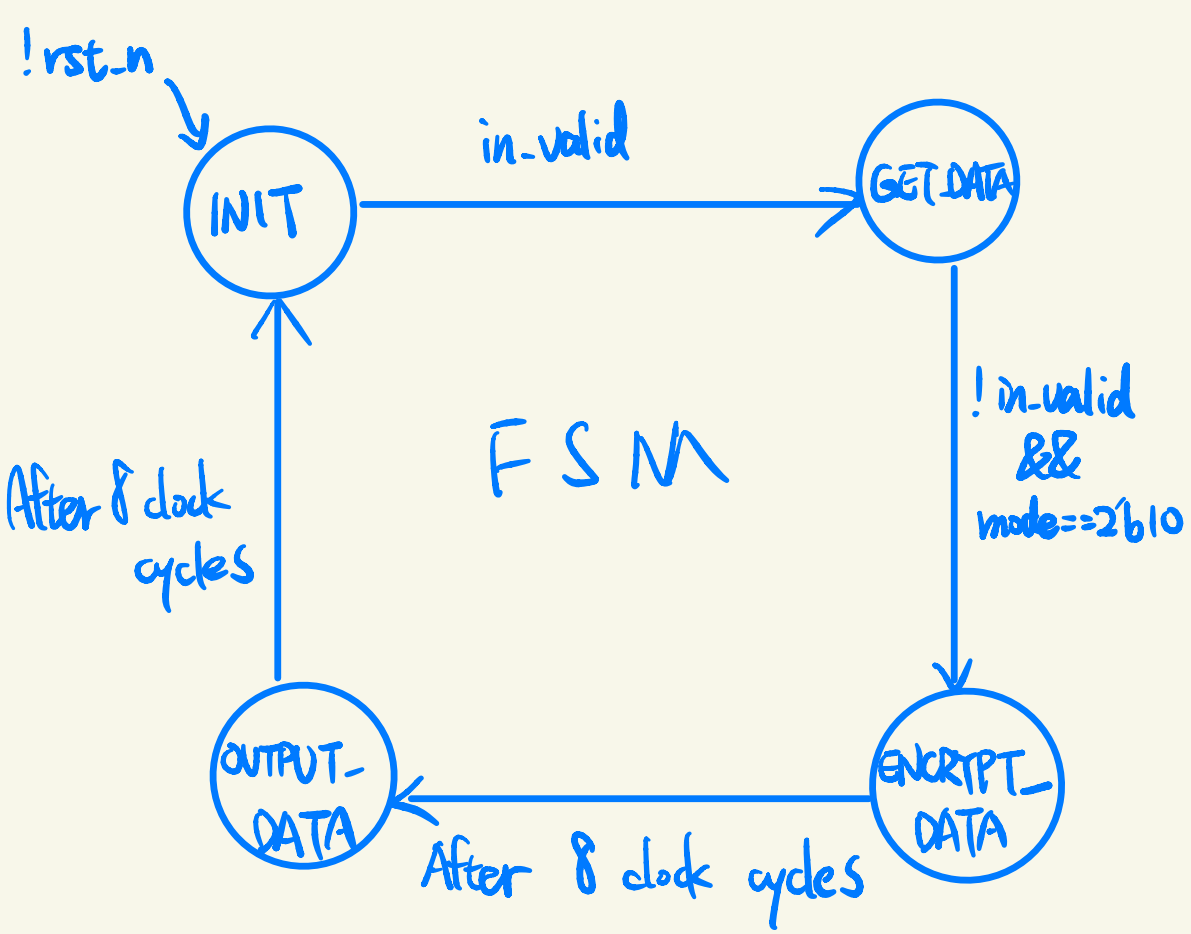
The block diagram of lab1-2



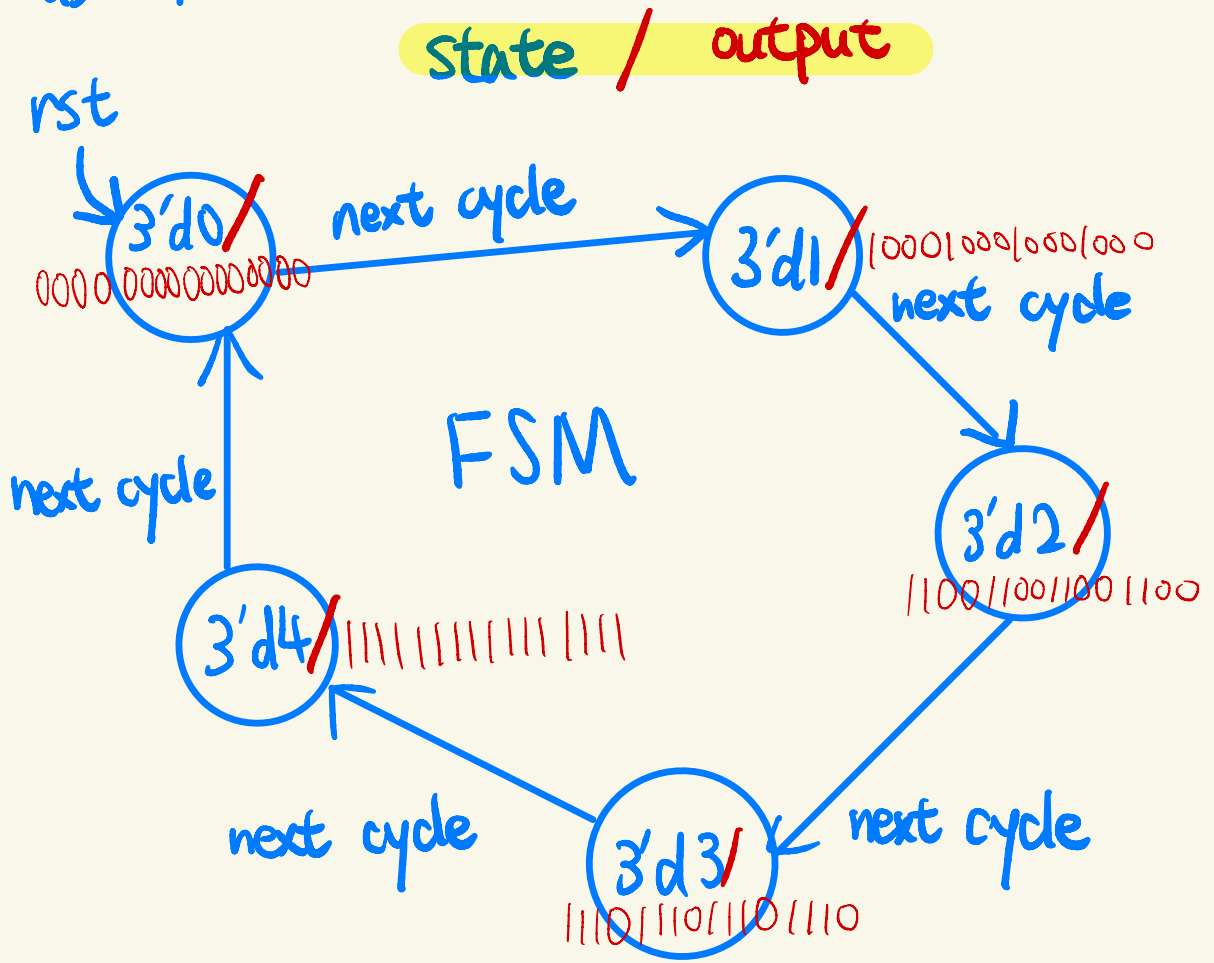
Lab 2


input
clk
rst_n
max
4
min
4
in_valid
mode
2
in_data
8
PPPC
clk
rst_n
max
min
flip
enable
mode[0]==1
mode==10
output_tmp
in_valid
offset_cnt
encrypt data
state
offset_cnt
in_valid
out
direction
output
12
out_data
3
state
4
counter_out
direction


input
PPPC
output
clk
rst_n
enable
flip
max
4
min
4
out
0
4
out
direc-
tion
direction

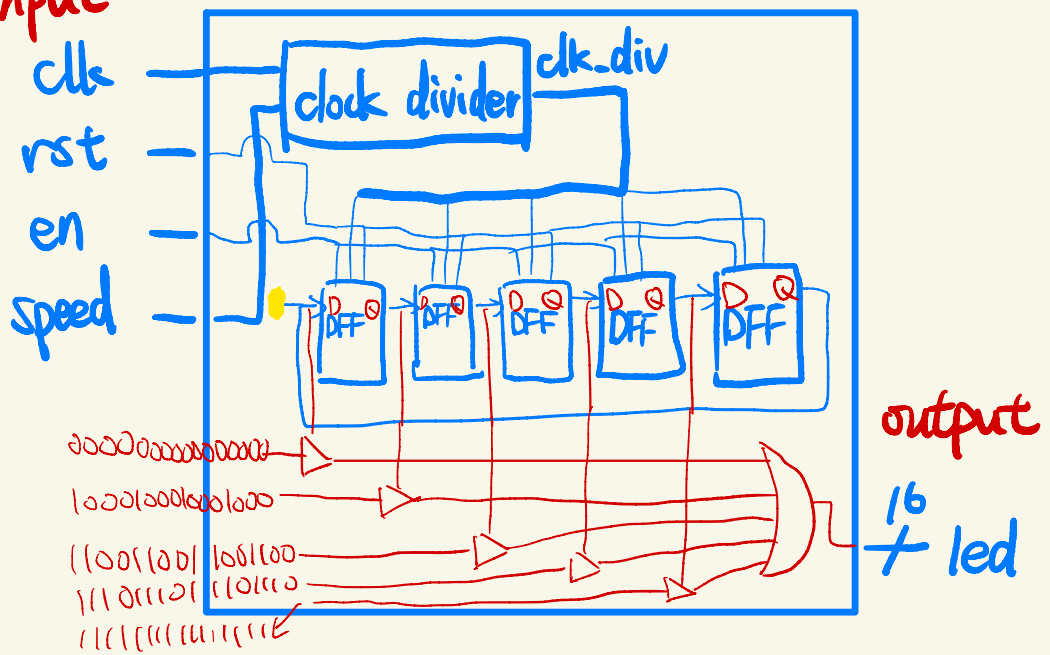

!rst_n
INIT
in_valid
GET_DATA
!in_valid
&&
mode==2'b10
ENCRYPT_
DATA
After 8 clock cycles
OUTPUT_
DATA
After 8 clock cycles
FSM

Lab3-1

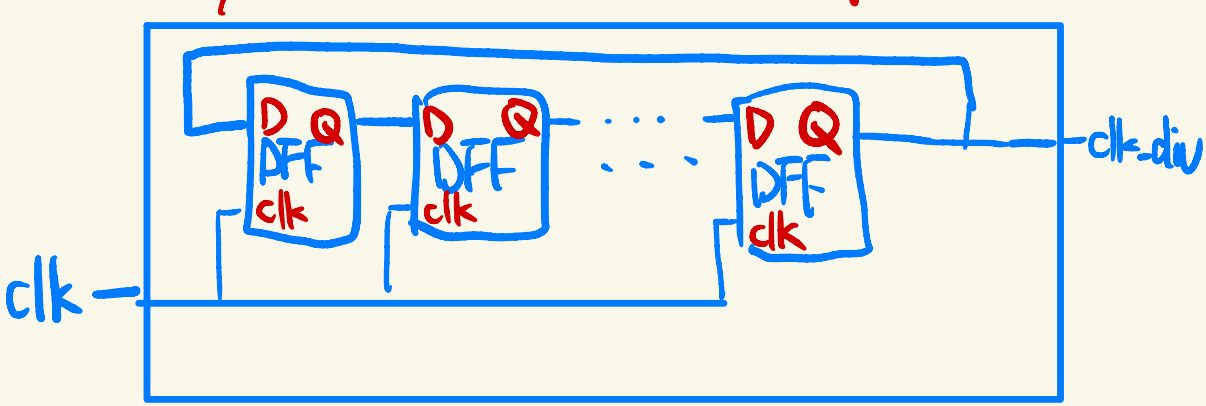

State / output
rst
3'd0
next cycle
3'd1
next cycle
FSM
3'd2
next cycle
3'd4
next cycle
3'd3
next cycle

Lab3_1

input



For clock divider total 2^n DFFs



total n DFFs