```
            else
            begin
                temp_x <= temp_x + 1;
                temp_enable <= 0;
            end
        end
    end

    always @(posedge clock)
    begin
        if(!resetn)
            temp_y <= 2'b00;
        else if(temp_enable)
        begin
            if(temp_y == 2'b11)
            begin
                temp_y <= 2'b00;
            end
            else
            begin
                temp_y <= temp_y + 1'b1;
                end
        end
    end

    assign x_out = out_x + temp_x;
    assign y_out = out_y + temp_y;
    assign colour_out = out_colour;
endmodule
```