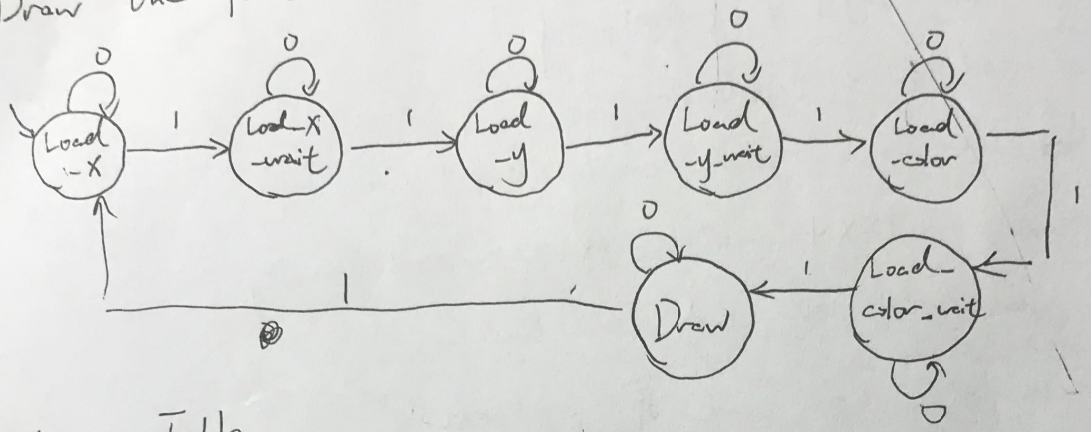
Part II

2. The verilog code has been submitted on Quercus

Draw the finite state machine.



State Table.

current state	go	next state
Load_X	0	Load_X.
Load_X	1	Load_X_wait
Load_X_wait	0	Load_X_wait
Load_X_wait	1	Load_Y
Load_Y	0	Load_Y
Load_Y_wait	1	Load_colour.
Load_colour	0	Load_colour
Load_colour	1	Load_colour_wait
Load_colour_wait	0	Load_colour_wait
Load_colour_wait	1	~~Load~~ Draw.
Draw	0	Draw.
Draw	1	Load_X.

3. Verilog code and simulation in Modelsim has been submitted on Quercus.