Lab 7.

Part I.

8. Perform the following steps.

   Have generated ram32x4.v successfully.

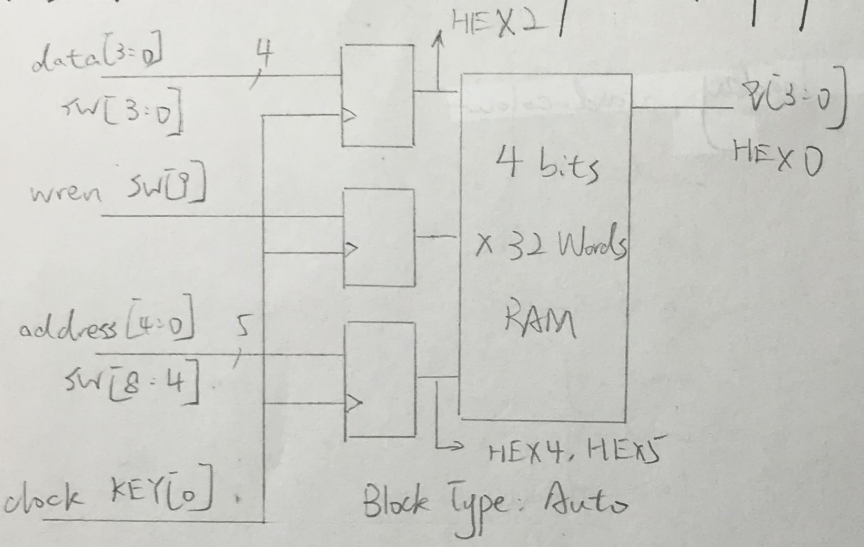
9. Simulate the module in Modelsim.

   Simulation has been submitted on Quercus with the Verilog code.

10. Instantiate the ram32x4 module in top-level Verilog.

    Verilog code has been submitted on Quercus.

11. Draw the schematic as part of preparation.



Part II.

1. Verilog has been submitted on Quercus

Draw Schematic.