```verilog
            end
        else
        begin
            if(load_x)
                out_x[6:0] <= location;
                out_x[7] <= 1'b0;
            if(load_y)
                out_y <= location;
            if(load_color)
                out_colour <= colour;
        end
    end

    reg temp_enable;
    reg [1:0] temp_x, temp_y;

    always @(posedge clock)
    begin
        if(!resetn)
            temp_x <= 2'b00;
        else if(enable)
        begin
            if(temp_x == 2'b11)
            begin
                temp_x <= 2'b00;
                temp_enable <= 1;
            end
            else
            begin
                temp_x <= temp_x + 1;
```