```
module hex_ram(KEY,SW,HEX0,HEX2,HEX4,HEX5);
    input [9:0] SW; //[3:0]data, [8:4]address, [9:9]enable
    input [0:0] KEY; //clock
    output [6:0] HEX0, HEX2, HEX4, HEX5;
    //hex0 output, hex2 input, hex45 address
    wire [3:0] q;

    ram32x4 r1(SW[8:4],KEY[0],SW[3:0],SW[9],q);

    hex h1(q,HEX0);
    hex h2(SW[3:0],HEX2);
    hex h3(SW[8],HEX5);
    hex h4(SW[7:4],HEX4);
endmodule

module hex(num, seg);
    input [3:0] num;
    output reg [6:0] seg;

    always @(*)
        case (num)
            4'h0:seg = 7'b1000000;
            4'h1:seg = 7'b1111001;
            4'h2:seg = 7'b0100100;
            4'h3:seg = 7'b0110000;
            4'h4:seg = 7'b0011001;
            4'h5:seg = 7'b0010010;
            4'h6:seg = 7'b0000010;
            4'h7:seg = 7'b1111000;
            4'h8:seg = 7'b0000000;
```