```
next_state
                                                                                                                                                                                        always @(posedge clock) begin
if(!resetn)
    current_state <= 3'd0;</pre>
                                                                                                                                    _{colour} = 1'b1;
                                                                               1,b1
1,b1
                                                                                                          1'b1
1'b0
                                                              case(current_state)
                                                                                                                                                                                                                              II
load_x = 1'b0;
load_y = 1'b0;
load_colour = plot = 1'b0;
1.b0
1.b0
                                                                                                                                                    = 1'b1;
                                                                                                                                                                                                                             current_state
                                                                                                Load_y:
load_y =
enable =
Load_colour
load_colo
                                                                                                                    II
                                                                                 II
                                                                                         II
                                                                      Load_x:
load_x
enable
                                                                                                                                             Draw:
plot
                                            (*)
                                                                                                                                                               endcase
                                                                                                                                                                                                                   else
                                            always
begin
assign
assign
assign
assign
                                                                                                                                                                                                                                              endmodule
                                                                                                                                                                       end
                                                                                                                                                                                                                                      end
```