

# 搭建你的数字积木 ——数字电路与逻辑设计 ( Verilog HDL&Vivado版 ) —— 参考课件PPT

东南大学 & Xilinx大学计划部



東南大學  
SOUTHEAST UNIVERSITY



XILINX®



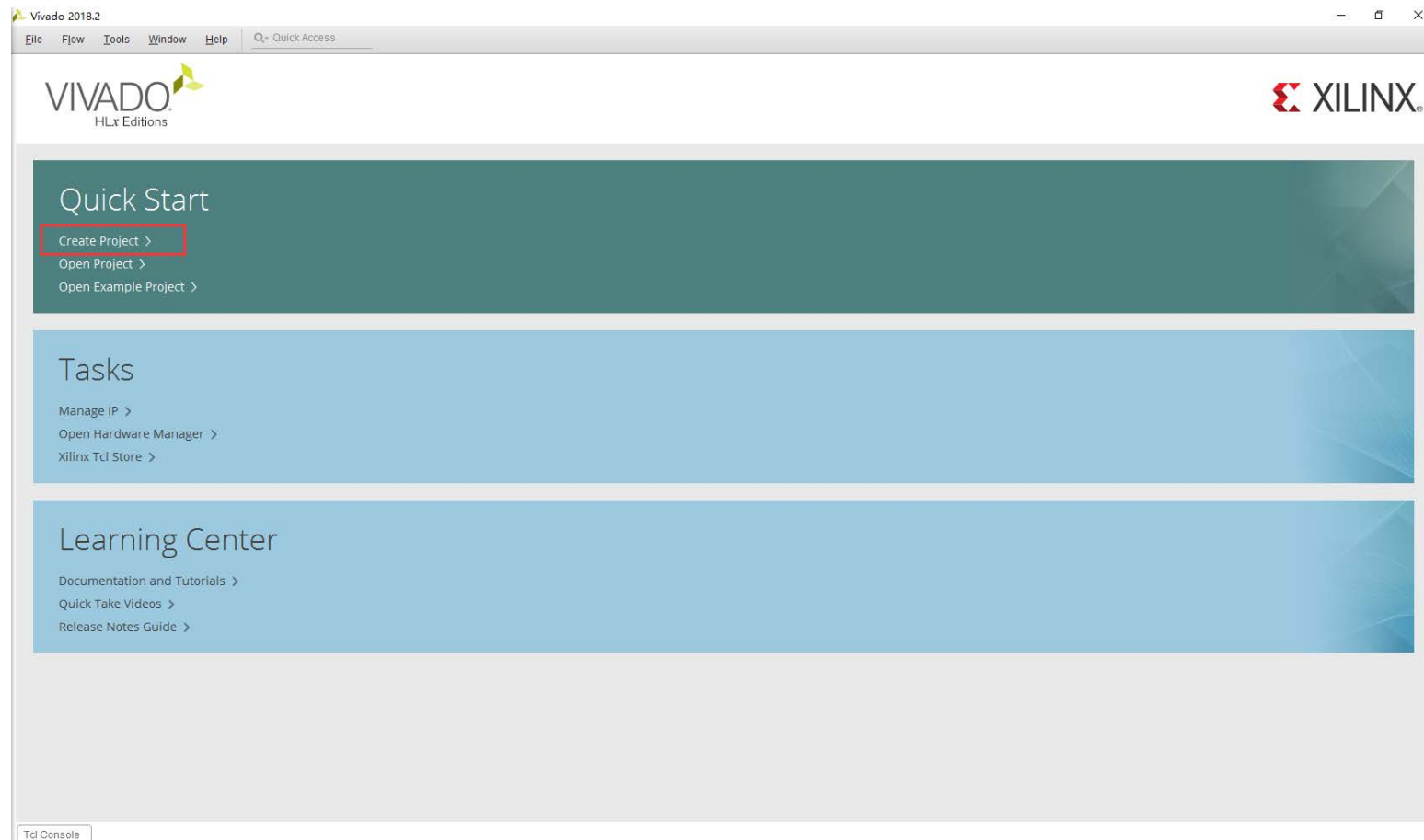
# Chap.7.数字积木（IP）设计流程

# 主要内容

- IP设计：设计一个四输入与非门IP
- IP调用：IP核在其他工程中例化调用

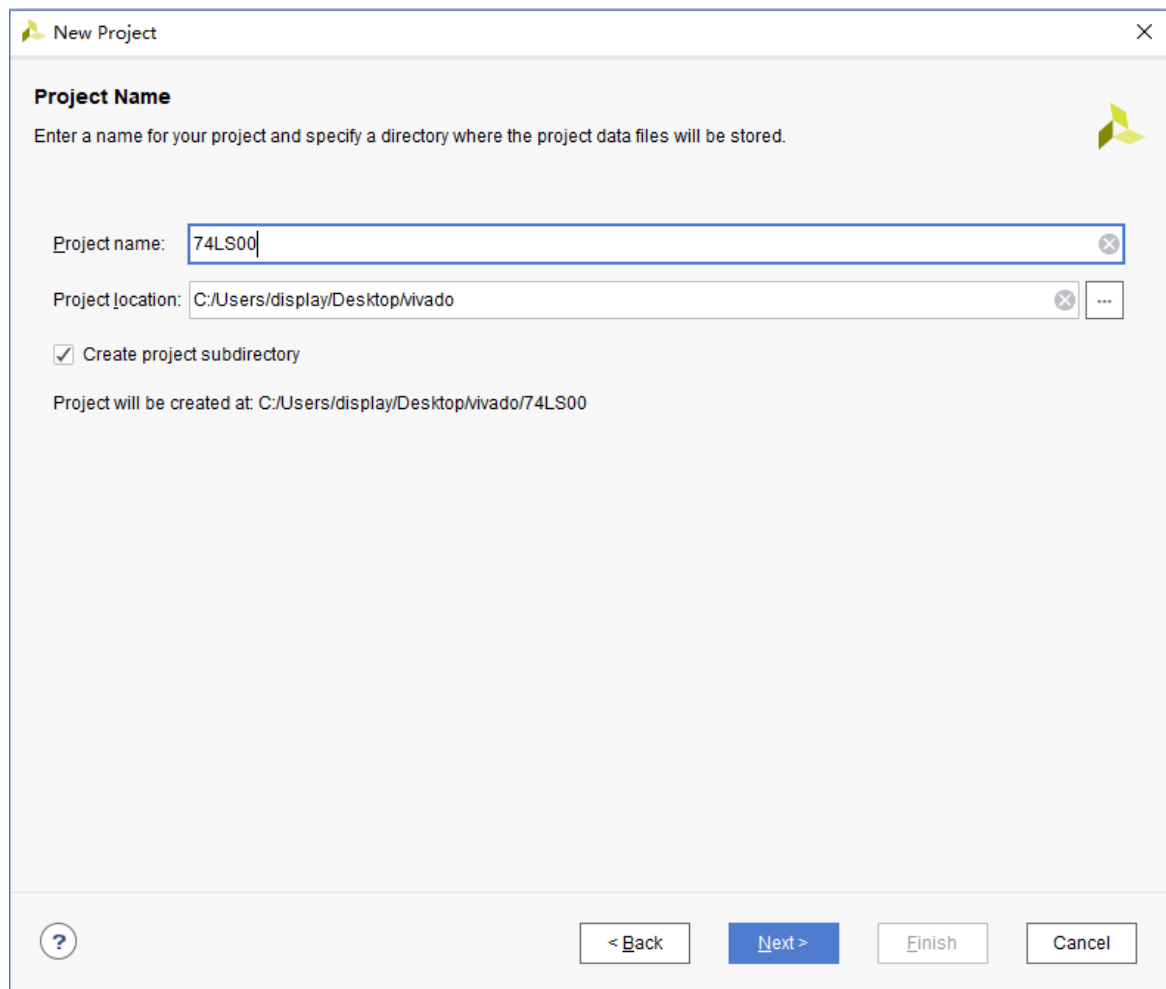
# IP设计

## ➤ 创建vivado工程



# IP设计

## ➤ 选择工程文件位置以及工程名



New Project

**Project Name**  
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: 74LS00

Project location: C:/Users/display/Desktop/vivado

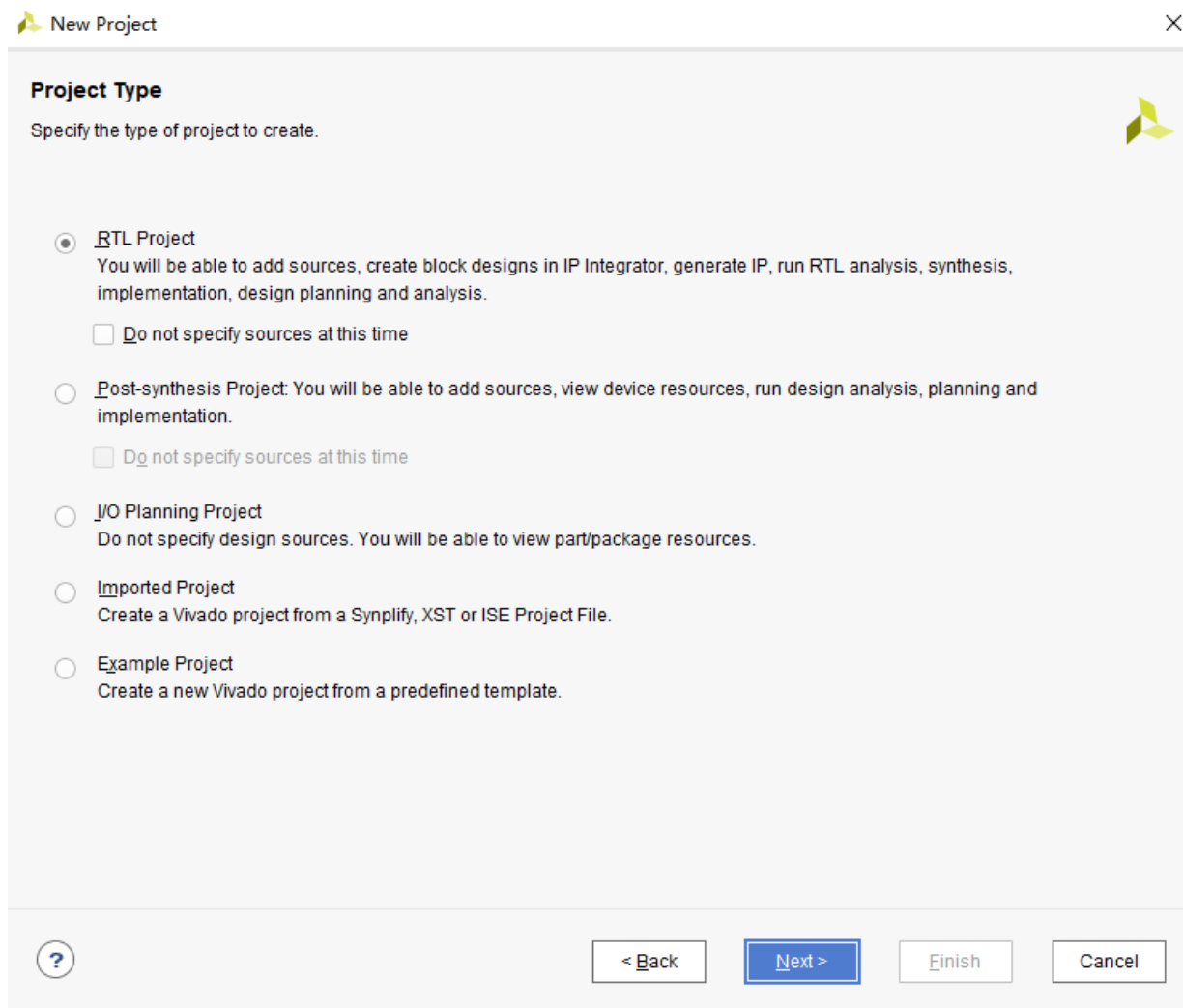
☒ Create project subdirectory

Project will be created at: C:/Users/display/Desktop/vivado/74LS00

? < Back Next > Finish Cancel

# IP设计

➤ 选择第一个RTL project即可



# IP设计

## ➤ 选择语言为verilog

New Project

**Add Sources**

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

Target language: Verilog Simulator language: Verilog

# IP设计

## ➤ 选择板卡芯片型号

New Project

**Default Part**

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All

Family: All Speed: All

Search:  (4 matches)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gt
xc7a35tcp236-3	236	106	20800	41600	50	0	90	2
xc7a35tcp236-2	236	106	20800	41600	50	0	90	2
xc7a35tcp236-2L	236	106	20800	41600	50	0	90	2
xc7a35tcp236-1	236	106	20800	41600	50	0	90	2

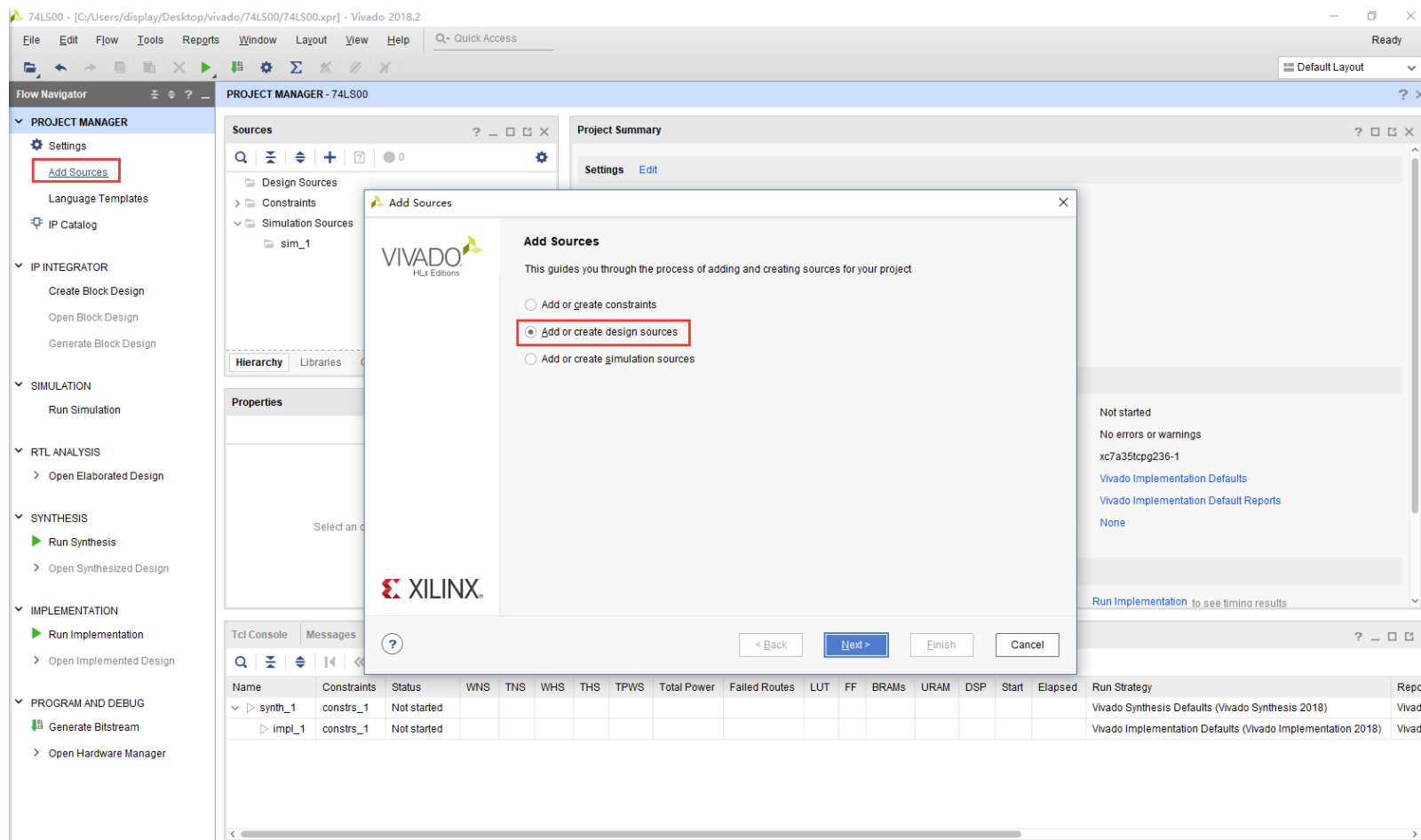
< >

? < Back Next > Finish Cancel



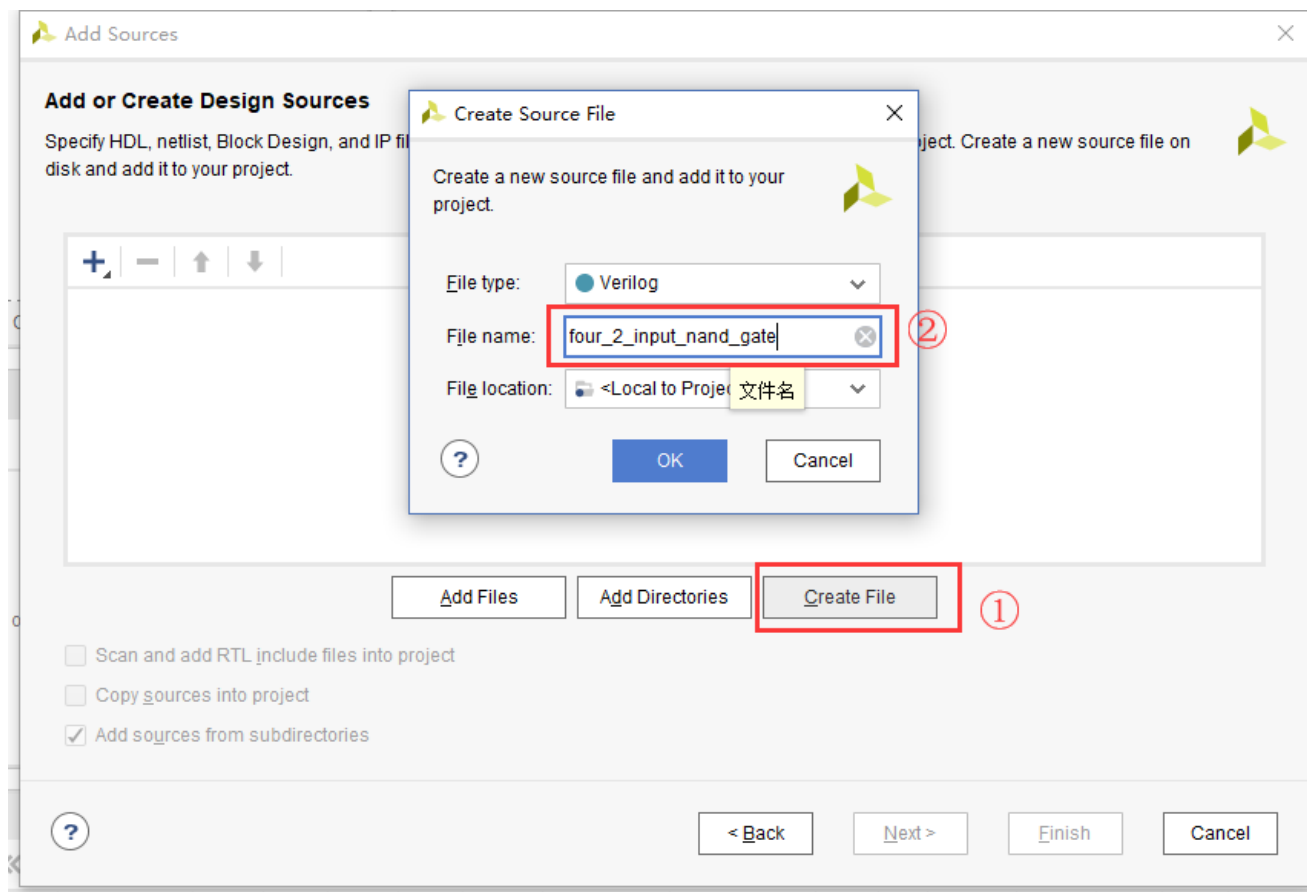
# IP设计

## ➤ 添加源文件



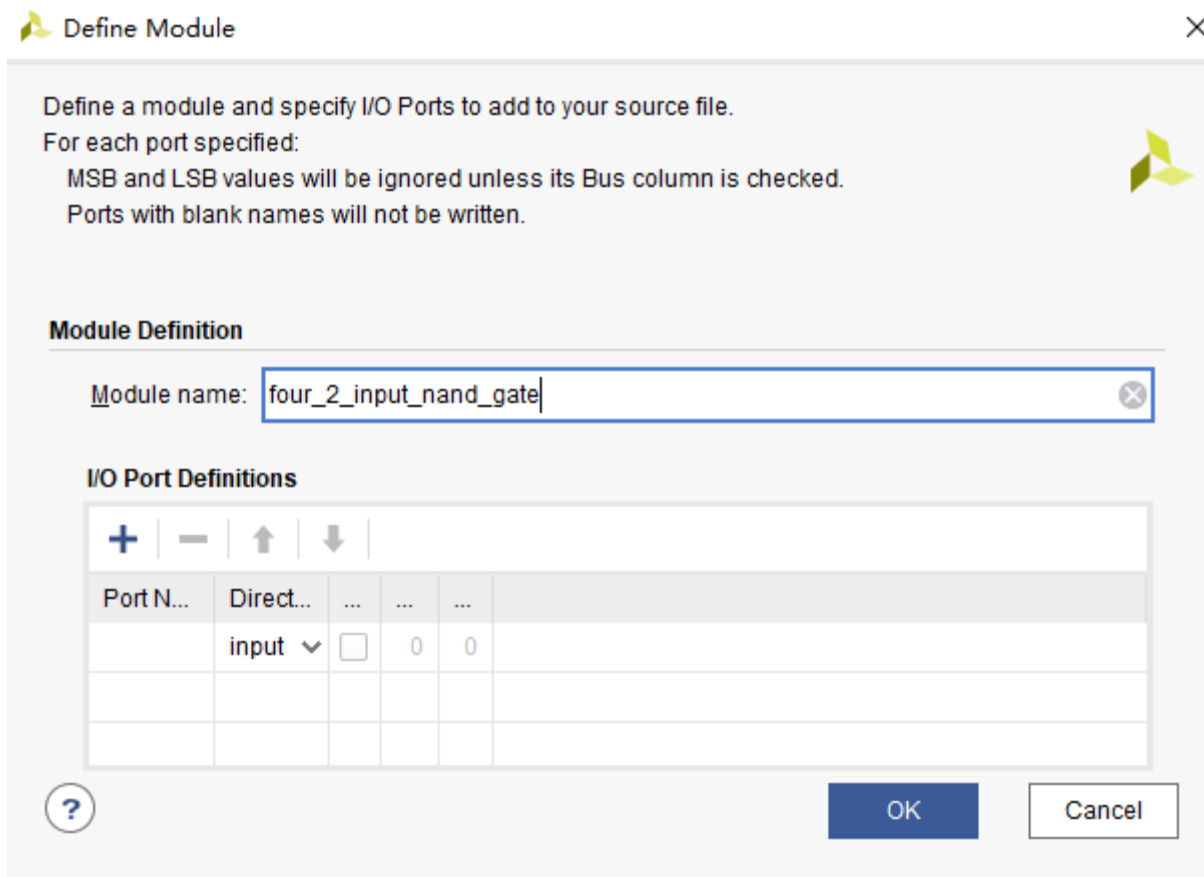
# IP设计

## ➤ 源文件名称



# IP设计

➤ 可以添加源文件输出管脚，一般默认即可



Define Module

Define a module and specify I/O Ports to add to your source file.  
For each port specified:  
MSB and LSB values will be ignored unless its Bus column is checked.  
Ports with blank names will not be written.

**Module Definition**

Module name:

**I/O Port Definitions**

Port N...	Direct...	...	...	...
	input ▾	<input type="checkbox"/>	0	0

?

OK Cancel

# IP设计

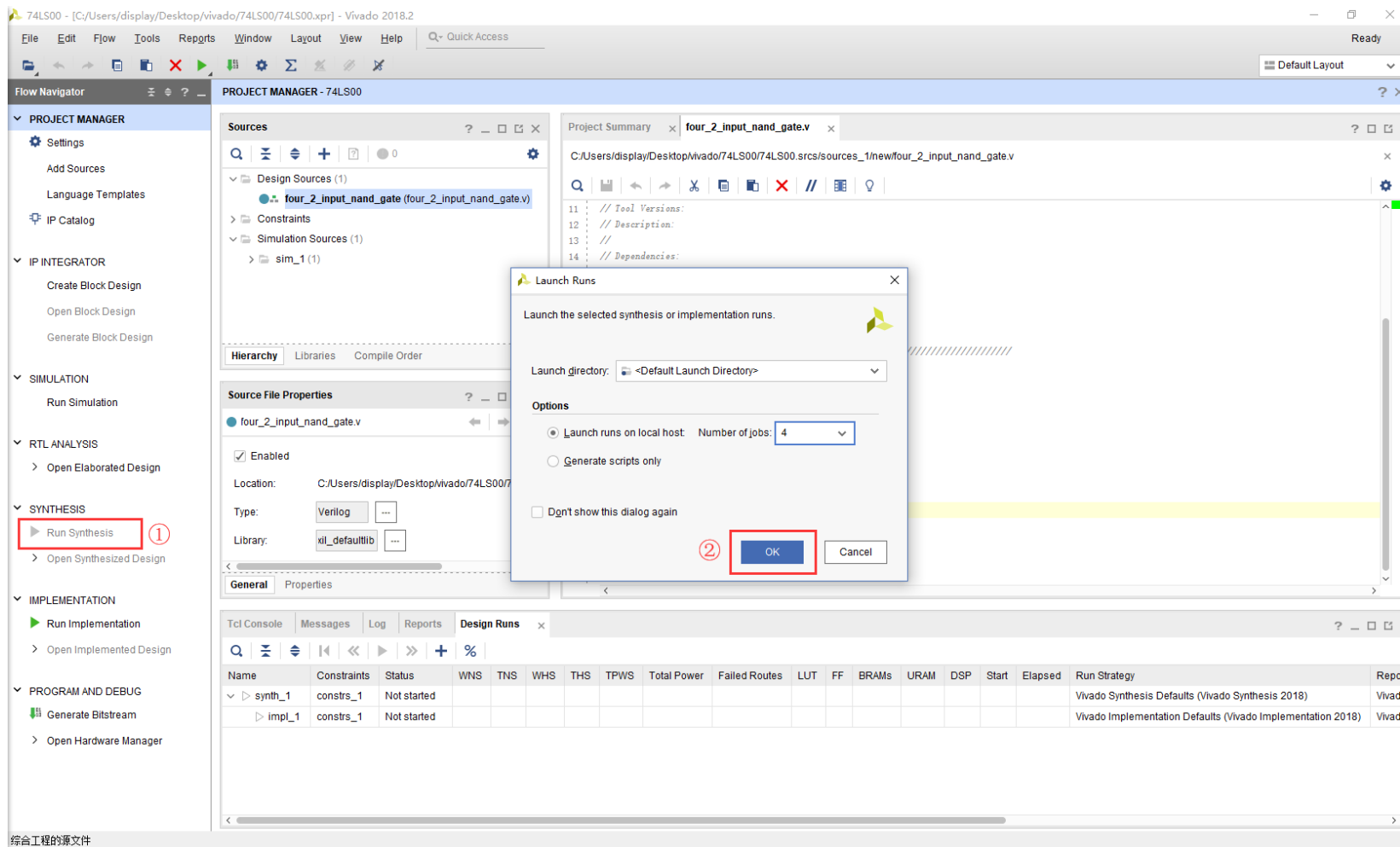
## 编写源文件

The screenshot displays the Xilinx Vivado Project Manager interface. The top window, titled "PROJECT MANAGER - 74LS00", shows a "Sources" panel on the left with a tree view containing "Design Sources (1)", "Constraints", and "Simulation Sources (1)". The "Design Sources (1)" folder is expanded, showing a file named "four\_2\_input\_nand\_gate (four\_2\_input\_nand\_gate.v)". Below this, the "Source File Properties" window is open, showing the file's location as "C:/Users/display/Desktop/vivado/74LS00/74LS00.srcs/sources\_1/new/four\_2\_input\_nand\_gate.v", its type as "Verilog", and its library as "xil\_defaultlib". The main editor window, titled "four\_2\_input\_nand\_gate.v", shows the Verilog code for a 4-input NAND gate. The code includes comments for tool versions, description, dependencies, revision, and additional comments. The main code block defines a module "four\_2\_input\_nand\_gate" with a parameter "DELAY = 10". It has four inputs: "a1, b1, a2, b2, a3, b3, a4, b4" and four outputs: "y1, y2, y3, y4". The module body contains four NAND gate instances, each with a delay of "DELAY". The code ends with "endmodule".

```
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////
21
22
23 module four_2_input_nand_gate #(parameter DELAY = 10)(
24     input wire a1, b1, a2, b2, a3, b3, a4, b4,
25     output wire y1, y2, y3, y4
26 );
27
28     nand #DELAY (y1, a1, b1);
29     nand #DELAY (y2, a2, b2);
30     nand #DELAY (y3, a3, b3);
31     nand #DELAY (y4, a4, b4);
32
33 endmodule
34
```

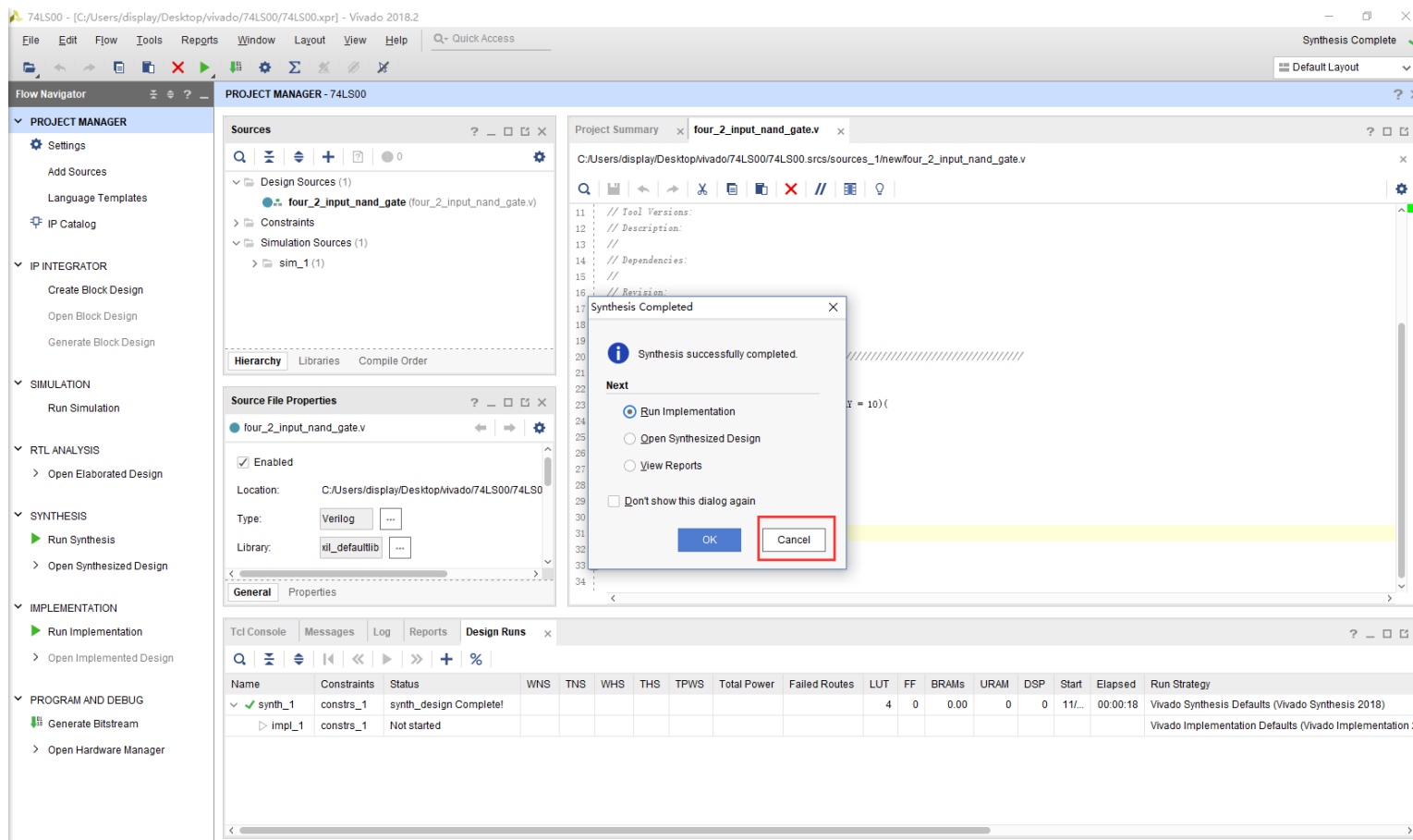
# IP设计

## 源文件综合编译



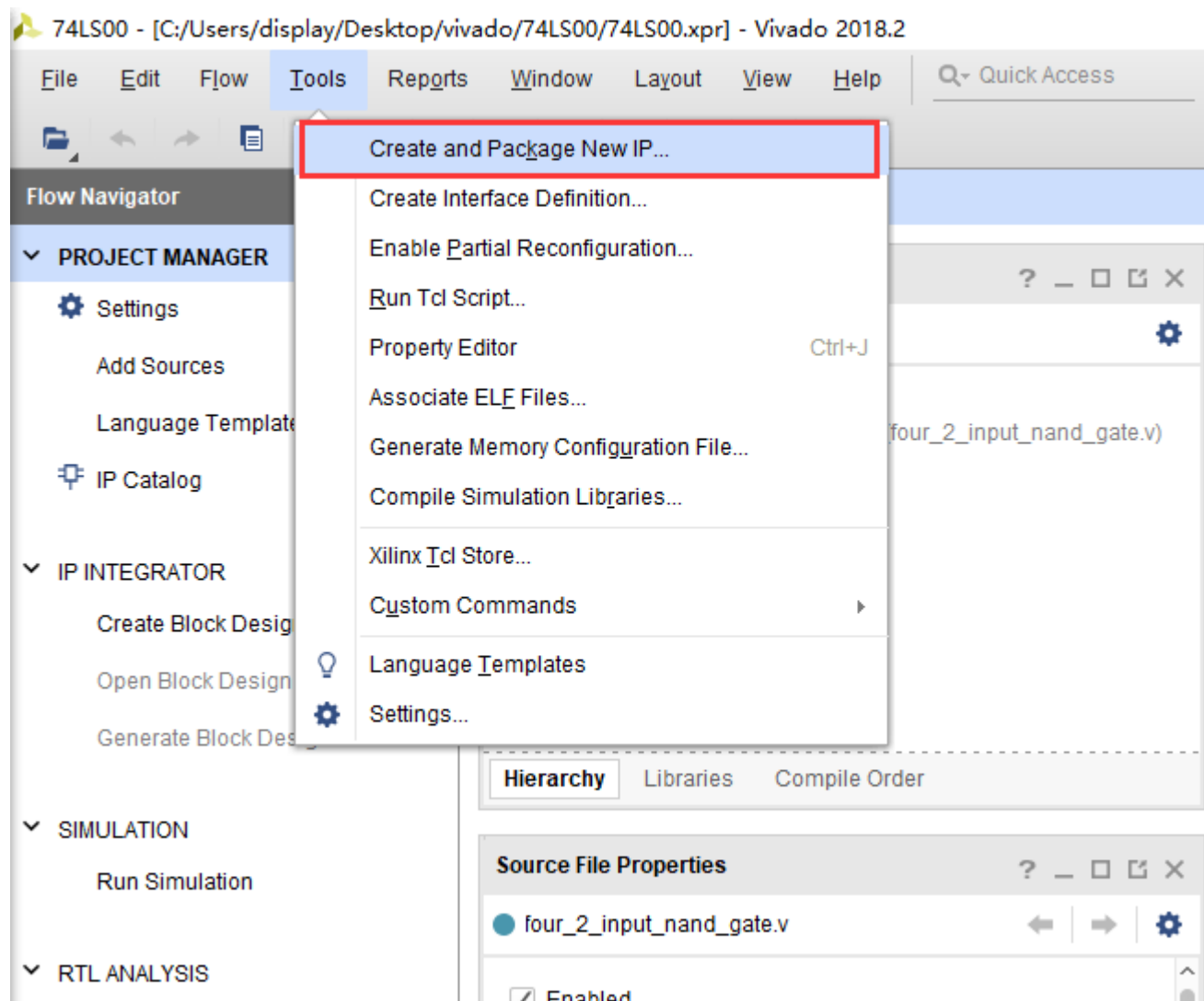
# IP设计

➤ 创建IP不需要implement, 所以cancel即可



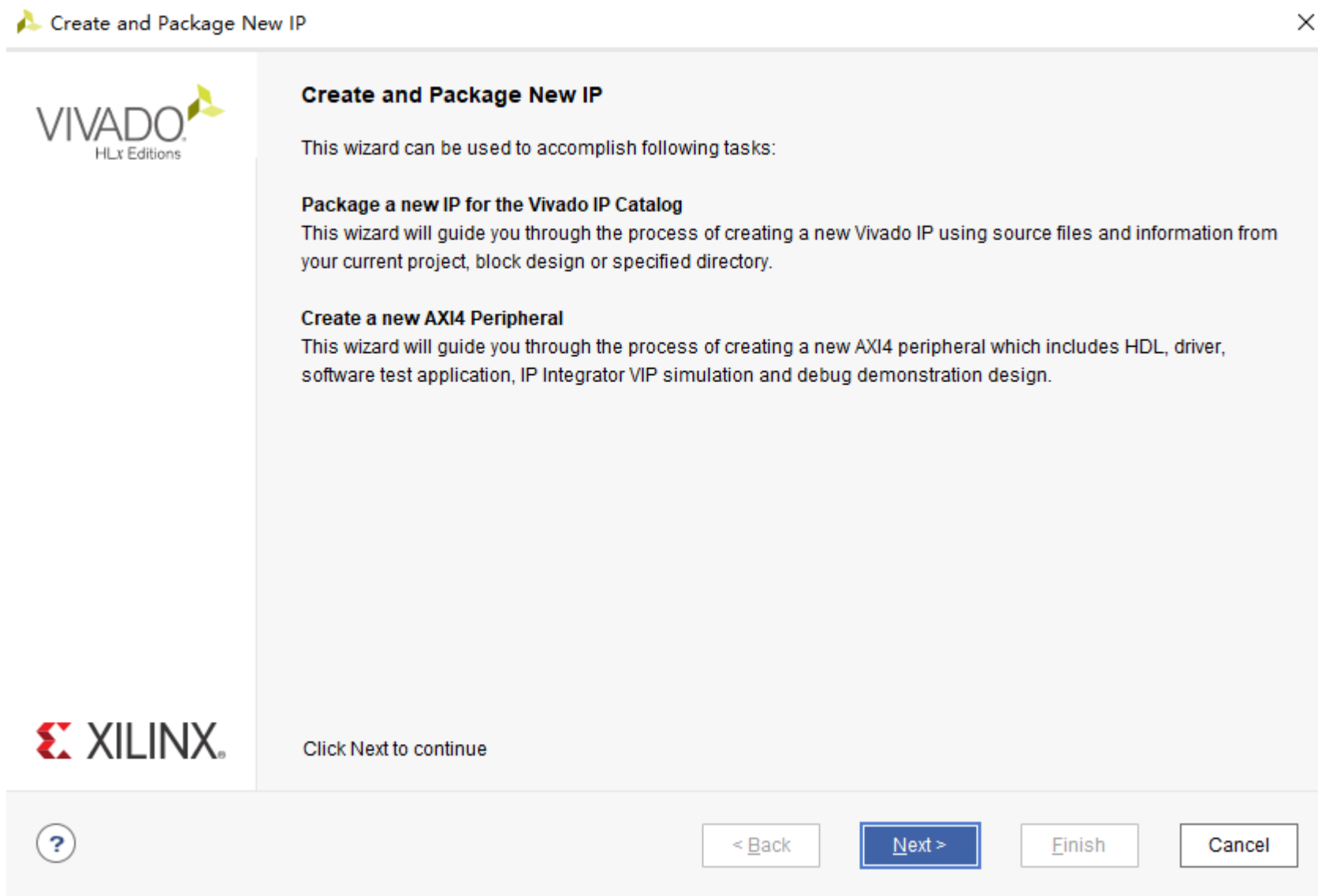
# IP设计

➤ 点击Tools下的Create and Package New IP...创建IP



# IP设计

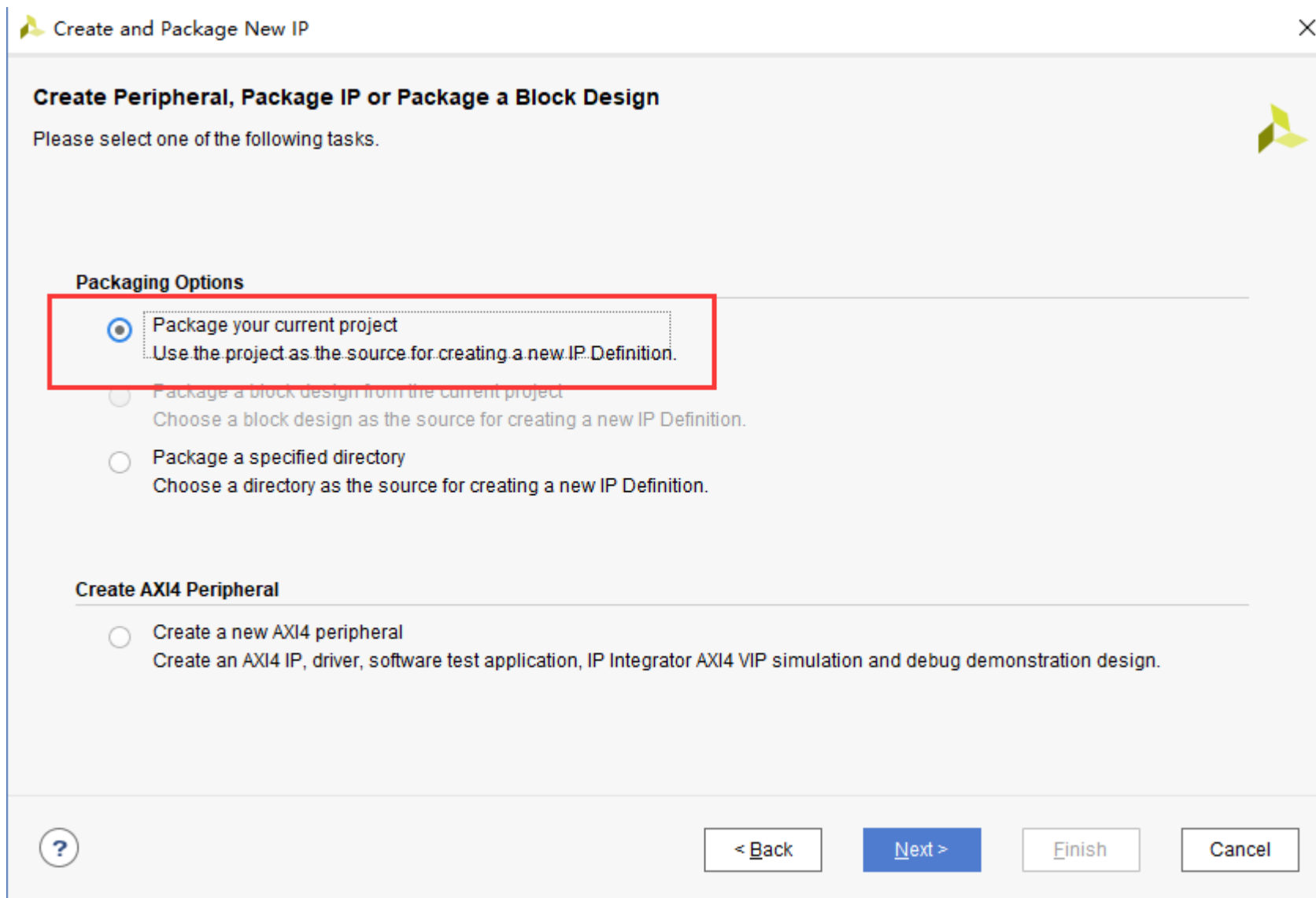
➤ 默认next





# IP设计

➤ 选择第一个，封装当前工程为IP



Create and Package New IP

Create Peripheral, Package IP or Package a Block Design

Please select one of the following tasks.

**Packaging Options**

- ☒ Package your current project  
Use the project as the source for creating a new IP Definition.
- ☐ Package a block design from the current project  
Choose a block design as the source for creating a new IP Definition.
- ☐ Package a specified directory  
Choose a directory as the source for creating a new IP Definition.

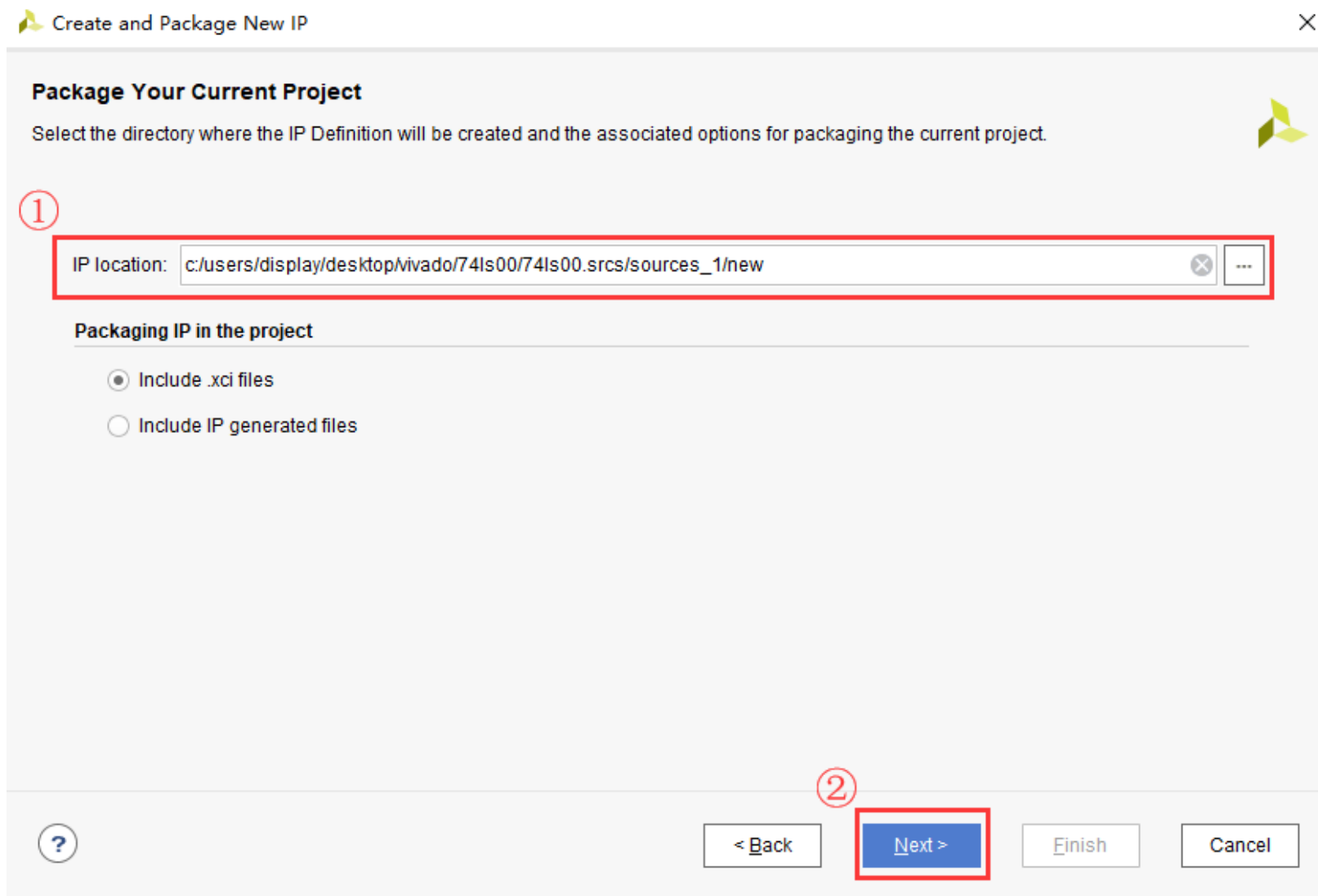
**Create AXI4 Peripheral**

- ☐ Create a new AXI4 peripheral  
Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.

? < Back Next > Finish Cancel

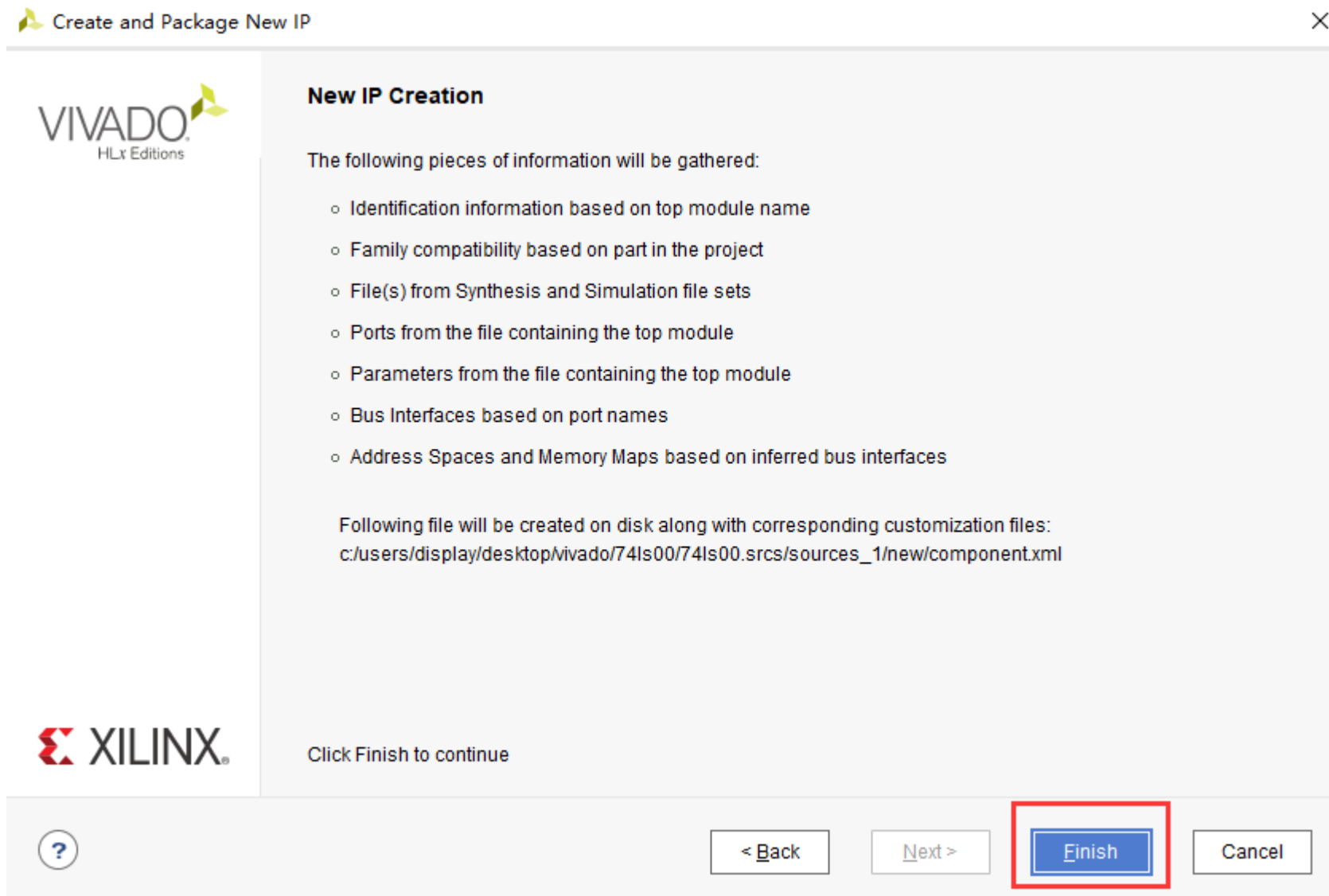
# IP设计

➤ 选择IP文件的位置，后面调用IP要选择此位置



# IP设计

## ➤ 默认finish完成IP的信息设置



# IP设计

➤ 选择IP的name和display name

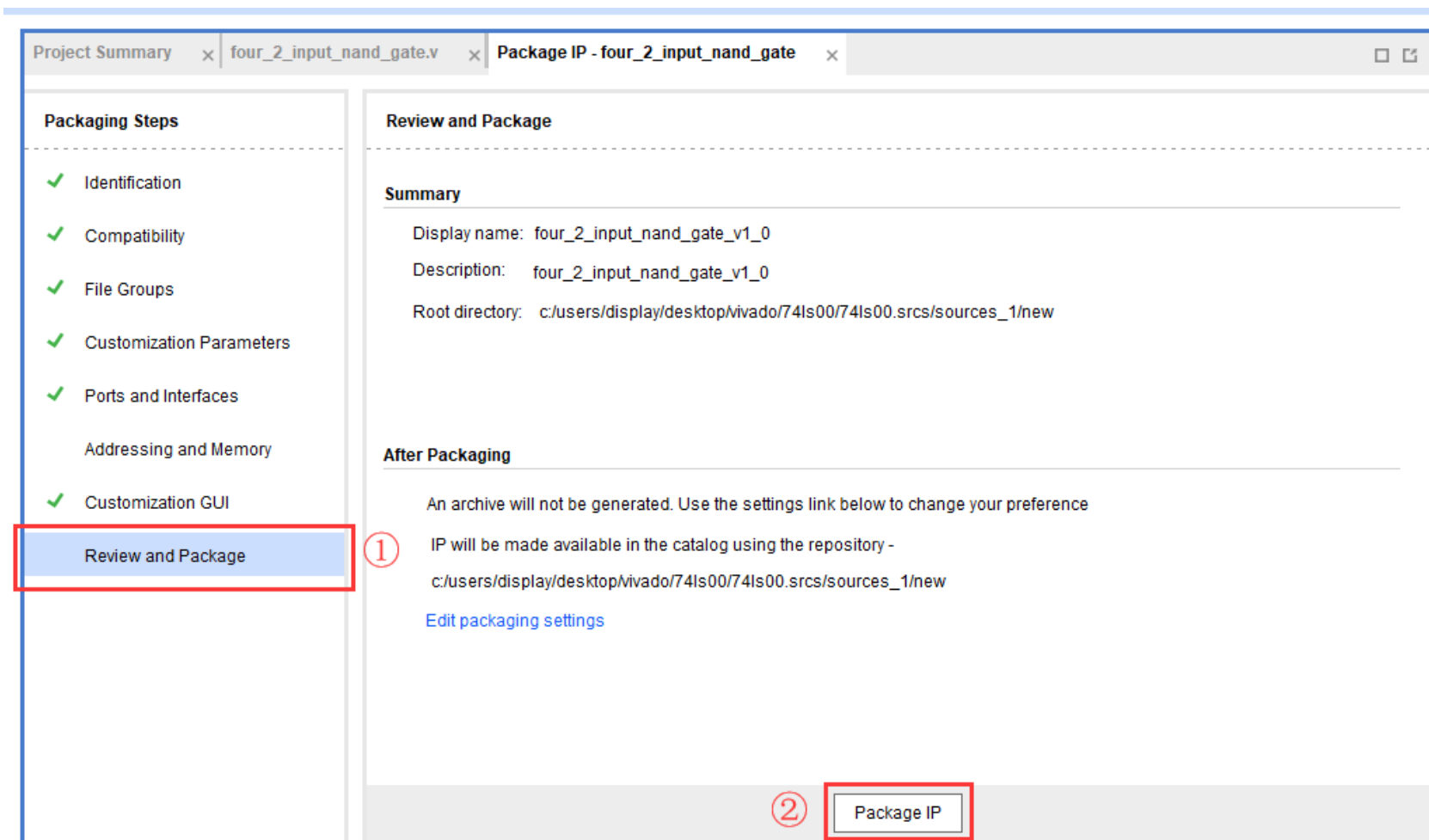
The screenshot shows the 'Package IP - four\_2\_input\_nand\_gate' configuration window in Xilinx Vivado. The left sidebar lists 'Packaging Steps' with 'Identification' selected and marked with a green checkmark. The main area displays the 'Identification' tab with the following fields:

Field	Value
Vendor:	xilinx.com
Library:	user
Name:	four_2_input_nand_gate
Version:	1.0
Display name:	four_2_input_nand_gate_v1_0
Description:	four_2_input_nand_gate_v1_0
Vendor display name:	
Company url:	
Root directory:	c:/users/display/desktop/vivado/74ls00/74ls00.srcs/sources_1/new
Xml file name:	c:/users/display/desktop/vivado/74ls00/74ls00.srcs/sources_1/new/component.xml

Below the identification fields is the 'Categories' section, which includes a list of categories with a '+' button to add new ones. The current category is '/UserIP'.

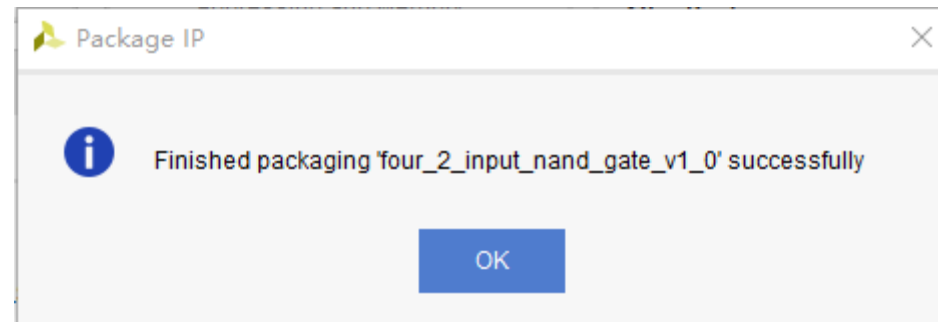
# IP设计

➤ 点击review and package, 然后点击Package IP



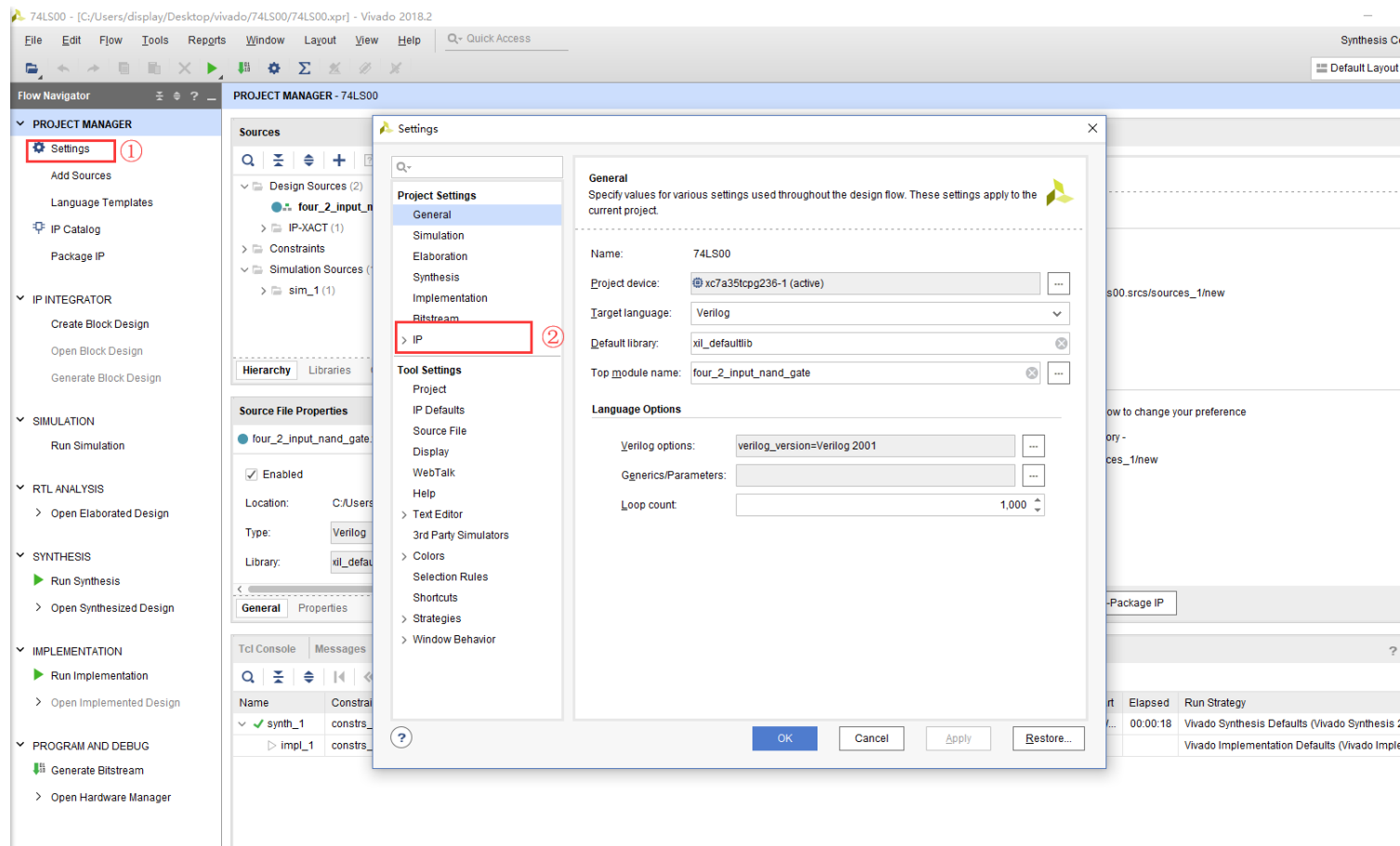
# IP设计

➤ 创建成功



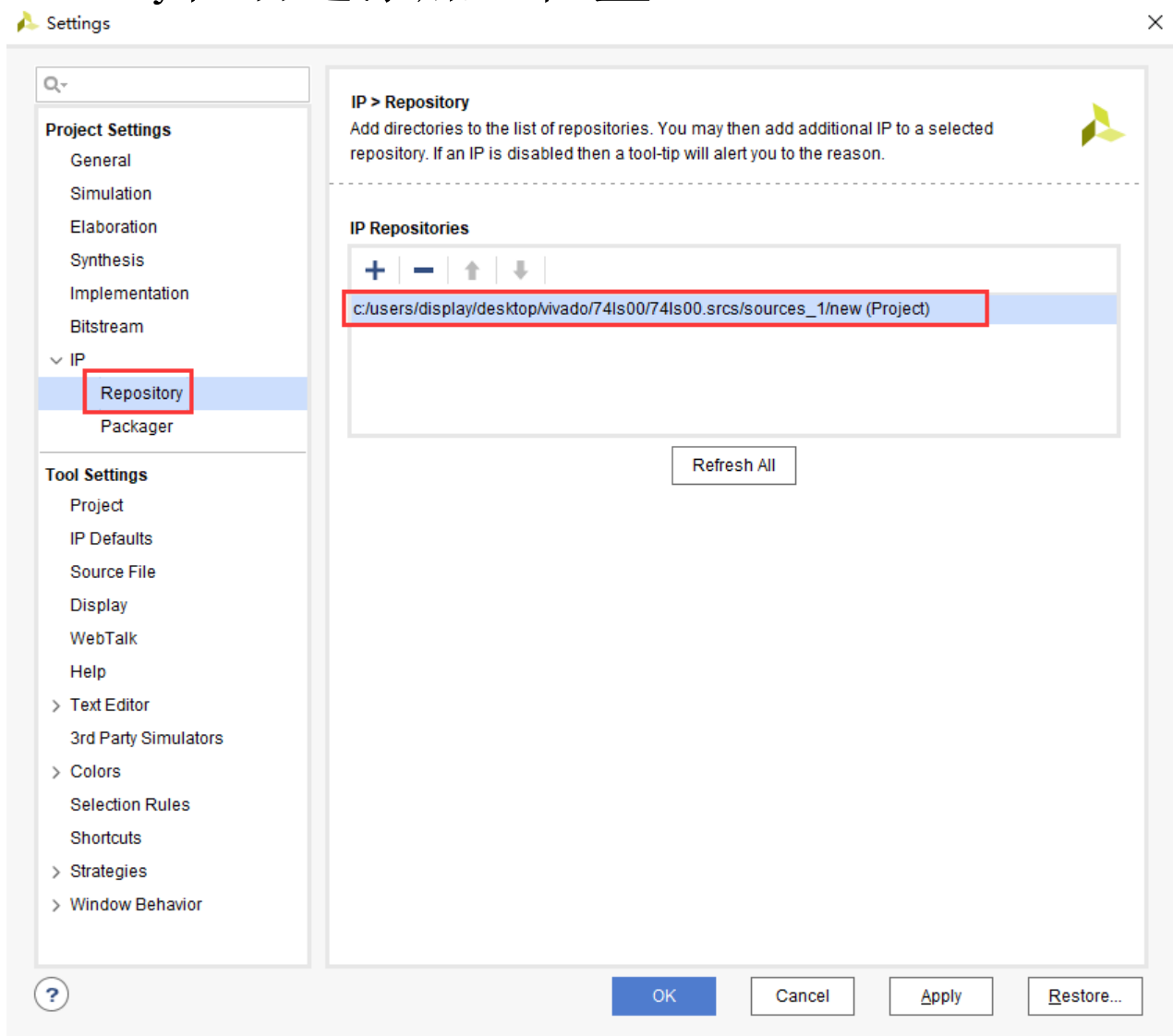
# IP调用

➤ 打开要调用IP的工程，然后点击setting下的IP



# IP调用

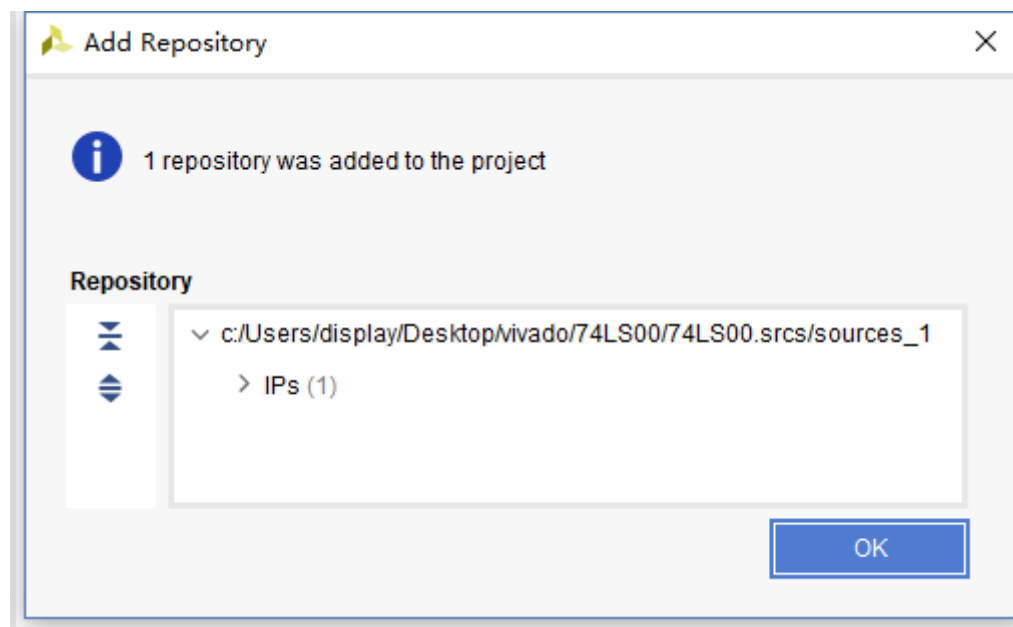
➤ 点击IP下的Repository在右边添加IP位置





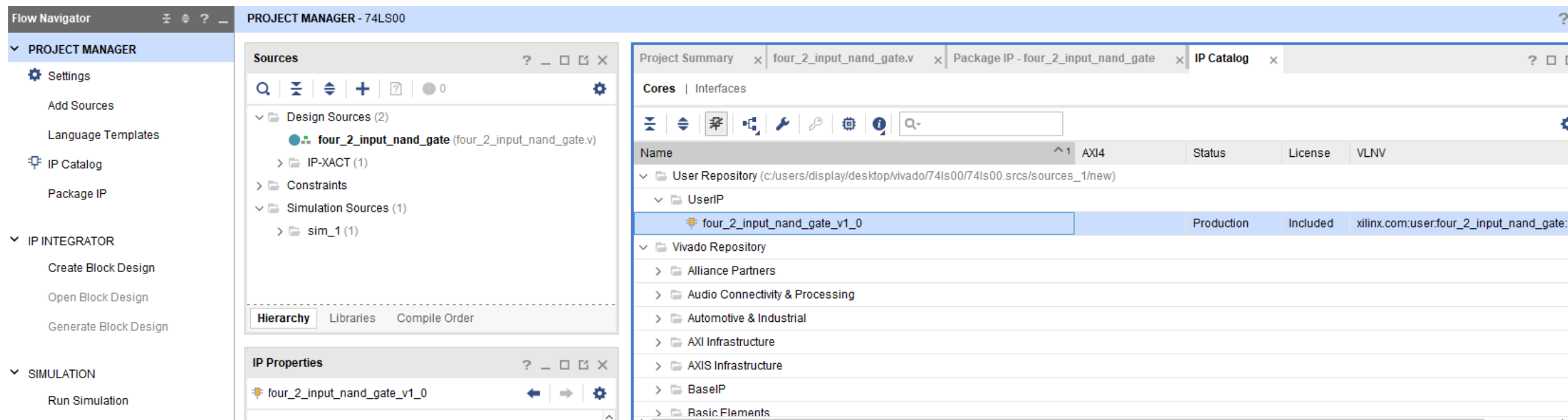
# IP调用

➤ 添加位置时若弹出以下命令框，则表明是一个正确的IP



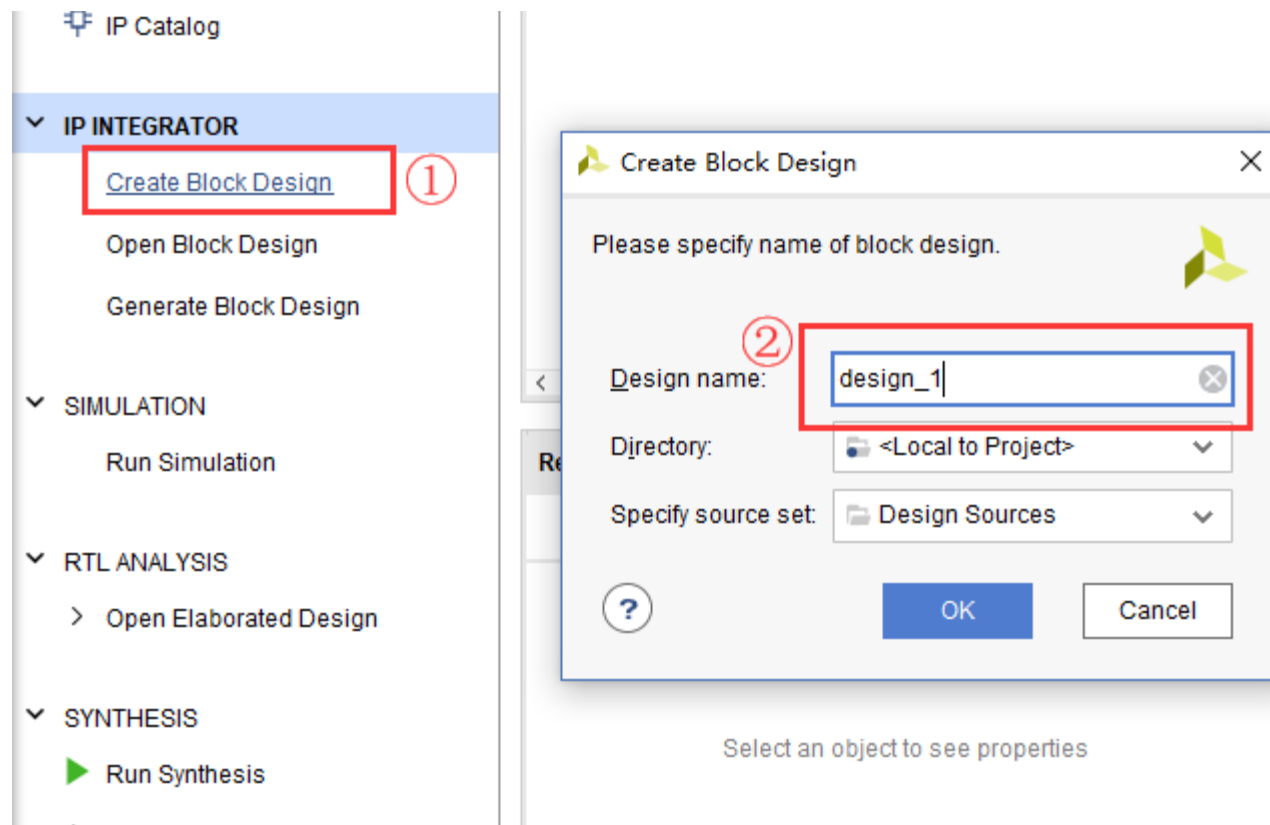
# IP调用

➤ IP Catalog打开可以在UserIP下看见创建的IP，或者在命令框搜索IP的名称



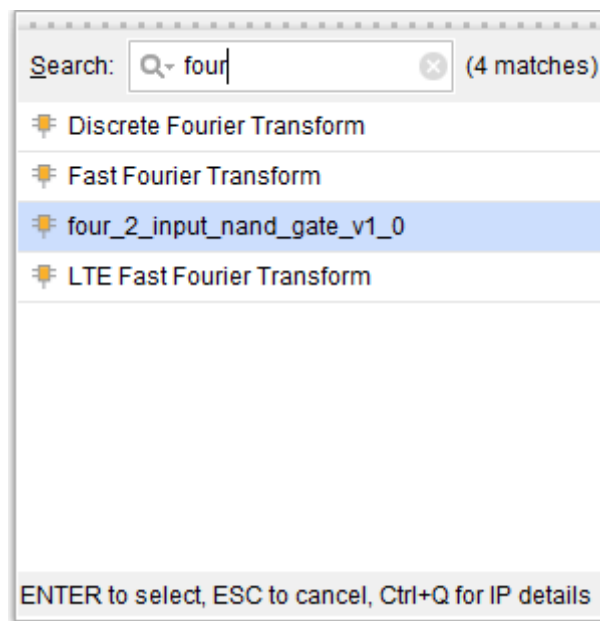
# IP调用

## ➤ 创建Block Design并命名



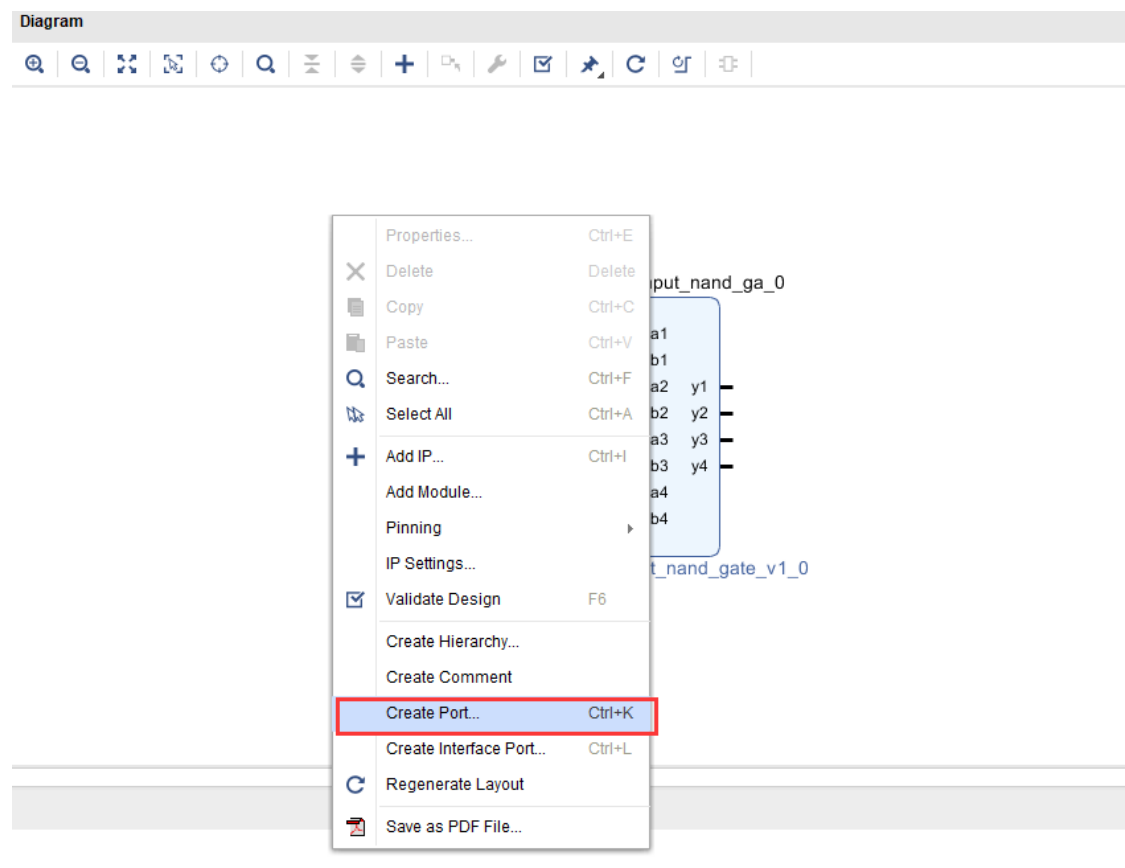
# IP调用

➤ 调用刚刚添加到工程的IP



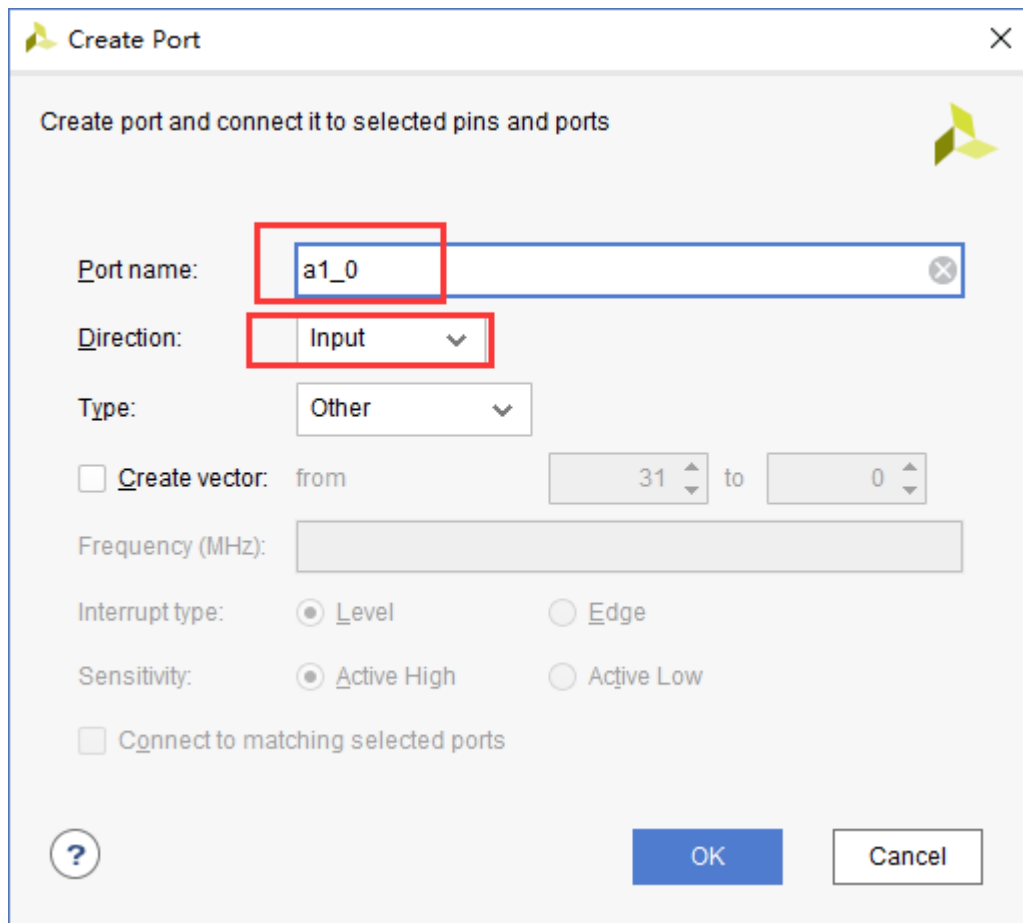
# IP调用

➤ 然后在Block Design中添加Port



# IP调用

➤ Port命名以及选择输入输出



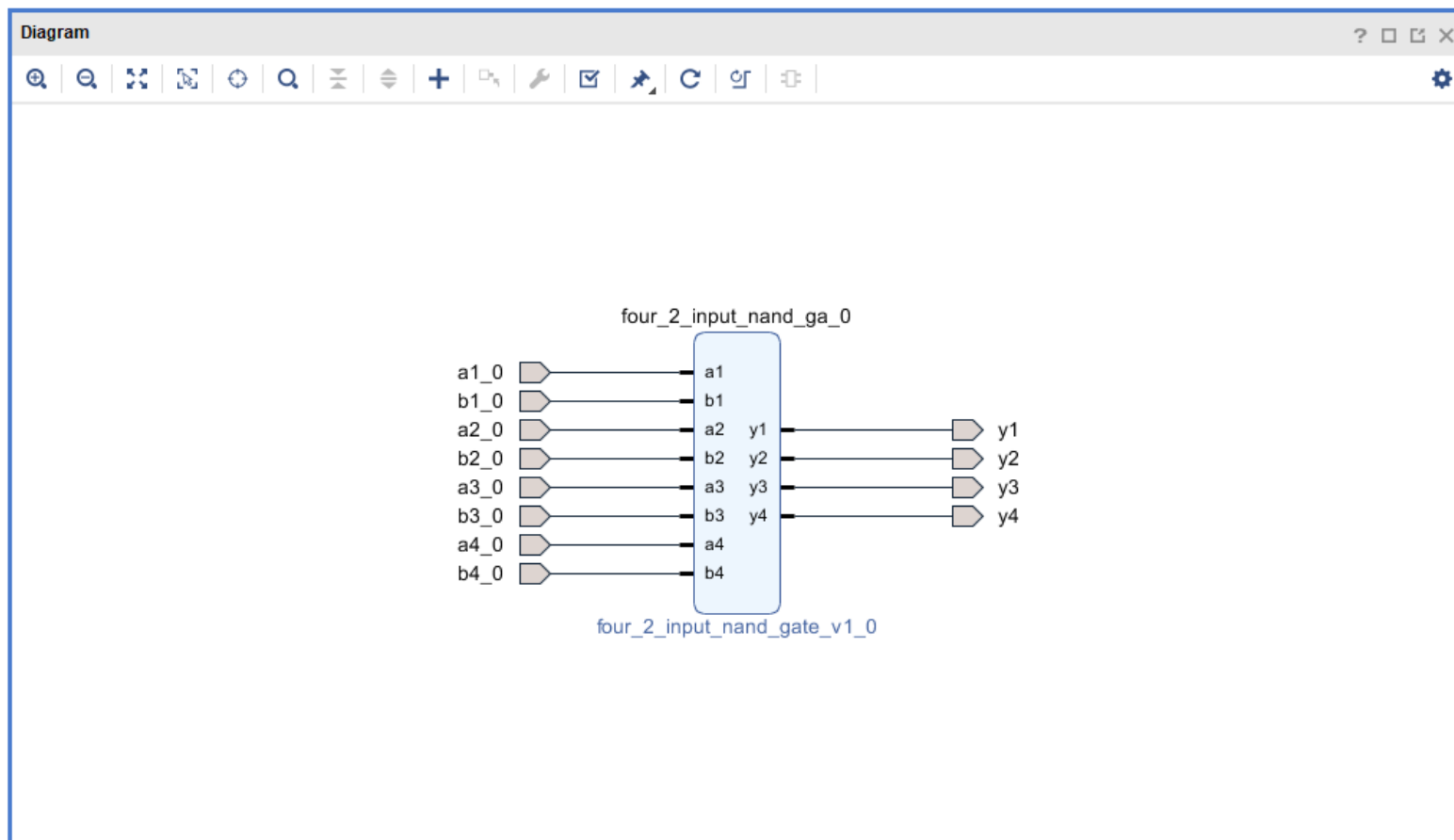
The image shows a 'Create Port' dialog box from a software tool. The dialog has a title bar with a green icon and a close button. The main area contains the following fields and options:

- Port name:** A text field containing 'a1\_0', which is highlighted with a red rectangle.
- Direction:** A dropdown menu set to 'Input', also highlighted with a red rectangle.
- Type:** A dropdown menu set to 'Other'.
- Create vector:** An unchecked checkbox. If checked, it would show a range from 31 to 0.
- Frequency (MHz):** An empty text field.
- Interrupt type:** Two radio buttons: 'Level' (selected) and 'Edge'.
- Sensitivity:** Two radio buttons: 'Active High' (selected) and 'Active Low'.
- Connect to matching selected ports:** An unchecked checkbox.

At the bottom, there is a help icon (question mark in a circle), an 'OK' button, and a 'Cancel' button.

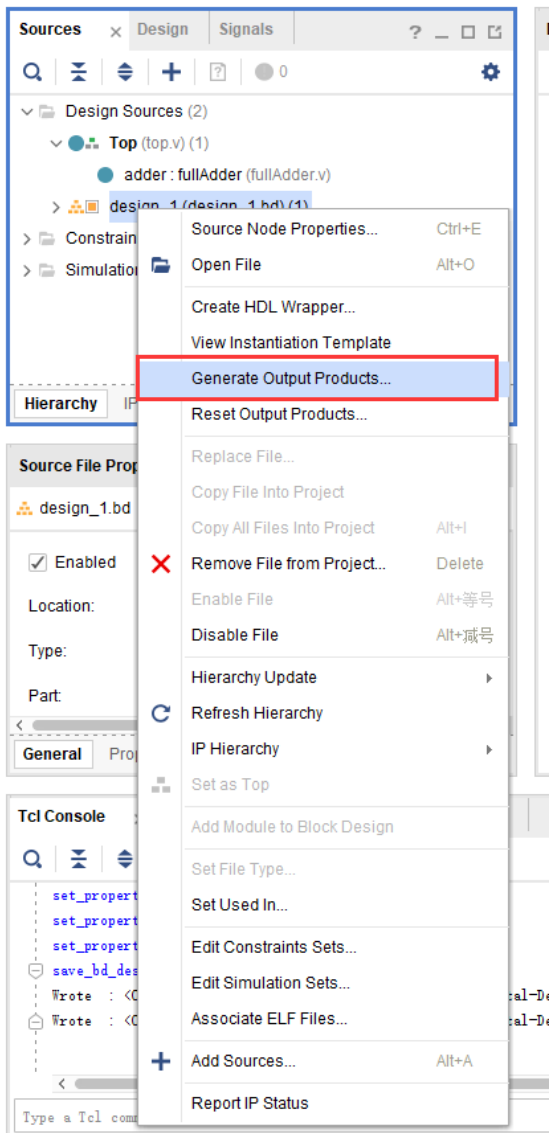
# IP调用

➤ 完成以下的连线



# IP调用

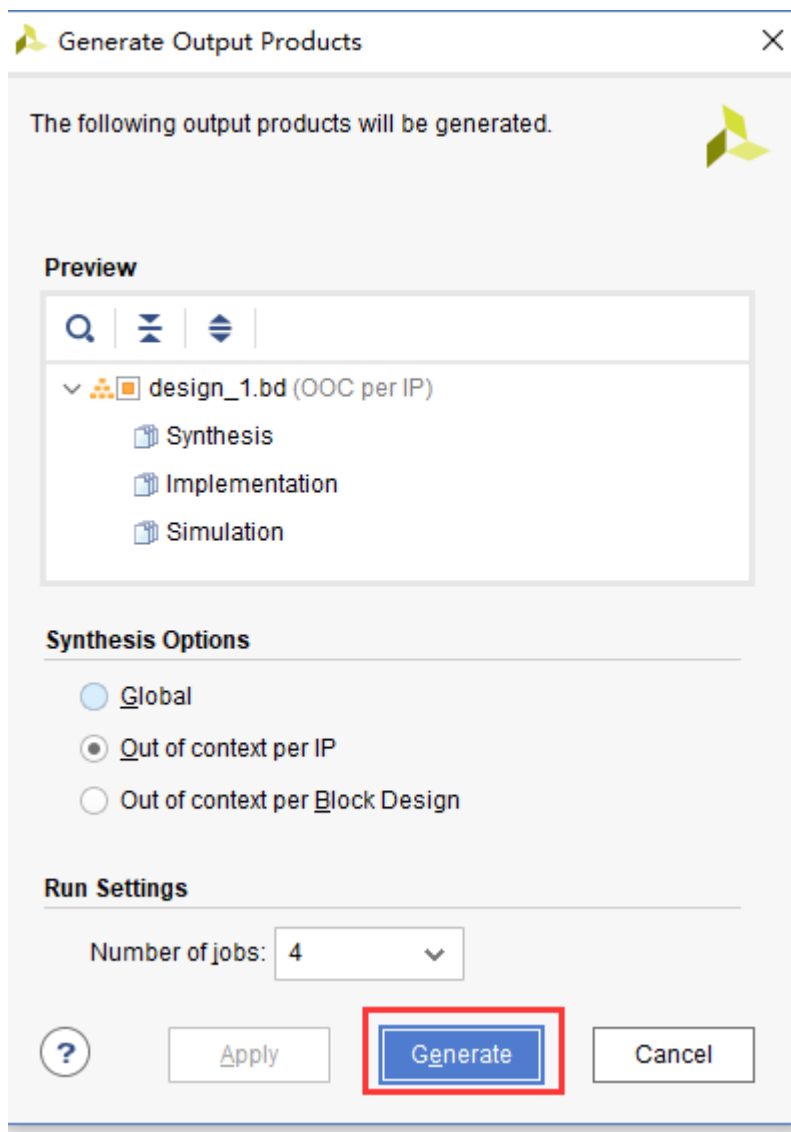
➤ 右击Block Design后选择Generate Output Products...





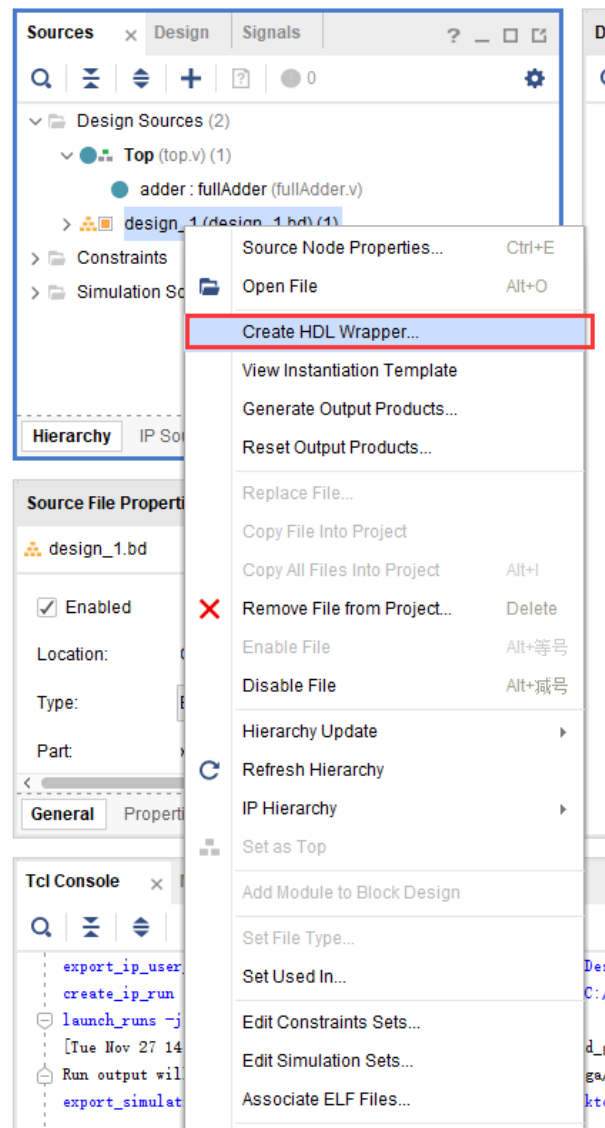
# IP调用

➤ 默认Generate



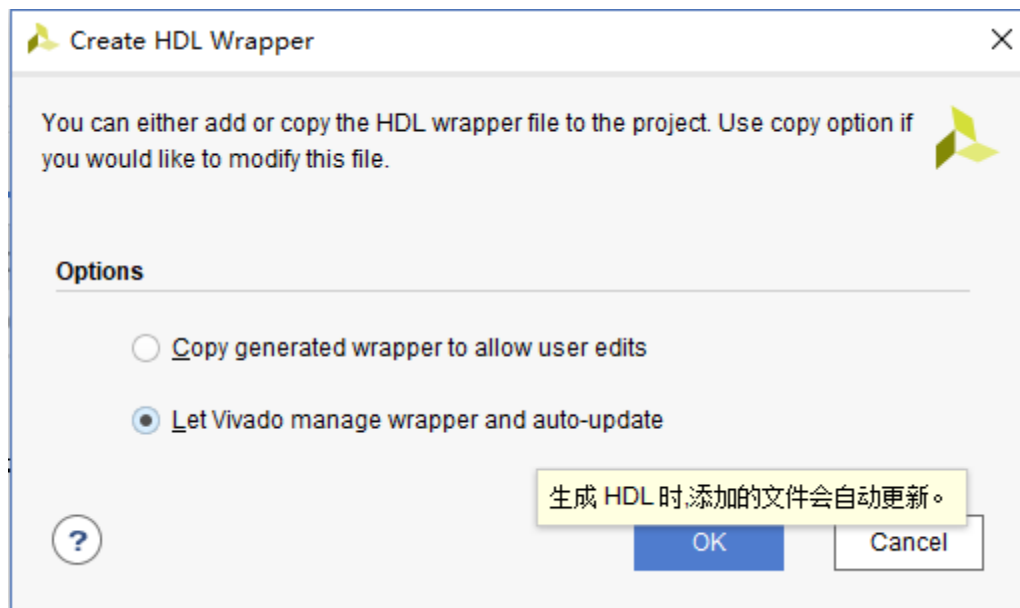
# IP调用

➤ 右击Block Design后选择Create HDL Wrapper...



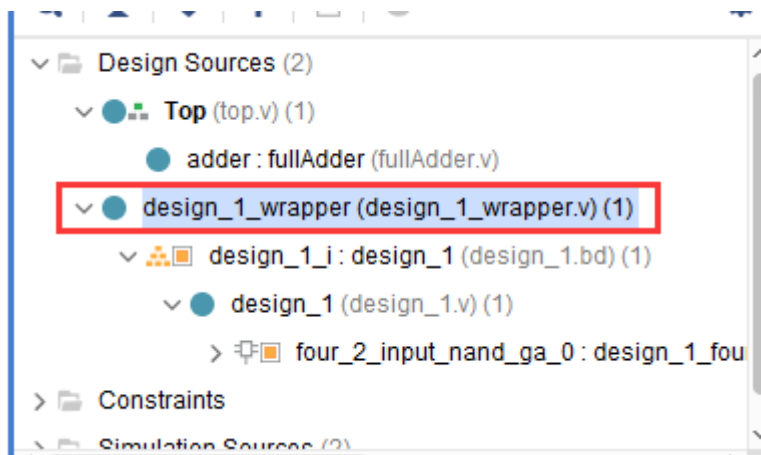
# IP调用

➤ 选择第二个将会自动更新IP



# IP调用

➤ 此时完成IP的例化，即可看见Block Design对应的模块，即可进行后续工作





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