搭建你的数字积木
—数字电路与逻辑设计
（Verilog HDL&Vivado版）
— 参考课件PPT

东南大学 & Xilinx大学计划部

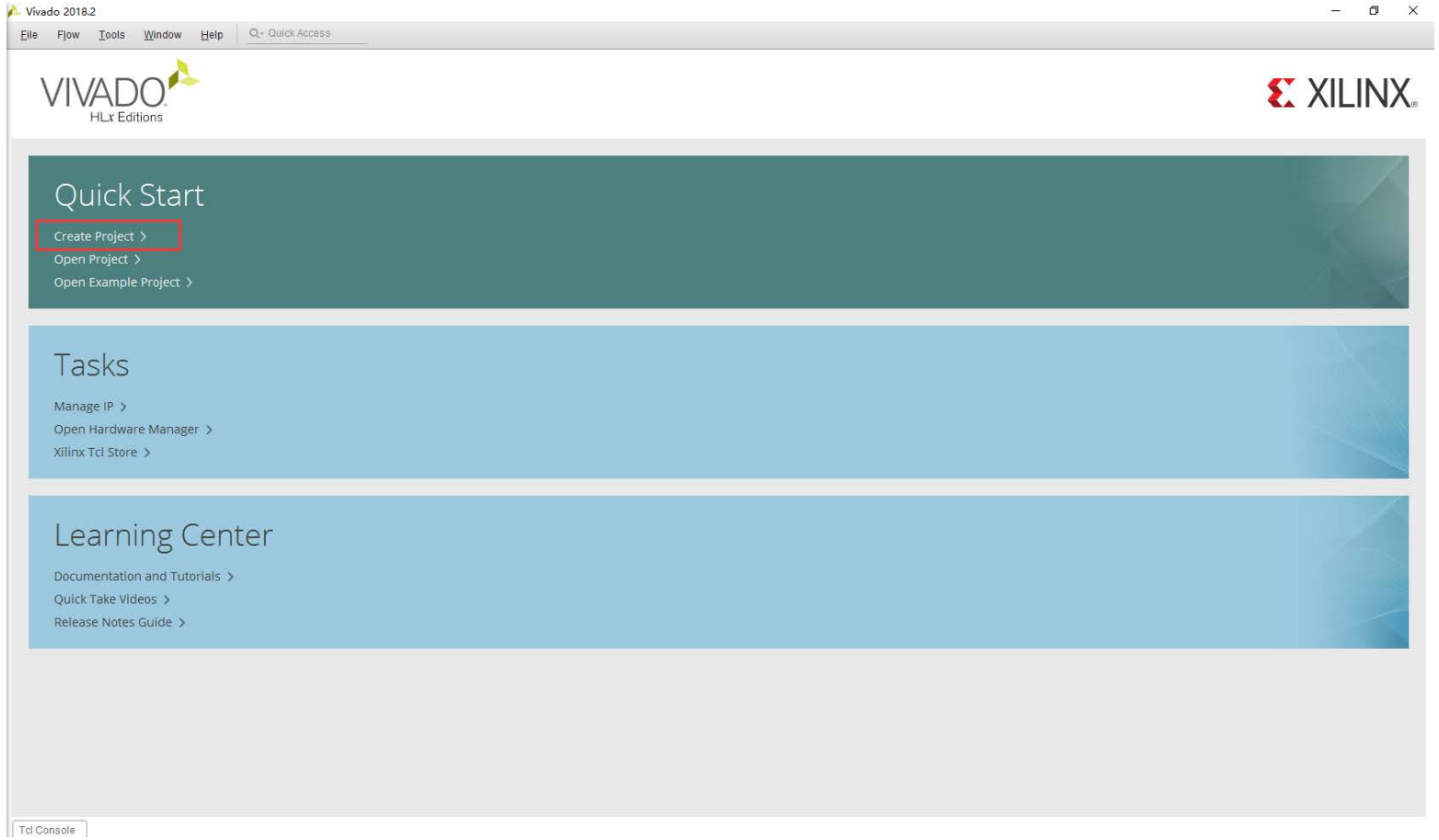
Chap.7.数字积木（IP）设计流程

主要内容

- IP设计：设计一个四输入与非门IP
- IP调用：IP核在其他工程中例化调用

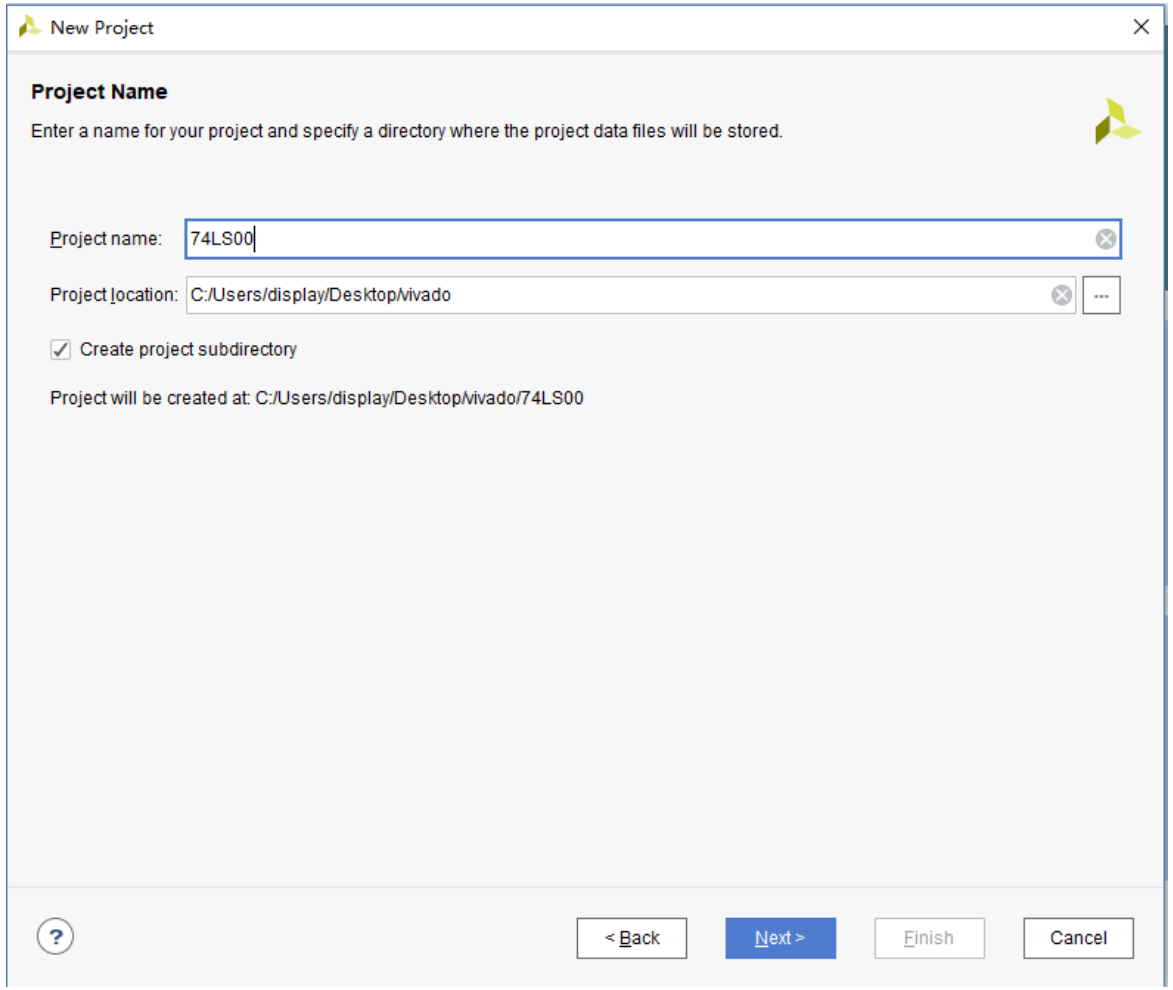
IP设计

- 创建vivado工程



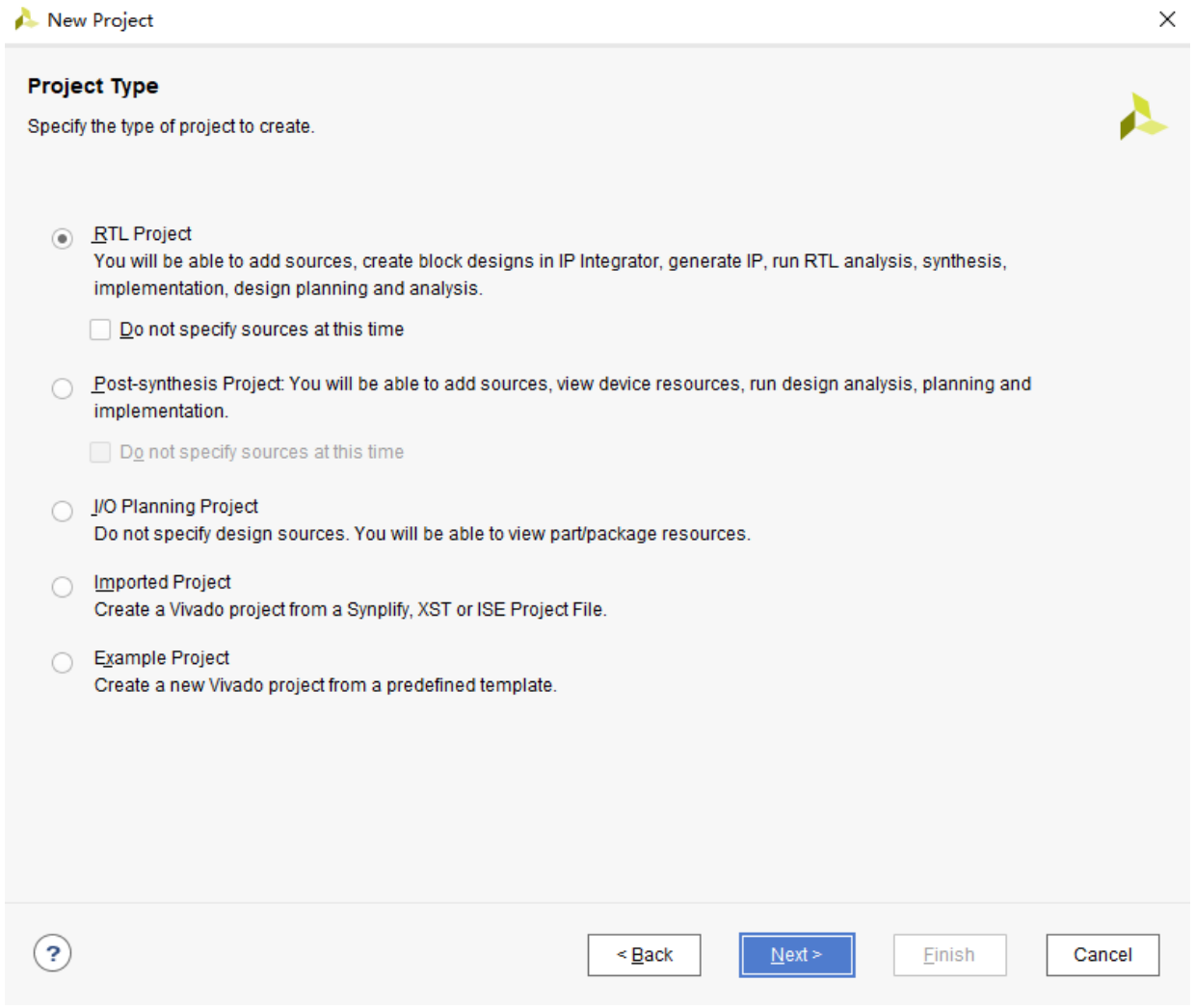
IP设计

- 选择工程文件位置以及工程名



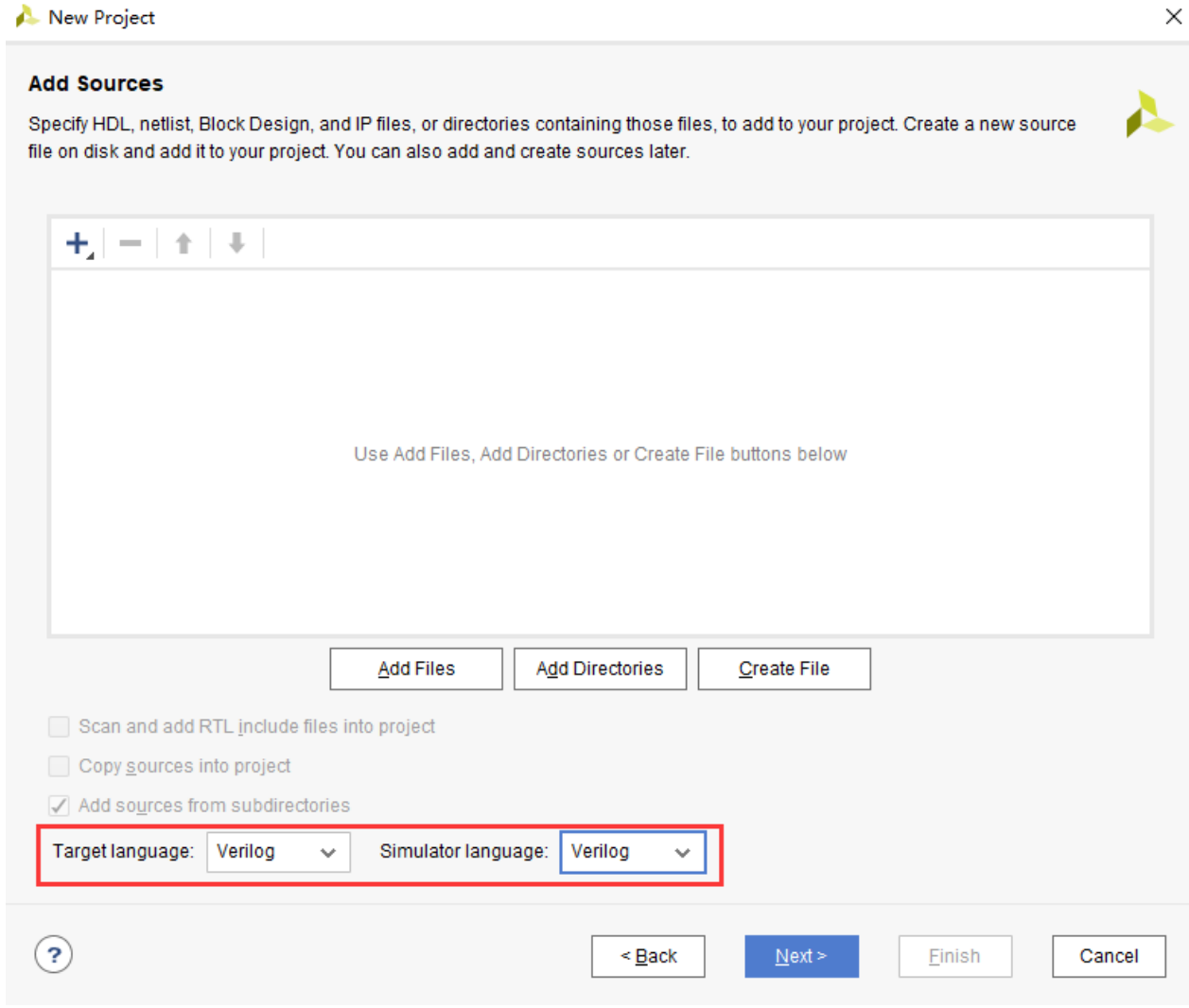
IP设计

- 选择第一个RTL project即可



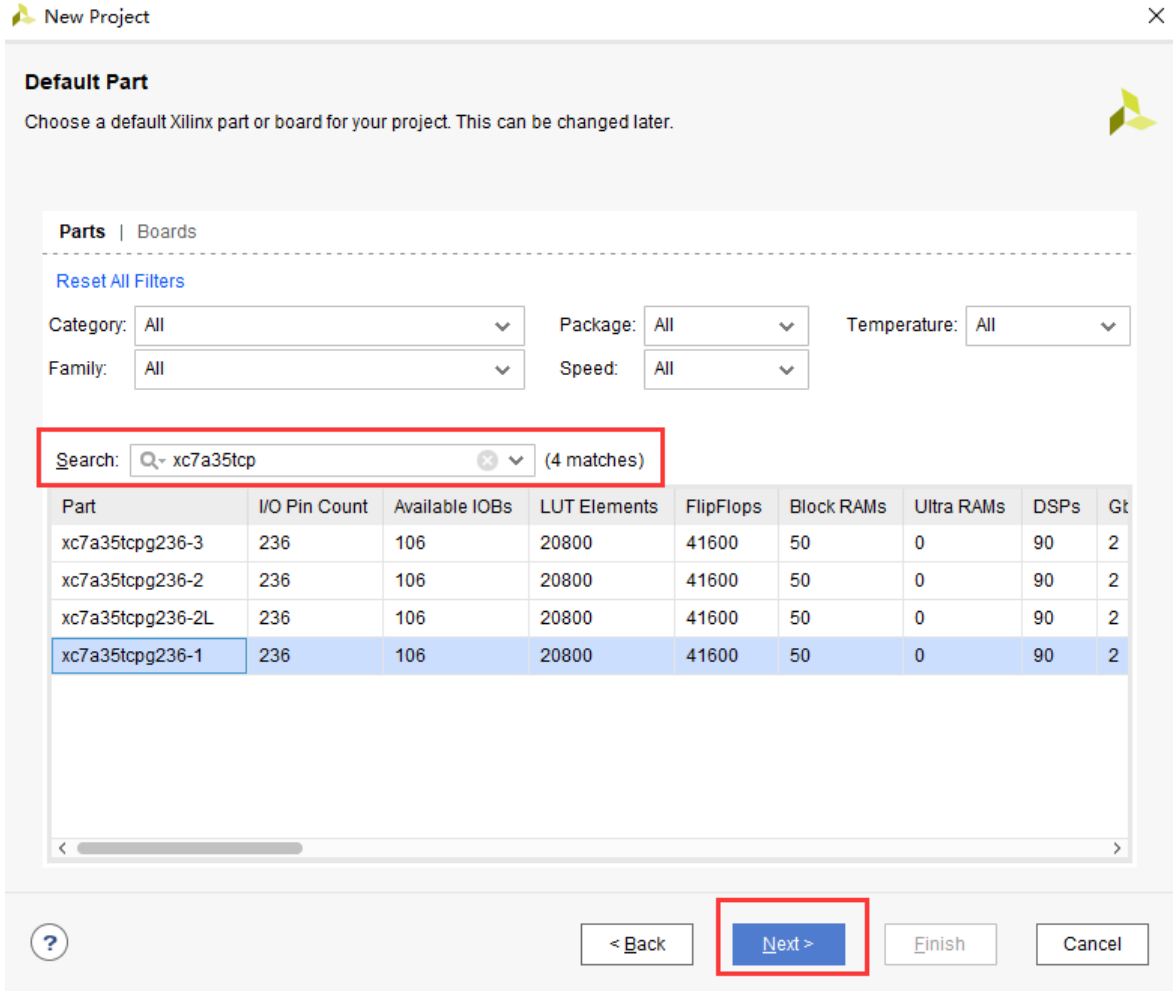
IP设计

- 选择语言为verilog



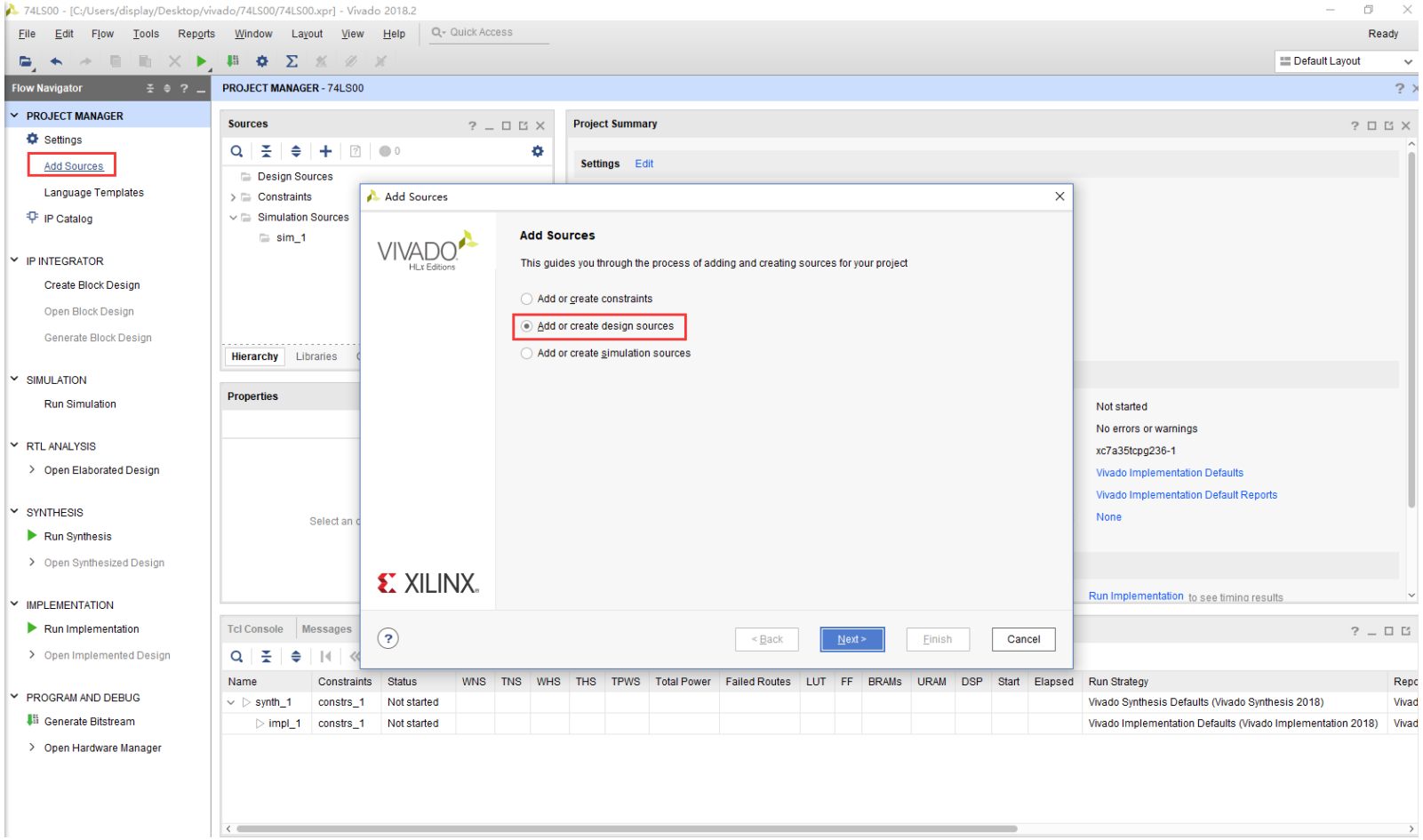
IP设计

- 选择板卡芯片型号



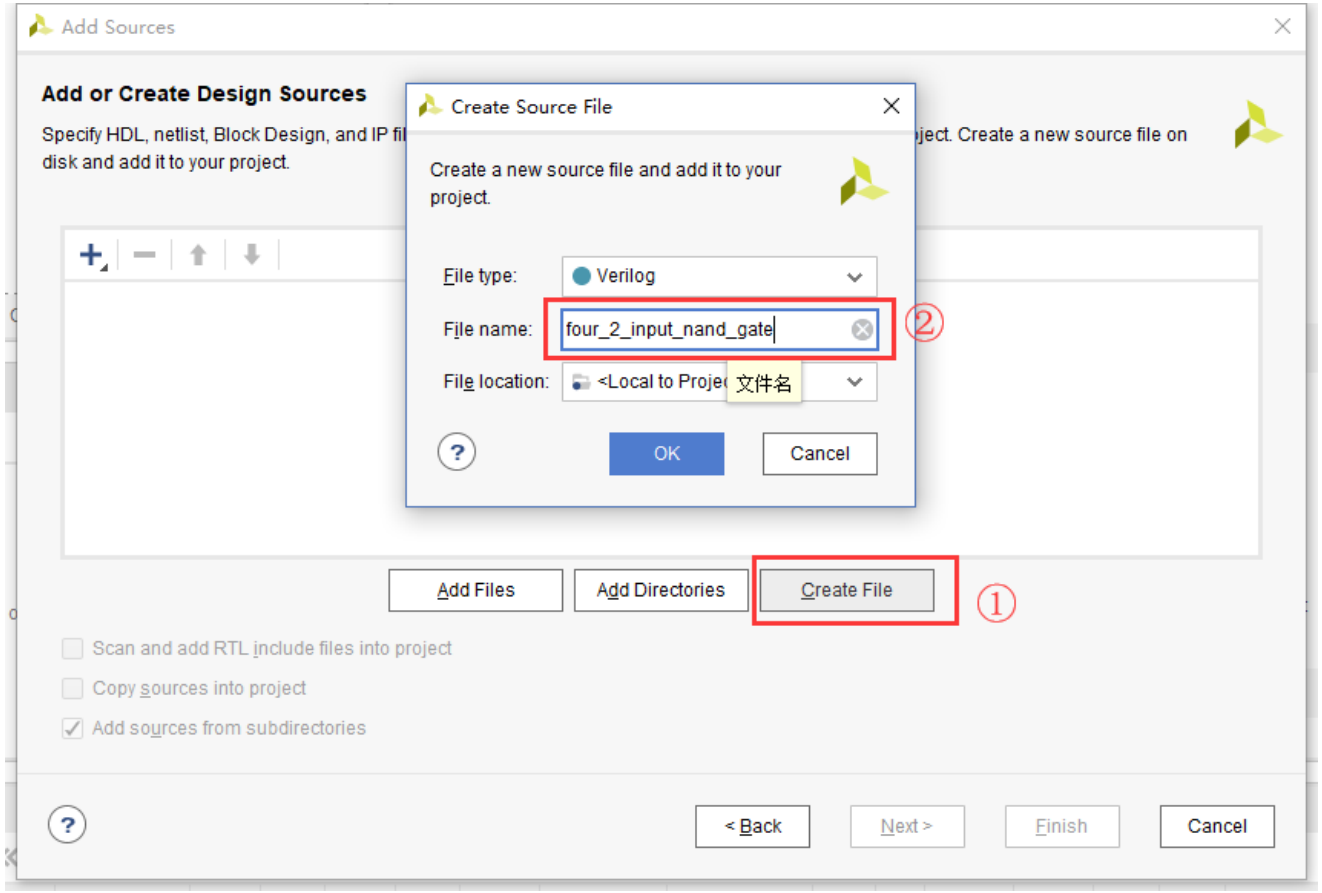
IP设计

- 添加源文件


74LS00 - [C:/Users/display/Desktop/vivado/74LS00/74LS00.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - 74LS00
Sources
Design Sources
Constraints
Simulation Sources
sim_1
Hierarchy
Libraries
Properties
Project Summary
Settings Edit
Not started
No errors or warnings
xc7a35tcpg236-1
Vivado Implementation Defaults
Vivado Implementation Default Reports
None
Run Implementation to see timing results
Add Sources
VIVADO HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel
Tcl Console
Messages
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAMs URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2018)
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2018)

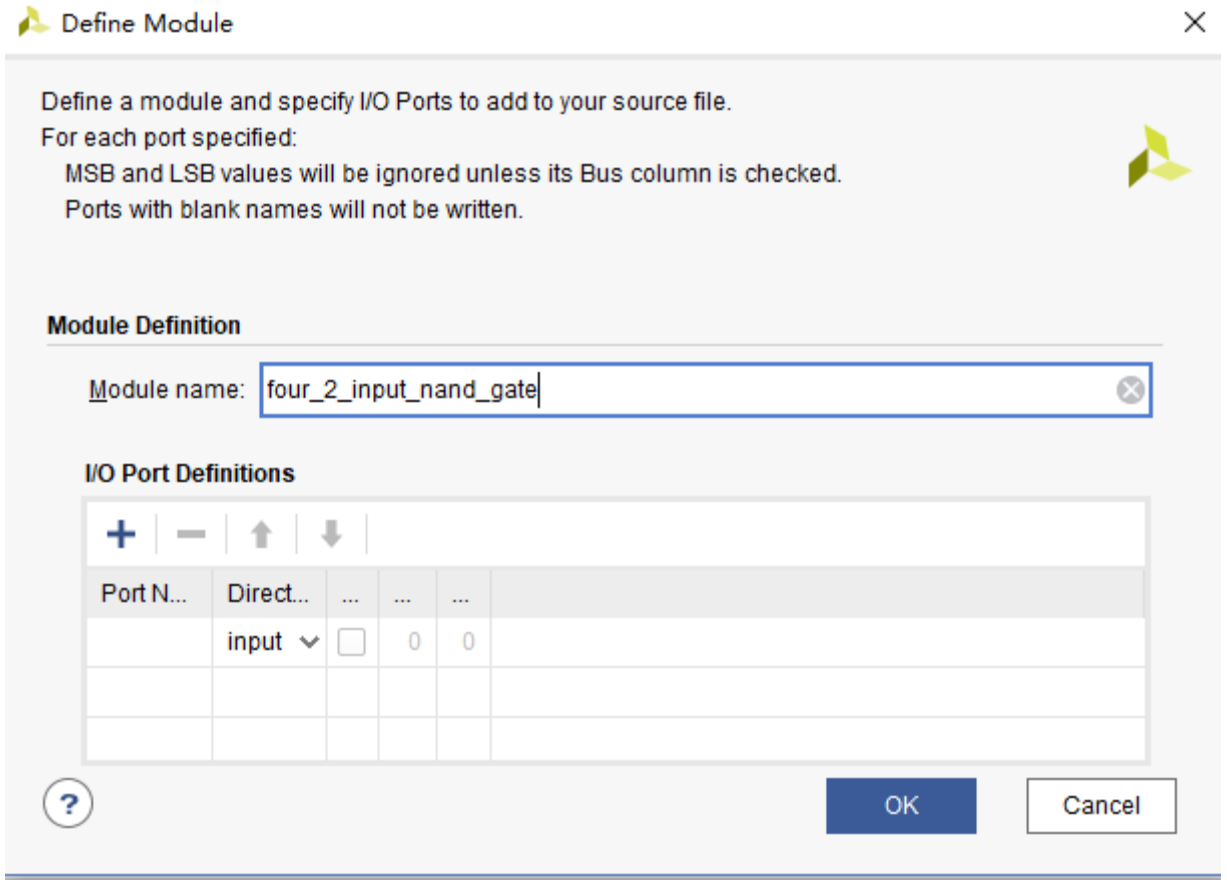
IP设计

- 源文件名称


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP fi
disk and add it to your project.
ject. Create a new source file on
Create Source File
Create a new source file and add it to your project.
File type:
Verilog
File name:
four_2_input_nand_gate
②
File location:
<Local to Proje
文件名
OK
Cancel
Add Files
Add Directories
Create File
①
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel

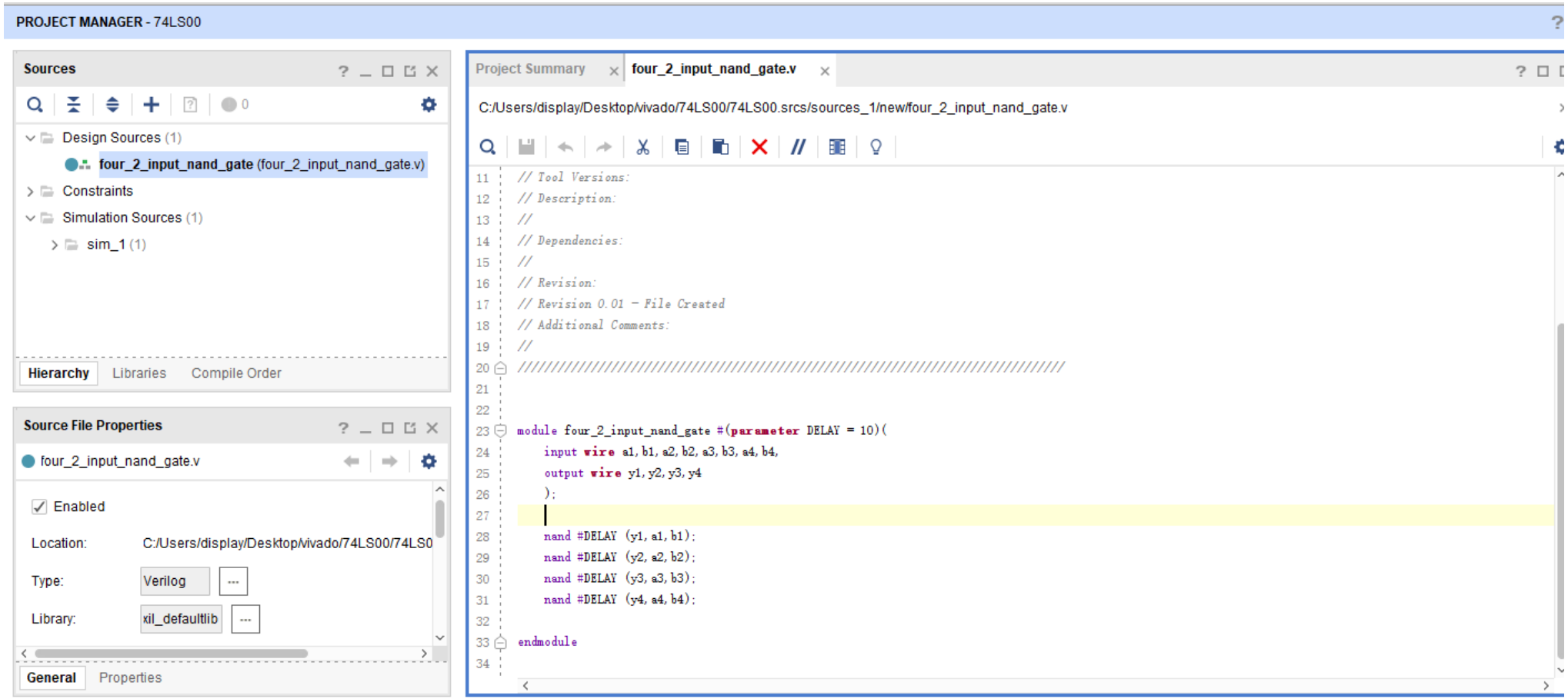
IP设计

- 可以添加源文件输出管脚，一般默认即可



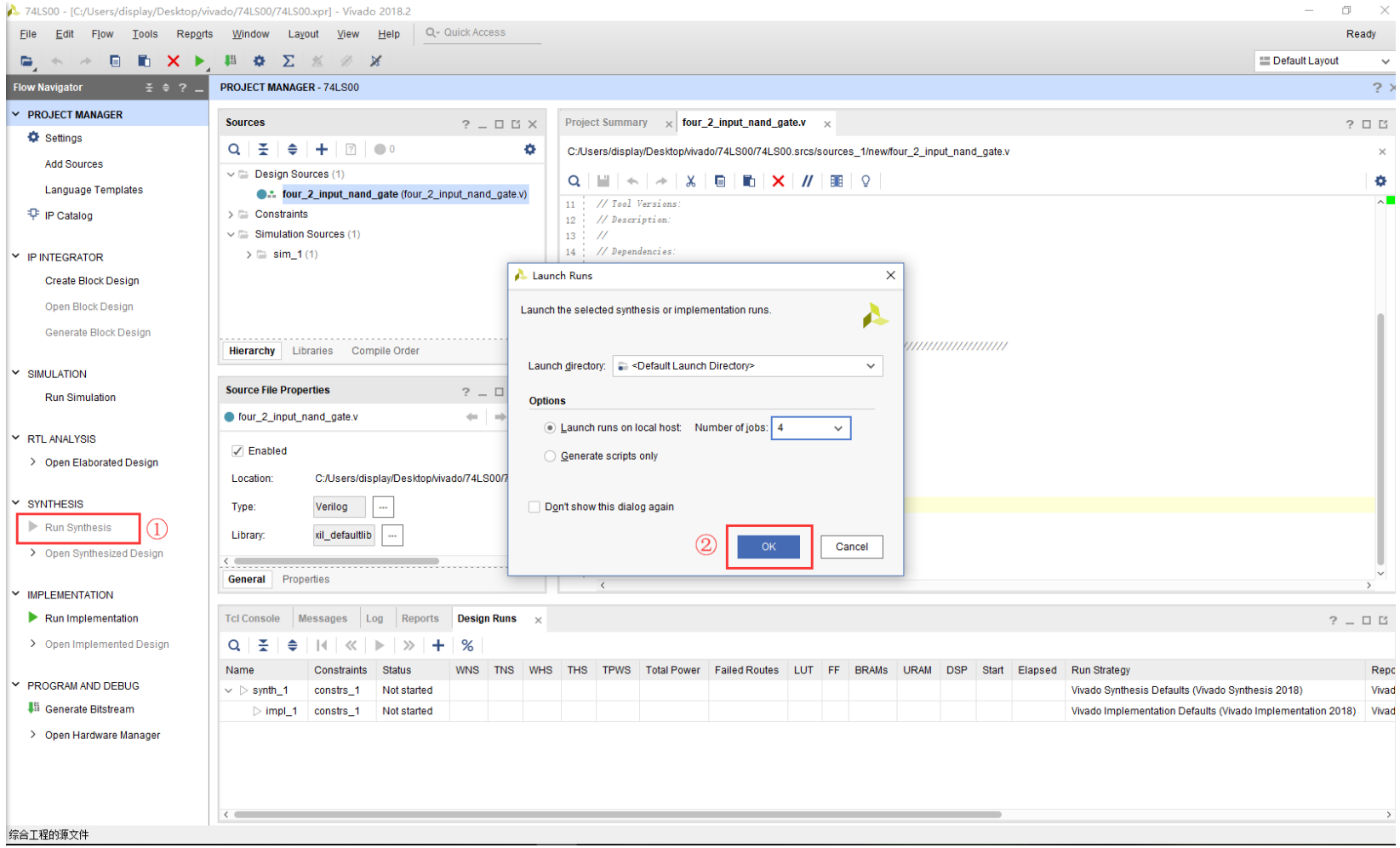
IP设计

- 编写源文件


PROJECT MANAGER - 74LS00
Sources
Design Sources (1)
four_2_input_nand_gate (four_2_input_nand_gate.v)
Constraints
Simulation Sources (1)
sim_1 (1)
Hierarchy
Libraries
Compile Order
Source File Properties
four_2_input_nand_gate.v
Enabled
Location:
C:/Users/display/Desktop/vivado/74LS00/74LS0
Type:
Verilog
Library:
xil_defaultlib
General
Properties
Project Summary
four_2_input_nand_gate.v
C:/Users/display/Desktop/vivado/74LS00/74LS00.srcs/sources_1/new/four_2_input_nand_gate.v
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module four_2_input_nand_gate #(parameter DELAY = 10)(
input wire a1, b1, a2, b2, a3, b3, a4, b4,
output wire y1, y2, y3, y4
);
nand #DELAY (y1, a1, b1);
nand #DELAY (y2, a2, b2);
nand #DELAY (y3, a3, b3);
nand #DELAY (y4, a4, b4);
endmodule

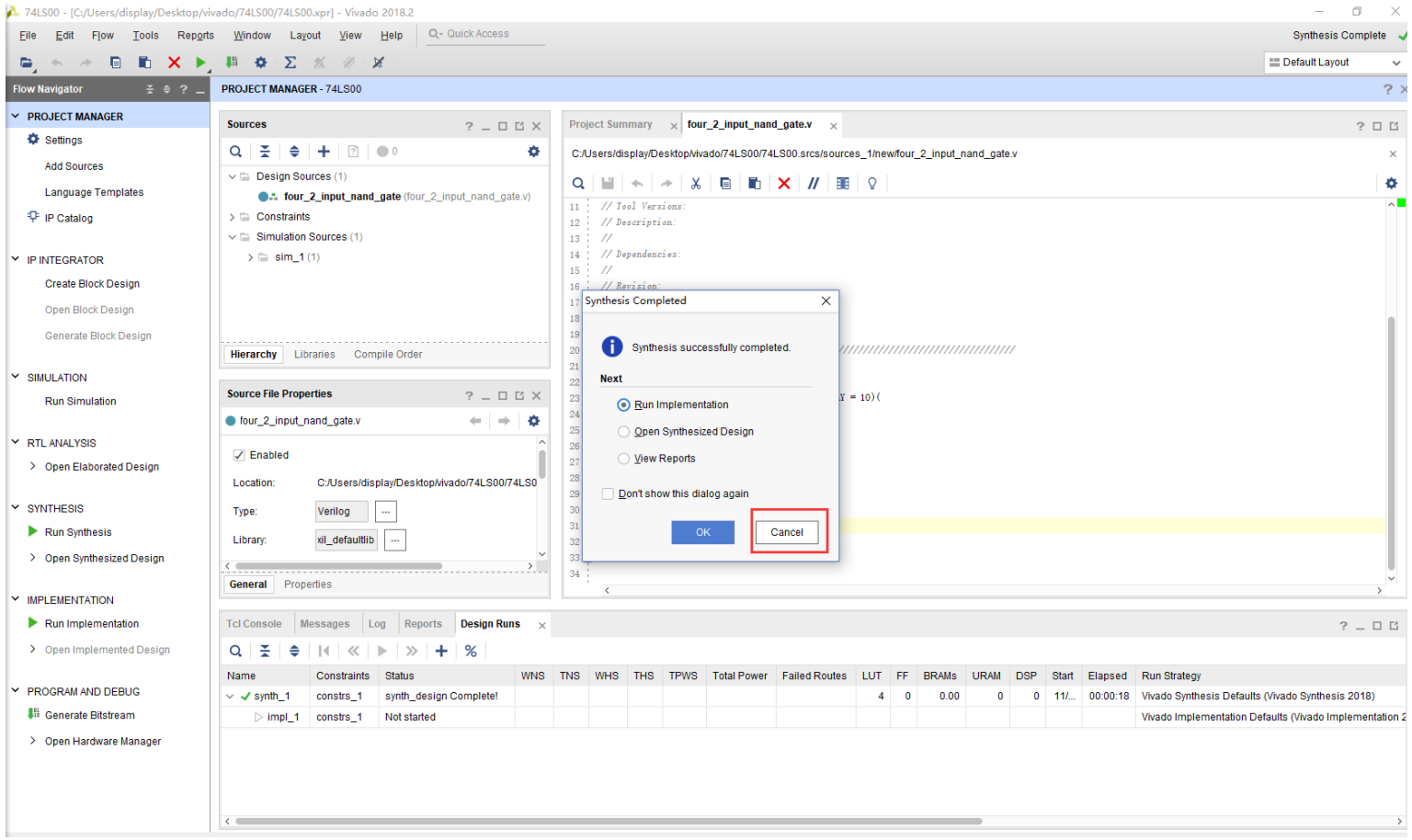
IP设计

- 源文件综合编译



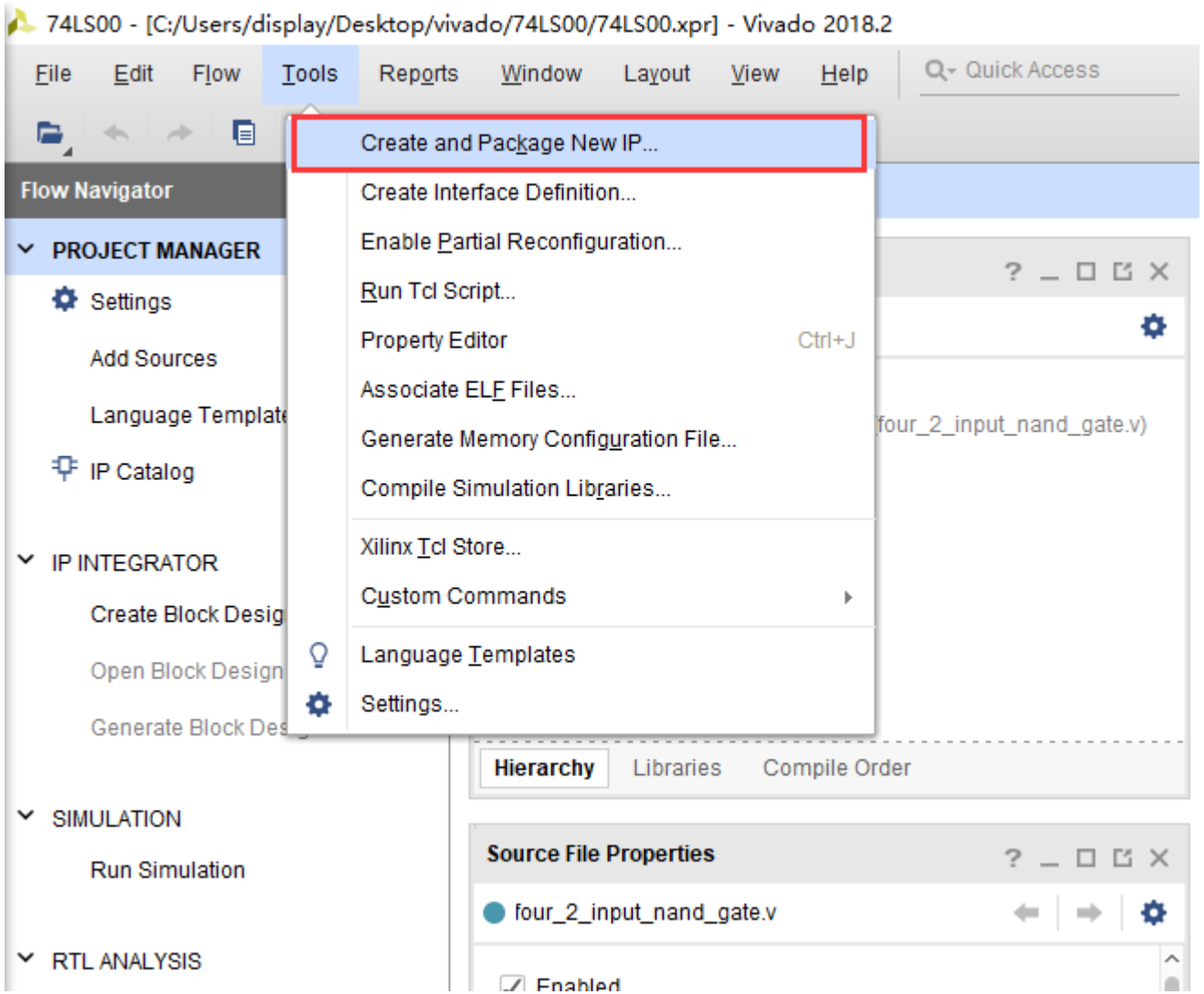
IP设计

- 创建IP不需要implement，所以cancel即可



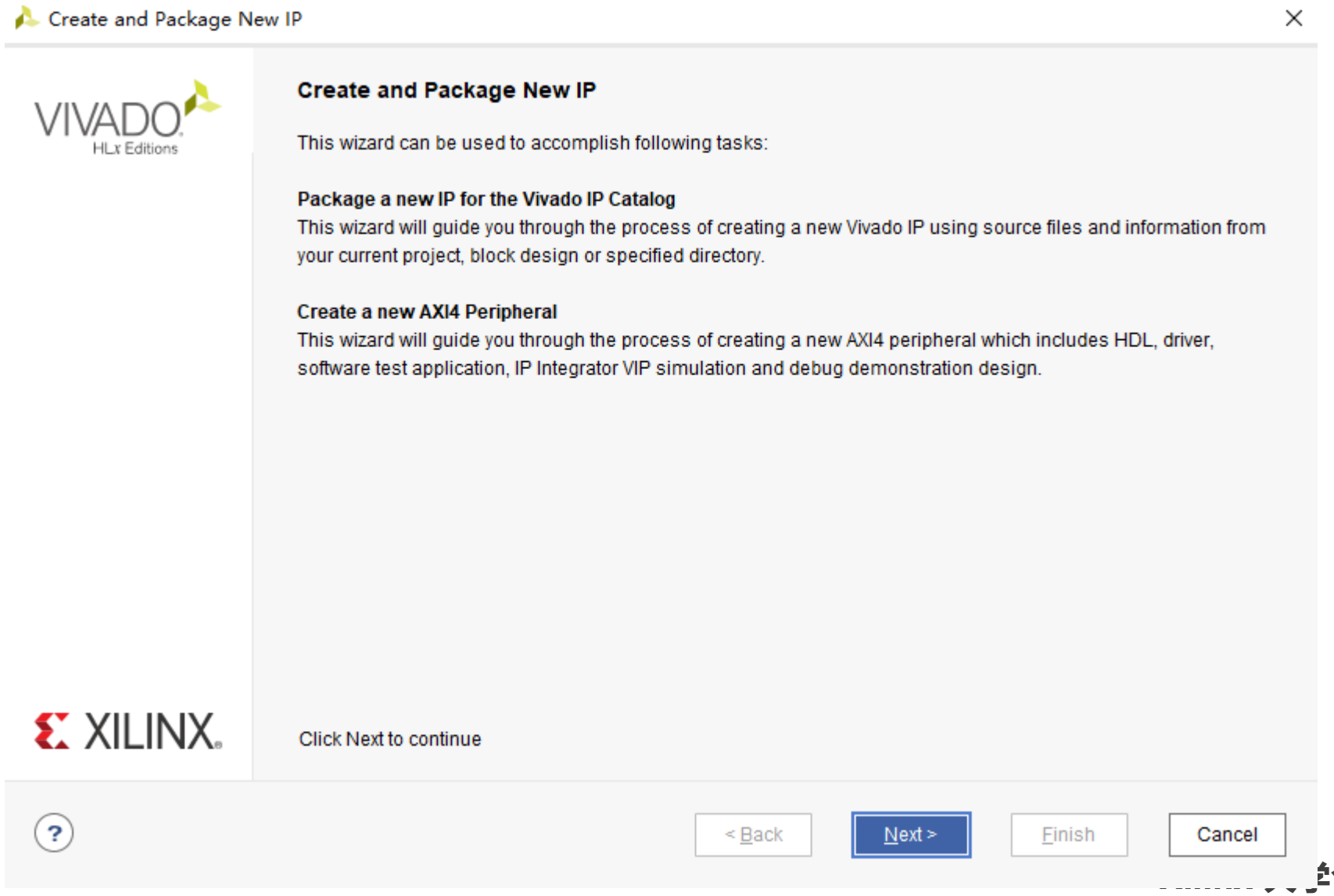
IP设计

- 点击Tools下的Create and Package New IP…创建IP



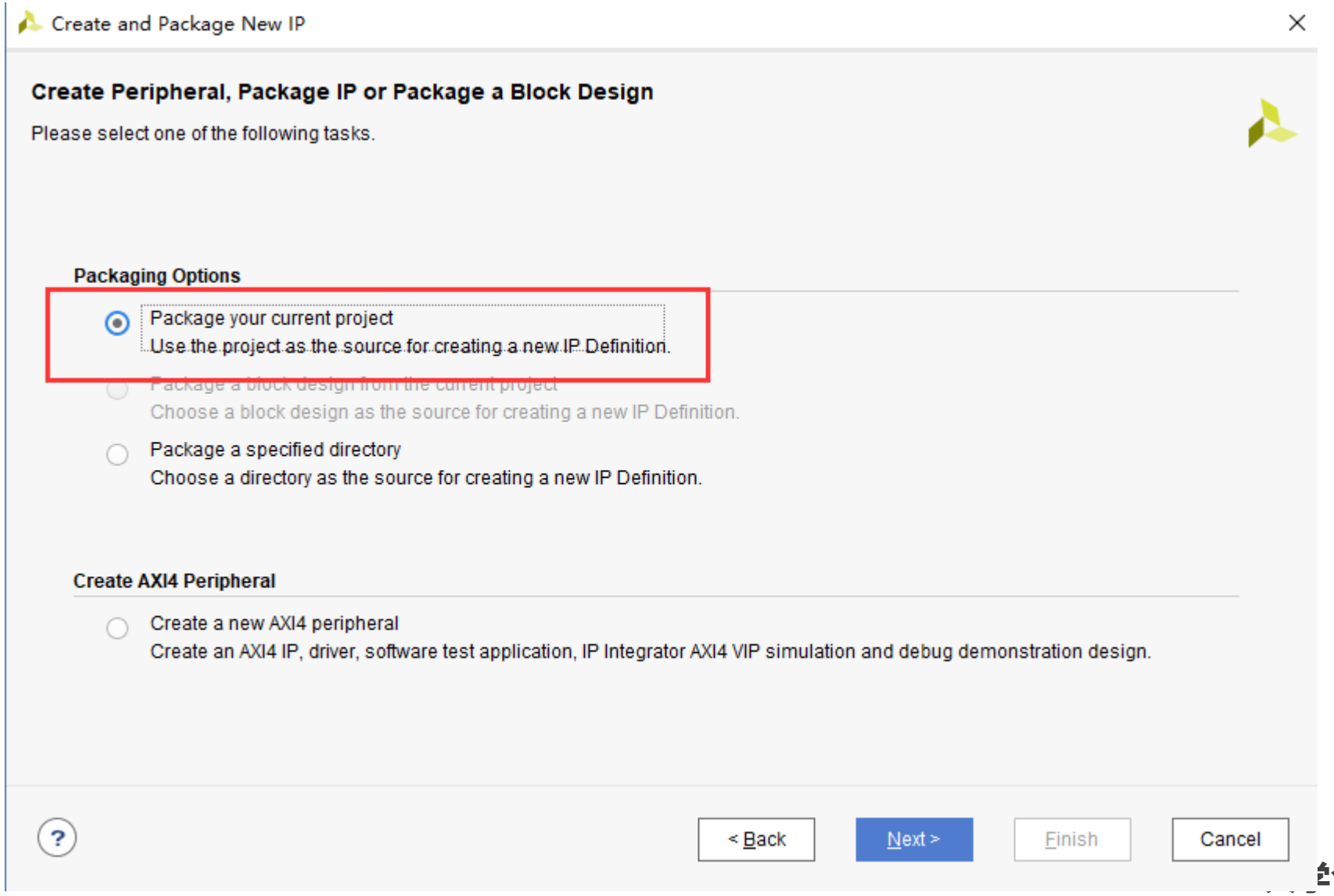
IP设计

- 默认next


Create and Package New IP
VIVADO
HLx Editions
Create and Package New IP
This wizard can be used to accomplish following tasks:
Package a new IP for the Vivado IP Catalog
This wizard will guide you through the process of creating a new Vivado IP using source files and information from your current project, block design or specified directory.
Create a new AXI4 Peripheral
This wizard will guide you through the process of creating a new AXI4 peripheral which includes HDL, driver, software test application, IP Integrator VIP simulation and debug demonstration design.
XILINX
Click Next to continue
< Back
Next >
Finish
Cancel

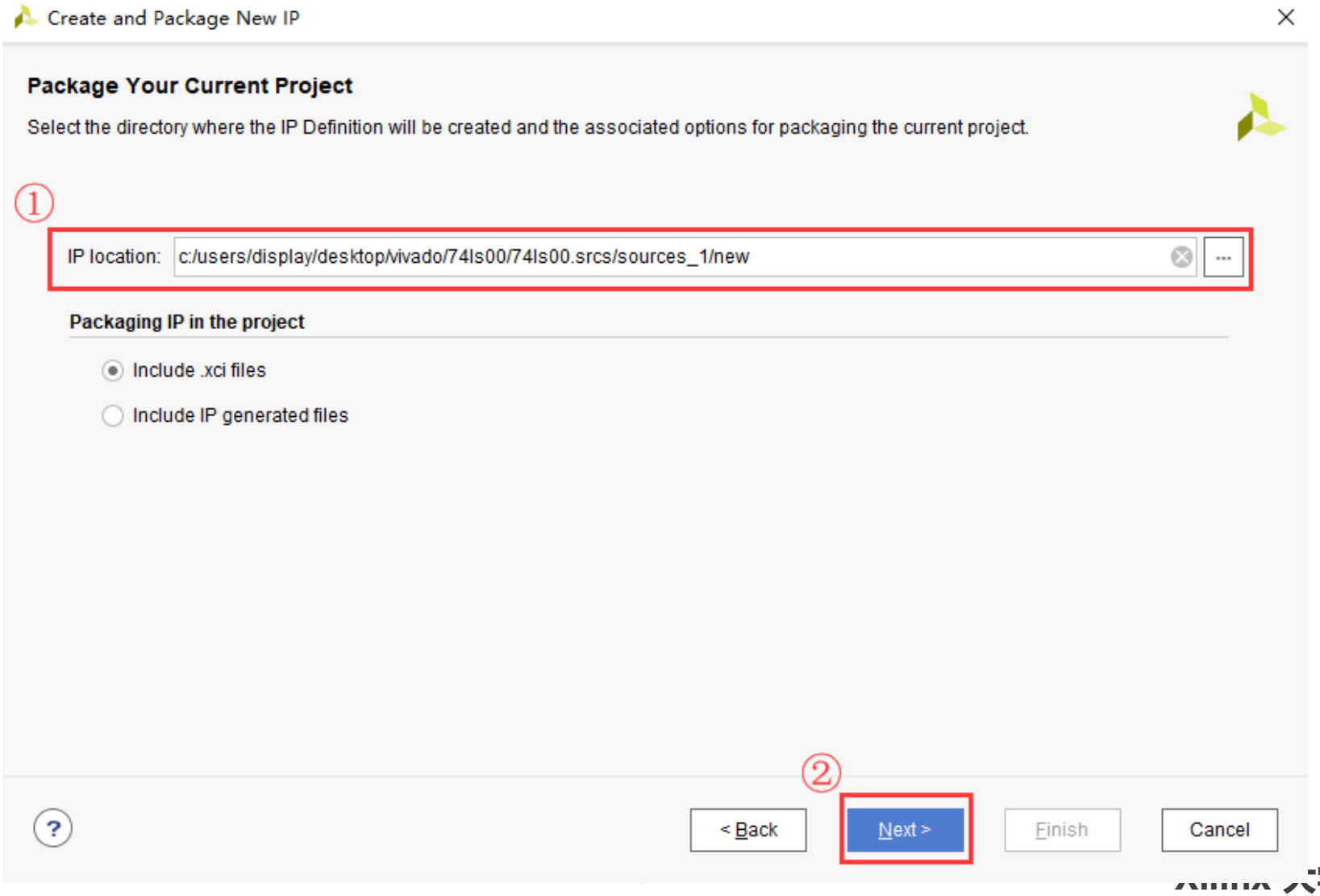
IP设计

- 选择第一个，封装当前工程为IP



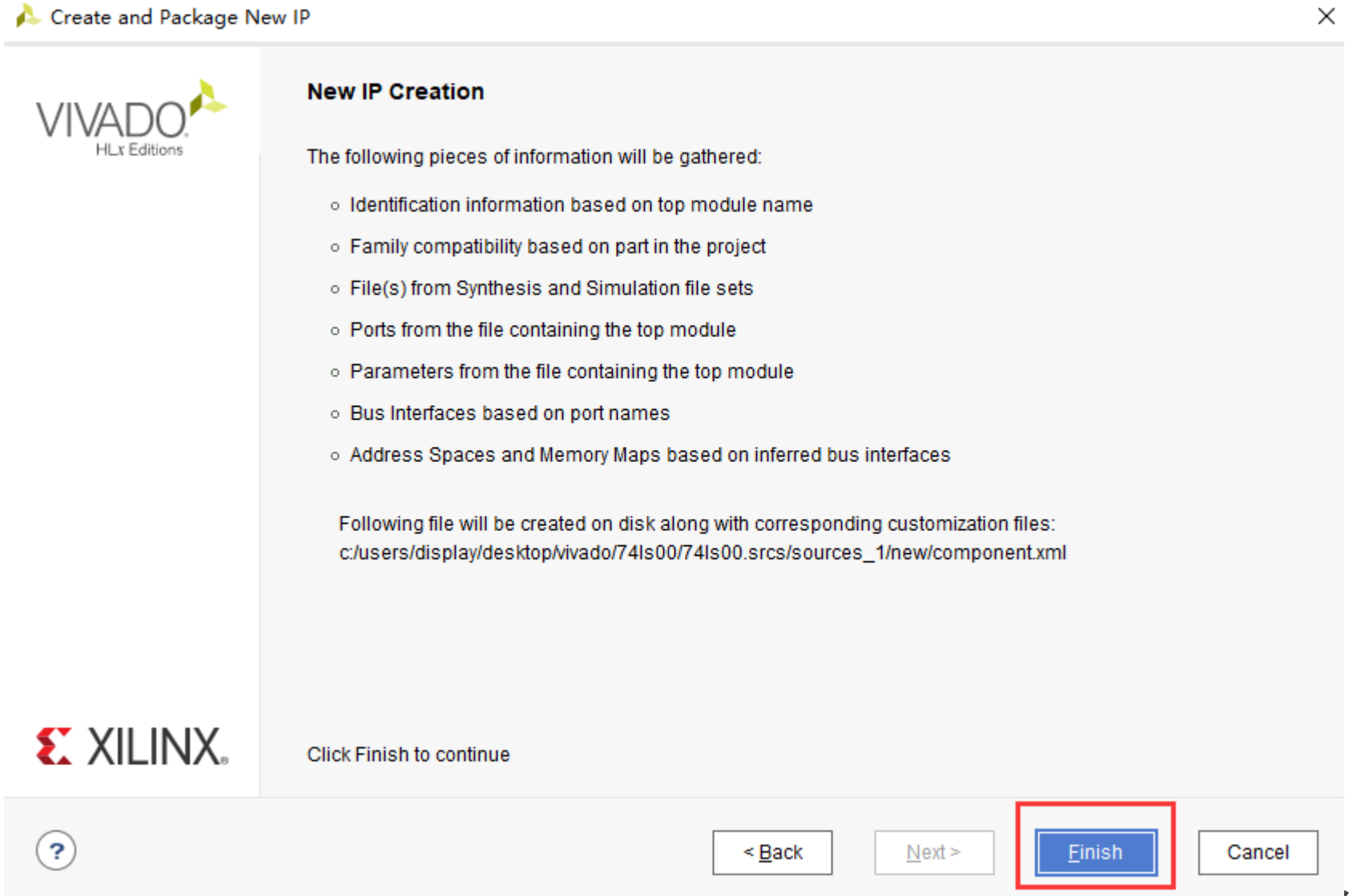
IP设计

- 选择IP文件的位置，后面调用IP要选择此位置



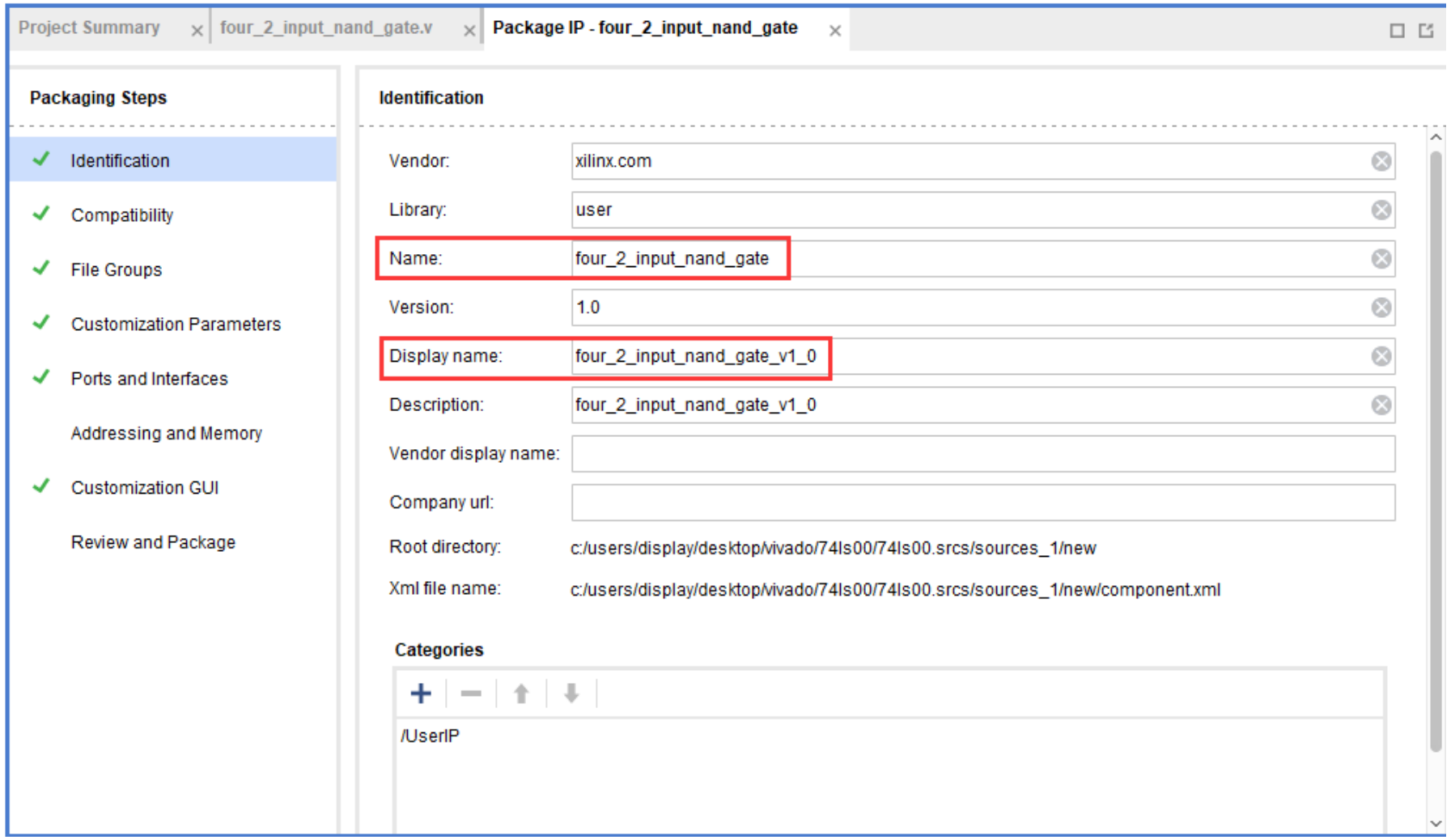
IP设计

- 默认finish完成IP的信息设置



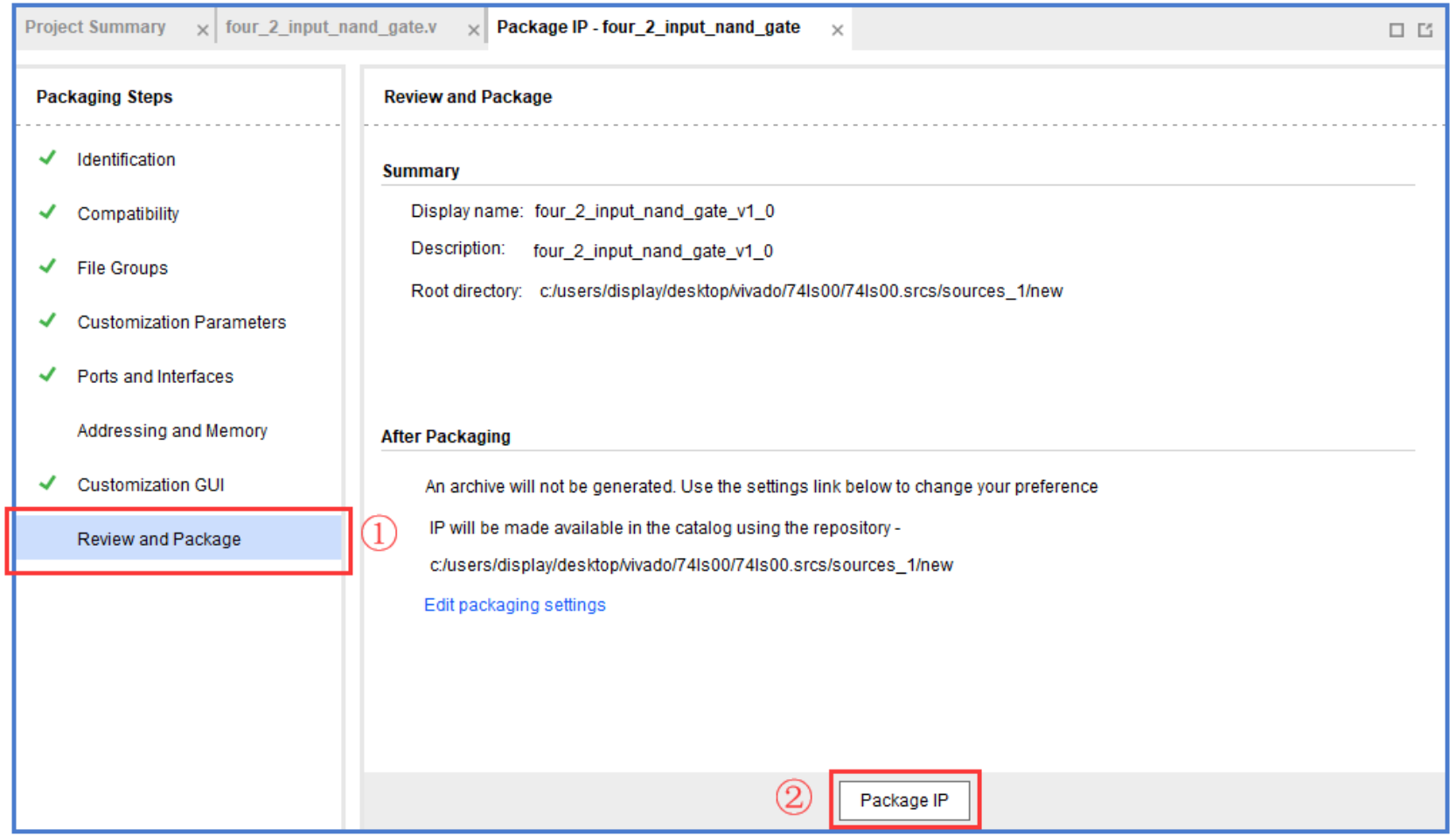
IP设计

- 选择IP的name和display name



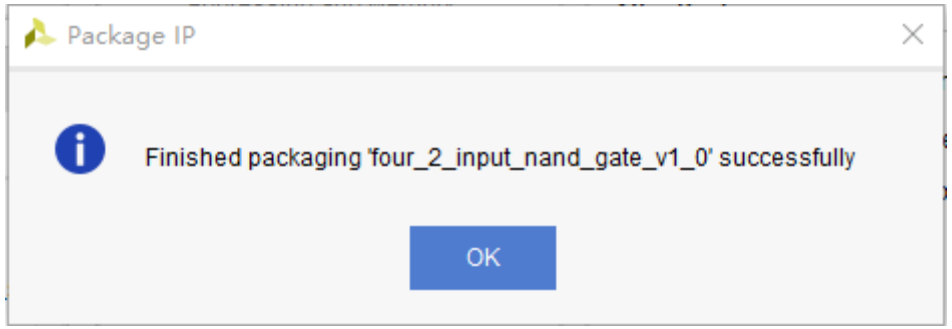
IP设计

- 点击review and package，然后点击Package IP



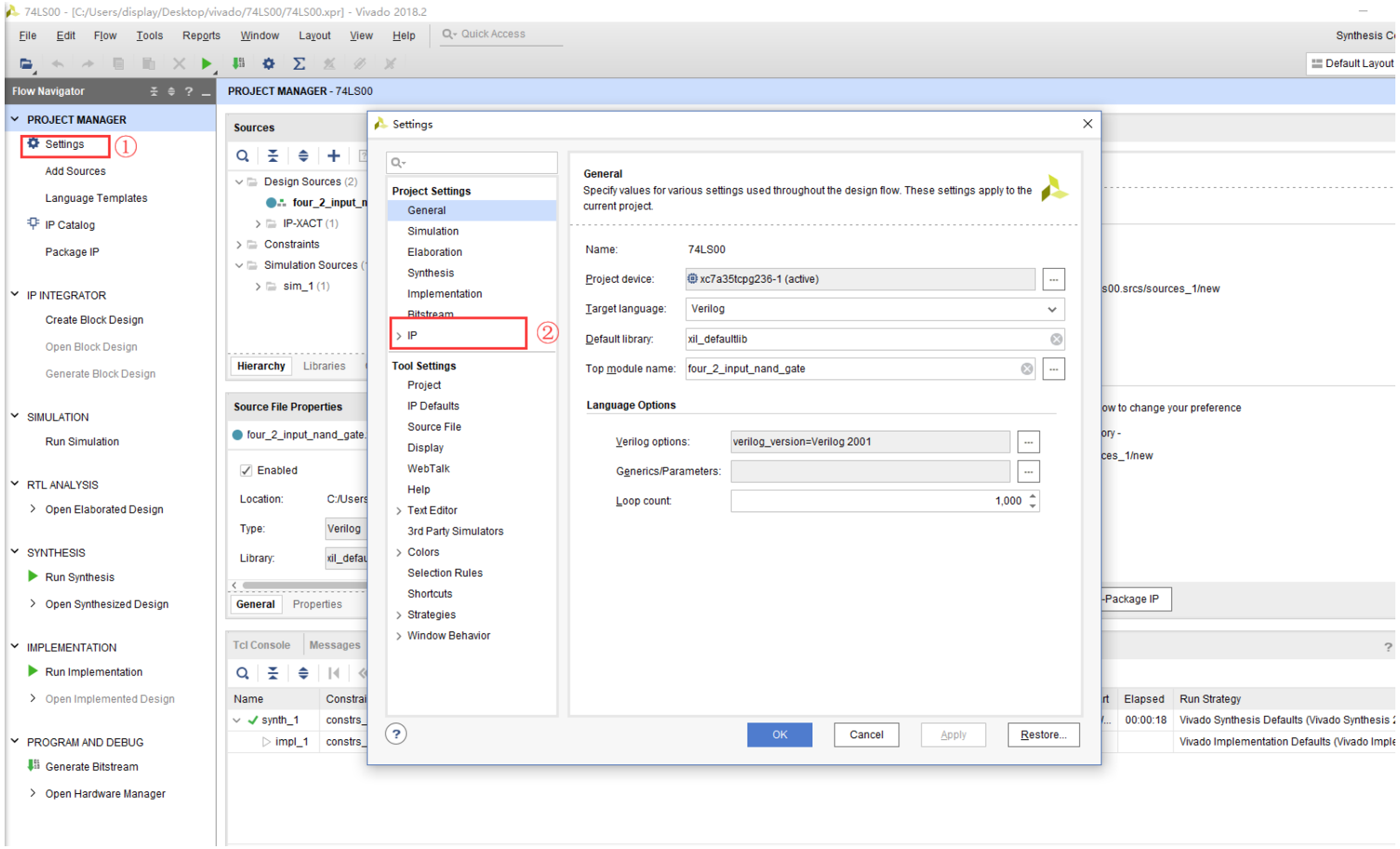
IP设计

- 创建成功


Package IP
Finished packaging 'four_2_input_nand_gate_v1_0' successfully
OK

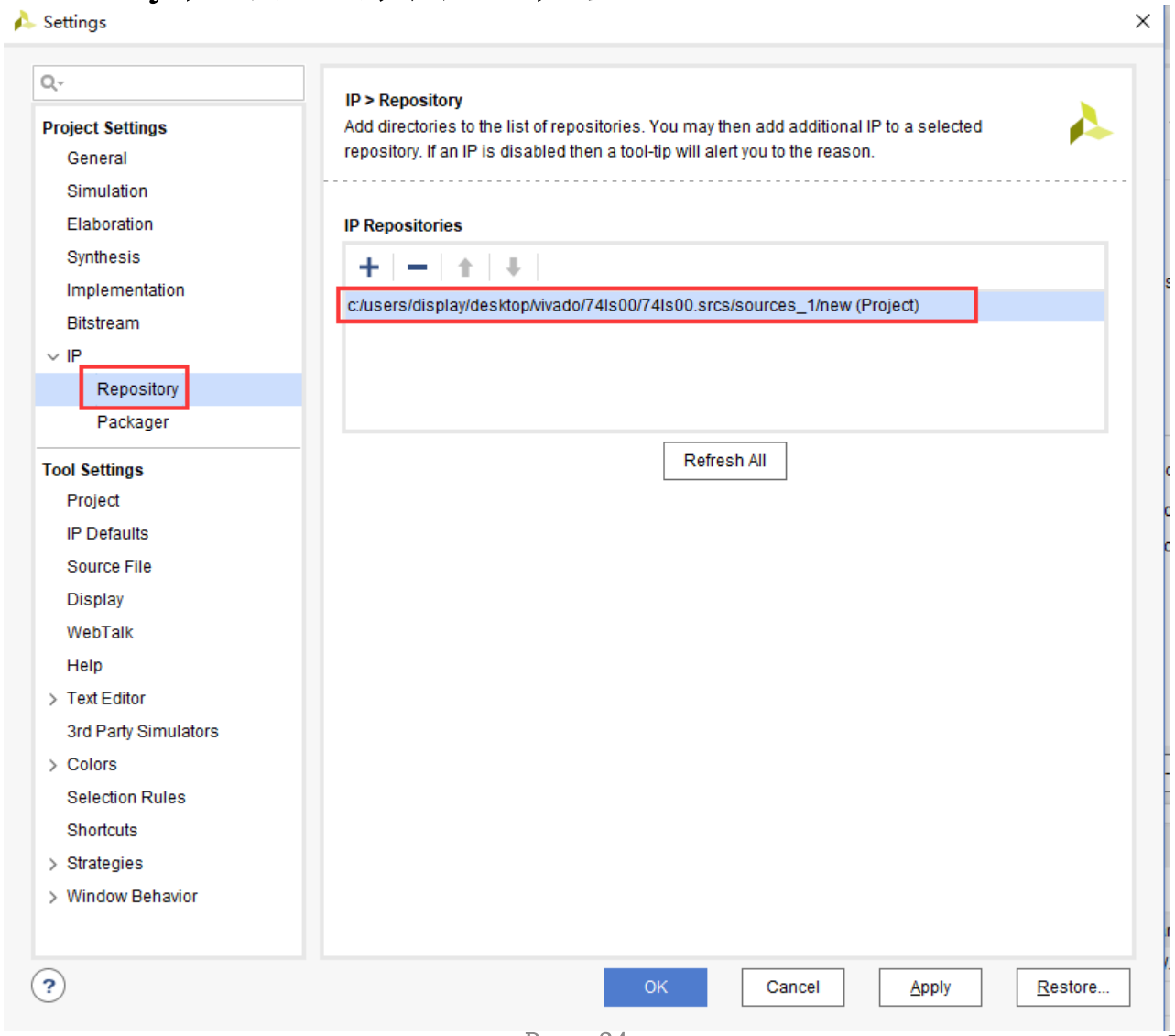
IP调用

- 打开要调用IP的工程，然后点击setting下的IP



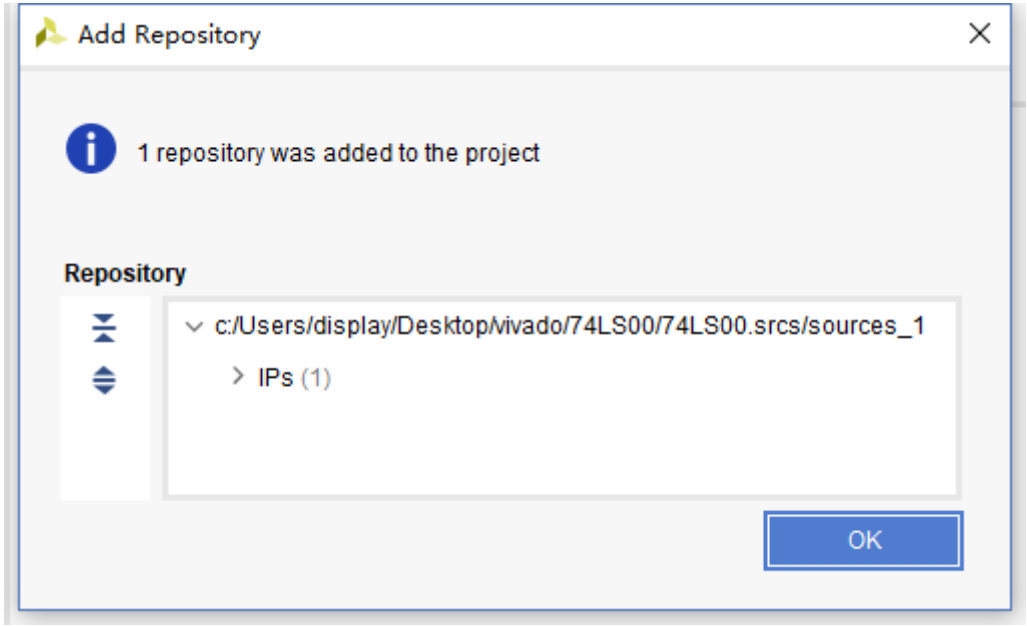
IP调用

- 点击IP下的Repository在右边添加IP位置



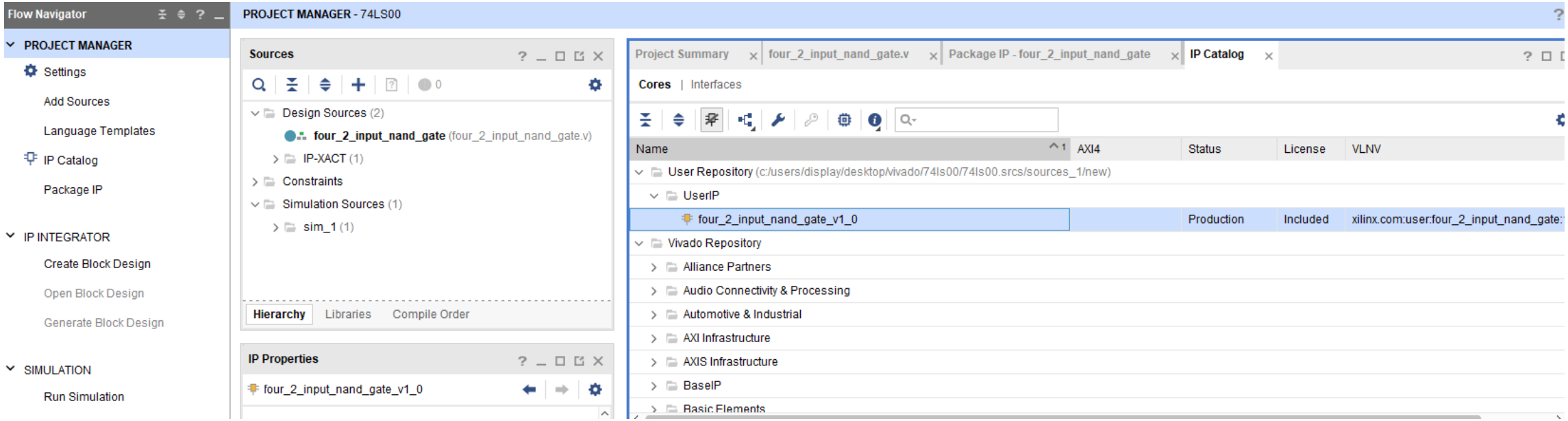
IP调用

- 添加位置时若弹出以下命令框，则表明是一个正确的IP



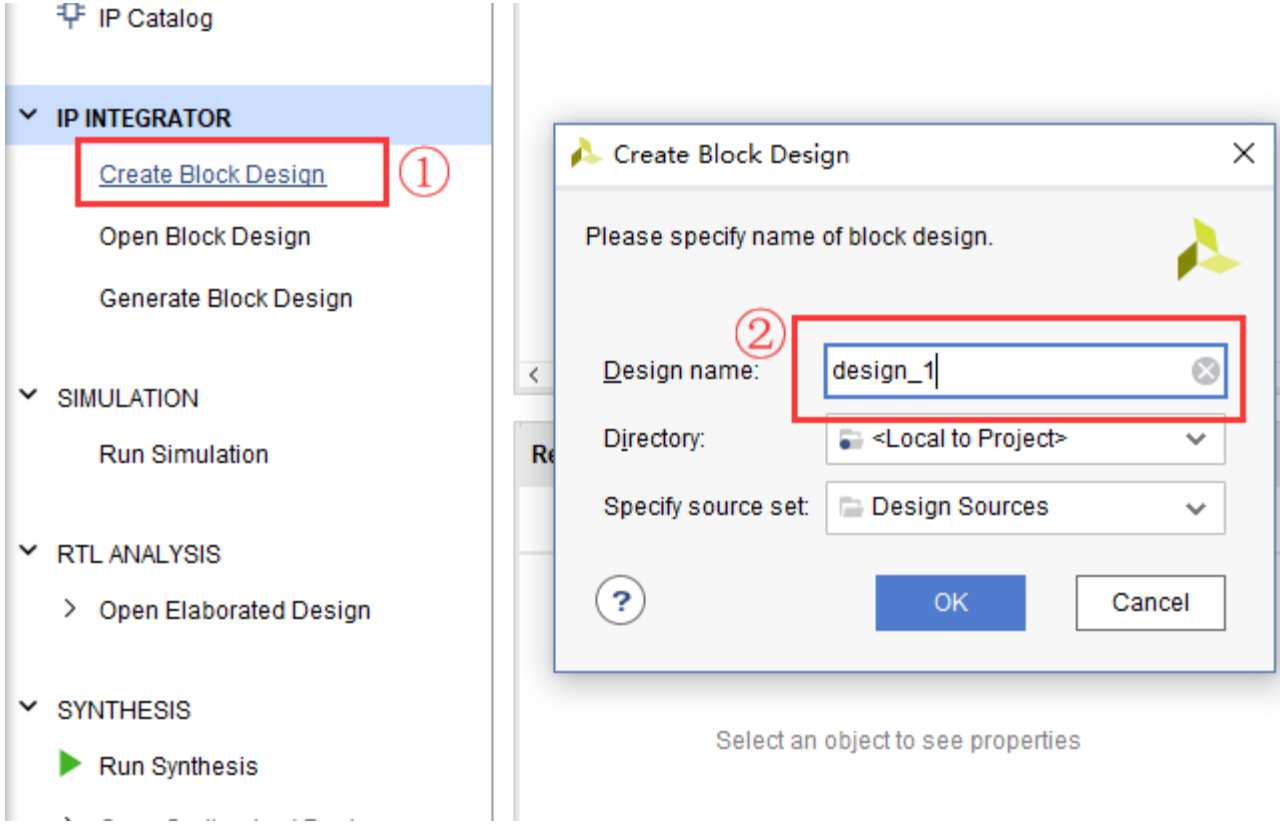
IP调用

- IP Catalog打开可以在UserIP下看见创建的IP，或者在命令框搜索IP的名称



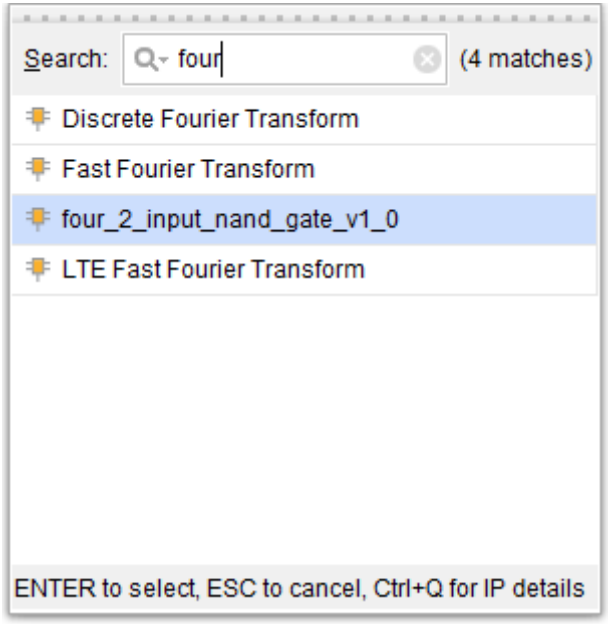
IP调用

- 创建Block Design并命名



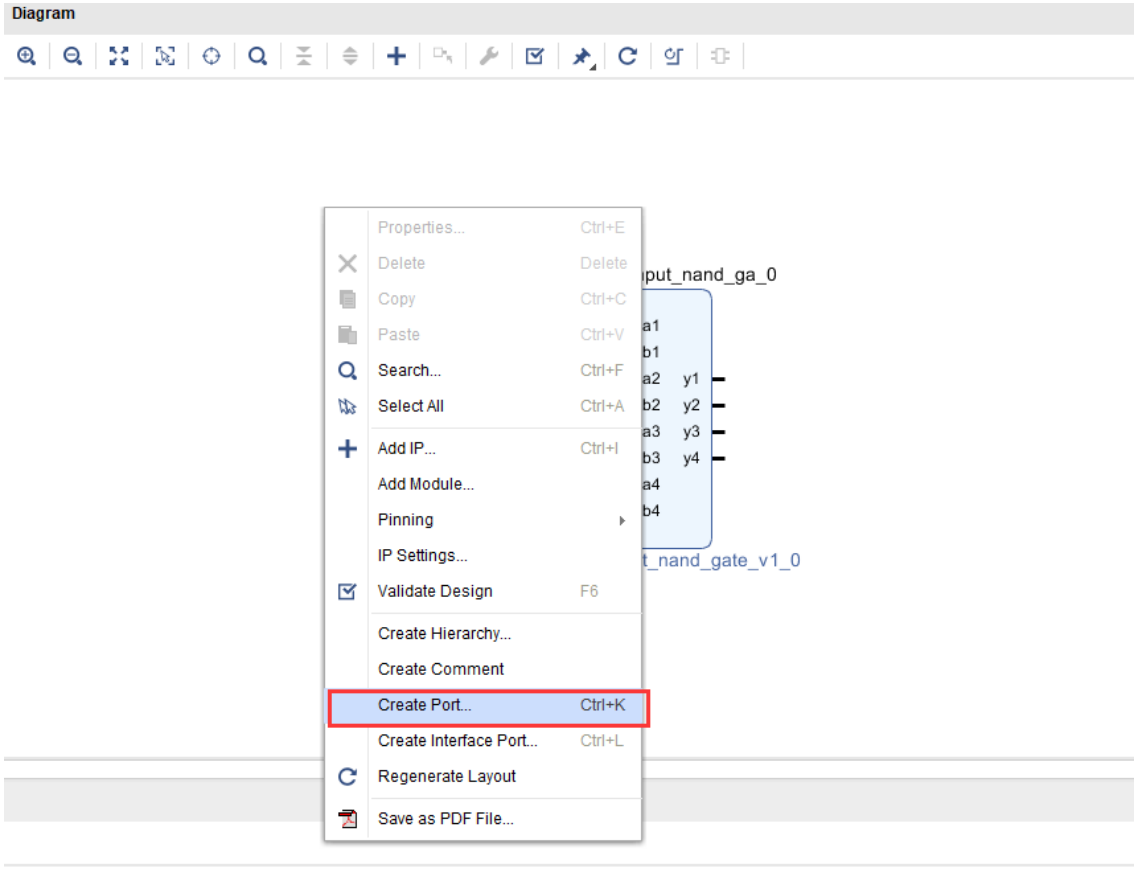
IP调用

- 调用刚刚添加到工程的IP



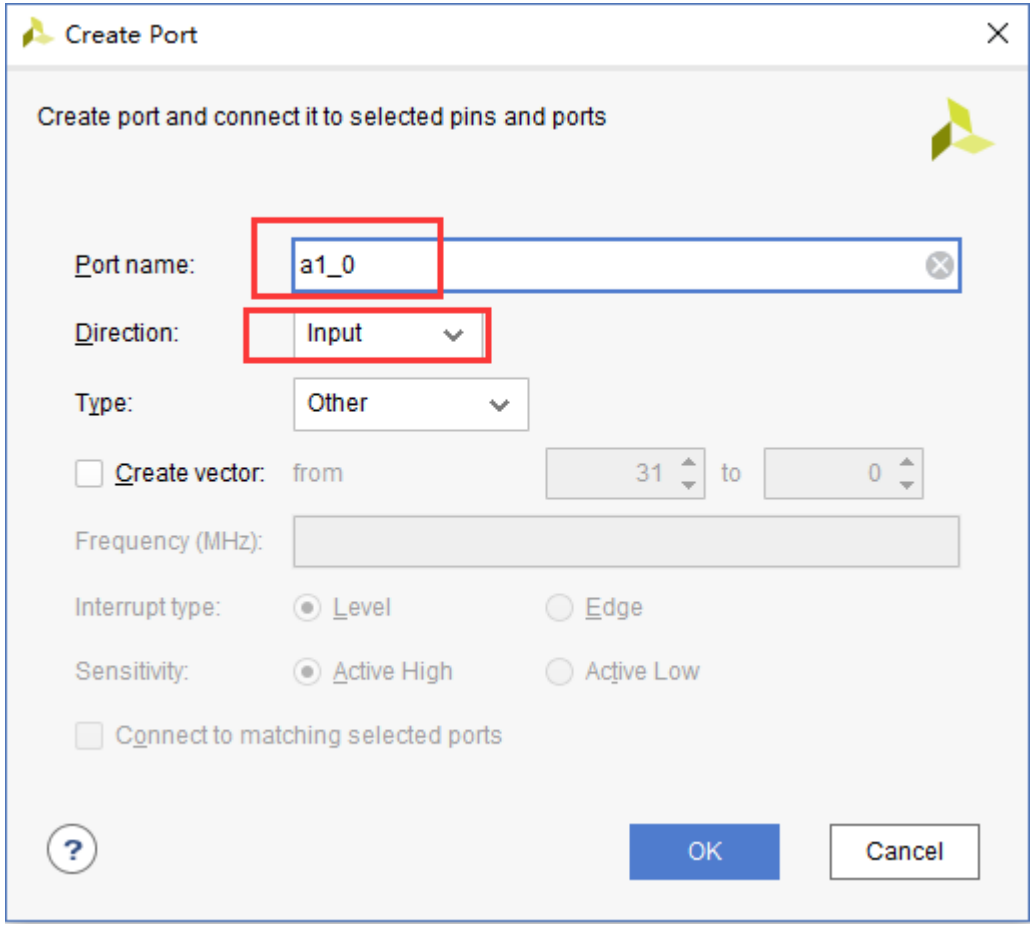
IP调用

- 然后在Block Design中添加Port



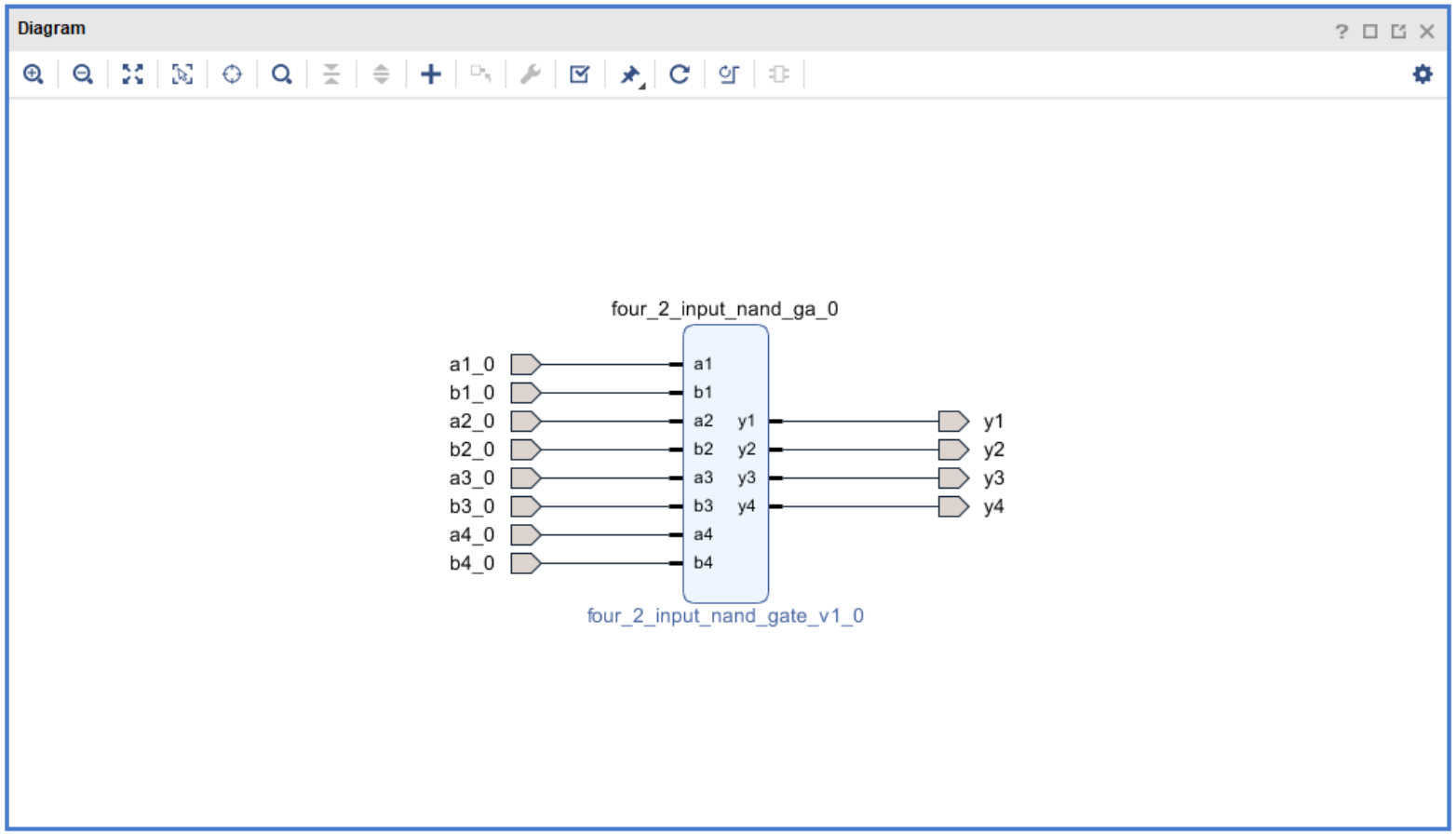
IP调用

- Port命名以及选择输入输出



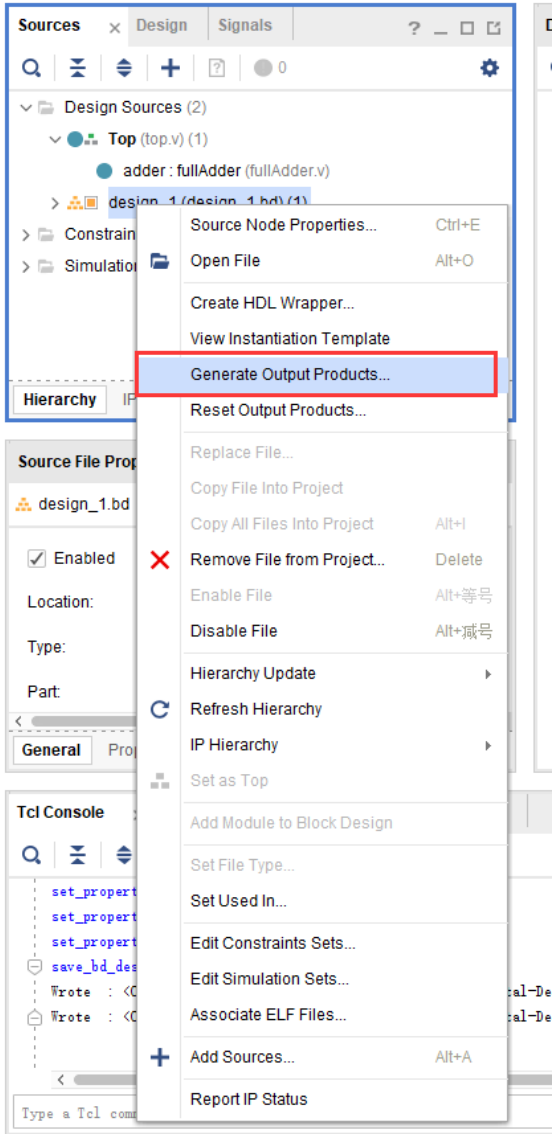
IP调用

- 完成以下的连线



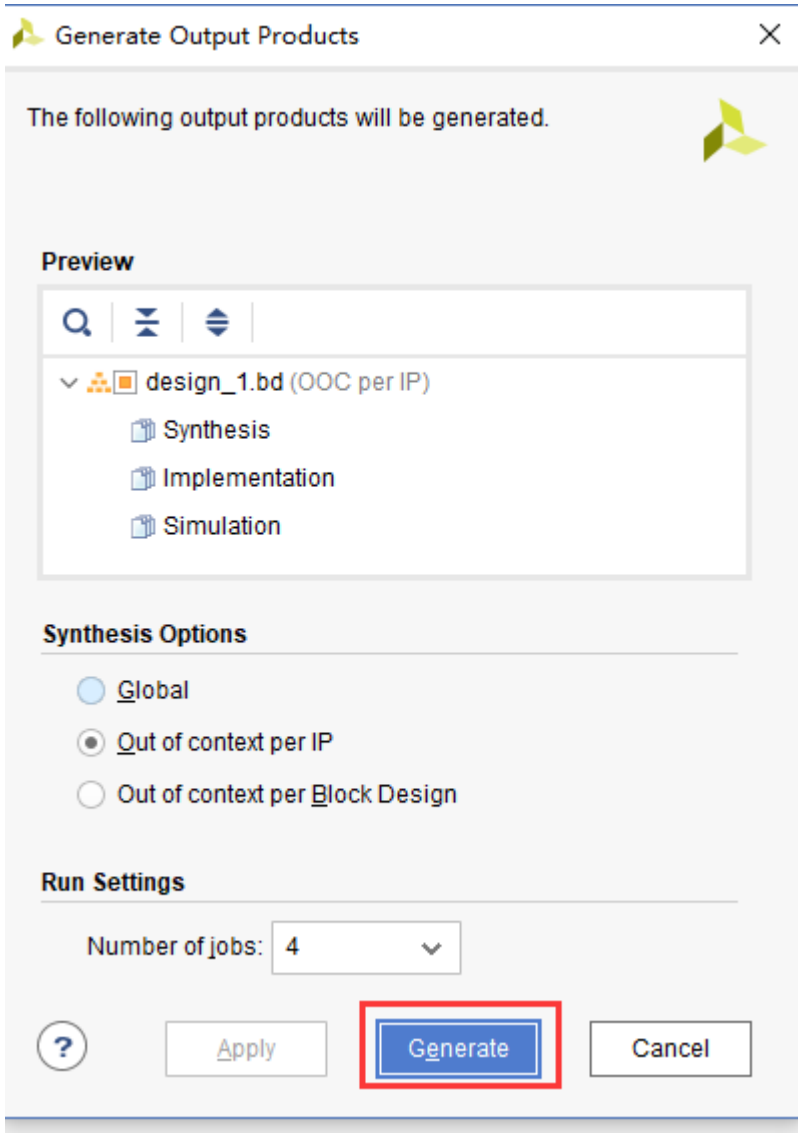
IP调用

- 右击Block Design后选择Generate Output Products…



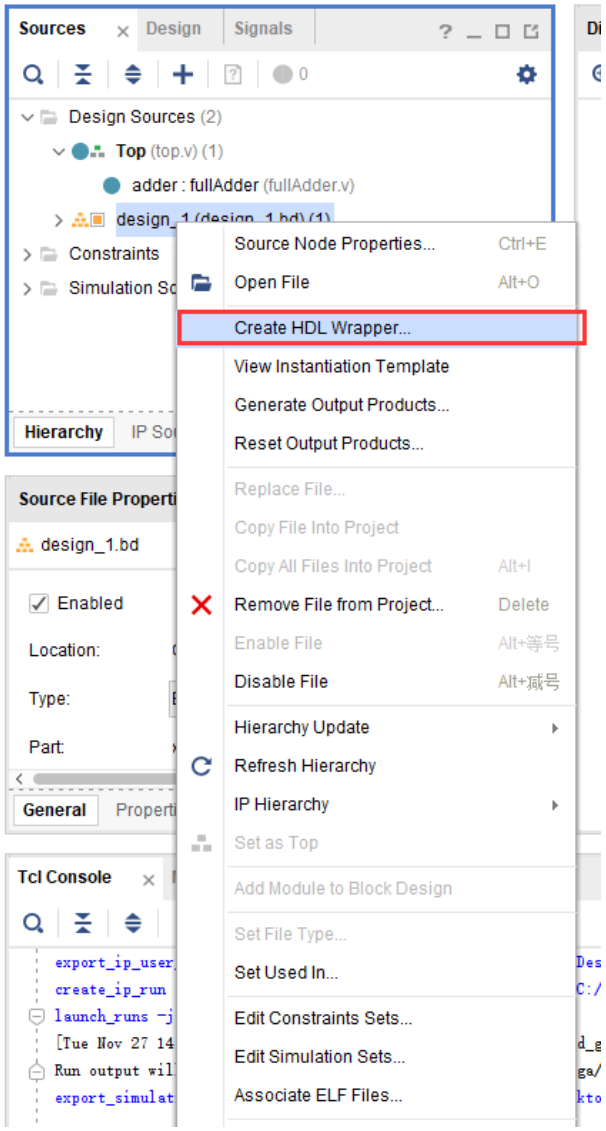
IP调用

- 默认Generate



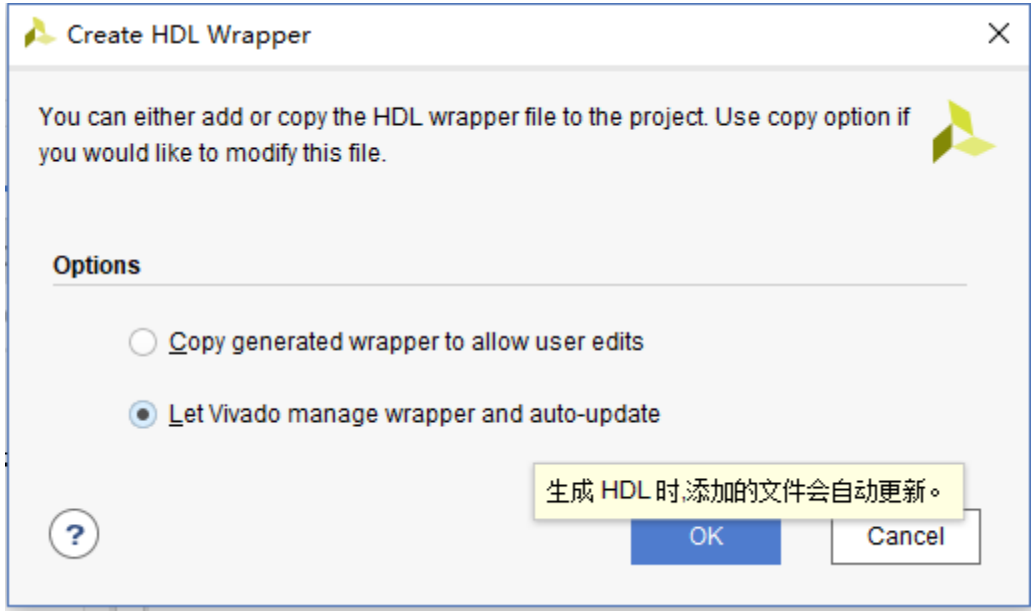
IP调用

- 右击Block Design后选择Create HDL Wrapper…



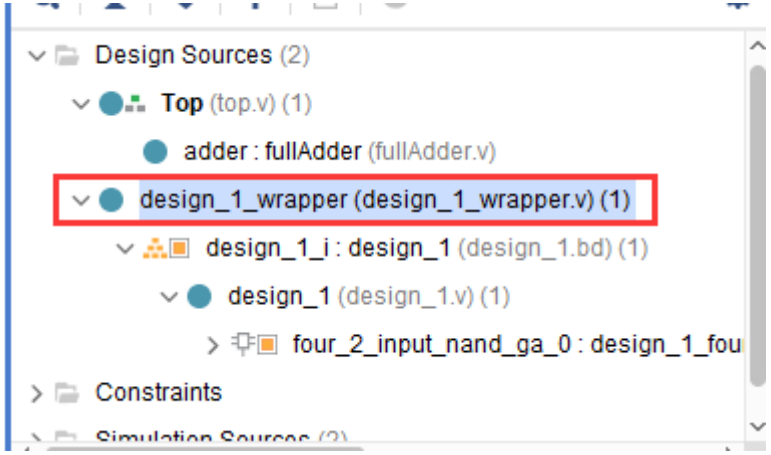
IP调用

- 选择第二个将会自动更新IP



IP调用

- 此时完成IP的例化，即可看见Block Design对应的模块，即可进行后续工作



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