Please make a comparison of the simulated cycles between splited and non-splited input features.

顏敬祐 105061255

Shows the resource usage of the synthesized circuits. To show the RTL Summary page, access the Analysis pane for the HLSConfig, then click the RTL Summary button in the Dashboard pane (refers to page 406 of the Stratus High-Level Synthesis User Guide).

因為embossfilter的rgb可以個別分開計算，所以我分成兩種case，一起傳輸rgb與分開rgb個別傳輸再各別計算，之後合再一起。

分開傳輸的話，面積會變大，但是運算時間可以加快。

	no splited input	splited input
systemc simulation time	1.44E8	1.83E8
BAISC time(ns)	2.68E11	2.49E8
BASIC cycles	2.68E10	2.49E7
BASIC AREA	3820	4939
DPA time(ns)	2.09E11	2.49E8
DPA cycles	2.09E10	1.9E8
DPA AREA	3306	4034