

**PROTECTION OF MULTI-TERMINAL DIRECT CURRENT TRANSMISSION
SYSTEMS**

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The Academic Faculty

By

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PROTECTION OF MULTI-TERMINAL DIRECT CURRENT TRANSMISSION SYSTEMS

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To my wife and parents.

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LIST OF ABBREVIATIONS

AAC: Alternate Arm Converter

AC: Alternating Current

CAGR: Compound Annual Growth Rate

CCP: Current Commutation Path

CPU: Central Processing Unit

CUDA: Compute Unified Device Architecture

CUSUM: Cumulative Sum

DAE: Differential-Algebraic Equation

DC: Direct Current

DSP: Digital Signal Processor

EAP: Energy Absorption Path

EI: Eastern Interconnection

ERCOT: Electric Reliability Council of Texas

EM: Expectation Maximization

EMT: Electromagnetic Transients

EMTDC: Electromagnetic Transients including DC

Exp3: Exponential-Weight Algorithm for Exploration and Exploitation

FP32: Single Precision Floating Point

FP64: Double Precision Floating Point

FPGA: Field-programmable Gate Array

GMLC: Grid Modernization Laboratory Consortium

GMM: Gaussian Mixture Models

GPU: Graphics Processing Unit

HBM2: High Bandwidth Memory 2

HIL: Hardware-in-the-loop

HPC: High Performance Computing

HVDC: High Voltage Direct Current

KNN: K Nearest Neighbor

LCS: Load Commutation Switch

MMC: Modular Multilevel Converter

MPI: Message Passing Interface

MTDC: Multi-Terminal Direct Current

NCP: Normal Current Path

P2P: Pole-to-pole

P2G: Pole-to-ground

PCA: Principal Component Analysis

PCIe: PCI-Express

PSCAD: Power System Computer Aided Design

QCD: Quickest Change Detection

ROCOV: Rate of Change of Voltage

ROTV: Ratio of the Transient Voltages

SM: Submodule

TFLOPS: Tera Floating Point Operations per Second

TGOV1: Turbine Governor Model 1

ULM: Universal Line Model

UFD: Ultra-fast Disconnector

VSC: Voltage Source Converter

WI: Western Interconnection

SUMMARY

Over the past few years, the evolution of power electric converters has enabled the High Voltage Direct Current (HVDC) technology to further enhance reliability and functionality of the legacy grid and to reduce cost and power losses [1–3]. Concomitantly, significant changes in generation, transmission, and loads such as integration and tapping renewable energy generation in remote areas, increasing transmission capacity, and the need to feed the large cities have emerged [2]. These new trends have called for Multi-Terminal DC (MTDC) systems, which when embedded in the existing Alternating Current (AC) grid, can enhance stability, reliability, and efficiency of the present power grid [1].

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of the major technical challenges. In an event of a DC fault, the fault current rises beyond its nominal value within a few milliseconds, which, if not cleared in a timely manner, will take the entire system out of service. Unlike its AC counterpart, the DC fault current has no zero-crossing, which makes it even harder to be interrupted.

To address these challenges, a complete approach towards protection of MTDC grid has been proposed. Firstly, to understand propagation of faults on DC transmission networks, a time-domain method to analyse the DC fault response and characteristics has been proposed. This analysis enables optimal sizing of DC circuit breakers, which reduces the maximum overcurrent and overvoltage applied to the system as well as the fault interruption time. To further improve the performance of DC circuit breakers, a new control strategy to sequentially trip the breaker modules has been proposed. This strategy expedites the fault clearance and reduces the amount of energy that needs to be absorbed. Meanwhile, to address the challenges on DC fault detection, novel protection relaying algorithms, including both primary and backup protection functionalities, have been developed. These relaying algorithms are designed to comply with the reliability, selectivity, speed, sensitivity, robustness, and seamless requirements for MTDC grid protection. Finally, a faster-than-real-time

simulation platform accelerated by Graphics Processing Unit (GPU) is developed. This simulator is able to capture fast dynamic transients with $5\text{ }\mu\text{s}$ resolution. Its high scalability on large-scale MTDC grids and low per unit cost on the hardware make it a promising candidate to test and evaluate the MTDC grid protection system.

CHAPTER 1

INTRODUCTION

1.1 The HVDC Transmission and MTDC Grids

The entire energy system is currently at the beginning of a complete and fundamental transformation, i.e., stepping away from fossil fuels (and in some countries also from nuclear fuels) towards new renewable energy sources, in which USD 10 Trillion is expected to be invested in the next 30 years [4]. This transformation is driven by the desire to make clean energy available and affordable for everyone [5] and is typically considered as one of the most important challenges humanity currently faces.

The majority of existing electricity grid is built upon the generation and transmission of AC power. Over the past few decades, with increasing demands on transmitting bulk power over long distances with low cost and integrating renewable resources into the existing grid, a comprehensive effort has been made around the world in the development of HVDC technology. The global HVDC market, which was valued at USD 7.90 Billion in 2017, is projected to grow at a Compound Annual Growth Rate (CAGR) of 7.92%, from 2017 to 2022, to reach a market size of USD 11.57 Billion by 2022 [6].

With a growing number of HVDC links installed, the Multi-Terminal HVDC (MTDC) grids connecting more than two terminals with HVDC lines, tend to be established to enhance stability, reliability, and flexibility of the system operation [1]. The strategic importance of MTDC grids is evidenced by the number of worldwide projects currently in their advanced planning stage. By the end of 2017, more than 500 HVDC projects were actively planned globally [10], including European “Supergrids” (shown in Fig. 1.1) [7, 11] and the Baltic Sea project along with a few projects in China [12]. In the United States, the cross-continental DC/AC grid (shown in Fig. 1.2) is expected to enable the connec-

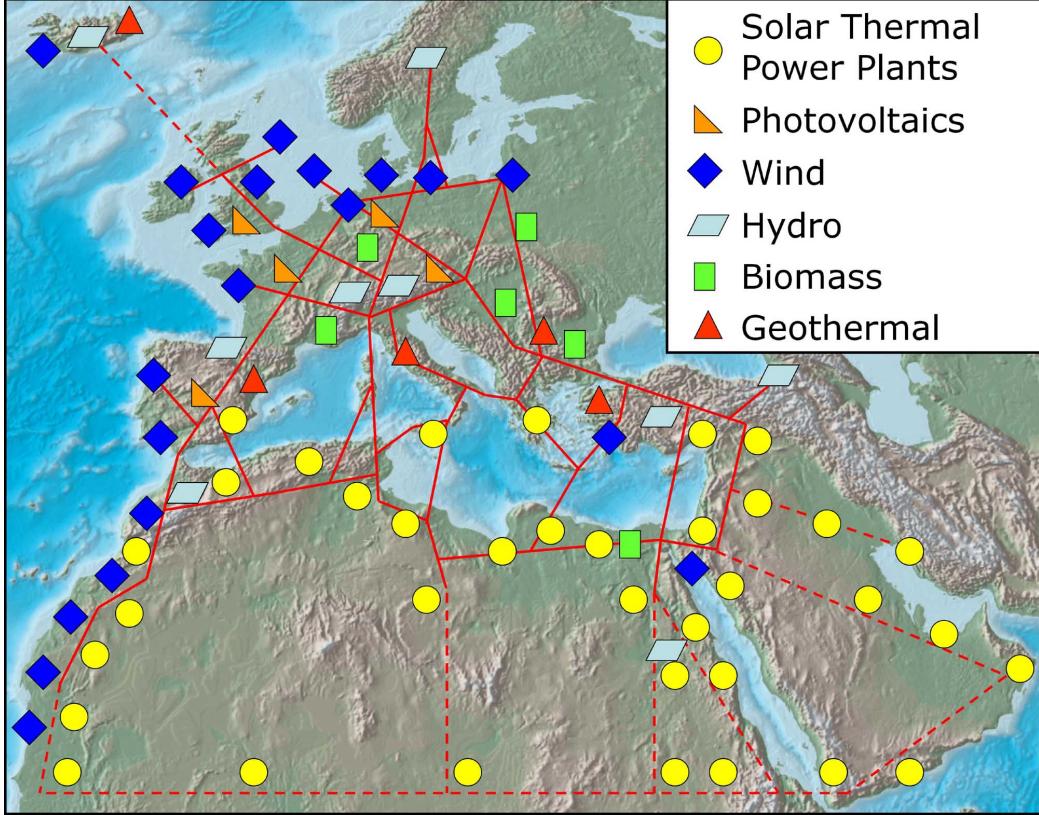


Figure 1.1: The envisioned “Supergrids” connecting Europe, North Africa, and the Middle East, proposed by Desertec [7].

tion of three primary interconnections [8], i.e., the Western Interconnection (WI), Eastern Interconnection (EI), and Electric Reliability Council of Texas (ERCOT).

1.2 Protection of MTDC Grids

The technology for a MTDC grid is, in principle, available today. However, its protection is still one of the major bottlenecks. [1, 13].

1.2.1 Why is MTDC Grid Protection Difficult?

Compared to the protection of legacy AC power grids, protection of MTDC grids is far more challenging. Subsequent to a DC fault occurrence, the fault current rises sharply. The DC fault current could rise to twice as large as its nominal value within just a few milliseconds [14, 15]. Additionally, different from the AC fault current, which naturally

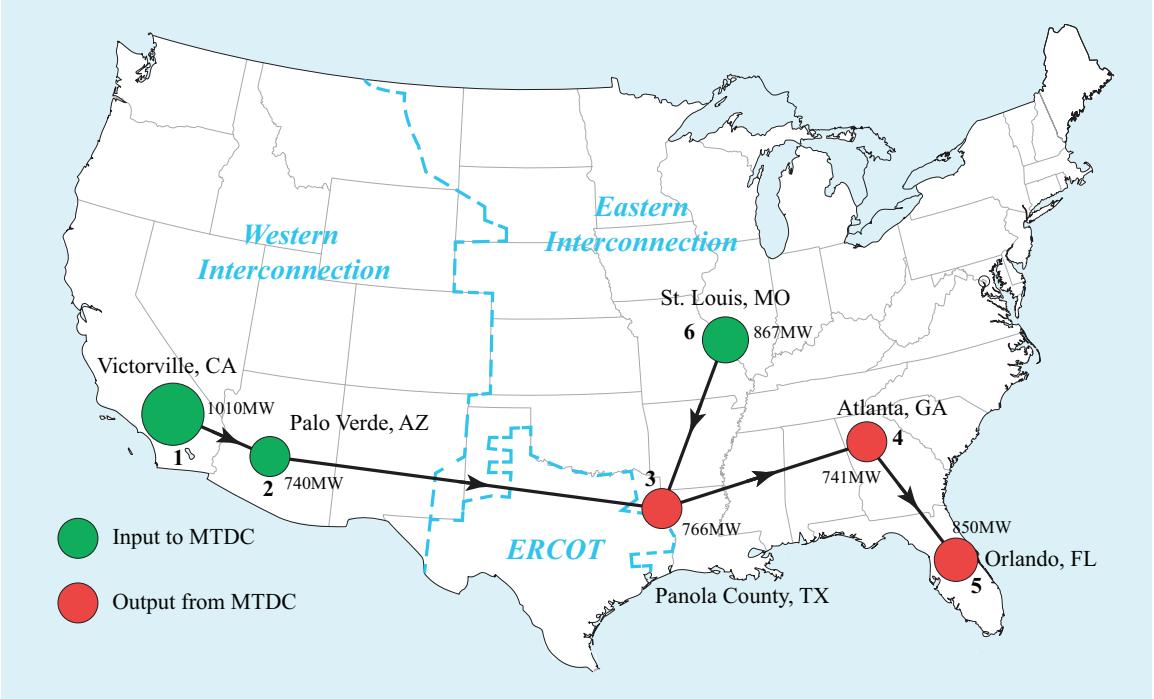


Figure 1.2: The United States six-terminal cross-continental DC/AC grid [8, 9].

crosses zero, the DC fault current rises monotonically. Therefore, it is infeasible for a DC circuit breaker to use zero crossing of fault current to minimize the arcing during fault clearance. As a result, the fast rate of rise of DC fault current makes it cumbersome to be isolated by the conventional DC circuit breakers available in the market.

Fundamentally, there are two approaches to protect a MTDC grid. One option, which is adopted by the most existing projects, is to completely cut off the power from the MTDC grid, by opening the AC circuit breakers on AC sides. This is a viable solution for a point-to-point HVDC link, given the fact that there is only one line/cable in the system which constitutes the fault zone that should be isolated. However, in a MTDC grid with more than two terminals, opening all AC circuit breakers would shut the entire MTDC grid down, including the non-faulty DC lines/cables. The risk of a complete MTDC blackout makes this option not acceptable in real applications. Another option is to only isolate the faulty line/cable, i.e., the fault zone and leave the rest of the grid running normally. This option greatly reduces the risk of a large loss-of-infeed and, therefore, is more stable and

economical. This option, however, is only achievable with the development of a reliable MTDC grid protection.

A practical MTDC grid protection system requires two major building blocks, the hardware of DC circuit breakers and the software of protection algorithms.

1.2.2 Hardware Innovations behind MTDC Grid Protection

Proper protection of MTDC grids necessitates the DC circuit breakers to selectively and quickly isolate any faulty line/cable without interrupting the entire system. Such breakers can be realized based on either resonant circuits [16, 17], or solid-state switches [14, 15, 18, 19].

The resonant-based DC circuit breakers have been developed since mid-1980s and typically take 30 - 100 ms to clear the fault [20]. This interruption time is too long for MTDC grid protection. The solid-state DC breakers, on the other hand, are faster than the resonant-based breakers. However, since a number of solid-state switches stay turned on during the normal operation, the on-state power losses are high [18].

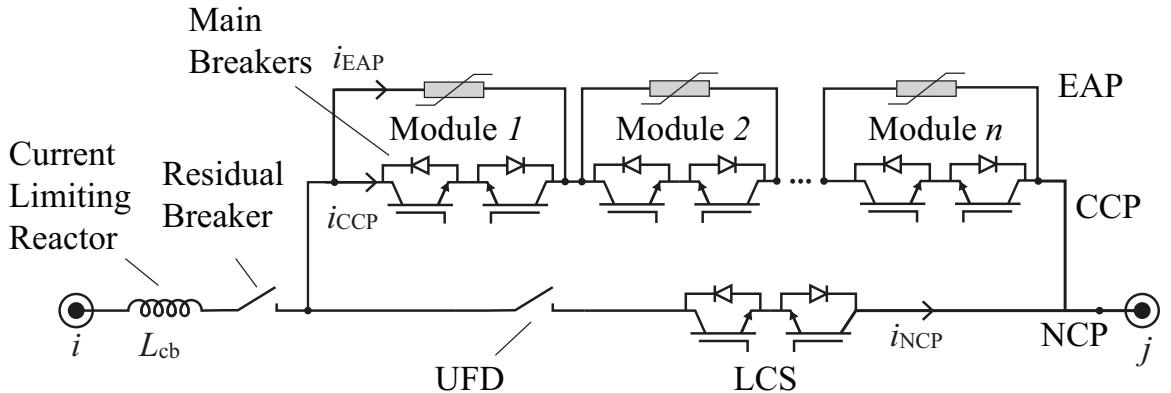


Figure 1.3: Circuit diagram of the hybrid DC circuit breaker [19].

Among the recently proposed DC circuit breakers, the hybrid solid-state one shown in Fig. 1.3 is the most promising option [19]. It is hybrid in the sense that a mechanical switch, i.e., an ultra-fast disconnector (UFD) is connected in series with a number of solid-state switches, i.e., the load commutation switch (LCS) in the normal current path (NCP).

This design provides a reasonable trade-off between lower on-state power losses and faster fault clearance. The breaking time is in the order of a few milliseconds while its conduction losses during normal operation are low [19]. Subsequent to a fault, the fault current is routed to the current commutation path (CCP), which is comprised of a number of identical modules with parallel connected main breakers and arrester banks. Once the current on the NCP reaches zero, the UFD opens immediately to prevent the LCS from exposure to high voltage. The main breakers are then tripped and arrester banks are inserted simultaneously [19] or sequentially [9, 15] to dissipate the energy and extinguish the fault. The availability of fast mechanical switches and the optimization of breaker control strategies are major challenges of developing such hybrid breakers.

1.2.3 Software Innovations Enabling MTDC Grid Protection

In addition to the advancement of MTDC grid protection hardware, the development of software component, i.e., protection relaying algorithms, is another challenge to be addressed. A practical MTDC grid protection system should offer six basic requirements [21, 22]:

- *Reliability:* To provide consistent functionalities under fault conditions, which may occur rarely following a long idle time. A backup protection system should be deployed to respond in case of primary system failure.
- *Selectivity:* To avoid false and unwanted trips. The protection system should only respond under fault conditions within its protection zone.
- *Speed:* To operate and interrupt a fault quickly to minimize the delays and fault clearance time. The protection system should function to reduce potential damage to the equipment.
- *Sensitivity:* To capture and detect any fault occurrence. The relaying algorithm should not miss any fault.

- *Robustness*: To function under both normal and degraded working conditions. The protection system should not be affected by normal operations like controller adjustment.
- *Seamlessness*: To isolate only the faulty part and leave the healthy components of the system working normally.

The protection philosophy of MTDC grids is similar to the AC grid protection in the sense that both primary and backup protection relaying algorithms are required to fulfill these requirements [1, 23].

The primary protection, which is designed as the first layer of a MTDC grid protection, should respond to any type of fault in a fast and reliable manner. The covered fault types include DC-side faults such as pole-to-pole (P2P) and pole-to-ground (P2G) faults, AC-side faults, and converter internal faults.

The backup protection, on the other hand, is designed to respond in case of primary protection failure [23]. Such cases include failure of primary protection system itself, and failure of a DC circuit breaker. In the former case, the backup protection is responsible for detecting the faults that are not captured by the failed primary detection. The latter case occurs when the corresponding DC circuit breakers fail to respond to the given trip signals. The backup protection should detect any breaker failure and coordinate other circuit breakers to clear the fault.

1.3 Simulation Platforms for MTDC Grids

Simulation is one of the most important elements in the design, specification, planning, procurement, and operation of any MTDC grid [24]. In each phase of a MTDC grid project, different studies are performed using different simulation platforms and tools to help understand the key performance metrics [25–28]. These tools and their applications are summarized in Table 1.1.

Table 1.1: Simulations tools and their applications

Simulation Tools	Applications
Power flow	System adequacy study Transmission planning
Transient stability	Transient stability study Dynamic stability study
Frequency domain	Harmonic analysis Fault analysis
Electromagnetic transients (EMT)	Controller evaluation Transient stability study Dynamic stability & performance study

1.3.1 Key Considerations in MTDC Grid Simulation for Protection Study

To understand the protection of a MTDC grid, fast transients and dynamic behavior of both power system and power electronics devices present in the system have to be investigated [24]. This requires the use of detailed high-fidelity EMT models to address the extensive appearance of nonlinear devices in the simulation [29, 30]. EMT studies have been comprehensively conducted in both AC and DC networks, including transmission lines [31], modular multilevel converters (MMCs) [27, 32–35], and transformers and generators [25, 26, 36]. These models provide building blocks for the detailed analysis, like the study of fault transients, stability, and frequency support, of MTDC grid study.

Based on case specific requirements, EMT simulations can be performed either offline or in real time. Real-time simulation synchronizes the program execution with the real-world clock, enabling the interaction with actual control and protection equipment. This makes it a perfect choice for the design and evaluation of control and protection systems. To meet real-time requirements in simulation of a MTDC grid, each component should be carefully modelled. The MMCs typically consist of hundreds of submodules (SMs) in each arm. The large number of SMs in a MMC results in thousands of states [37, 38]. These states include arm currents, capacitor voltages, switching signals, and controller states. To capture the fast transients and cope with high bandwidth of MMC controllers, time steps

in the order of few microseconds should be applied [39]. Real-time calculation of large number of states within small time intervals requires sufficient computation power and precise calibration of parallelism [40]. In the transmission networks, propagation of travelling waves and frequency dependent effects are critical for analysis of DC/AC-side faults [23, 41]. Fast transients should also be captured for study of controller stability [30]. To these ends, both AC and DC lines/cables should be modelled with high fidelity and based on frequency-dependent models. Additionally, any AC grid connecting to a MTDC grid consists of synchronous generators, transformers, and AC lines/cables [38]. The computational complexity of simulating MTDC grids with models of components mentioned above, makes it difficult to achieve real-time simulation at small time-steps. It is also challenging to keep the simulation system scalable as more AC and DC terminals are introduced while expanding the grid.

1.3.2 GPU-based Simulation: Why and How?

To solve the problem of high computational burden and meet the demand of high scalability in MTDC grid simulation, the CPU & GPU co-simulation platform is designed and implemented [42].

Compared to CPUs, which are good for serial processing with low latency, the GPUs, composed of thousands of cores running at lower frequency, are capable of handling massive amount of threads simultaneously. As a result, GPUs are good for tasks which require higher throughput and can be broken into a large number of mutual independent parts. These parts can be processed at a much higher speed in parallel per unit time.

Fig. 1.4 presents the architecture of Nvidia Pascal GP100 GPU, which is designed for computing acceleration markets and High Performance Computing (HPC) applications. Equipped with 3584 Compute Unified Device Architecture (CUDA) cores and 16 Gigabytes of High Bandwidth Memory 2 (HBM2) memory, GP100 delivers 5.3 TFLOPS of double precision floating point (FP64) and 10.6 TFLOPS of single precision (FP32) per-

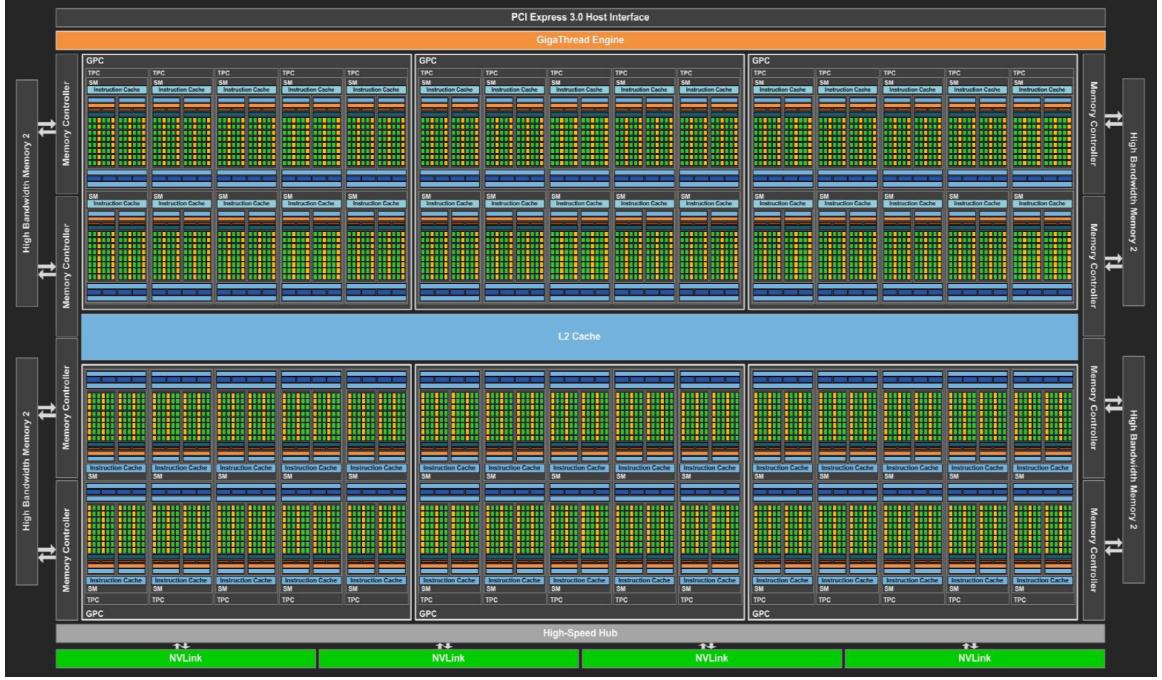


Figure 1.4: Architecture of Nvidia Pascal GP100 GPU [43].

formance.

The huge computation capability provided by the large number of cores within a GPU makes it a preferable platform for parallel computation of internal states for MMCs. These states, e.g., SM capacitor voltages, are independent from module to module and would be time-consuming to be processed sequentially on CPU. By moving computationally intensive parts like MMC internal states to the GPU, the speed of overall simulation is dramatically improved.

Meanwhile, the CPU & GPU co-simulation platform can be easily scaled horizontally by adding more GPUs to the system when a larger MTDC grid is to be deployed. This is an economic option since the simulation algorithms stay the same for both small- and large-scale MTDC grids. The investment of such simulation platform is thus linear to the scale of the target MTDC grid.

1.4 Summary of the Contributions

This research focuses on developing an end-to-end approach to address the challenges in MTDC grid protection and to enable the practical applications of such protection system. The contributions are summarized as follows:

1. Propose a time-domain method to analyse the fault characteristics during DC-side faults in MTDC grids. The proposed method, based on travelling waves, (i) provides a sound representation of fault performance by considering all created travelling waves, (ii) introduces a new approach to estimate the reflection coefficients, and (iii) provides an approximation of the worst-case fault location. This method is applied to calculate the DC fault response and the performance metrics of DC circuit breakers.
2. Develop a design tool to determine the optimal parameters of DC circuit breakers based on performance metrics, i.e., maximum overcurrent, maximum overvoltage, fault clearance time, and energy absorption capability. The optimized parameters are current limiting reactor, arrester rated voltage, and time delay of DC circuit breakers.
3. Propose a new control strategy, named sequential switching strategy, for DC circuit breakers to improve their transient performance during a DC fault interruption in MTDC grids. Compared to the conventional switching strategy, the proposed one, which sequentially trips the breaking modules within a circuit breaker, reduces the peak fault current and overvoltage as well as fault clearance time.
4. Propose a hybrid primary fault detection algorithm for the MTDC grids. The proposed primary detection algorithm provides the following advantages over the existing methods: i) P2P, P2G, and external DC fault are covered; ii) various fault locations and fault impedances are covered; iii) the system is robust to noisy input signals.

5. Propose a backup protection algorithm based on quickest change detection (QCD) technique. The proposed algorithm offers fast and robust backup protection functionalities for the primary relay in case of primary protection failure and DC circuit breaker failure.
6. Propose a cost-effective high-performance real-time EMT simulation platform for large-scale cross-continental MTDC grids based on the CPU & GPU co-simulation architecture. The proposed simulation platform: i) incorporates detailed EMT models of all components of an MTDC-AC grid within a single platform. This setup provides a complete simulation solution to capture fast transient signals required for high-bandwidth controller design [30, 44] and protection studies, without any compromise; ii) implements the first GPU-based simulation architecture and corresponding algorithms for MTDC-AC grids with real-time performance at scales of 1 s; iii) is highly-efficient and balances the high utilization of GPU resources and low latency required for the simulation; and iv) outperforms the existing CPU- and DSP/FPGA-based simulators in terms of its higher scalability on large-scale MTDC-AC grids and superior price-performance ratio on the hardware.

1.5 Outline of Chapters

Chapter 2 reviews the existing approaches in the literature with respect to analysis of DC fault characteristics in MTDC grids, parameter optimization and control strategies of DC circuit breakers, primary and backup protection algorithms, and simulation platforms for MTDC grids.

In Chapter 3, a DC fault transient response is modelled in time-domain considering all the corresponding travelling waves. Based on the analysis, the fault behavior within the first few milliseconds is analytically modelled. The accuracy of the proposed time-domain analysis is evaluated through comparison with EMT simulation.

In Chapter 4, the optimization of protection hardware, i.e., DC circuit breakers is dis-

cussed. A multi-objective design optimization problem is formulated to explore the Pareto-optimal fronts of the transient response of the system versus the breaker parameters and to establish trade-offs among the breaker parameters and fault transient response. Additionally, the proposed sequential tripping strategy is introduced. By rescheduling the tripping sequence and optimal rating and number of individual modules of the circuit breaker, the energy distributed among the modules is well balanced. Finally, analytical evaluation of the proposed sequential tripping is performed and, subsequently, the best practice and the optimal design process are provided.

In Chapter 5, the software of MTDC grid protection system is presented. The layout of a unified protection unit located on local terminals of a MTDC grid are illustrated. This protection unit consists of the proposed hybrid primary replaying algorithm and QCD-based backup relaying algorithm. These two algorithms are discussed in details. Performance and effectiveness of the proposed algorithms are evaluated and verified based on time-domain simulation studies in the PSCAD/EMTDC software environment.

In Chapter 6, the proposed simulation platform is described. The EMT models of various MTDC components, i.e., MMCs, transmission lines/cables, generators and transformers are presented. The CPU & GPU co-simulation architecture along with the simulation algorithm design, memory and communication optimization are explained.

Chapter 7 summarizes and concludes the dissertation and highlights the major contributions. The future work of MTDC grid protection is also explored.

CHAPTER 2

LITERATURE SURVEY

2.1 Analysis of DC faults in a MTDC System

Primarily, there are two types of faults in a DC transmission network, i.e., P2P faults and P2G faults. Analysis of propagation and response of these faults is essential in understanding the protection challenges associated with MTDC grids.

In calculating a fault response, several approaches have been proposed. A three-stage short-circuit current calculation method, using the lumped π -section cable model, is reported in [45, 46]. Although the three-stage method is helpful to understand the behavior of a DC system after a fault, it is not sufficiently accurate within the first few milliseconds when the maximum fault current and over voltage occur. Considering the travelling wave phenomenon, the authors in [47] derive the time-domain solutions of the fault current contributed by DC capacitors. Based on the response of frequency-domain models, fault behavior in multiple MTDC configurations has been studied in [48]. However, only the first travelling wave is taken into account in both [47] and [48]. Subsequently reflected and transmitted waves are important in estimating the maximum transient overvoltage as well. To this end, detailed and accurate calculation of subsequent travelling waves is necessary.

2.2 Optimization of a DC Circuit Breaker

While the protection of point-to-point HVDC systems can be fulfilled by relying on converter controls and AC circuit breakers, proper protection of the MTDC grids necessitates the DC circuit breakers to selectively and quickly isolate the faulty DC line/cable without interrupting the entire system. Among the proposed DC circuit breakers [49], the hybrid solid-state circuit breaker [14, 50] is one of the most promising options as its current break-

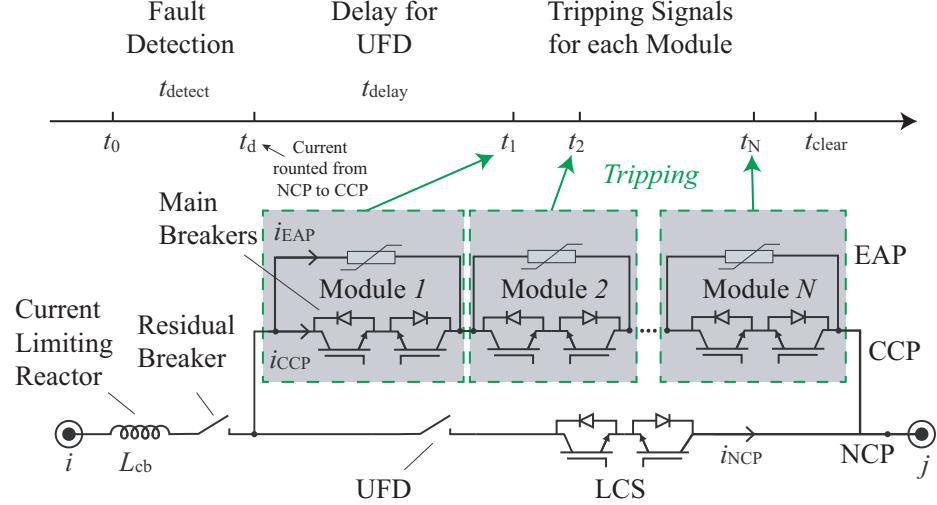


Figure 2.1: Circuit diagram and sequential tripping timeline the hybrid DC circuit breaker [9].

ing time is in the order of a few milliseconds while its conduction losses during normal operation are low [50]. However, incorporating such DC circuit breakers into a MTDC grid adds another level of complexity as the DC short circuit current increases with commensurate increase in transient overvoltage stress, current limiting reactor and energy absorption capability of arresters. To determine the fault clearing capability and performance of these DC breakers, there is a need for an optimal parameter selection method to size the circuit breaker components and to achieve satisfactory performance.

Once a quantitative estimation of maximum fault current, overvoltage, clearance time and energy absorption in arresters is obtained, optimum selection of circuit breaker components can be performed. The authors in [51, 52] investigate the operation of hybrid circuit breakers and develop a parallel genetic algorithm in the MATLAB-EMTP environment to select breaker parameters. However, a large number of parallel processors are required to reduce the computation time even when dealing with simplified models of the point-to-point HVDC systems. This computation stress limits the applicability and expansion of the method to larger MTDC systems.

Consisting of three paths, i.e., the NCP, CCP, and energy absorption path (EAP), a hybrid DC circuit breaker, as shown in Fig. 2.1, is designed to clear a fault through forcing

the fault current from the NCP to the CCP and the EAP. During normal conditions, the current flows through the UFD and the LCS in the NCP. Subsequent to a fault, the fault current is routed to the CCP, which is comprised of a number of identical modules with parallel connected main breakers and arresters. Once the CCP establishes a conducting path, the UFD opens. Conventionally, the opening of the UFD is followed by simultaneous tripping of all series-connected modules on the CCP and the EAP [19, 49, 50]. This tripping method results in a high voltage applied to the arresters, which are used to extinguish the fault current. However, this voltage introduces a high voltage stress across the UFD, which takes a few milliseconds to establish a sufficient voltage withstand capability [53]. This delay ultimately limits the speed of the DC circuit breaker.

2.3 Protection Strategies for MTDC Systems

2.3.1 Primary Protection

The primary fault detection of MTDC grids has become a timely topic over the past few years. Various algorithms have been proposed to address this challenge. To improve fault detection speed, as well as reliability of the protection system, methods solely based on local measurements without relying on the communication across multiple MTDC terminals have attracted significant interest [53–60]. These algorithms are summarized in Table 2.1, and can be categorized by the type of input signals, i.e., currents or voltages measured at one end of the transmission line [53–56, 58], and voltages measured across the DC current limiting reactors [57, 59, 60].

Upon occurrence of a DC fault, the DC capacitors at the terminals on both ends of the faulty transmission line start to discharge [67]. Following this discharge, the faulty line current increases rapidly from its nominal value. The fast rate of rise of the transient current is used as an indicator of a DC fault in [55]. However, this method might trigger false alarms under high impedance faults. The average value of this signal over a fixed window is used in [54], but at the expense of sacrificing detection speed. Line currents

Table 2.1: The existing primary fault detection algorithms for MTDC grids

Paper	Year	Method	Input Signals	Covered Fault Types	Fault Characteristics
[54]	2020	threshold, transient average current	line currents	P2P, external	locations, impedances
[55]	2017	threshold, transient current	line currents	P2G, P2P, external	breaker tripping, line & converter outage
[56]	2012	Fourier transform	line currents	P2G, external	locations, impedances
[56]	2016	ROCOV	line voltages	P2G, P2P, external	locations, impedances
[57]	2017	ROTV & transient voltage	line voltages	P2G, P2P, external	locations, impedances
[58]	2017	ROCOV	DC reactor voltage	P2G, P2P	locations, impedances, power reversal
[59]	2017	threshold, absolute value of voltage	DC reactor voltage	P2G, P2P	locations, impedances
[57]	2018	threshold, travelling wave	DC reactor voltage	P2G, P2P	sampling frequencies, reactor sizes
[60]	2019	hybrid of current threshold & ROCOV	line currents	P2G, P2P, external	different locations, impedances, reactor sizes, noisy signals
The Proposed Method		DC reactor voltage			

Table 2.2: The existing and proposed real-time simulation specifications of the MTDC grid

Paper	Year	Step size	MMC model	SMs/arm	Transmission line	Terminals	Platforms
[40]	2018	5 μ s	detailed	400	N/A	1	CPU & DSP
[61]	2014	2.5 μ s (MMC), 50 μ s (test)	detailed	200	Bergeron	3	RTDS(CPU) & FPGA
[39]	2015	9 μ s	detailed	400	distributed	1	CPU & FPGA
[62]	2016	8 μ s (MMC), 30 μ s (test)	detailed	100	N/A	2	CPU & FPGA
[63]	2019	20 μ s	device & equivalent	24	distributed	3	MPSoC (CPU & FPGA)
[64]	2018	2.7 μ s (MMC), 51 μ s (test)	detailed	400	N/A	2	RTDS(CPU) & FPGA
[65]	2017	5 μ s (MMC), 25 μ s (test)	detailed	500	N/A	2	Opal-RT (CPU & FPGA)
[66]	2018	20 μ s	arm equivalent	200	frequency dependent	11	multiple CPU
The Proposed Method		5 μ s	detailed	400	frequency dependent	3+	CPU & GPU

are used differently in [56] by extracting the transient harmonic from the signal through a discrete Fourier transform. This information is used for fault detection and identification of the fault types. Since this method relies on a single frequency component of fault current, it is vulnerable to signal noise. In addition to the rising fault current, voltages at faulty terminals also drop abruptly upon the arrival of travelling waves from the fault location on the transmission line. The rate of change of voltage (ROCOV) measured at the transmission line side of the current limiting reactor is used to determine the fault [53]. This method is sensitive to fault impedance and can be affected by high frequency noise, as well. In [58], the transient voltages measured at both sides of the current limiting reactor are collected and combined into the ratio of the transient voltages (ROTV). This primary fault detection method is designed to work with a backup method, which requires the communication of ROTV from both ends of the line, hence reducing detection speed.

The other category of primary fault detection algorithms takes advantage of the voltage signal measured across the current limiting reactor connected in series with the DC circuit breaker. The absolute value of this signal is used in [57] for primary detection. In [59], the rate of change of DC reactor voltage is monitored. This is essentially equivalent to monitoring the second derivative of the DC fault current. However, a high sampling frequency is required for such measurement, which is neither realistic nor cost-effective in real applications. Another usage of DC reactor voltage is proposed in [60], where the authors calculate the positive sequence voltage travelling waves to detect the fault, at the expense of increased computational burden.

2.3.2 Backup Protection

The protection philosophy of the MTDC grids, nevertheless, is similar to the AC counterparts in the sense that both primary and backup protection schemes are required. In case the primary protection fails to act properly, backup protection should trip as quickly as possible to minimize the loss of power in-feed [21].

In the technical literature, the following backup protection algorithms have been proposed for HVDC grids [68–71]:

- A current threshold-based algorithm [68] in which the breaker failure is identified after a certain time delay following the trip signal from primary protection. To avoid misdetection in backup protection, the time interval is selected to be 20 ms. This results in a low detection speed and high ratings of circuit breakers.
- A local backup protection algorithm [69] in which classifiers are designed to detect primary protection failure using voltage-current signals from corresponding relays. The uncleared and cleared faults are distinguished by a decision boundary on the voltage-current curve found by a classifier, which is trained using a large amount of data. The robustness of this method is evaluated in [71] under various system conditions and operating delays. Although the speed of this algorithm is faster than the previous current based method, it has the following drawbacks: a) detailed system modeling and accurate measurements are required to find an accurate boundary; b) the classifier has to be trained with lots of pre-acquired data under various conditions including different fault locations, fault impedance, and power flow; c) the scalability of this method is limited because the classifier has to be reset to be used in modified system topologies.

Additionally, both of the aforementioned methods are vulnerable to noise or spikes from measurement instruments such as current and voltage sensors.

2.4 Real-time Simulation of MTDC Systems

The benefits of MTDC technology have initiated the exploration of large-scale systems integration including a cross-continental AC-DC grid, which provides an economic way to connect the three major interconnections in the United States, i.e., WI, EI, and ER-COT. To understand the operation, control, and protection of a sophisticated system like

this, fast transients and dynamic behavior of both power system and power electronics devices involved have to be investigated [24]. This requires the use of detailed high-fidelity EMT models to address the extensive appearance of nonlinear devices in the simulation [30]. EMT studies have been comprehensively conducted in both AC and DC networks, including transmission lines [31], MMCs [32], Alternate Arm Converters (AACs) [72], transformers and generators. These models provide the building blocks for the detailed analysis, i.e., fault transients, stability, frequency support, etc. of the MTDC grid study.

Based on case specific requirements, EMT simulations can be performed either off line or in real time. Real-time simulation synchronizes the program execution with the real-world clock, enabling the interaction with actual control and protection equipment. This makes it a perfect choice for the design and evaluation of control and protection systems. To meet real-time requirements in simulation of a MTDC grid, each component should be carefully modelled. The MMCs typically have hundreds of SMs in each arm, and as a result, the number of states in each MMC is in the order of thousands including those for controllers, arm currents, capacitor voltages, and switching signals [37]. To capture the fast transients and cope with high bandwidth of MMC controllers, time steps in the order of few microseconds should be applied [39]. Real-time calculation of such a large number of states within small time intervals requires sufficient computation power and precise calibration of parallelism [40]. In the transmission networks, propagation of travelling waves and frequency dependent effects are critical for analysis of DC-/AC-side faults. To this end, both AC-and DC-lines/cables should be modelled with high fidelity with the frequency-dependent models [30]. Additionally, the synchronous generators and transformers should also be modelled to reflect their electromagnetic dynamic behaviors and provide insights into study of the AC frequency response between multiple interconnections. These requirements make it difficult to achieve real time with detailed switching and frequency dependent models simulated at small steps. It is also challenging to keep the simulation system scalable as more AC and DC terminals are introduced while expanding a MTDC

system.

Real-time simulation platforms of MTDC systems have been implemented on different computing hardware with various levels of details, as summarized in Table 2.2. Most of these platforms are built based upon CPUs and FPGAs [39, 61–65], where the simulation of MMC is performed on FPGAs. A high-end FPGA board is capable of simulating 1500 to 3000 SMs, which are the typical numbers of SMs in a single MMC [61, 62, 65] and vary depending on the SM circuit configurations and FPGA models. Consequently, the number of FPGAs has to be scaled out linearly as the size of MTDC system grows, which is not an economic option for simulation of a large MTDC grid. Additionally, extensive matrix-matrix or matrix-vector computation is required for simulating frequency-dependent transmission line models. It is challenging to implement these data-intensive operations efficiently on an FPGA. The MMC models adopted include detailed equivalent models [39, 40, 61, 62, 64, 65], device-level models [63], and arm equivalent models [66]. To study the fault transients and frequency support of a large MTDC system with high fidelity, the detailed equivalent models are preferable since these models strike a reasonable balance between modelling details and the computational load [30]. Real-time simulations with these MMC models have time steps within ten microseconds including the controllers. However, the rest of the system, i.e., the transmission lines and generators, are simulated at much larger steps using the lumped or non-frequency-dependent models. The highly simplified AC/DC networks limit the application of these real-time platforms on frequency-sensitive high-bandwidth controller and protection system designs.

CHAPTER 3

ANALYTIC FAULT TRANSIENT APPROXIMATION

3.1 DC Fault Transients Analysis

To design and implement MTDC grid protection systems, it is critical to understand the fast transients subsequent to a DC fault occurrence. Started from DC faults locations, travelling waves are propagated to the MTDC terminals within a few milliseconds and reflected between them. Large variances on current and voltage measurements introduced by the travelling waves trigger the protection of multiple devices, i.e., converters, DC buses, and transmission lines/cables. As a result, the fault transients become more complicated and require more involved analysis. In this chapter, the DC fault transients are estimated through a series of frequency- and time-domain analysis, which provides the foundation for protection studies in the following chapters.

There are mainly two types of DC faults on the DC network, i.e., P2G and P2P faults. Compared to the former one, the latter is more severe because of its larger fault current [1, 48]. Although the discharging circuit of a P2G fault is quite different, the principle and the method to build the equivalent circuit and the procedure to calculate fault transients for both cases are the same.

The layout of one terminal (Bus_i) of a MTDC grid is shown in Fig. 3.1. A P2P fault is assumed to be on cable $Line_{i1}$. The adjacent cables on Bus_i are denoted as $Line_{ij}, j \notin \{1, i\}$. The fault current, $i_{f,1}$ is broken down into two parts, i.e., $i_{f,CON}$ and $\sum_{j \notin \{1, i\}} i_{f,j}$, which are contributions from converter and adjacent cables, respectively. The incident surge e_i is transmitted to Bus_i and reflected as e_r , resulting in a fast voltage drop on the terminal. The detailed analysis of this travelling wave phenomenon, which has a significant impact on fault transients, is presented as follows.

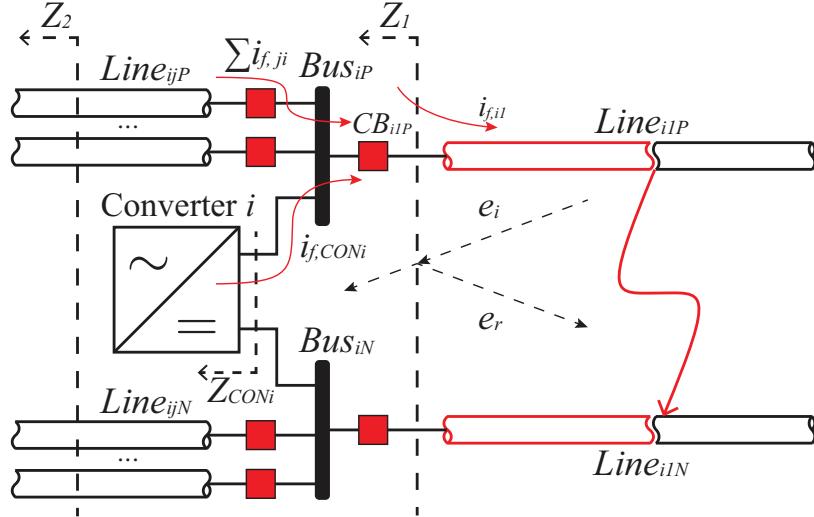


Figure 3.1: Fault current contributions during a P2P fault at Bus_i .

3.2 Frequency-domain Expression of Travelling Waves

When the positive and negative poles are shorted at a certain distance from the terminal of the transmission line, the voltage surge generated at the fault location starts travelling to both ends of the faulty line. For a uniformly distributed lossy transmission line, the relationship of voltage $v(z, t)$ and current $i(z, t)$ at position z from the fault location is described by telegrapher's equations. In frequency domain, they yield the second-order differential equations expressed by:

$$\frac{d^2V(z)}{dz^2} = \gamma^2(s)V(z), \quad (3.1)$$

$$\frac{d^2I(z)}{dz^2} = \gamma^2(s)I(z), \quad (3.2)$$

where $\gamma = \sqrt{Z(s)Y(s)}$ is the propagation constant of the transmission line. $Z(s)$ and $Y(s)$ are line series impedance and shunt admittance, respectively. The solution to (3.1) and (3.2) is

$$V(z) = V^+(z) + V^-(z) = V_0^+e^{-\gamma z} + V_0^-e^{+\gamma z}, \quad (3.3)$$

$$I(z) = I^+(z) + I^-(z) = \frac{V_0^+}{Z_0} e^{-\gamma z} - \frac{V_0^-}{Z_0} e^{+\gamma z}, \quad (3.4)$$

where $Z_0(s) = \sqrt{Z(s)/Y(s)}$ is the characteristic impedance of the transmission line. Equations (3.3) and (3.4) are general expressions for travelling waves. $V^+(z)$ and $V^-(z)$ represent the forward and backward waves at point z , respectively.

The fault generated travelling waves include high-frequency components. A reasonable approximation of cable impedance is $Z(s) = L \cdot s + K\sqrt{s}$, where K is the skin effect factor [73]. The shunt capacitor C is constant and the inductance is assumed constant at high frequencies.

Assuming an initial voltage step V_0 at the fault location on an infinite-length cable, the backward wave V^- is zero while the incident wave can be expressed by [74]:

$$V_1^+(z) = \frac{V_0}{s} \exp\left(\frac{-z}{c}s - \frac{Kz}{2Lc}s^{1/2}\right), \quad (3.5)$$

where $c = 1/\sqrt{LC}$ is the propagation speed of the cable [47].

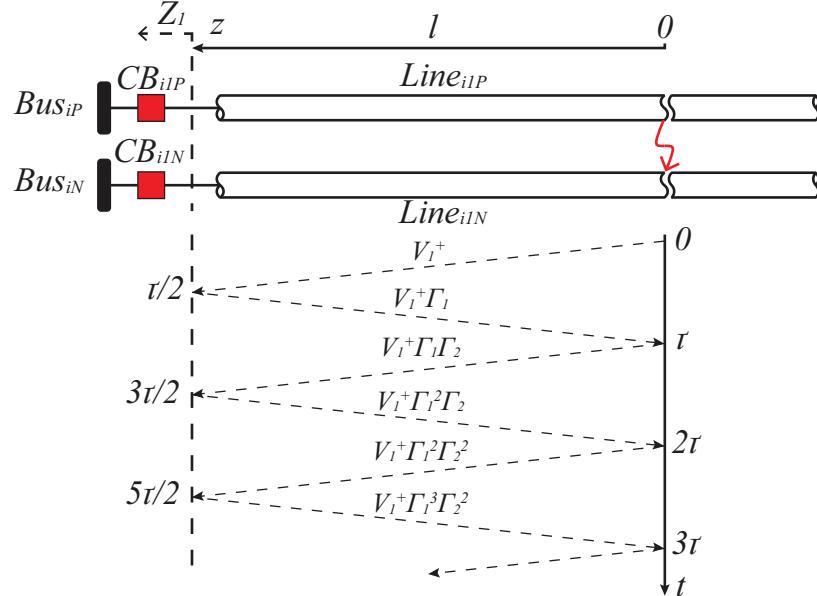


Figure 3.2: Lattice diagram for travelling waves of a faulty cable.

With the first incident wave described by (3.5), the subsequent travelling waves on a finite-length cable can be also derived. The fault generated incident wave will be reflected at the terminal because the impedance changes to Z_1 , including the series current limiting reactor L_{cb} in the DC circuit breaker and the equivalent impedance seen by the terminal. This reflected wave will be reflected again once it arrives at the fault location. These reflections are depicted in the lattice diagram in Fig. 3.2. Thus, within the first few milliseconds when the breaker has not opened yet, the voltage at the breaker, $V_{i1}(l)$, can be expressed as the superposition of several forward and backward travelling waves as

$$V_{i1}(l) = \sum_{m=0}^{\infty} V_1^+(l)(1 + \Gamma_1)(\Gamma_1\Gamma_2)^m, \quad (3.6)$$

where Γ_1 and Γ_2 are the reflection coefficients at the terminal and fault location, respectively. The reflection coefficients are given by

$$\Gamma_1 = \frac{Z_1 - Z_0}{Z_1 + Z_0}, \quad \Gamma_2 = -1, \quad (3.7)$$

$$Z_1 = sL_{cb} + Z_{CON}/Z_2, \quad (3.8)$$

where Z_{CON} and Z_2 represent the equivalent impedance of the converter and the adjacent cables, respectively, as illustrated in Fig. 3.1. Although the transfer function of the subsequent waves with the reflection coefficients in frequency domain can be written directly, it is not trivial to derive the analytical expressions in time-domain, especially for meshed DC grids. To analyze the transient performance of the system, time-domain estimation of the travelling waves is necessary.

3.3 Time-domain Estimation of Travelling Waves

As shown in Fig. 3.1, a P2P fault occurs on $Line_{i1}$ connected to terminal (Bus_i) of the MTDC grid. The time-domain expression for the surge voltage travelling towards Bus_i can be attained by solving (3.5) as [75]:

$$v_1(z, t) = V_0 \cdot \operatorname{erfc}\left(\frac{K}{4L\sqrt{t-z/c}} \cdot \frac{z}{c}\right) \cdot u(t - \frac{z}{c}), \quad (3.9)$$

where $u(t)$ is a step function and $\operatorname{erfc}(t)$ is the complementary error function.

The equivalent circuit for the travelling wave at the terminal of $Line_{i1}$ is shown in Fig. 3.3(a), where u_q is the incident wave arriving at the terminal before the circuit breaker. Based on Peterson's rule, u_q is doubled and set as the voltage source in equivalent circuit of Fig. 3.3(a). The equivalent circuit is composed of the parallel branches connected to Bus_i . The cable $Line_{ij}$ is represented by its characteristic impedance Z_0 , with the limiting reactor $L_{cb,ij}$ in series with the DC circuit breaker on this line. Subsequent to a fault occurrence, the converter is not immediately blocked and can be represented by an R-L-C branch [76]. The reflection coefficient at the terminal of the faulty cable Γ_1 can be estimated in time domain by

$$\begin{aligned} \Gamma_1 &= \frac{u_f}{u_q} = \frac{u_t}{u_q} - 1, \\ u_t &= u_q - Z_0 \cdot i_{f,1}, \end{aligned} \quad (3.10)$$

where, u_q is the first incident voltage arriving at the terminal with the time-domain expression described in (3.9), u_f is the reflected backward voltage and u_t is the refracted voltage transmitted into the terminal. The fault current $i_{f,1}$ is contributed by the converter capacitance and the adjacent cables discharge, denoted as $i_{f,CON}$ and $i_{f,j}$ respectively, yielding

$$i_{f,1} = i_{f,CON} + \sum_{j \notin \{1,i\}} i_{f,j} = C_{CON} \frac{du_{C_{CON}}}{dt} + \sum_{j \notin \{1,i\}} i_{f,j}. \quad (3.11)$$

The differential equations governing the behavior of the equivalent circuit are expressed by

$$\begin{aligned} 2u_q &= Z_0 i_{f,1} + L_{cb,i1} \frac{di_{f,1}}{dt} + u_{bus}, \\ u_{bus} &= Z_0 i_{f,j} + L_{cb,ij} \frac{di_{f,j}}{dt} \\ &= L_{CON} \frac{di_{f,CON}}{dt} + R_{CON} i_{f,CON} + u_{C_{CON}}, \end{aligned} \quad (3.12)$$

where u_{bus} represents the voltage at the busbar. Therefore, the reflection coefficient can be computed based on the solution of (3.12). As shown in Fig. 3.3(b), due to the increase of $i_{f,1}$, Γ_1 decreases over time, which can be fitted as a linear function of time. As the network remains the same, the approximate reflection coefficient is used for the rest of the waves. Consequently, the superposition of all the incident waves at the terminal of the faulty cable yields:

$$u_q = \sum_{m=0}^{\infty} u_{mq} = \sum_{m=0}^{\infty} v_1(l + 2ml, t) (\Gamma_1 \Gamma_2)^m. \quad (3.13)$$

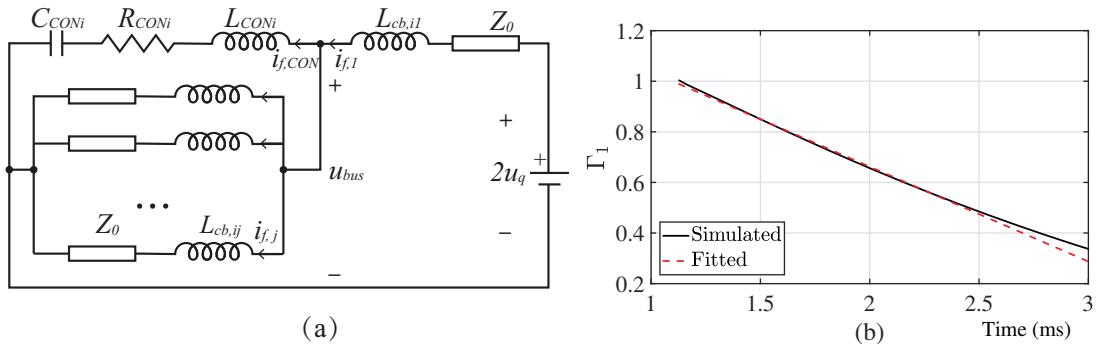


Figure 3.3: a) Equivalent DC circuit under a P2P fault; and b) the reflection coefficient at the terminal of the faulty cable.

Upon detection of a DC fault, the converter is blocked. The blocking signal generated by DESAT protection of the converter switches is faster than any other protective action. In this work, 1 ms is added to the signal of fault detection to represent the time delay in real system [77]. At the same time, the trigger signal for DC breaker is generated and the current starts to commutate to the main breaker. Then, after a delay, the main breaker opens

to clear the DC fault. Based on the operation of the breaker, the analysis and calculation are divided into three stages, and based on the state of the converter, the time interval before the main breaker opens can be subdivided into three stages, of which the equivalent models of converter are different. Based on the time-domain estimation of the travelling waves for the P2P fault at distance l from Bus_i on $Line_{i1}$, as shown in Fig. 3.1, the following transient response of the system during the fault clearance can be calculated by using the equivalent circuit at each stage, of which the maximum fault current and the maximum voltage can be determined.

Stage 1: before the main breaker opens ($t_0 \leq t \leq t_1$): The fault occurs at $t = 0$ and the first wave reaches the terminal of the faulty cable at $t = t_0$. Once the fault is detected and the trip signal is generated, the DC breaker starts to operate and the fault current is commutated from the LCS to the main breaker. Next the UFD opens. Subsequently, the main breaker opens after a delay t_{delay} , which is equal to the summation of the fault detection time and the turn-off time of NCP. Thus, the time at which the main breaker opens is $t_1 = t_0 + t_{\text{delay}}$. The converter is blocked when the fault is detected. Thus, this stage can be divided into the followings:

A) *discharging* ($t_0 \leq t \leq t_{b1}$): As the fault detection delay is t_{detect} , the blocking time of the converter is $t_{b1} = t_0 + t_{\text{detect}}$. The equivalent circuit of this stage is the same as the one shown in Fig. 3.3(a). The only difference is in the value of u_q . Instead of using only the first incident wave, all subsequent waves are considered in Stage 1. The superposition of these waves is calculated in (3.13). Prior to blocking, the discharging of the capacitors in the converter contributes to the fault current, which is modeled as an equivalent R-L-C circuit.

B) *diode free wheeling* ($t_{b1} \leq t \leq t_{b2}$): The DC components of the arm currents increase rapidly in the discharging stage. The arm currents are all below zero at the time the IGBTs are blocked, so the current flows through diode D_2 in each SM and starts to decrease, as shown in Fig. 3.4(a). This stage continues until current zero crossing occurs in any

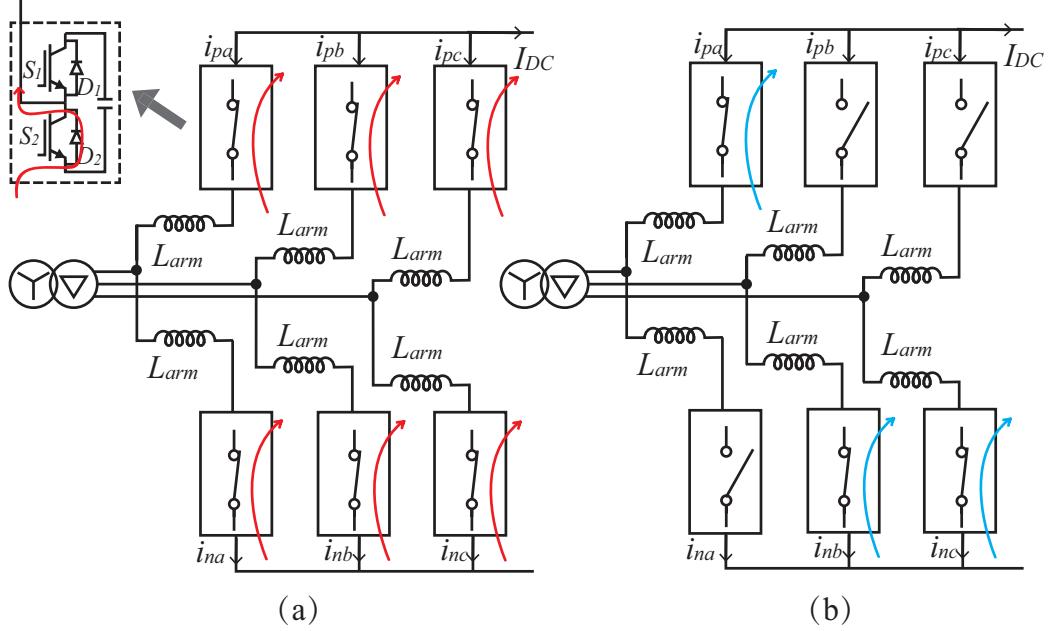


Figure 3.4: Conducting arms of the MMC: a) Stage 1B and b) Stage 1C.

arm of the converter. The DC voltage of the converter can be equal to zero while the AC side contributions are balanced and sum to zero. In each arm, the arm current contains an increasing AC component and a decreasing DC component, which is used to determine the end of this stage. The equivalent circuit in this stage is shown in Fig. 3.6(a), where $U_{\text{coni}} = 0$.

C) diode rectifier ($t_{b2} \leq t \leq t_1$): At this stage, as shown in Fig. 3.4(b), three arms are conducting from the upper and lower arms of different phases. Thus, by converting this connection of the three phases of the AC voltages, the converter becomes equivalent to a voltage source. To simplify the calculation, the same equivalent circuit in Fig. 3.6(a) can be applied, where

$$U_{\text{CON}_i} = \frac{3}{2} U_{\text{maxp}}, \quad (3.14)$$

where U_{maxp} is the peak phase-to-neutral voltage. The converter is blocked until the fault is isolated, thus the model of the converter stays the same in the following stages. During this stage, fault current continues to increase until the main breaker opens at $t = t_1$, so the

maximum current I_{\max} can be obtained based on the solution of (3.11) and (3.15).

$$\begin{aligned} 2u_q &= Z_0 i_{f,1} + L_{cb,i1} \frac{di_{f,1}}{dt} + u_{bus}, \\ u_{bus} &= Z_0 i_{f,j} + L_{cb,ij} \frac{di_{f,j}}{dt} \\ &= L_{CON} \frac{di_{f,CON}}{dt} + R_{CON} i_{f,CON} + U_{CON}. \end{aligned} \quad (3.15)$$

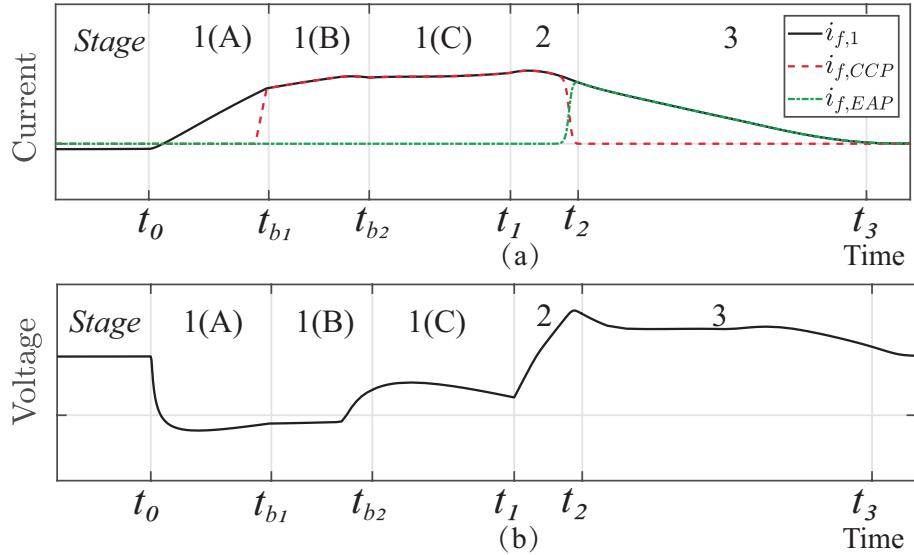


Figure 3.5: The waveforms during DC breaker operation: a) current on each branch of DC circuit breaker and b) bus-side voltage of DC circuit breaker.

The fault current $i_{f,1}$ and bus-side voltage v_{ca} during DC breaker operation in Stage 1 are shown in Fig. 3.5. As shown, the bus-side voltage of DC breaker drops below zero at t_0 and the fault current $i_{f,1}$ continues to increase until the main breaker opens at $t = t_1$. The increase rate of the fault current becomes much lower when the converter is blocked at t_{b1} , as shown in Fig. 3.5(a).

Stage 2: current commutation to the arrester ($t_1 \leq t \leq t_2$): When the main breaker is switched off at $t = t_1$, the transient voltage across the main breaker rapidly increases until the arrester starts to conduct and clamps the voltage. The fault current in the main breaker is forced to the arrester and finally reaches zero at $t = t_2$. As shown in Fig. 3.5, Stage 2 starts at $t = t_1$, i.e., the moment the main breaker opens. The current $i_{f,CCP}$ decreases

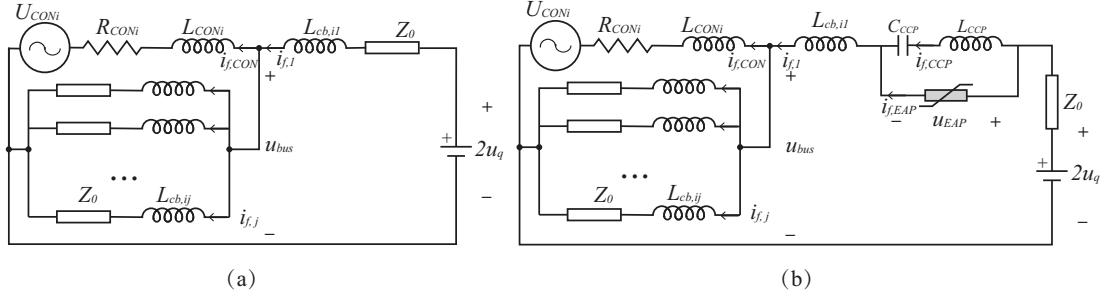


Figure 3.6: Equivalent DC circuits of a P2P fault: a) Stages 1B and 1C; and b) Stage 2.

to zero and $i_{f,EAP}$ increases rapidly when the voltage across the arrester reaches its rated voltage. The equivalent model of the DC breaker during Stage 2 is shown in Fig. 3.6(b). The main breaker is equal to an equivalent capacitor C_{CCP} and an equivalent inductance L_{CCP} when the IGBTs are switched off. The nonlinear V-I characteristics of the arrester can be expressed as the fitted curve by:

$$i_{f,EAP} = k \cdot u_{EAP}^{\alpha}, \quad (3.16)$$

where k and α are the constants of the arrester and the voltage u_{EAP} is equal to the voltage across the main breaker, which is charged by its current $i_{f,CCP}$. Hence, the equations governing the breaker transient behavior are:

$$i_{f,1} = i_{f,CCP} + i_{f,EAP}, \quad (3.17a)$$

$$i_{f,CCP} = C_{CCP} \frac{du_{CCP}}{dt}, \quad (3.17b)$$

$$u_{EAP} = L_{CCP} \frac{di_{f,CCP}}{dt} + u_{CONi}. \quad (3.17c)$$

KVL for the circuit of Fig. 3.6(b) yields

$$2u_q = u_{EAP} + Z_0 i_{f,1} + L_{cb,i1} \frac{di_{f,1}}{dt} + u_{bus}. \quad (3.18)$$

The elevation of voltage across the DC breaker also causes over voltage on the bus-side voltage of the breaker, of which the maximum voltage V_{\max} occurs at the time the arrester starts to clamp the voltage, as shown in Fig. 3.5(b). By solving (3.16) to (3.18) in this stage, V_{\max} can be found from the numerical solutions of the voltage.

Stage 3: fault current down to zero ($t_2 \leq t \leq t_3$): After the main breaker completely opens at $t = t_2$, the increase impedance of the arrester forces the DC fault current to rapidly decrease. As shown in Fig. 3.5, the bus-side voltage of DC breaker is clamped and the current $i_{f,EAP}$ decreases until reaches zero at $t = t_3$, which is the end of the breaker operation. Thus, in Fig. 3.6(b), the equivalent circuit of the CCP is removed and only the arrester remains connected in the equivalent circuit during Stage 3. The currents and voltages during Stage 3 can be computed by the same method in Stage 2. The time from t_2 to t_3 is called the breaking time, t_{breaking} , of the DC breaker. The operation time of the DC breaker, defined as t_{clear} , is from t_0 to t_3 . Subsequently, the energy absorbed by the arrester, W_{EAP} , can be computed by

$$W_{EAP} = \int_{t_0}^{t_3} u_{EAP,i} i_{f,EAP} dt. \quad (3.19)$$

3.4 Estimation of the Worst-case Fault Location

Based on the aforementioned time-domain analysis, I_{\max} , V_{\max} , t_{clear} and W_{EAP} can be obtained from the numerical solutions for the fault at distance l from the terminal, which are taken as the metrics for optimum selection of the DC breaker parameters. Since the fault can happen anywhere on the cable and the distance of the fault location has an impact on I_{\max} , V_{\max} , t_{clear} and W_{EAP} , it is necessary to indicate the fault location for the worst case scenario with maximum I_{\max} and V_{\max} . The worst-case fault location problem has been investigated in [78][79]. However, the relationships between fault location and fault metrics have not yet been analyzed. Additionally, the worst-case distances of the transmission lines that are shorter than the critical distance are not calculated. The following analysis fills this

gap and provides a guidance for the optimal selection of system parameters.

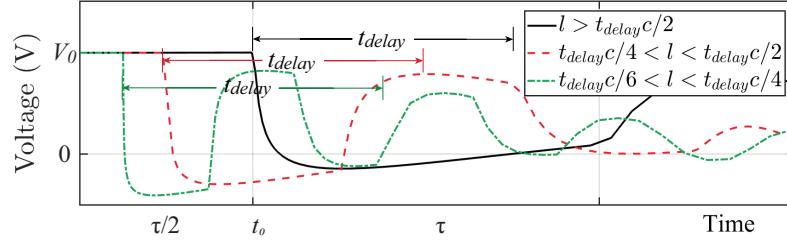


Figure 3.7: Voltage at the terminal of the faulty cable with different fault location.

For P2P faults at different distance l , the waveforms of the voltage at the terminal of the faulty cable are shown in Fig. 3.7. As shown, several reflections result in several voltage peaks. The duration of each reflection is $\tau = 2l/c$. The increase rate of fault current depends on the voltage across L_{cb} . If the voltage wave u_q is at the lower peak, the increased voltage across L_{cb} results in a higher rate of increase of the fault current. On the contrary, during the duration of u_q at the higher peak, the fault current increases slowly due to the reduced voltage difference across L_{cb} .

The maximum current within the time interval t_{delay} changes with the fault location. The relationship between the maximum current I_{\max} and l is as follows:

- If $l > t_{\text{delay}}c/2$, which corresponds to $t_{\text{delay}} < \tau$, the increase rate of the fault current is at a high level. Considering the attenuation of the propagation wave, a lower distance l results in a higher di/dt and subsequently a larger I_{\max} . Thus, the worst fault location with maximum current is when $\tau = t_{\text{delay}}$. This location, which is $l_0 = t_{\text{delay}}c/2$, is defined as the characteristic length.
- If $t_{\text{delay}}c/4 < l < t_{\text{delay}}c/2$, which corresponds to $\tau < t_{\text{delay}} < 2\tau$, there will be an interval in which the current increases slowly and the duration of this interval increases with l . Therefore, as l increases, I_{\max} decreases.
- When the fault is located closer to the terminal in the next interval, as mentioned earlier, the longer the duration of the lower peak of the wave u_q is, the higher I_{\max} is.

If the fault location is too close to the terminal, τ becomes much less than t_{delay} and the time interval with higher increase rate can be regarded as equal to half of t_{delay} . Hence, I_{\max} increases with shorter l due to the attenuation of u_q .

Furthermore, at a fault location with a larger maximum current, when the main breaker opens, the next increasing reflection adds to the voltage generated by the breaker, causing a higher maximum overvoltage. The relationship between the maximum voltage V_{\max} and l is similar to I_{\max} . For optimum parameter selection, I_{\max} and V_{\max} should be calculated for the worst case scenario, which is when the fault occurs at the defined characteristic location l_0 on the faulty cable. In addition, if the length of the cable is lower than l_0 , the fault location should be given by comparing the possible peak values.

3.5 Simulation Results

3.5.1 The Test MTDC Grid

Fig. 3.8 shows the layout of the test system adopted in this chapter. It represents a ± 200 kV five-terminal symmetric monopole meshed HVDC grid, constructed from the CIGRE benchmark model [80]. The DC lines $Line_{34}$, $Line_{45}$, $Line_{56}$ are 300 km long while the rest are 200 km long. DC circuit breakers are located at both ends of each HVDC link. In Fig. 3.8, for the sake of simplicity, the $Line_{56}$ is represented with its associated breakers at its two ends, while the other lines simply show the connections between the buses. The VSC stations use the well-known MMCs [29].

The MMC-MTDC system of Fig. 3.8 is built in the PSCAD/EMTDC software environment for time-domain simulations with frequency-dependent, distributed cable model. To evaluate the degree of accuracy and examine the validity of the calculations based on the equivalent circuits, the calculation results are compared with the corresponding results obtained from the exact model of the study system in the PSCAD. The main parameters of the system are listed in Table 3.1. The distributed parameters of the cable used in the cal-

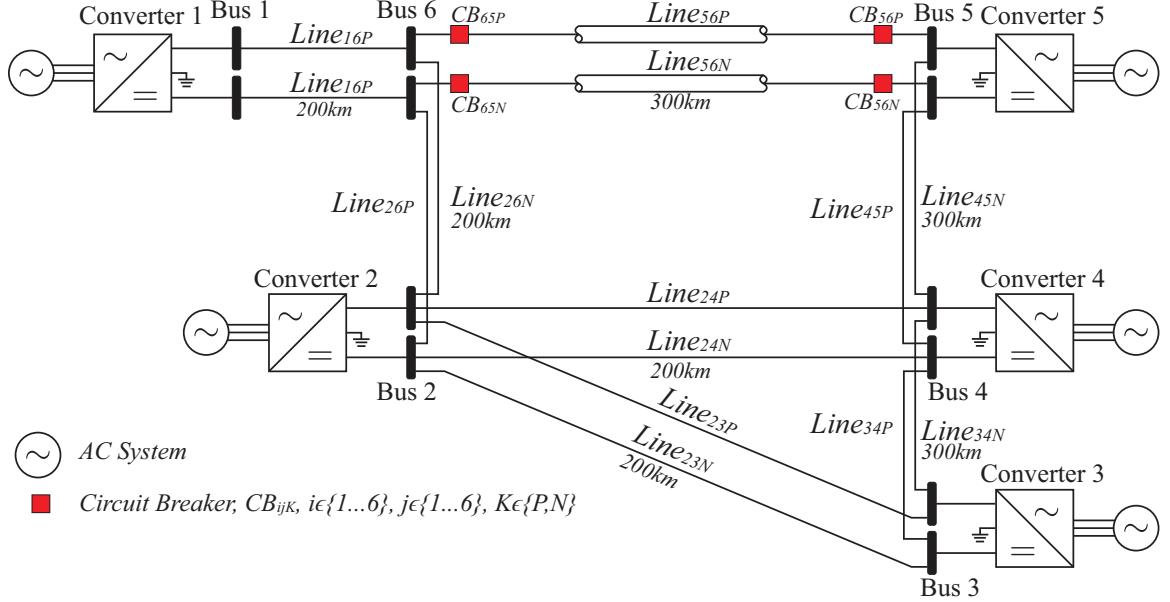


Figure 3.8: Layout of the CIGRE MTDC grid test system [80].

culations are from the PSCAD Line Constants Program at the frequency of 0.1 MHz [47], which is based on the fact that the high frequency range of propagation matrix quantities are almost constant. Considering the skin effect at high frequency, the characteristic impedance is $Z_0 = \sqrt{(sL + K\sqrt{s})/(sC)} \approx \sqrt{L/C}$. The skin effect factor $K = R_{HF}/\sqrt{\pi \cdot f_{HF}}$.

Table 3.1: Converter and grid parameters of the five-terminal MTDC test system,

	Conv. 1	Conv. 2-5
Rated capacity [MVA]	450	120
Rated DC Voltage [kV]	±200	±200
Rated AC voltage [kV]	220	220
Operation Mode Setpoints	±200 [kV]	-100 [MW]
Sub-module capacitance C_{SM} [μF]	2400	600
Arm reactor L_{arm} [mH]	40	160
Sub-module resistance R_{SM} [Ω]	0.001	0.001

3.5.2 Evaluation of the Transient Analysis

Case 1: The positive and negative poles are shorted at a distance of 200 km from *Bus₄* on *Line₃₄*. The breakers CB_{43} and CB_{34} operate once the trip signals are generated. In this

case, the current limiting reactors L_{cb} are equal to 100 mH and t_{delay} is set at 4 ms. The switching voltage of the breaker is usually designed from 1.2 pu to 1.5 pu with considering fast current interruption and insulation level [50][52]. Therefore, the rated voltage of arresters in DC breakers is set at 300 kV. The fault current $i_{f,43}$, the current contributed from the converter $i_{f,CON4}$ and the current from the adjacent cable $i_{f,54}$ are measured in the simulation. The cable-side and the bus-side voltages of the DC breaker are also recorded as v_{41} and v_{42} , respectively.

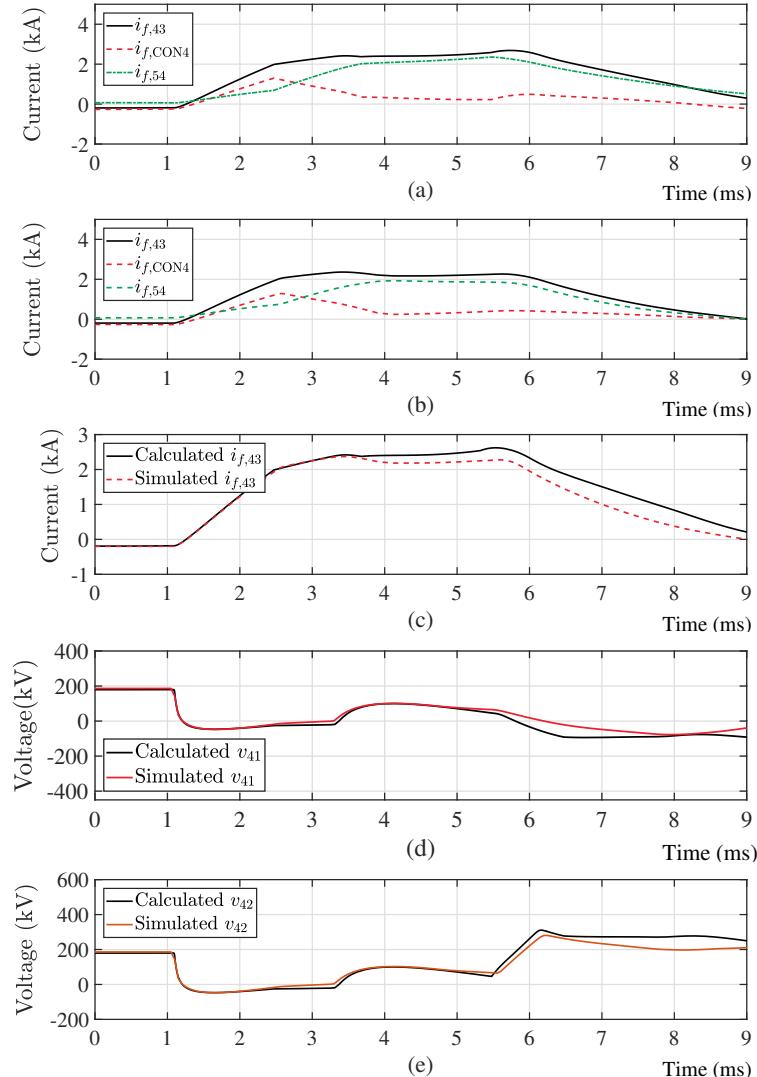


Figure 3.9: Calculated and simulated results for Case 1: a) calculated currents; b) simulated currents; c) fault current $i_{f,43}$; d) cable-side voltage v_{41} ; and e) the bus-side voltage v_{42} .

The waveforms of the corresponding current and voltage from calculation based on the

equivalent circuit model are compared with the simulation results in Fig. 3.9. The fault occurs at $t = 0$ ms and reaches the terminal at $t = 1.08$ ms. The fault current through the DC breaker increases very fast. Based on the computed and the simulated currents shown in Figs. 3.9(a) and (b), the current of the faulty cable is contributed by the converter and the adjacent cable. The increase rate at the first stage, which is determined by the voltage across L_{cb} , is quite high because the voltage at the cable side of the breaker, v_{41} , drops below zero due to the first reflection at the terminal, shown in Fig. 3.9(d). When the converter is blocked at $t = 2.53$ ms, the increase rate is much lower due to the decrease of current from converter. During the next stage, on one hand, the equivalent voltage source of the converter contributes to the increase of the fault current. On the other hand, the voltage v_{42} at the second reflection limits its increase rate. Therefore, the fault current does not increase any longer during this interval and reaches its maximum value at the end of the first reflection at $t = 3.24$ ms. At $t = 5.53$ ms, the main breaker opens and the voltage across it rises very fast because of the restored energy in the inductance of the DC circuit. Consequently, as shown in Fig. 3.9(e), the voltage at the bus side of DC breaker v_{42} increases as well until the arrester clamps the voltage. The maximum voltage is mainly based on the rated voltage of the arrester U_r . The voltage v_{41} at its second reflection can also increase the maximum voltage of v_{42} . In this stage, the counter voltage forces the fault current to decrease until it reaches zero. So, a higher U_r causes a higher maximum voltage and a larger decrease rate of current, thereby reducing the fault clearance time.

Figs. 3.9(c)-(e) show a close agreement between the exact response obtained from the PSCAD/EMTDC model and that of the calculated one from the equivalent circuit. Since the computation is based on the high-frequency model, the differences with the simulation occur at the later stage of the wavefront. Consequently, the maximum current and the maximum voltage are slightly larger than the simulated ones. However, in view of the safety margin of fault protection, this is acceptable in the parameter optimization algorithm.

Case 2: The objective of this case, performed at Bus_5 with three cables connected in parallel, is to examine the applicability of the calculation method to several adjacent cables in a complex network. In this case, $L_{cb}=100\text{ mH}$ and the delay time $t_{delay}=3\text{ ms}$, so the worst case is taken with a P2P fault at 275 km, i.e., the characteristics length l_0 , from Bus_5 at $Line_{45}$.

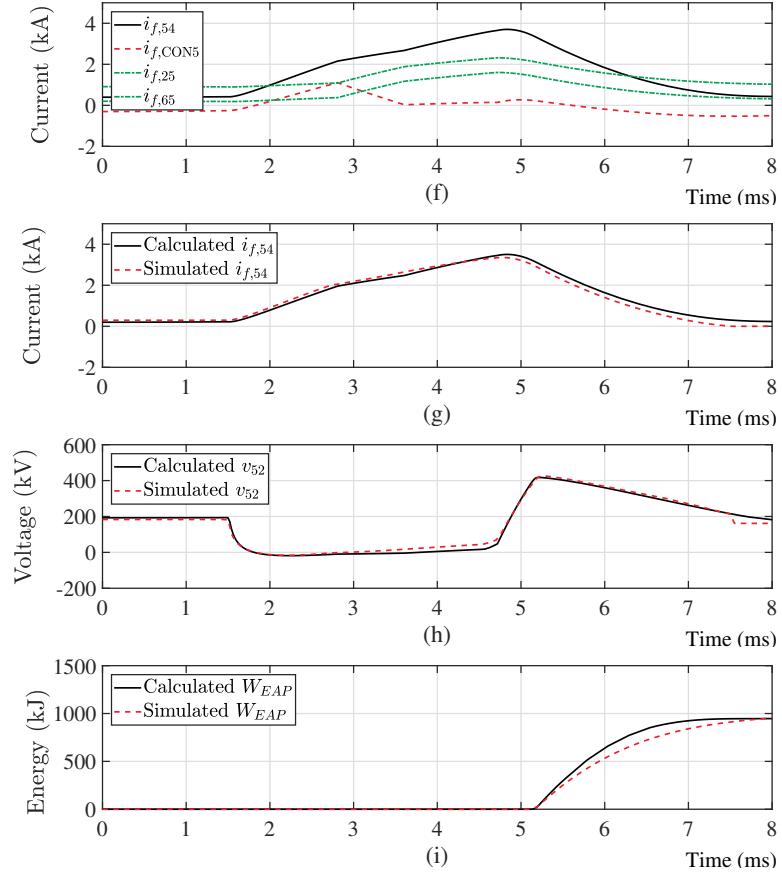


Figure 3.10: Calculated and simulated results for Case 2: a) calculated currents; b) fault current $i_{f,54}$; c) bus-side voltage v_{52} ; and d) energy absorption W_{EAP} .

The comparison of the calculated and simulated results is shown in Fig. 3.10. Based on the currents from calculation and simulation shown in Figs. 3.10(a) and (b), respectively, the fault current $i_{f,54}$ is the summation of the currents from converter and the adjacent cables. The increase rates of the current from adjacent cables, $i_{f,25}$ and $i_{f,65}$, are the same due to the same L_{cb} and Z_0 . Prior to opening the main breaker, the cable-side voltage of the breaker v_{51} is mainly at the first reflection. Thus, the fault current $i_{f,54}$ keeps in-

creasing fast in this interval, except the duration with lower increase rate at the stage after converter blocking, because of the large voltage difference across L_{cb} . At the moment the main breaker opens at $t = 4.75$ ms, voltage v_{51} starts to increase at its second reflection. Therefore, the voltage on the bus side of DC breaker v_{52} equals to the superposition of v_{51} and the voltage across the DC breaker, resulting in the most severe overvoltage of v_{52} . This confirms that not only the limiting reactor and the rated voltage of the arrester impact the transients, but also the delay time before main breaker opens, influences the maximum current and the maximum voltage, which determines the fault location of the worst case and the increasing time of fault current. At the moment when the voltage across the main breaker reaches the rated voltage, the arrester starts to conduct and absorb the residual energy, as shown in Fig. 3.10(d).

CHAPTER 4

OPTIMIZATION OF DC CIRCUIT BREAKERS

4.1 Parameter Optimization of DC Circuit Breakers

The maximum current and voltage, clearing time, and energy absorption in the arresters of a DC circuit breaker are critical in system protection and fast recovery from DC faults. These metrics are influenced by the parameters of the DC breaker components, which should be optimally selected/sized when designing the system.

Among all the parameters of a DC circuit breaker, the current limiting reactor, the rated voltage of the arrester and the delay time are of the most critical factors influencing the breaker performance. The current limiting reactor is used to limit the maximum current within the interruption capability of the breaker. The rated voltage of the arrester determines the overvoltage level and the decrease rate of the fault current directly. The delay time, which is limited by the opening speed of the UFD, is always one of the most important determinants of the operation time of the DC breaker.

Due to the different impacts of each parameter on the transient response, it is difficult to select an optimal combination of them. The series-connected current limiting reactor of the DC breaker can limit the increase rate of fault current. However, it ironically impacts the maximum voltage by increasing the reflection coefficient and lengthening the interruption time of the circuit breaker. In addition, the reactors in the adjacent cables can also influence the overcurrent and overvoltage. The increase of the delay time for the UFD before the main breaker opens, can increase the maximum current. However, the maximum voltage also depends on the travelling wave during the time delay. Furthermore, reducing the rated voltage of the arrester can reduce the overvoltage to a lower level. However, it will lengthen the operation time of the breaker. Therefore, all the trade-offs among I_{\max} , V_{\max} , t_{clear}

and W_{EAP} should be taken into the optimization. In this chapter, the time-domain method proposed in Chapter 3 and the genetic algorithm are used to solve the optimization problem. The process includes the followings:

- Based on the detailed analysis during the fault clearance process presented in Chapter 3, I_{max} , V_{max} , t_{clear} and W_{EAP} can be obtained from the numerical solutions. I_{max} , V_{max} , t_{clear} and W_{EAP} are nonlinear functions of the parameters $L_{cb,i1}...L_{cb,ij}$, t_{delay} and U_r , which can be expressed by

$$f_m(x), m = 1, 2, 3, 4; \quad (4.1a)$$

$$x = [L_{cb,i1}...L_{cb,ij}, t_{delay}, U_r]; \quad (4.1b)$$

$$I_{max} = f_1(x); \quad (4.1c)$$

$$V_{max} = f_2(x); \quad (4.1d)$$

$$t_{clear} = f_3(x); \quad (4.1e)$$

$$W_{EAP} = f_4(x); \quad (4.1f)$$

where $L_{cb,i1}...L_{cb,ij}$ represent the reactors in the faulty cable and the adjacent cables. In the practical MTDC systems, the reactors of different lines might be different and need to be optimized independently at the same time.

- The bound of each parameter is based on the voltage class and rated power of the system. These bounds, which are determined by the cost, insulation coordination, etc., can be obtained from the specifications of a real system. The current limiting reactor should be large enough to limit the maximum current within the interruption capability of the DC breaker. However, it is constrained by the cost and volume. The range of the rated voltage of the arrester is based on the insulation level of the DC lines. The delay time of the DC breaker is mainly limited by the opening speed and the voltage withstanding capability of the UFD.

- The multi-objective problem, which aims to minimize the I_{\max} , V_{\max} , t_{clear} and W_{EAP} by optimal selection of the parameters within their bounds, can be formulated as

$$\underset{x}{\text{minimize}} \quad f_m(x) \quad (4.2a)$$

$$\text{subject to} \quad x_i^L \leq x_i \leq x_i^U, i = 1, 2, \dots, n. \quad (4.2b)$$

where $x = [L_{\text{cb},i1} \dots L_{\text{cb},ij}, t_{\text{delay}}, U_r]$, and $f_m(x)$ represents the metrics I_{\max} , V_{\max} , t_{clear} and W_{EAP} with respect to the variables L_{cb} , t_{delay} and U_r . In addition, for the sake of convenience for computation, it is assumed that all the reactors are identical and denoted by L_{cb} in this work. The genetic algorithm is then applied to compute Pareto-optimal sets for (4.9).

- By the genetic algorithm, a set of solutions of this multi-objective problem can be obtained with the corresponding metrics. Although the metrics are not minimized at the same time, the optimal parameters can be selected from the solutions according to the requirements of the system protection. Some of the metrics can be the minimum while others are limited within their specified ranges.

4.2 Sequential Tripping Strategy of DC Circuit Breaker

The hybrid DC circuit breaker, shown in Fig. 2.1, comprises the parallel connection of the NCP, which is formed by the LCS in series with the UFD, the CCP known as the main breaker, which consists of several modules, consisting of a number of series-connected semiconductor devices, and the energy absorption path (EAP), on which the arrester banks are deployed on the modules of the CCP to limit the voltage and absorb the residual energy when the main breaker is switched off. A series current limiting reactor L_{cb} is also connected in the circuit breaker to limit the rate of rise of the fault current.

To demonstrate the fault response subsequent to a DC-side fault, a timeline is presented in Fig. 2.1. The fault current reaches the DC circuit breaker at the terminals of the faulty

line at t_0 . Upon detection of the DC-side fault at t_d and considering a detection delay of t_{detect} , the DC circuit breaker starts to isolate the faulty line. The LCS in the NCP is switched off subsequently to the closing of switches in the CCP to force the current to the CCP. Conventionally, a time delay is inserted to ensure successful opening of the UFD. The IGBTs within all N modules are then tripped simultaneously. The opening of these modules introduces a fast increased voltage across the breaker due to the release of energy stored in the circuit inductance [1]. This transient voltage exceeds the threshold voltage of the arresters until it is clamped by their highly nonlinear V-I characteristics. To ensure a successful operation of the NCP under high voltage stress, a certain delay t_{delay} has to be inserted before a sufficient voltage withstand capability is fully built up across the UFD [81–85]. This delay ultimately limits the speed of hybrid DC circuit breaker.

To expedite the operation of hybrid DC circuit breaker, a sequential switching strategy is proposed, in which the switches of the N modules in the main breaker are switched off sequentially. The opening of the breaker is divided into N stages. Consisting of semiconductor switches and their paralleled arresters, each module is treated as an individual breaker. These modules do not necessarily need to be tripped at the same time. Instead, the trip signals for them are generated sequentially at $t_1, t_2 \dots t_N$. The arresters within these modules are rated at lower voltages, enabling them to introduce a lower voltage stress when inserted into the circuit individually. By tripping these modules sequentially, the voltage across the UFD is built up step by step. Since the voltage withstand capability of the UFD is established incrementally [81–85], the breaker modules can be tripped earlier, even before it is fully opened. For example, the switches of Module 1 are commanded to open at t_1 , which is earlier than the original tripping instant in the conventional method. The fault current tends to increase slowly with the arresters in Module 1 been inserted. Sequentially, Module 2 is tripped at t_2 , thereby the rate of rise of fault current is further limited. This process is repeated until all of the N modules are switched off, which allows the voltage across the hybrid circuit breaker to increase incrementally. Consequently, the fault clear-

ance time can be reduced, and the overvoltage and the overcurrent stresses on the system are relieved as well.

The currents and voltages of the hybrid circuit breaker tested with simultaneous conventional and a four-stage sequential tripping strategies are shown in Fig. 4.1. A fault occurs at $t = 0$ ms and reaches the circuit breaker at $t = 1.1$ ms. Upon fault detection at $t = 1.7$ ms, the current is routed from the NCP to the CCP. After 1.1 ms delay for the opening of UFD connectors, in sequential tripping case, the switches of Module 1 open 0.9 ms earlier than the simultaneous case. The voltage across the hybrid circuit breaker increases step by step with the sequential tripping of the modules. Compared to the abrupt voltage increase in simultaneous switching, the reduced voltage stress on the UFD allows the breaker to be opened earlier. Meanwhile, the fault current can be reduced since the voltage is applied earlier.

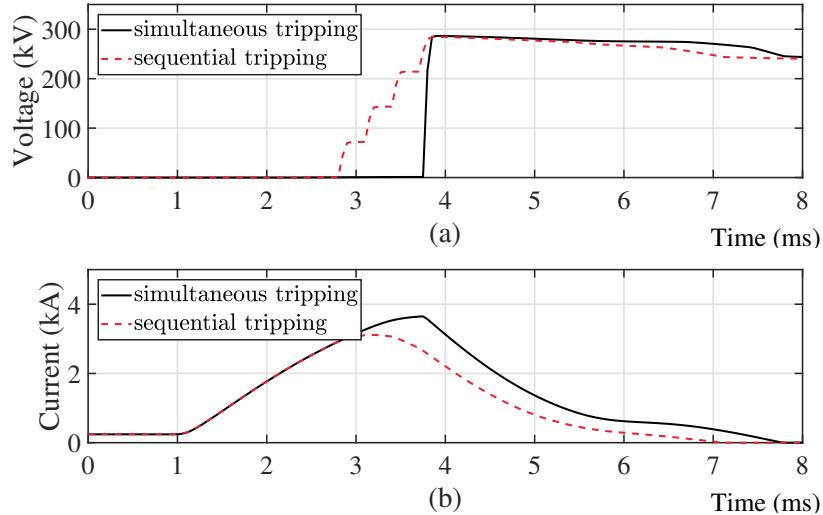


Figure 4.1: Simulated results in simultaneous and sequential tripping cases: a) voltage of the hybrid circuit breaker; and b) fault current.

4.3 Energy Distribution among Arresters

Apart from the advantages offered by the sequential tripping, the energy absorbed by each module tends to be distributed unevenly, as shown in Fig. 4.2(a). Those modules that are

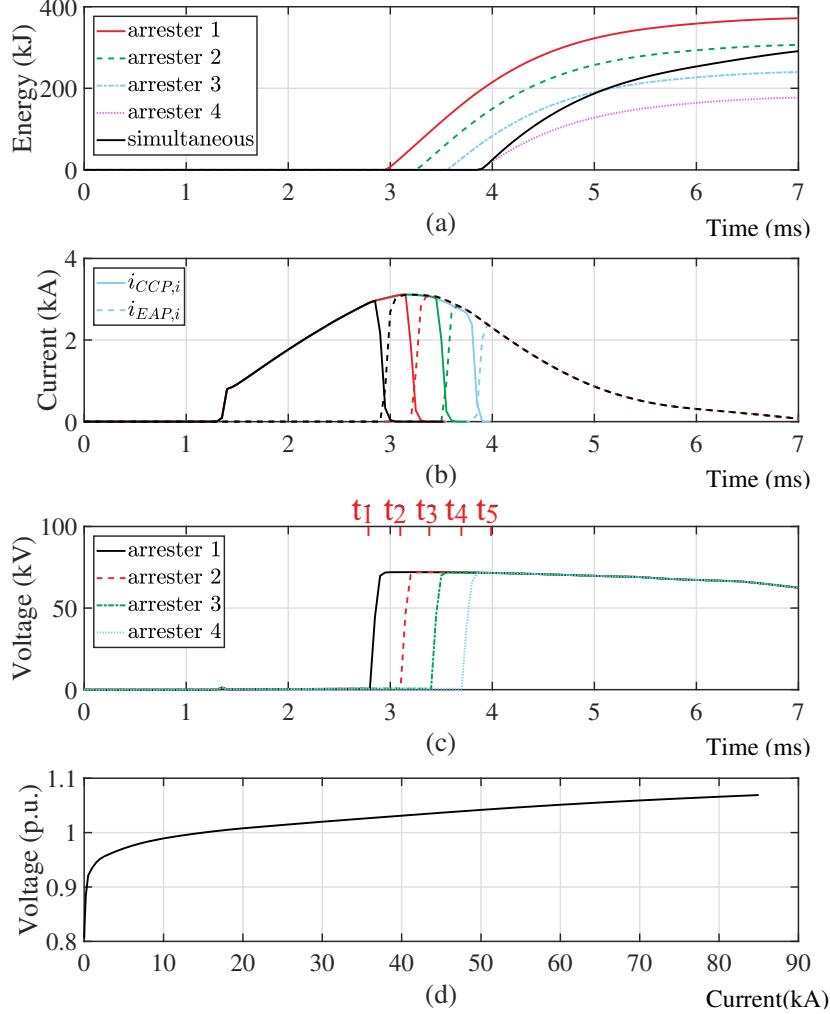


Figure 4.2: Simulated results of each module: a) currents of each module; b) voltage of various module arresters; c) absorbed energy by arresters and d) V-I characteristic of the arrester.

tripped earlier tend to dissipate more energy, making them vulnerable to thermal overloading. Assuming that the clamped voltage of an arrester inside Module i is $v_{EAP,i}$ and the corresponding current is $i_{EAP,i}$, the energy absorption of the arrester i can be expressed by

$$W_{EAP,i} = \int_{t_i}^{t_{\text{clear}}} v_{EAP,i} i_{EAP,i} dt, \quad (4.3)$$

where $W_{EAP,i}$ is the absorbed energy, and t_1 and t_2 are the starting and ending time instants of insertion of the arrester in Module i , respectively.

The current and voltage profiles of breaker modules tripped by the proposed strategy are provided in Figs. 4.2(b) and (c). Starting from the tripping of Module 1, the current does not substantially change till the opening process of all modules is completed. The voltage is also clamped at the same value by the non-linear V-I characteristic of the arrester, as shown in Figs. 4.2(d). Therefore, the absorbed energy of each arrester is largely proportional to the duration in which each of them is inserted into the circuit. The arrester within the earlier switched module absorbs more energy, as shown in Fig. 4.2(a). The energy difference is enlarged when a higher delay is applied between each module.

To address this issue, a modified sequential strategy is proposed to equally distribute the energy among all arresters, which adjust the sequence of the tripping to achieve equal inserting duration for each arrester [9]. $t_i, i \in [1, 4]$, represent the time instants when the arresters 1 to 4 are tripped with the normal sequential tripping, as annotated in Fig. 4.2(c). Time t_5 is the instant when all four arresters are completely inserted. The periods t_1 to t_5 are evenly divided into 10 subintervals. The circle indicates the insertion of the corresponding arrester during the specific subinterval indicated on the left most column. In normal sequential tripping method, arrester 1 is inserted within all ten subintervals while arrester 4 is just inserted within two subintervals.

Table 4.1: Demonstration of the modified sequential tripping strategy [9].

subinterval	Original Sequential				Modified Sequential			
	1	2	3	4	1	2	3	4
$t_1 \sim (t_2 - t_1)/2$	○					○		
$(t_2 - t_1)/2 \sim t_2$	○					○		
$t_2 \sim (t_3 - t_2)/2$	○	○				○	○	
$(t_3 - t_2)/2 \sim t_3$	○	○			⇒		○	○
$t_3 \sim (t_4 - t_3)/2$	○	○	○			○	○	○
$(t_4 - t_3)/2 \sim t_3$	○	○	○			○	○	○
$t_4 \sim (t_5 - t_4)/2$	○	○	○	○		○	○	○
$(t_5 - t_4)/2 \sim t_5$	○	○	○	○		○	○	○

The modified strategy, which is provided in Table 4.1, controls the number of circles in each row such that the inserted voltage increases incrementally to clear the fault current.

Meanwhile, the tripping sequence is redistributed in such a way that every arrester is inserted for the same duration of time (the summation of each column is the same) before t_5 , from when all four arresters are inserted at the same time. Taking arresters 1 and 2 as an example, the absorbed energy of the original and modified sequential tripping strategies can be calculated by (4.3) and (4.5), respectively, as

$$\begin{aligned} W_{\text{EAP},1} &= \int_{t_1}^{t_5} v_{\text{EAP},1} i_{dc} dt, \\ W_{\text{EAP},2} &= \int_{t_2}^{t_5} v_{\text{EAP},2} i_{dc} dt. \end{aligned} \quad (4.4)$$

$$\begin{aligned} W_{\text{EAP},1} &= \int_{t_1}^{(t_3-t/2)/2} v_{\text{EAP},1} i_{dc} dt + \int_{t_4}^{t_5} v_{\text{EAP},1} i_{dc} dt, \\ W_{\text{EAP},2} &= \int_{t_2}^{(t_3-t/2)/2} v_{\text{EAP},2} i_{dc} dt + \int_{t_3}^{t_5} v_{\text{EAP},2} i_{dc} dt. \end{aligned} \quad (4.5)$$

Since the eight subintervals are equally divided, the energy absorbed by Module 1 and Module 2 are close, as indicated by $W_{\text{EAP},1}$ and $W_{\text{EAP},2}$ in (4.5). In this way, the energy distribution is significantly improved.

4.4 Tripping Sequence Optimization

Based on the aforementioned modified strategy, the energy of the arresters can be theoretically distributed evenly to avoid any thermal overload. However, the fault current does not strictly remain the same during the opening of the modules as assumed. The energy difference among modules still exists, demanding further improvement of this tripping strategy. Moreover, the rated voltage of arresters and the tripping intervals between each module do not necessarily need to be the same. These parameters are to be determined in such a way that the voltage withstand capability established by the UFD can be optimally utilized at every instant. While ensuring successful opening of each module, this optimization makes a further improvement on transient performance.

The voltage withstand capability of the UFD is a function of time largely determined by its contact travel curve and insulation medium [81–85]. This capability is built up with the increment of distance between the contacts [85, 86]. The opening speed of the contacts varies for different UFDs. The detailed discussion on this topic will be presented in a future work. In this work, a non-decreasing characteristic of the UFD is generally assumed and depicted in Fig. 4.3. At the time Module i opens, the inserted voltage established by the arresters is applied to the UFD. At this moment, the corresponding voltage withstand capability of the UFD should be higher than this voltage. As shown in Fig. 4.3, the tripping schedule is determined by both the rated voltages u_r and tripping stages N . These two parameters will ultimately influence the system performance metrics, i.e., fault clearance time, overcurrent, overvoltage, and energy absorption.

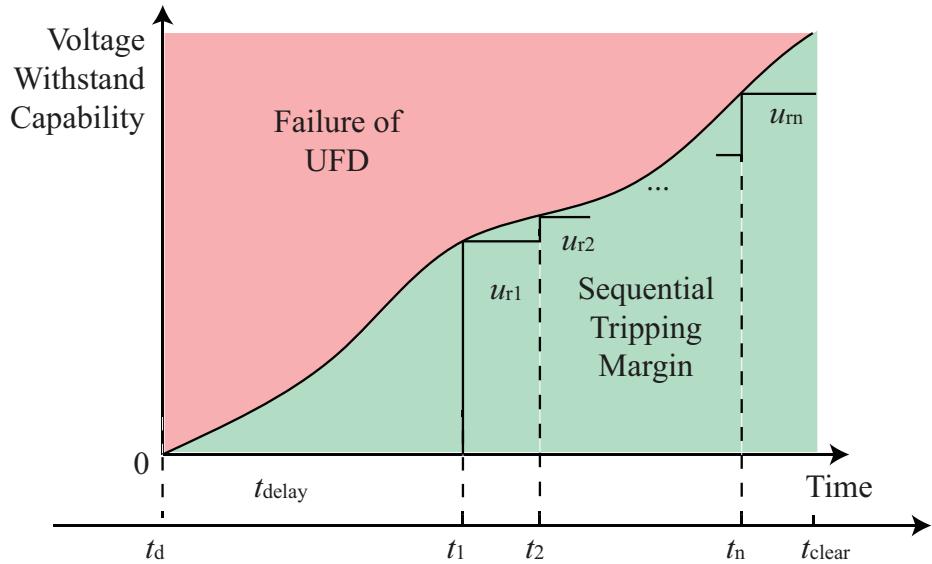


Figure 4.3: Generic voltage withstand capability versus opening time of the UFD.

Typically, a module with a smaller u_r can be tripped earlier provided that a smaller additional withstand capability is required. However, this will result in an increment of the tripping stages. A large number of stages will add to the complexity of the controller and will potentially lead to a higher overvoltage. Additionally, the clearance time cannot be further improved with too many stages involved. To this end, the parameters of the

sequential tripping should be selected wisely considering the trade-offs between different system metrics. An optimization should be performed to achieve such a balance. In a real application, it is likely that the arresters within the breaker modules are rated at the same level, for the sake of the simplicity of manufacturing maintenance. On the other hand, these arresters could be rated at different levels from an economical perspective. In this chapter, two optimization approaches are provided with respect to these considerations.

4.4.1 Approach 1

In the first approach, the rated voltage of the arresters of all modules are set to be same. The task is then to minimize the system performance metrics with respect to this rated voltage u_r and the number of tripping stages N .

In case u_r and N are selected, the earliest tripping instants of each module, t_i can be determined from the characteristic of the UFD. To prevent the UFD from failure, Module i should not be opened until the UFD is able to withstand the voltage inserted by the arresters. As shown in Fig. 4.3, at each instant t_i , an additional voltage u_{ri} is added on top of the previously accumulated voltage through the insertion of Module i . Intuitively, the earliest trip instant of Module i is the moment when this accumulated voltage curve intersects with the UFD characteristic curve. With this approach, t_i can be written as

$$t_i = f_1(u_r, N). \quad (4.6)$$

The expressions of the current flowing through DC circuit breaker, i_{dc} and the voltage across DC circuit breaker, v_{dc} are given as

$$i_{dc} = f_2(u_r, N) \quad (4.7a)$$

$$v_{dc} = f_3(u_r, N), \quad (4.7b)$$

where these transient functions can be obtained through the time-domain calculation method

proposed in Chapter 3, as described in detail in Section V. In this way, the system metrics, i.e., peak overcurrent i_{\max} , peak overvoltage v_{\max} , fault clearance time t_{clear} , and energy absorption W_{sum} , are given as functions of u_r and N as

$$i_{\max} = g_1(u_r, N), \quad (4.8a)$$

$$v_{\max} = g_2(u_r, N), \quad (4.8b)$$

$$t_{\text{clear}} = g_3(u_r, N), \quad (4.8c)$$

$$W_{\text{sum}} = \sum_{k=1}^N W_{\text{EAP},i} = g_4(u_r, N). \quad (4.8d)$$

Each of the four metrics can be used as the objective function for the optimization problem formulated in (4.9).

$$\underset{u_r, N}{\text{minimize}} \quad g(u_r, N) \quad (4.9a)$$

$$\text{subject to} \quad N_{\min} \leq N \leq N_{\max}, \quad (4.9b)$$

$$u_{r,\min} \leq u_r \leq u_{r,\max}, \quad (4.9c)$$

$$u_r \cdot N \leq u_{r,\text{sys}}, \quad (4.9d)$$

where $g(u_r, N)$ represents one of the system metrics in equation (4.8). Inequalities (4.9b) and (4.9c) ensure N and u_r stay within their reasonable limits. The total rated voltage of the DC circuit breaker is limited by the insulation capability of the system, $u_{r,\text{sys}}$. This constraint is given by (4.9d).

A set of u_r and N is obtained by solving the optimization problem (4.9). However, the energy among N modules are not strictly balanced using the modified sequential tripping strategy. Considering that the tripping intervals are not necessary to be same, the $N - 1$

tripping instants t_2, t_3, \dots, t_N are open to be manipulated around the previous values to balance the energy. Given u_r and N , each $W_{EAP,i}$ can be written as a function of t_2, t_3, \dots, t_N . Solving a set of $N-1$ energy balancing equations $W_{EAP,i} = W_{EAP,i+1}, i \in \{1, \dots, N-1\}$ with respect to the $N - 1$ tripping instants, the energy of each module is kept equal.

4.4.2 Approach 2

In some cases, the arrester within each module can be sized in such a way that the cost is minimized. The ratings of these arresters can thus be determined individually as $u_{r,1}, u_{r,2}, \dots, u_{r,N}$. It is assumed that the summation of all rated voltages is $u_{r,sys}$ and the number of tripping stage N is fixed.

Based on the time-domain calculation method provided in Section V, the four system metrics can be written as functions of the rated voltage of each arrester. The optimization problem is formulated as

$$\underset{u_{r,1}, \dots, u_{r,N}}{\text{minimize}} \quad h(u_{r,1}, \dots, u_{r,N}) \quad (4.10a)$$

$$\text{subject to} \quad \sum_{k=1}^N u_{r,k} = u_{r,sys}, \quad (4.10b)$$

$$u_{r,\min} \leq u_{r,k} \leq u_{r,\max}, k \in \{1, \dots, N\}, \quad (4.10c)$$

where $h(u_{r,1}, \dots, u_{r,N})$ represents one of the system metrics with respect to $u_{r,i}$.

4.5 Simulation Results

4.5.1 Evaluation of Parameter Optimization

The test MTDC grid shown in Fig. 3.8 is used to evaluate the proposed parameter optimization method. As demonstrated earlier, the parameters of the system and the DC

breaker have significant impacts on the transient performance during the fault clearance. The current limiting reactor L_{cb} , the delay time of the breaker t_{delay} and the rated voltage U_r are taken as the parameters to be optimized. With the algorithm shown in Section 4.1, the objectives including the maximum current I_{max} , the maximum voltage V_{max} , the operating time t_{clear} and the energy absorption W_{EAP} during breaker operation are written as functions of these variables. Based on the layout of Bus_4 in Case 1, three sets of parameters are chosen:

- $L_{cb} = 100 \text{ mH}, t_{delay} = 3.0 \text{ ms}, U_r = 350 \text{ kV}.$
- $L_{cb} = 50 \text{ mH}, t_{delay} = 2.0 \text{ ms}, U_r = 250 \text{ kV}.$
- $L_{cb} = 200 \text{ mH}, t_{delay} = 2.5 \text{ ms}, U_r = 450 \text{ kV}.$

For each set of parameters, calculations for I_{max} , V_{max} , t_{clear} and W_{EAP} are made by changing one variable. The relationship between the objectives with each variable is analyzed with the results shown in Fig. 4.4.

As shown in Fig. 4.4(a-1), by increasing L_{cb} , the increase rate of the fault current and consequently the maximum current is reduced. Due to the increase of L_{cb} , on one hand, the voltage generated by the reactor to limit the current increases. On the other hand, the larger L_{cb} causes a larger reflection coefficient, resulting in a lower voltage at the terminal. Consequently, as shown in Fig. 4.4(a-2), with the increase of L_{cb} , the maximum voltage first increases and then decreases. The operation time increases due to the reduced decrease rate of current with a larger L_{cb} after the main breaker opens, as demonstrated in Fig. 4.4(a-3). The energy absorption, shown in Fig. 4.4(a-4), increases with the increase of L_{cb} when L_{cb} is lower than 100 mH. As the red curve shown in Figs. 4.4(a-3) and 4.4(a-4), the fault is hard to clear when the reactor is too large with a much lower U_r . It is shown in Fig. 4.4(b-1) that a longer t_{delay} provides a longer time for increase of current, which results in a larger I_{max} . When the delay time increases, the characteristic length l_0 increases and the attenuation of the surge voltage decreases the voltage drop after the fault. Thus, V_{max} shown

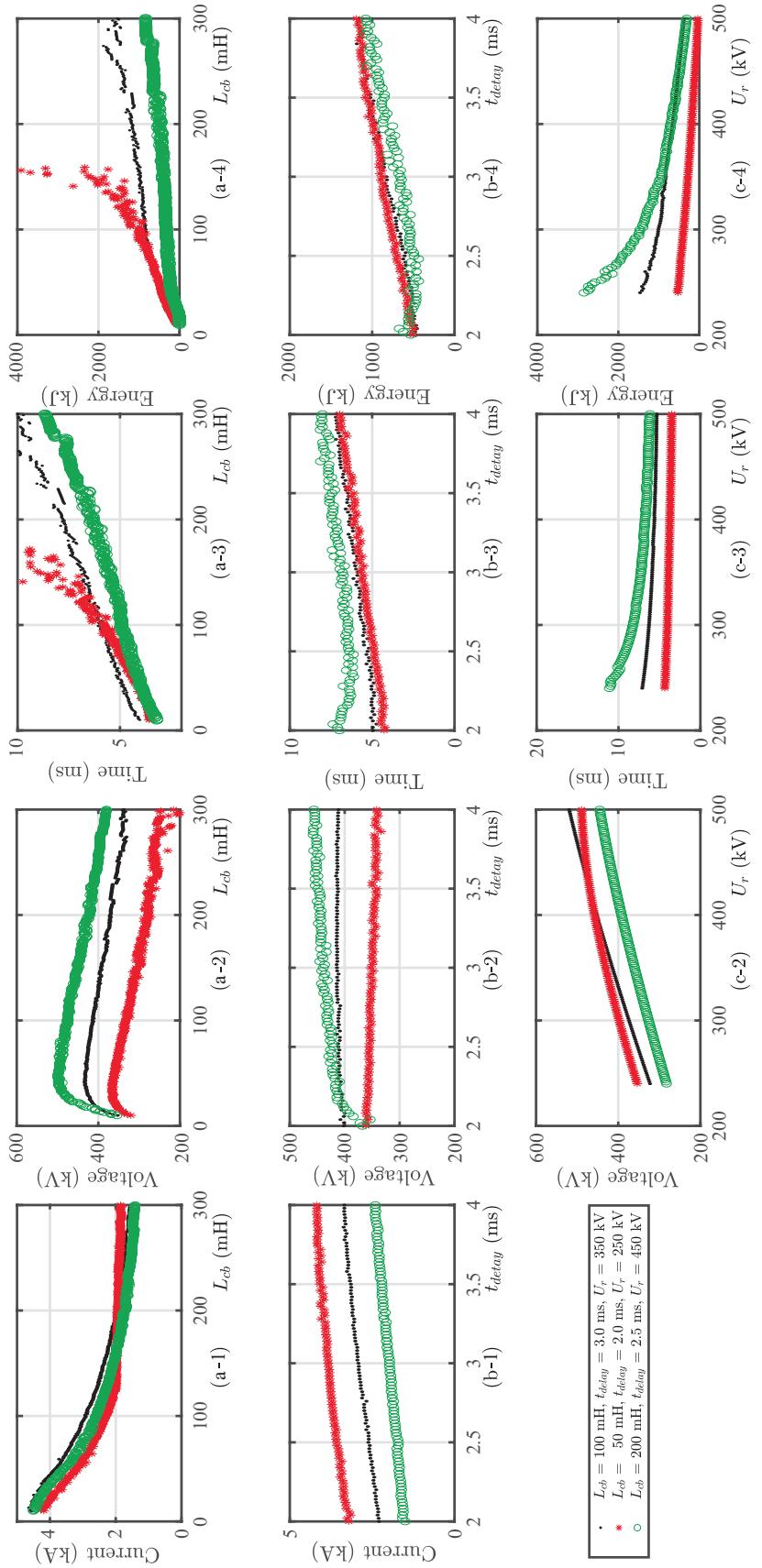


Figure 4.4: Calculated results for I_{max} , V_{max} , t_{clear} and W_{EAP} with one parameter being changed: (a-1)-(a-4) objectives vary with L_{cb} ; (b-1)-(b-4) objectives vary with t_{delay} ; and (c-1)-(c-3) objectives vary with U_r .

in Fig. 4.4(b-2) increases with the increase of t_{delay} . The increase is more pronounced when t_{delay} is lower because the surge voltage attenuates faster at a closer distance. The operation time in Fig. 4.4(b-3) shows that a longer t_{delay} results in a longer t_{clear} . Also, the energy absorption W_{EAP} increases with the increase of t_{delay} . Although increase of U_r does not have a significant impact on I_{max} , it directly increases V_{max} and reduces t_{clear} and W_{EAP} , as shown in Figs. 4.4(c-1), (c-2) and (c-3).

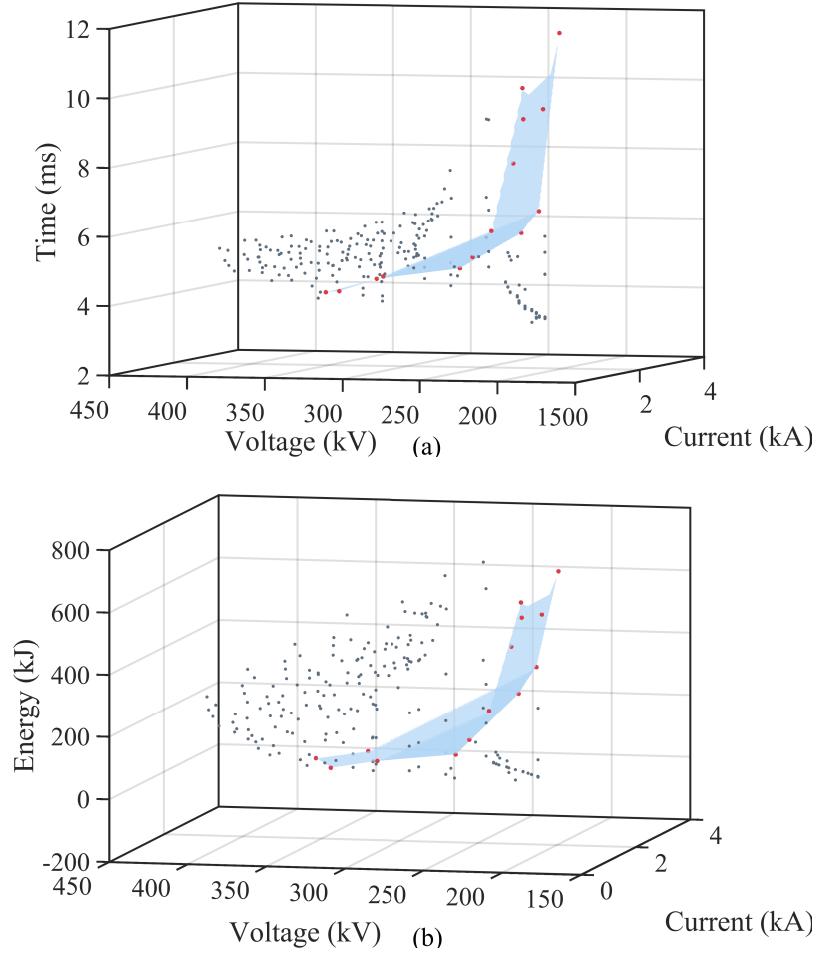


Figure 4.5: Pareto-optimal front of the feasible objective space.

All the aforementioned trade-offs are considered in the multi-objective optimization problem described in Chapter 4.4, where L_{cb} is varied within a range from 1 mH to 200 mH, t_{delay} is varied from 2.5 ms to 3.5 ms and U_r is varied from 240 kV to 450 kV.

With the variable ranges, the feasible objective space consists of the corresponding ob-

Table 4.2: Selected parameters for optimized objectives.

		Case 1	Scheme 1	Scheme 2	Scheme 3
Parameters	L_{cb} [mH]	100	180	135	150
	t_{delay} [ms]	3.0	2.5	2.6	2.5
	U_r [kV]	300	260	410	330
Objectives	I_{\max} [kA]	2.30	1.67	1.92	1.83
	V_{\max} [kV]	353	310	397	360
	t_{clear} [ms]	6.12	8.80	5.85	6.30
	W_{EAP} [kJ]	352	488	143	304

jectives is shown in Fig. 4.5. The trade-offs among the four objectives are revealed from the three dimensional graphs in Fig. 4.5. I_{\max} and V_{\max} are relatively independent of each other, while the increase of I_{\max} or V_{\max} will increase t_{clear} and W_{EAP} . By solving the multi-objective optimization problem, the best trade-off among the objectives is explored. This problem is solved with genetic algorithms and the solutions are shown by the red points in Fig. 4.5. The solutions composing a curved surface to the boundary of the objective space is the Pareto-optimal front, on which the points have optimized objectives. The corresponding variables provide optimal combinations of parameters for DC breakers. From the solutions, the DC circuit breaker can be designed in coordination with other factors in a real system. Three sets of parameters are chosen from the solutions and listed in Table 4.2 to show the improved transients. The transient performance of the system with the optimized parameters is tested by simulations. I_{\max} , V_{\max} , t_{clear} and W_{EAP} with the selected parameters are compared with the worst case at *Bus*₄ with the same parameters as Case 1. Compared to the case before optimization, as shown in Table 4.2, the objectives with optimal parameters are reduced to a certain extent. In Scheme 1, I_{\max} and V_{\max} are much lower while in Scheme 2, I_{\max} , t_{clear} and W_{EAP} are reduced. Moreover, Scheme 3 reduces I_{\max} and W_{EAP} while avoiding the increase of V_{\max} and t_{clear} . Although the four objectives are not minimized simultaneously due to the trade-off, it would be ideal if they are limited within their specified ranges.

4.5.2 Evaluation of Sequential Tripping Strategy

In this section, the proposed sequentially tripping strategy is verified using the test system shown in Fig. 3.8. The arrester is modeled using the V-I characteristic shown in Fig. 4.2(d). The transient performance of the proposed sequentially switched hybrid circuit breaker is compared with the conventional one. Based on the calculation results of the optimization problem, the parameters of the proposed tripping strategies are optimally sized through the two approaches described in Section 4.4. The results of optimization are also evaluated by simulations in this section.

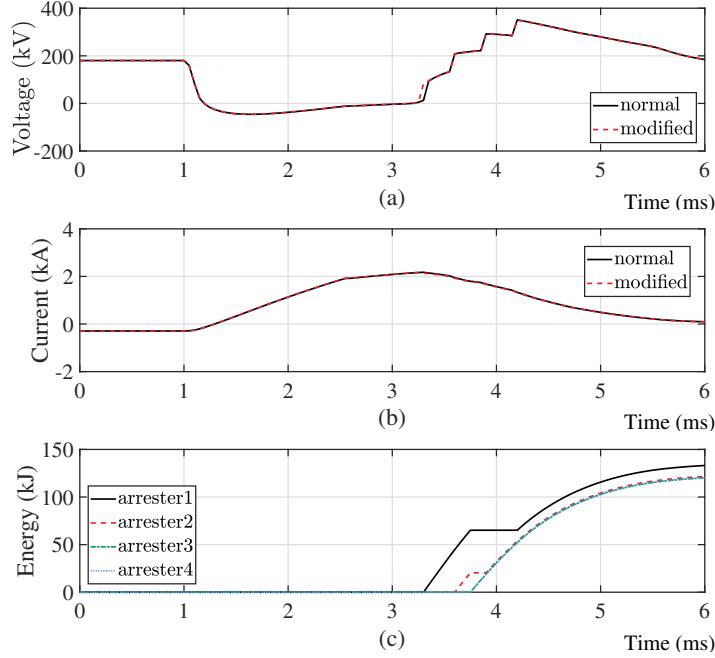


Figure 4.6: Transients of the modified sequentially tripped hybrid circuit breaker: a) bus-side voltage, b) fault current and c) absorbed energy.

Base Case: The base case is tested on $Line_{45N}$ where the positive and negative poles are shorted at 200 km away from Bus 4. The operation of hybrid DC circuit breaker are tested by both simultaneous and sequential tripping strategies. The waveforms of the currents and voltages, as well as the energy absorptions are compared in Figs. 3.10(a)-(d). This pole-to-pole fault occurs at $t = 0$ and reaches the terminal at $t = 1.1$ ms. When the fault is detected

at $t = 2.2$ ms, the LCS opens to force the current to the CCP of the circuit breaker. In the simultaneous case, 2 ms is left for full opening of the UFD to withstand transient recovery voltage of 1.5 p.u. For the four-stage sequential tripping circuit breaker, the trip signal for the first stage is generated at $t = 3.3$ ms, i.e., 0.9 ms earlier than the simultaneous tripping circuit breaker, while the delay time for each stage is 0.3 ms.

Compared to the abrupt increase of voltage in the simultaneous tripping case, the bus-side voltage of four-stage circuit breaker increases incrementally and is clamped by the arrester at each stage, as shown in Fig. 3.10(a). The modules can be tripped earlier since the voltage across the UFD is applied step by step. This voltage helps reduce the voltage across the DC reactor and, consequently, reduce the rate of rise of fault current in the main circuit.

As shown in Fig. 3.10(b), the maximum current and the clearance time is reduced by sequentially switched hybrid circuit breaker as well. The maximum overvoltage of the system is also lower with the sequential tripped hybrid circuit breaker. However, compared to the balanced energy distribution of the arresters in simultaneous case in Fig. 3.10(c), the energy absorbed by the arresters in the sequential tripped modules is distributed unevenly. As shown in Fig. 3.10(d), the arresters within the earlier switched modules are inserted earlier in the circuit. These arresters tend to absorb more energy. Therefore, the proposed sequential tripping strategy should be updated to balance the energy distribution among modules.

Modified Sequential Case: To equally distribute the energy among the arresters in Fig. 3.10(d), a modified sequential tripping strategy is proposed. The tripping signals of the four-stage circuit breaker is rearranged as in Table 4.1, where the four arresters are inserted in the circuit for an equal duration.

The simulation results in the modified strategy are compared with the normal case in Fig. 4.6. The waveforms of currents and voltages in the modified case are close to the base

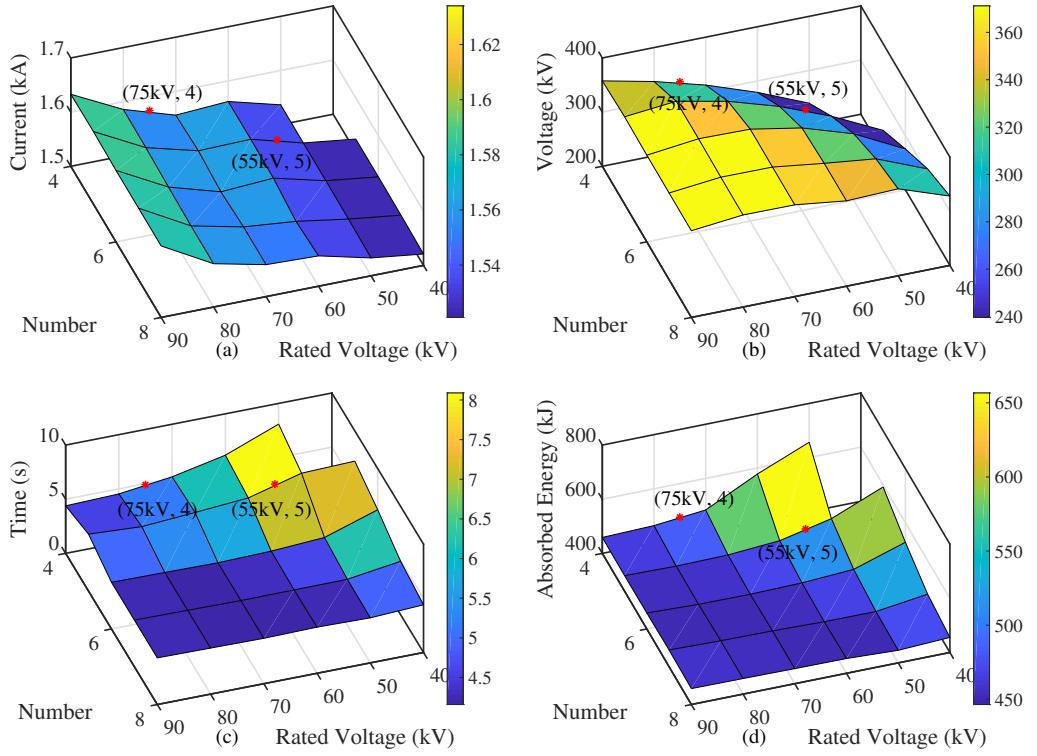


Figure 4.7: Fault transient performance variation versus u_r and N : a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy.

case, which means that the modified sequential tripping reserves the benefits of the original strategy. The energy absorption in Fig. 4.6(c) shows that the modified strategy balances the energy distribution of the arresters within the sequentially tripped modules. This is further proved by the data in Table 4.3. However, since the fault current during each stage is not exactly the same, the first arrester absorbs more energy than the others.

Table 4.3: Absorbed energy by arresters

$W_{EAP,i}$ [kJ]	1	2	3	4
Normal strategy	117.7	88.9	60.6	36.7
Modified strategy	80.4	75.5	74.9	74.9

Optimized Sequential Strategy (Case 1): In the first optimization approach, the rated voltage, u_r of each module are set to be the same. It is assumed that the voltage withstand capability of the UFD is built up linearly to be 1.5 p.u. of the rated DC voltage at $t = 2$ ms.

With the help of time-domain calculation, the four metrics of the fault performance, i.e., maximum overcurrent, maximum overvoltage, fault clearance time and absorbed energy with different combination of u_r and N are shown in Fig. 4.7.

With the increase of u_r , the minimum allowed time delay increases, resulting in higher maximum overcurrent, higher maximum overvoltage but shorter clearance time. With the same u_r , the fault current goes down to zero much faster and the maximum overvoltage becomes higher as N increases. However, the maximum overcurrent does not change much since the slope of fault current is changed in the same way. Similar to the trend of clearance time, the absorbed energy decreases while u_r and N increase. When N is too large, the fault is cleared before the last several modules are inserted. As a result, the absorbed energy remains unchanged when u_r and N are large enough.

The results in Fig. 4.7 can be used in the design process to determine the parameters to optimize any of the system metrics. u_r and N can be optimally selected based on the requirements of the system. Hereafter, two sets of parameters are selected to be compared by simulation studies: (i) $u_r = 75$ kV, $N= 4$, and (ii) $u_r = 55$ kV, $N= 5$. The transient performance of these two scenarios are compared in Fig. 4.8. The lower u_r in scenario (ii) allows the module to open earlier to limit the fault current, resulting in a lower maximum overcurrent as shown in Fig. 4.8(a). The total inserted voltage and maximum voltage in scenario (i) are larger than scenario (ii) and, consequently, the clearance time is reduced. The total energy absorbed by the arresters in scenario (i) is 493 kJ, which is lower than 508 kJ of scenario (ii), as verified by Fig. 4.7(d).

As discussed in Section 4.4, the energy is not strictly balanced with the modified sequential tripping strategy. This can be observed from Fig. 4.7(d). Based on the values obtained from scenario (ii), the tripping instants are further improved to balance the energy. The updated energy distribution is plotted in Fig. 4.7(e).

Optimized Sequential Strategy (Case 2): In the second optimization approach, a three-

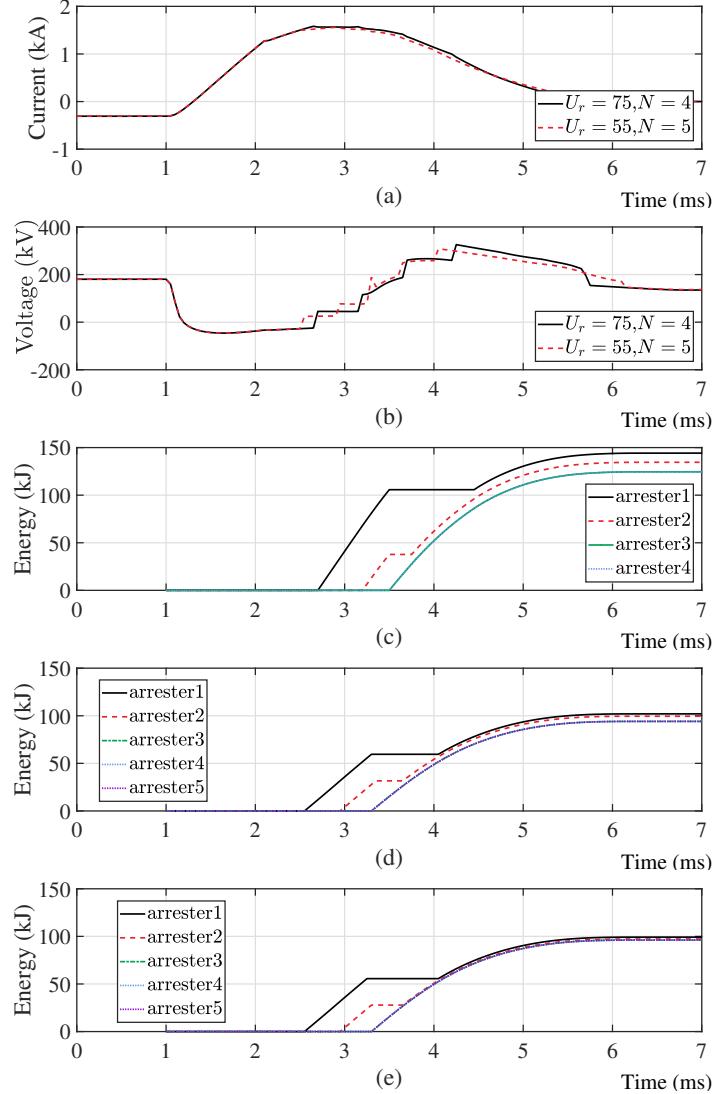


Figure 4.8: Simulation results of the selected scenarios: a) fault current, b) bus-side voltage, c) absorbed energy in scenario (i), d) absorbed energy in scenario (ii), and e) absorbed energy with updated time instants.

stage tripping strategy is applied while the total inserted voltage $u_{r,sys}$ is set to be 300 kV. The transient performance of the system is calculated with different combinations of u_{r1} , u_{r2} and u_{r3} . The calculation results of the four metrics are plotted in Fig. 4.9. As shown in Fig. 4.9(a), the rated voltage of first arrester determines the maximum overcurrent during the operation of the DC circuit breaker. With lower u_{r1} , the Module 1 can be triggered earlier to limit the increase of the fault current and reduce the maximum overcurrent. The maximum voltage decreases as u_{r1} increases. When u_{r1} remains the same, the clearance

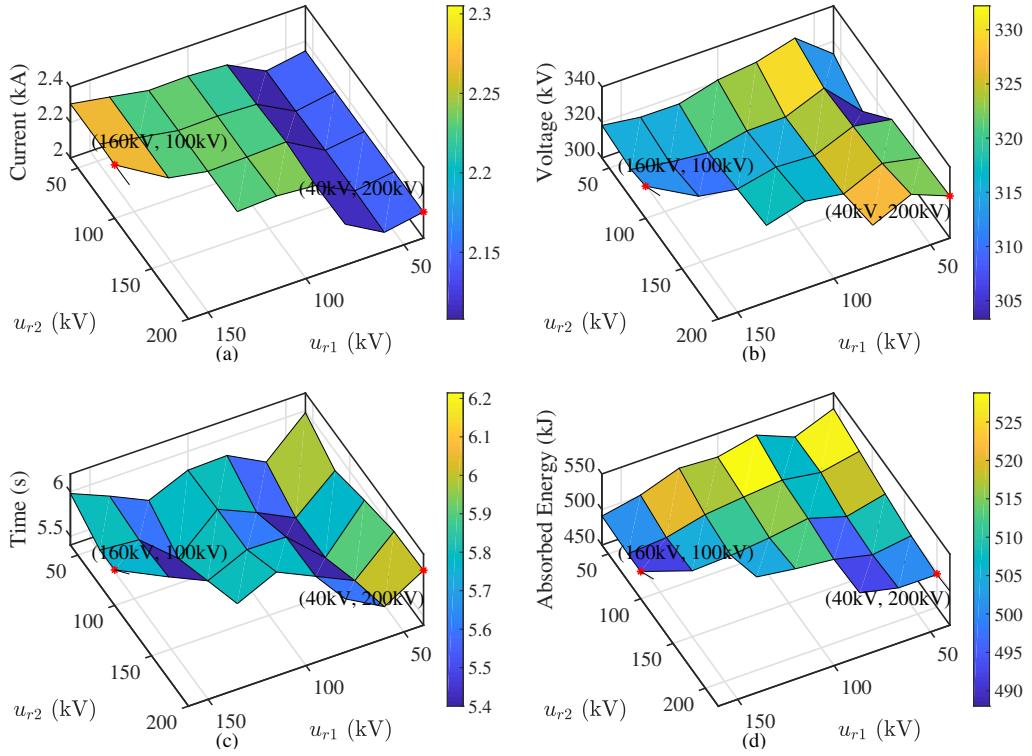


Figure 4.9: Fault transient performance variation versus u_{r1} and u_{r2} : a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy.

time decreases and then increases while u_{r2} increases. The total energy absorbed by the arresters is also presented in Fig. 4.9(d), which tends to decrease with the increase of u_{r1} and u_{r2} .

This approach helps determine the parameters for those systems that are flexible in using different rated arresters. To demonstrate the design process, two scenarios are selected as following: (i) $u_{r1} = 40 \text{ kV}$, $u_{r2} = 200 \text{ kV}$, $u_{r3} = 60 \text{ kV}$; and (ii) $u_{r1} = 160 \text{ kV}$, $u_{r1} = 100 \text{ kV}$, $u_{r1} = 40 \text{ kV}$. The simulation results of the two scenarios are provided in Fig. 4.10. The system metrics are compared in these two scenarios. It is verified that the results presented in Fig. 4.9 provide a solid guidance for the design process. In the second optimization approach, the ratings of the arrestors are considered to be non-identical. As a result, the voltages inserted into the circuit are not the same anymore. In this case, the energy distribution should no longer be balanced based on the same modified sequential strategy shown in Table I. The arresters, which are rated at higher voltages and are tripped

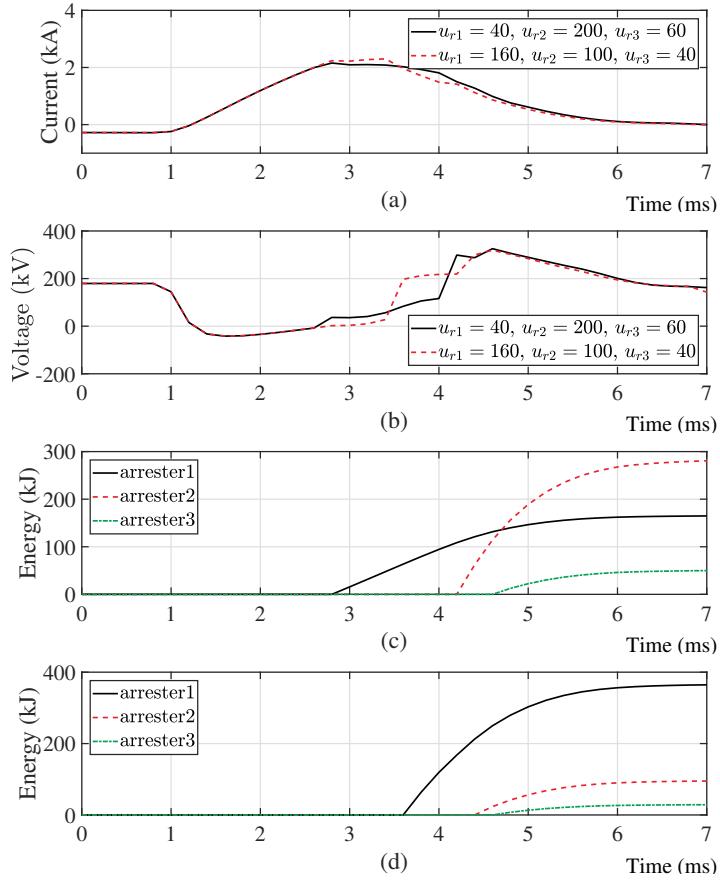


Figure 4.10: Simulation results of the selected scenarios: a) fault current, b) bus-side voltage c) absorbed energy in scenario (i), and d) absorbed energy in scenario (ii).

earlier, tend to absorb more energy as shown in Figs. 4.10(c) and (d).

CHAPTER 5

PROTECTION RELAYING ALGORITHMS FOR MTDC GRIDS

5.1 MTDC Protection Relaying Algorithms

Protection based on DC circuit breakers necessitate fast, accurate, and selective relaying algorithms to detect a fault in the DC grids [14, 15]. In the MTDC grids, compared to their AC counterpart, DC fault detection is far more challenging because of the rapid rise of fault current and low impedance nature of the DC cables/lines [1, 9, 14]. The protection philosophy of the MTDC grids, nevertheless, is similar to the AC protection in the sense that both primary and backup protection schemes are required [1, 23]. The primary protection, which is designed to work under normal operations, should respond to any types of faults in a fast and reliable manner. In case the primary protection fails to act properly, backup protection should trip as quickly as possible to minimize the loss of power in-feed [21].

In this chapter, a protection unit consisting of both primary and backup protection relaying algorithms is proposed. These replying algorithms provide complete functionalities to support fast and reliable protection of MTDC grids.

5.2 Layout of the Protection Unit

The layout of the proposed protection unit is shown in Fig. 5.1. For the sake of simplicity, the positive and negative lines are represented in one line view. As shown in Fig. 5.1, Bus i is connected with Converter i through the breaker unit CB_i and with other N buses through breaker units $CB_{i1}, CB_{i2}, \dots, CB_{iN}$. These breaker units consist of series connected DC circuit breakers and sensors that are placed on each circuit breaker and at the end of each HVDC link. The breakers are tripped by signals $T_i, T_{i1}, T_{i2}, \dots, T_{iN}$, which are generated by their corresponding relaying algorithms in the primary and backup protection

modules. The measurements m_1, m_2, \dots, m_N consist of voltages across circuit breakers $v^{cbi1}, v^{cbi2}, \dots, v^{cbiN}$, line currents i^{lij} , and terminal voltages v^{lij} of those HVDC links that have one of their ends on the local Bus i , where i, j are the two terminals of link ij . These measurements are captured with a sampling frequency f_s and are then directly sent to the data processing unit. They serve as the input to both the primary and backup protection algorithms.

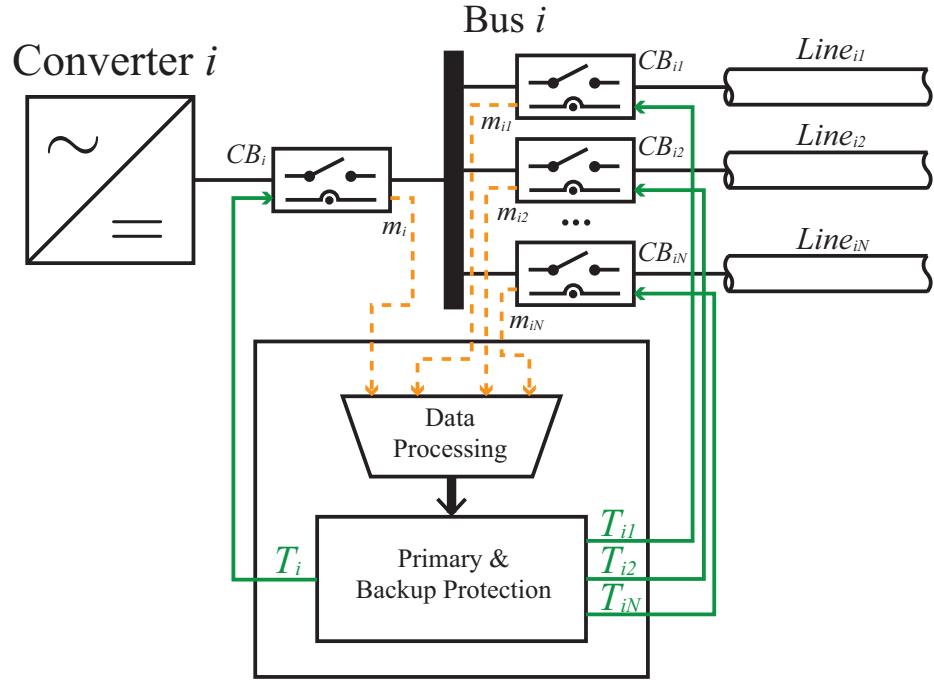


Figure 5.1: The layout of the protection unit at Bus i .

5.3 Primary Protection for MTDC Grids

In this section, the proposed hybrid primary fault detection algorithm is presented. The hybrid approach is built based upon the protection units installed at the MTDC terminals. These protection units aggregate the measurements collected from current and voltage sensors mounted on the points of interest. These measurements are processed by primary and backup fault detection algorithms to trip corresponding DC circuit breakers when necessary.

5.3.1 Architecture of the Hybrid Primary Fault Detection Algorithm

The proposed hybrid primary fault detection algorithm employs a two-level architecture to extract information from the signal measurements. The detailed architecture is presented in Fig. 5.2.

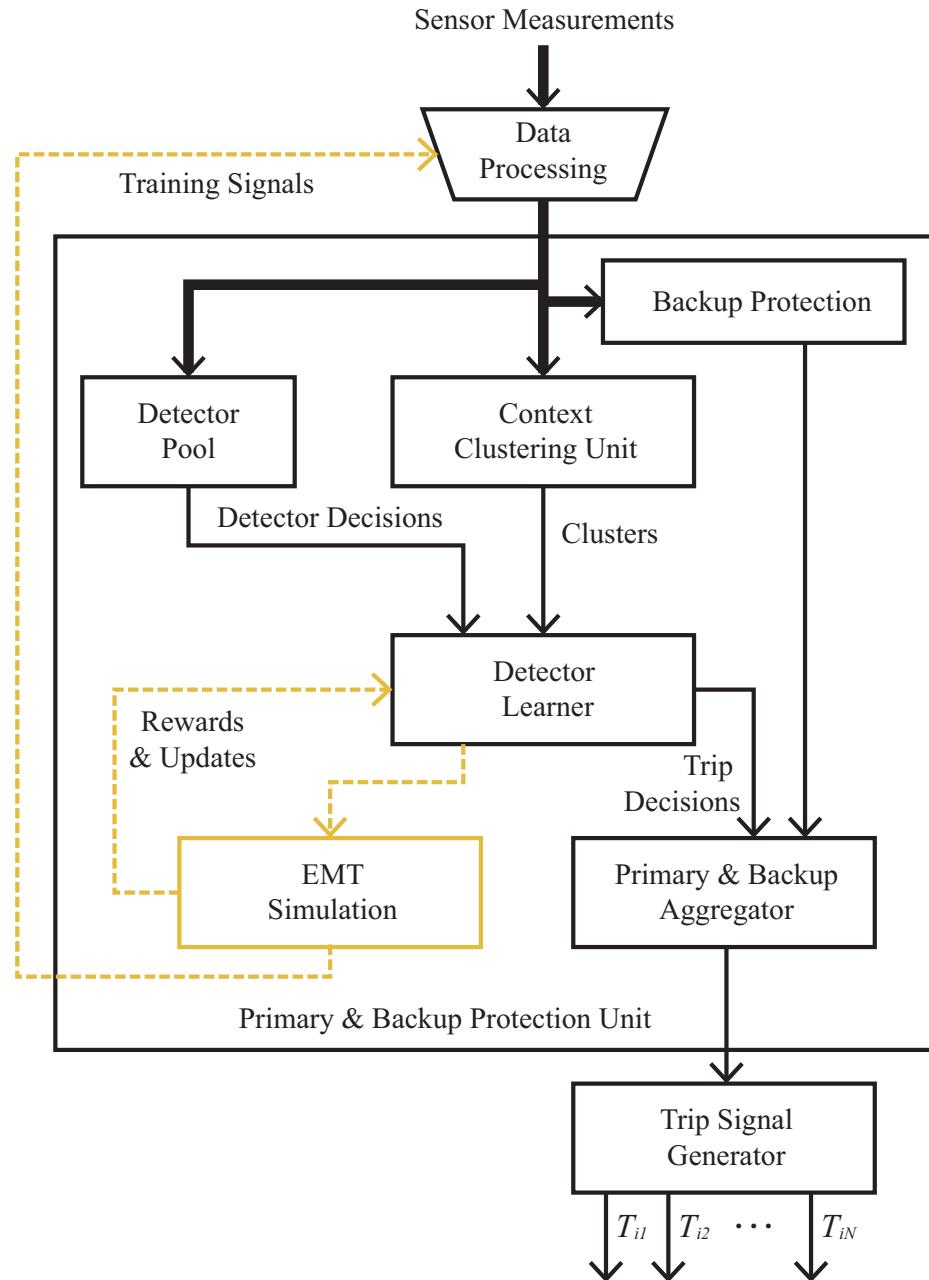


Figure 5.2: Architecture of the proposed hybrid primary protection unit.

The input measurements are first analysed by higher level processing elements, and associated to clusters capturing various modes of operation. Simultaneously, a pool of fault detectors is implemented. The detector pool consists of multiple candidate detectors that make decisions according to different subsets of measurements. Some of the detectors are deployed based on existing primary detection algorithms from literature [53–60].

The decisions made by the detector pool and clusters categorized by the context clustering unit serve as the input to the lower-level decision maker, which is a detector learner making the final decision. The trip decisions made by the detector learner are aggregated with the decisions made by the backup protection. The trip signal generator will finally assemble the trip commands to the corresponding destination DC circuit breakers.

The training of the detector learner is also illustrated by the dashed lines and yellow blocks in Fig. 5.2. While training the detector learner, it learns from previous samples generated by the electromagnetic transients (EMT) simulation. The simulation provides the feedback and rewards to the detector learner to help update its internal parameters. These parameters are used to generate the final decision based on the decisions made by individual detectors from the pool.

5.3.2 Context Clustering Unit

At the highest level of the primary protection hierarchy, the input measurements are first clustered by the context clustering unit. The idea of clustering takes root from the fact that different detectors deliver different performance under various operation conditions, which are separable given the sensor measurements. These separated operation conditions are considered as "context" for the detectors. Given a certain context cluster being identified, detectors in the pool are assigned different weights, which indicates their fatalities. This preprocessing of context clustering helps the system grasp a better understanding of the signals by providing the context information about which categories they belong to.

The k -means clustering [87] is applied for context clustering. The k -means clustering

strives to partition the given d -dimensional ($d = 6$ in this work) observations into k clusters with a minimized within-cluster variance. The details of this standard method can be found in [87] and are not repeated here.

As shown in Fig. 5.1, there are N HVDC links connected with the i -th MTDC terminal. For each connected HVDC link j , the line currents i^{lij} , line voltages beyond current limiting reactors v^{lij} , and voltages across the DC circuit breakers v^{cbij} from both positive and negative poles are collected. The six measurements form six dimensional feature vectors. The dataset is generated from simulations of P2P, low impedance P2G, and high impedance P2G faults located at 10 km intervals from each HVDC link. The fault impedances are also varied from 1Ω to 500Ω .

On the higher level of primary protection hierarchy, the patterns of the input measurements are first clustered and recognized by the context clustering unit. This preprocessing helps the system grasp a better understanding of the signals by providing the context information about which categories of patterns they belong to. The Gaussian Mixture Models (GMM) is applied in this work for the context clustering.

The output of the context clustering unit is a cluster label $c \in C$, where C is a finite set for context cluster labels. This label indicates which cluster the given input measurements follows. This clustering unit also greatly improves the performance of the overall primary detection with the ability to separate external faults from internal DC faults. This cluster label is sent as the input to the lower-level hierarchy of the system.

On each MTDC terminal, the context clustering unit trains independent cluster for each line/cable. The size of datasets used for training various given the length of the target line/cable. For example, 271 samples are used for training the cluster for Line13 on terminal 1. These samples consist of 35 P2P, 70 low impedance P2G, 70 high impedance P2G, and 96 normal operation cases.

It is also important to determine the the hyper-parameter k in the k means algorithm. Given how the datasets are generated, 2, 3 and 4 are potential candidates for the k . These

three candidates are evaluated though calculating their silhouette values [87], which are 0.749, 0.918, and 0.872, respectively. A higher silhouette value indicates a better matching of samples to their own cluster rather than the neighboring clusters. Therefore, $k = 3$ is determined in this study.

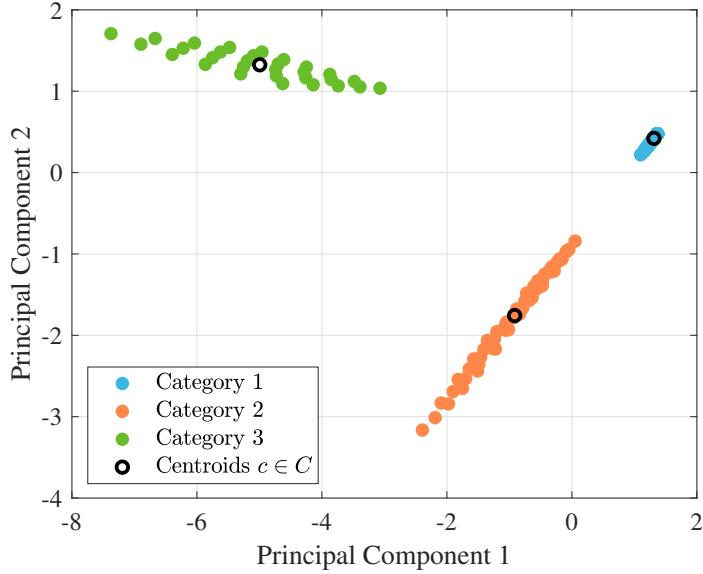


Figure 5.3: Context clustering using observations from terminal 1 and Line13.

The clustering results are presented in Fig. 5.3. The training simulations samples are generated on different locations on Line13 using various settings, as described above. The six-dimensional training observations are collected at terminal 1 and used for the k -means clustering, where $k = 3$. To better visualize the results, principal component analysis (PCA) [87] is performed on the six-dimensional data. The top two principal components are plotted in Fig. 5.3. Three categories, labelled 1 to 3, are separated apart. These categories provide a idea of the fault context of faults on Line13 observed from terminal 1. Category 1, located on top right corner of the graph, represents the observations from high impedance P2G faults and normal cases. They are not partitioned apart because the signals measured under high impedance P2G faults do not clearly deviate from normal operation, especially when there is noise in some of measurements. The clustering is not intended to

precisely detect or classify faults, it is used to provide high-level ideas of how the signals look like. These clusters help the detector from detector pool in following hierarchies to make better decisions.

5.3.3 Detector Pool

The same sensor measurements are sent to a pool of N detectors in parallel. Each detector within the detector pool takes a subset of the measurements as its input and makes decisions.

As summarized in the literature review, none of the existing fault detectors is perfect. Different detectors work best under different cases. Multiple existing detectors are implemented in the detector pool, including the threshold-based detectors [54, 55], ROCOV-based detectors [53, 59], and detectors based on Quickest Change Detection (QCD) [23]. These detectors make independent decisions $d_n, n \in N$, which are then fed to the detector learner.

5.3.4 Detector Learner

The detector learner works as the lower-level hierarchy of the primary detection system, and is inspired by ideas from the ensemble learning [87]. The detector pool is designed to make decisions using the inputs from multiple less powerful detectors from the detector pool. The final decision made by the ensemble method performs better than what could be obtained by any single detector alone.

For each the cluster label c obtained from the context clustering unit, one detector learner is trained. Given the independent decisions $d_{n,c}$ made by each detector n under each cluster label c , the final decision is made by taking weighted majority over these inputs.

Assuming a weight $w_{n,c}, n \in N, c \in C$ is assigned to each detector, for each cluster label, the weights from all detectors in the detector pool sum to 1, i.e., $\sum_{n=1}^N w_{n,c} = 1, c \in$

C . Each detector makes a binary decision to address a fault. An accumulated metric h_c is calculated as

$$h_c = \sum_{n=1}^N w_{n,c} \times d_{n,c}, c \in C. \quad (5.1)$$

The final decision d_c made by the detector learner is 1 if h_c is higher than 0.5 and 0 otherwise. The weights are assigned differently to each detector for different clusters. Detectors that make better decision and provide more robust performance are assigned higher weights. This adjustment is achieved through a single-round training, as shown in Algorithm 1.

Algorithm 1: Weighted majority update algorithm

```

Input: Training samples  $x_i$ 
Initialize  $w_{n,c} = 1/N$ 
for each cluster label  $c = 1, \dots, C$  do
    Filter out the  $m_c$  training samples matching label  $c$ 
    Initialize counter  $\text{cnt}_n = 0$  for detector  $n$ 
    for each detector  $n = 1, \dots, N$  do
        Test each training sample and accumulate decision  $d_n$  to the counter  $\text{cnt}_n$ 
    end
    Calculate correct rate  $r_{n,c} = \frac{\text{cnt}_n}{m_c}$  for each detector
    Update the weights as  $w_{n,c} = \frac{r_{n,c}}{\sum_{n=1}^N r_{n,c}}$ 
end

```

Initially, all weights are assigned to be $w_{n,c} = 1/N$. The training samples x_i have been assigned cluster labels c by the context cluster. For each cluster label, the samples with same label are filtered out. The number of samples for each cluster label is noted as m_c . The detectors are then tested on these samples by accumulating their binary decisions to the counters. Finally, new weights $w_{n,c}$ for detectors are computed and normalized proportional to their correct rate.

5.4 Backup Protection for MTDC Grids

5.4.1 The Proposed QCD Algorithm

In case of a DC fault inception, the voltages at bus terminals and across circuit breakers are subject to abrupt changes. These changes occur much faster than the sampling period of the corresponding measurements. The philosophy behind the proposed backup protection algorithm is to determine the operation status of the breakers (breaker failure backup) and primary relay (relay backup) by monitoring any abrupt change in the breaker voltage and the terminal voltage, respectively. A straightforward way to detect such changes would be to compare the target signal with a threshold. However, such an approach would be vulnerable to noise, spikes, or other unexpected errors in the measurements. This problem calls for a detection method with higher robustness. The QCD algorithm [88] is the proposed candidate to this end.

In the context of backup protection, without loss of generality, one can assume that the measurement sequence m_1, m_2, \dots, m_k is captured by the sensors and sent to the data processing unit. The sequence is an independent Gaussian sequence with a probability density $p_\theta(m)$. The parameter θ denotes the mean of this sequence. Before the unknown change time j , the mean of measurement sequence is θ_0 , while after the change time, it becomes $\theta_1 \neq \theta_0$. The goal of the algorithm is to detect this change as fast as possible.

There are two hypotheses to be considered, i.e., \mathbf{H}_0 and \mathbf{H}_1 . \mathbf{H}_0 denotes the hypothesis where there are no changes, while \mathbf{H}_1 means there is a change in the sequence.

$$\mathbf{H}_0 : \theta = \theta_0 \text{ for } 1 \leq i \leq k$$

$$\begin{aligned} \mathbf{H}_1 : & \text{there exists an unknown } 1 \leq j \leq k \text{ such that} \\ & : \theta = \theta_0 \text{ for } 1 \leq i \leq j - 1 \\ & : \theta = \theta_1 \text{ for } j \leq i \leq k \end{aligned} \tag{5.2}$$

The likelihood ratio between hypotheses \mathbf{H}_0 and \mathbf{H}_1 is

$$\Lambda_1^k(j) = \frac{\prod_{i=1}^{j-1} p_{\theta_0}(m_i) \cdot \prod_{i=j}^k p_{\theta_1}(m_i)}{\prod_{i=1}^k p_{\theta_0}(m_i)} \quad (5.3)$$

Equation (5.3) expresses the likelihood of measurements to be under \mathbf{H}_1 than \mathbf{H}_0 . The log-likelihood ratio S_j^k is obtained by taking the log of equation (5.3) as

$$S_j^k = \sum_{i=j}^k \ln \frac{p_{\theta_1}(m_i)}{p_{\theta_0}(m_i)} \quad (5.4)$$

To detect any unknown change, the maximum likelihood principle is applied on the log-likelihood ratio S_j^k . The decision is made based on the decision function expressed by

$$g_k^m = \max_{1 \leq j \leq k} S_j^k \quad (5.5)$$

With the aid of (5.5), the alarm time t_a is obtained based on the following rule:

$$t_a = \min\{k : g_k^m \geq h\} = \min\{k : \max_{1 \leq j \leq k} S_j^k \geq h\} \quad (5.6)$$

where h is a positive threshold chosen based on the system parameters. t_a is the earliest moment when the decision is in favor of \mathbf{H}_1 over \mathbf{H}_0 , i.e., $g_k^m \geq h$.

The calculation of g_k^m could be computationally expensive in digital implementation. Therefore, a new variable g_k , which is a non-negative version of g_k^m , is defined as

$$g_k = \max\{0, g_k^m\} = \max\{0, \max_{1 \leq j \leq k} S_j^k\} \quad (5.7)$$

g_k^m and g_k are equivalent in the sense that they result in the same alarm time t_a . The proof of this statement is presented in Appendix A.

Based on Appendix B, g_k can be rewritten into the recursive form as

$$g_k = \begin{cases} g_{k-1} + \ln \frac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)} & \text{if } g_{k-1} + \ln \frac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)} > 0 \\ 0 & \text{if } g_{k-1} + \ln \frac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)} \leq 0 \end{cases} \quad (5.8)$$

In the settings of the backup protection problem, it is assumed that the distribution of the observation m_i is Gaussian, which is a widely-applied assumption in the literature [89]. Under this assumption, the probability density function with the mean value θ and variance σ^2 is given as

$$p_\theta(m_i) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(m_i-\theta)^2}{2\sigma^2}} \quad (5.9)$$

In this case, the recursive update rule in (5.8) can be rewritten as

$$\begin{aligned} g_k &= \max\left\{0, g_{k-1} + m_k - \frac{\theta_1 + \theta_0}{2}\right\} \\ &= \max\left\{0, g_{k-1} + m_k - \left(\theta_0 + \frac{\nu}{2}\right)\right\} \end{aligned} \quad (5.10)$$

where $\nu = \theta_1 - \theta_0$ is the minimum possible magnitude of the abrupt change to be detected. Although the Equation (5.10) is derived under Gaussian assumption, the proposed algorithm can be generalized to other distributions as well by plugging their probability density functions into Equation (5.8).

Equation (5.10) corresponds to the well-known cumulative sum (CUSUM) method. The detailed QCD algorithm is shown in Algorithm 2.

Algorithm 2 is executed in real-time with the sampling frequency f_s . m_k denotes the measurement sample taken at each step $k \geq 0$. If there is no signal, k is set to be zero and the algorithm is initialized. g is the data accumulated from the last time step and is updated from the bottom up based on the new inputs. When $m_k > (\theta_0 + \frac{\nu}{2})$, g starts increasing. Once it hits the threshold h , d is set to be *True* and a change is declared.

The proposed method performs the cumulative summation process, which is immune to

Algorithm 2: Backup QCD Algorithm

Input: m_k : measurement sample at step k
 g : accumulated sum from last step

Output: Decision d

```
if  $k = 0$  then                                /* initialization */
    Read  $h, \theta_0, \nu$ 
     $g \leftarrow 0, d \leftarrow False$ 
end
 $g_{next} \leftarrow g + m_k - (\theta_0 + \frac{\nu}{2})$ 
if  $g_{next} > h$  then                         /* change detected */
     $d \leftarrow True$ 
     $g \leftarrow g_{next}$ 
else if  $g_{next} > 0$  then                  /* update g */
     $g \leftarrow g_{next}$ 
else                                         /* reset g */
     $g \leftarrow 0$ 
end
return  $g, d$ 
```

noise and spikes. In terms of computational effort, within each iteration, at most, three sum, one comparison, and three copy operations are involved in the calculation. Additionally, g, θ_0, ν , and h are the only four variables required to be stored in the memory for the use within each iteration. Based on these facts, the algorithm can be applied easily on most relaying platforms.

5.4.2 Backup Protection for Breaker Failure

In case of a successful fault detection in primary protection, the fault is sensed and a trip command is sent to the corresponding circuit breakers. *Breaker failure* addresses the scenario where a circuit breaker fails to trip after receiving the tripping signal.

Fig. 5.4 shows the simulated transients of the hybrid circuit breaker CB_{13p} under a P2P fault in the middle of Line13. After receiving the trip command from the primary relay at $t = 0.9$ ms, the fault current starts to be transferred from the auxiliary branch to the main breaker. Once the current commutation is finished, the fast mechanical disconnector opens. Then, starting from $t = 3.8$ ms, the current starts decreasing by transferring the fault current to the arrester bank, which establishes a counter voltage across the reactor.

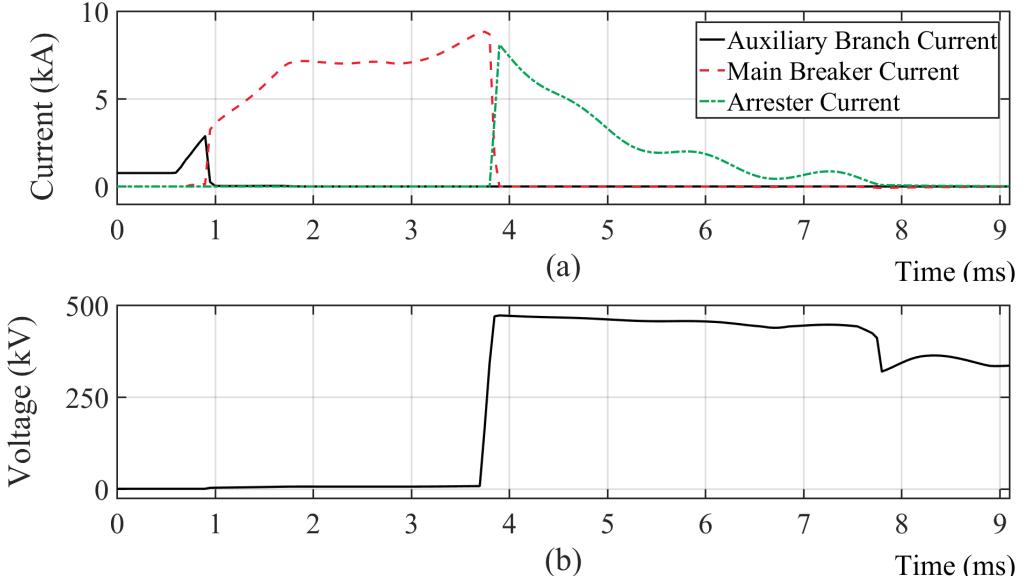


Figure 5.4: Simulated transients of the hybrid circuit breaker CB_{13p} under a P2P fault in the middle of Line13. a) auxiliary branch, main breaker and arrester currents; and b) voltage across the breaker.

The voltage across the breaker, as shown in Fig. 5.4(b), jumps to a high value, which is the summation of this counter voltage and the terminal voltage. The energy accumulated in the reactor and fault current path is then dissipated and the current flowing through the breaker reduces to zero at $t = 7.7$ ms. The breaker transients shown in Fig. 5.4 are representing only one of the possible breaker configurations.

In the DC circuit breaker design, to diminish the fault current, the voltage rating of the arrester bank must be larger than the DC voltage. After commutating the current to the arrester bank, the voltage across the breaker rises shapely from zero to a value which exceeds the nominal DC voltage. This counter voltage is a clear sign that the circuit breaker works properly and starts to interrupt the fault current as expected. Therefore, the problem of detecting breaker failure can be reduced to detecting an abrupt change in the sequence of the breaker voltage.

The proposed QCD method is applied here to detect the change in this case. Measurements $m_{k,k \geq 0}$ are voltage samples $v_k^{cb}, k \geq 0$ across the breaker. The overall scheme of the breaker failure backup protection is presented in Fig. 5.5. After receiving the trip signal

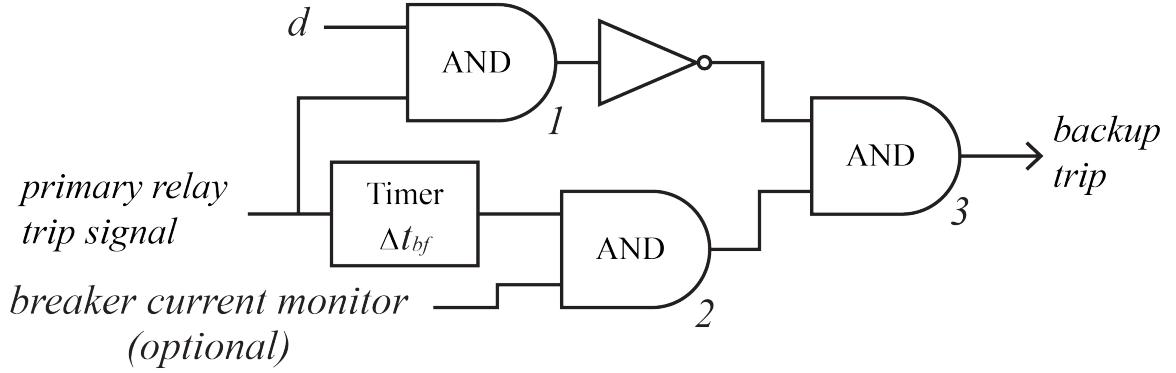


Figure 5.5: Breaker failure backup protection scheme.

from the primary relay at time instant t_d , AND gate 1 is activated and the QCD decision variable d is closely monitored. If an abrupt change is detected, a successful breaker operation is observed and d is set to be 1. In this case, AND gate 3 is deactivated and the backup protection will not trip. Meanwhile, at $t = t_d$, a timer is initialized with a delay of breaker normal clearing time Δt_{bf} (4 ms in this study). For additional security, the currents flowing through the breakers can be monitored as optional measurements. If the current is higher than twice the nominal current when the timer times out (exceeding Δt_{bf}), AND gate 2 will be satisfied. If d is 0 at this instant, it is concluded that the breaker has failed and the backup trip signals will be sent to the adjacent breakers located on the same bus. These breakers will take over and clear the fault.

5.4.3 Backup Protection for Relay Failure

Backup protection of breaker failure is based on the fact that the DC fault is detected correctly by the primary protection. However, due to failure of primary relying algorithm or communication system, there is a chance that the primary relay fails to detect the fault. In this case, it is crucial to equip the system with a backup protection scheme for relay failure as well.

Generally, during any P2P or low-impedance P2G faults in a MTDC grid, the fault current increases sharply and the system dynamics responses in three stages. The first stage

is a natural response of the DC link capacitors close to each terminal. During this stage the IGBTs are not blocked yet. In the second stage, the IGBTs are blocked and the fault current starts commutating to the converter freewheeling diodes. The third is the grid-side current feeding stage, in which the grid current contributes to the fault.

Effective design of primary and backup relaying algorithms ensures a detection of fault within 2 ms, which is in the first stage. Provoked by the fault, travelling waves propagate on the faulty link and reflect at either the fault location or a bus terminal. When the step-shaped wave arrives to the bus terminal, a rapid change in bus voltage is observed. This change is a critical alert for detection of a fault. Therefore, the backup protection of relay failure can be reduced to detection of an abrupt change in the probability distribution of the sequence of link voltages at each terminal. Similarly, the proposed QCD algorithm is implemented to identify this change. In this case, measurement samples $m_{k,k \geq 0}$ are $v_k^{lij}_{,k \geq 0}$. The relay failure backup algorithm works in cooperation with each primary relay. When a fault is detected by the QCD algorithm for relay failure, it will check if there exists a trip signal from the primary relay. If not, the backup algorithm will wait for Δt_{rf} (3 ms in this study) and trip the corresponding breaker after this delay.

5.4.4 Overall Protection Scheme

With the setup of backup protection scheme for both breaker and relay failures, the overall protection scheme is summarized here. Within each time step Δt , the status of the system is continuously monitored by both the primary and proposed QCD algorithm for relay backup. In case a fault is detected, the QCD algorithm for breaker failure is triggered. If the breaker is tripped successfully, no more action is required and the algorithm moves to the next step. If the fault is not cleared, an alert will be sent and the backup protection will take an action to trip other breakers on the same bus.

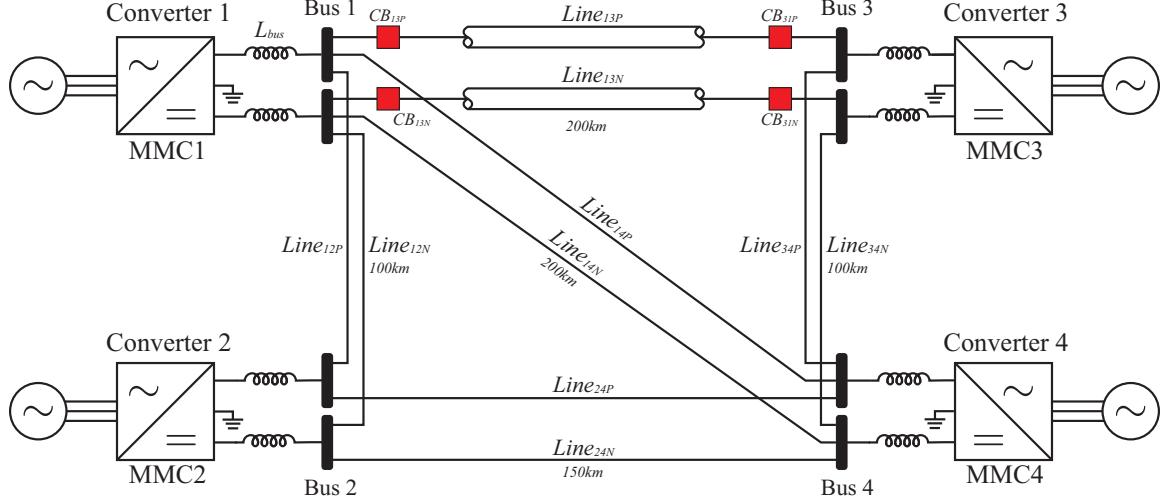


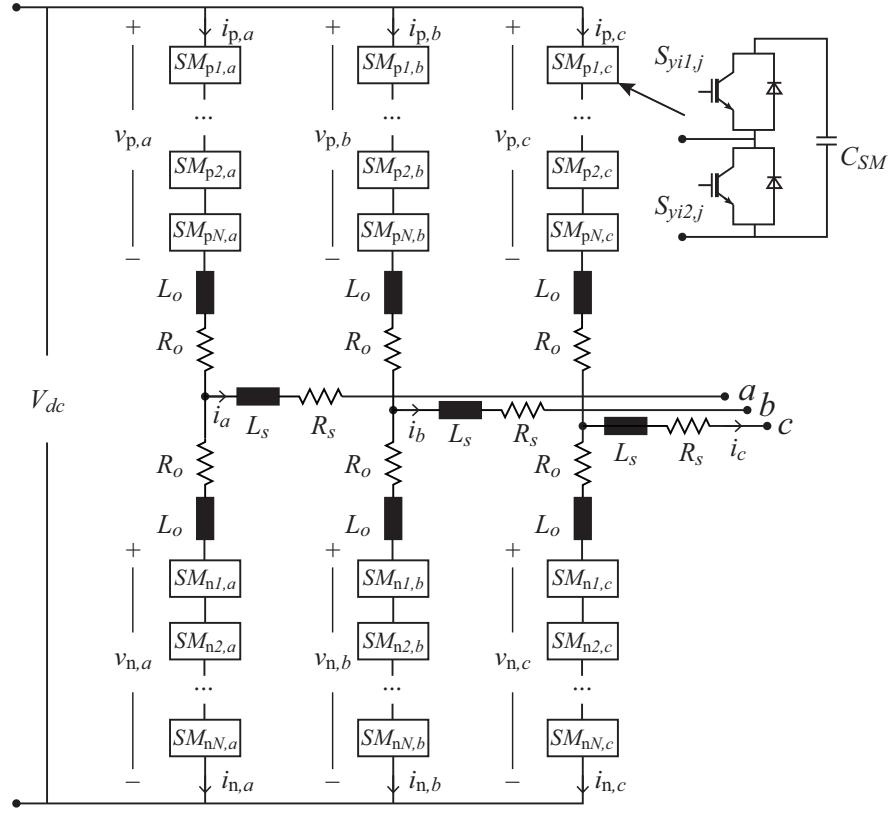
Figure 5.6: Layout of the four-terminal MTDC grid test system [90].

5.5 Simulation Results

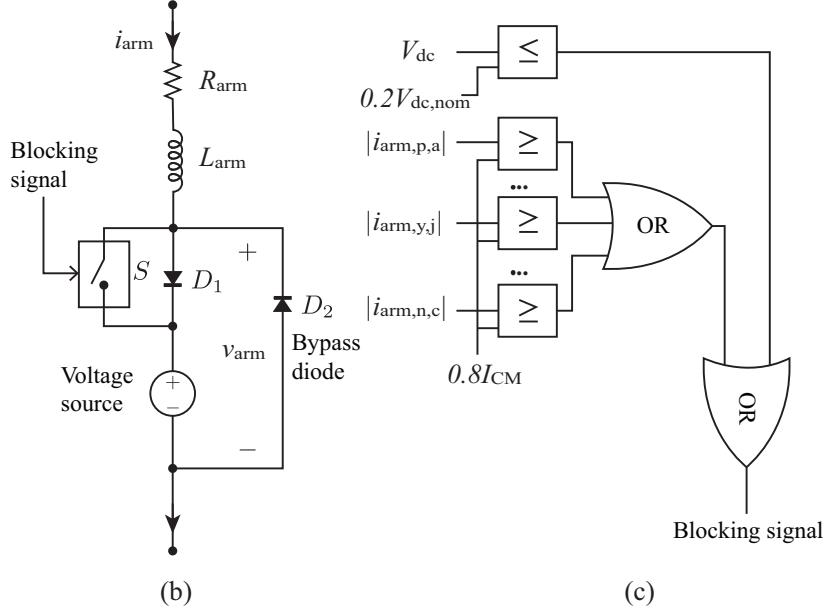
5.5.1 The Test MTDC Grid

Fig. 5.6 shows the layout of the test system adopted in this section [90]. The test system, which represents a ± 320 kV four-terminal meshed HVDC grid, is comprised of four VSC stations connecting two offshore wind farms to two onshore AC grids. The transmission lines include Line12 and Line34 with 100 km length, Line13 and Line14 with 200 km length, and Line24 with 150 km length. DC breakers are located at both ends of each HVDC link. The detailed configuration of Line13 is depicted in Fig. 5.6 while other lines use a simplified representation. Further details of the test system along with its parameters are described in [90].

The DC side of all VSCs are solidly grounded by using DC capacitors at the neutral point. The VSC stations, which are based on the well-known MMCs, shown in Fig. 5.7(a), are represented by their continuous equivalent models with blocking/de-blocking capabilities [90, 91], as presented in Fig. 5.7(b). The blocking signals of IGBTs are triggered by the converter internal protection shown in Fig. 5.7(c), which consists of overcurrent and undervoltage protection. The arm current threshold is set to be 80% of the maximum



(a)



(b)

(c)

Figure 5.7: Diagrams of the MMC models and their internal protection. a) circuit diagram and SMs; b) continuous equivalent MMC arm model with blocking/de-blocking capabilities [90, 91]; and c) MMC internal overcurrent and undervoltage protection.

instantaneous limit for the IGBT current, while the voltage threshold is selected to be 20% of the nominal DC voltage. The cables are represented by the frequency-dependent model.

The study system [90] is modeled in the PSCAD/EMTDC software environment with its parameters listed in Table 5.1. A sampling frequency of $f_s = 50$ kHz is adopted in all simulations.

Table 5.1: Converter and grid parameters of the four-terminal MTDC test system [90]

	Conv. 1,2,3	Conv. 4
Rated power [MVA]	900	1200
AC grid voltage [kV]	400	400
AC converter voltage [kV]	380	380
Transformer u_k [pu]	0.15	0.15
AC grid reactance X_{ac} [Ω]	17.7	13.4
AC grid resistance R_{ac} [Ω]	1.77	1.34
Arm capacitance C_{arm} [μF]	29.3	39
Arm reactor L_{arm} [mH]	84.8	63.6
Arm resistance R_{arm} [Ω]	0.885	0.67
Bus filter reactor [mH]	50	50

5.5.2 Evaluation of Primary Relaying Algorithm

In this section, a set of study results are presented to evaluate performance and effectiveness of the proposed hybrid primary fault detection algorithm under four scenarios: a) a P2P fault under normal operation conditions; b) a low-impedance P2G fault; and c) a high-impedance P2G fault. The study system [90] is modeled in the PSCAD/EMTDC software environment with its parameters listed in Table 5.1. A sampling frequency of $f_s = 50$ kHz is adopted in all simulations.

The Implemented Detector Pool and Detector Learner: There are four detectors, indexed from 1 to 4, implemented in the detector pool, i.e., current threshold, current derivative, ROCOV, and QCD based detector, respectively.

The current threshold based detector [54, 55] takes line current as the input and simply compares it with a pre-determined threshold. The threshold is selected to be 1.25 times the

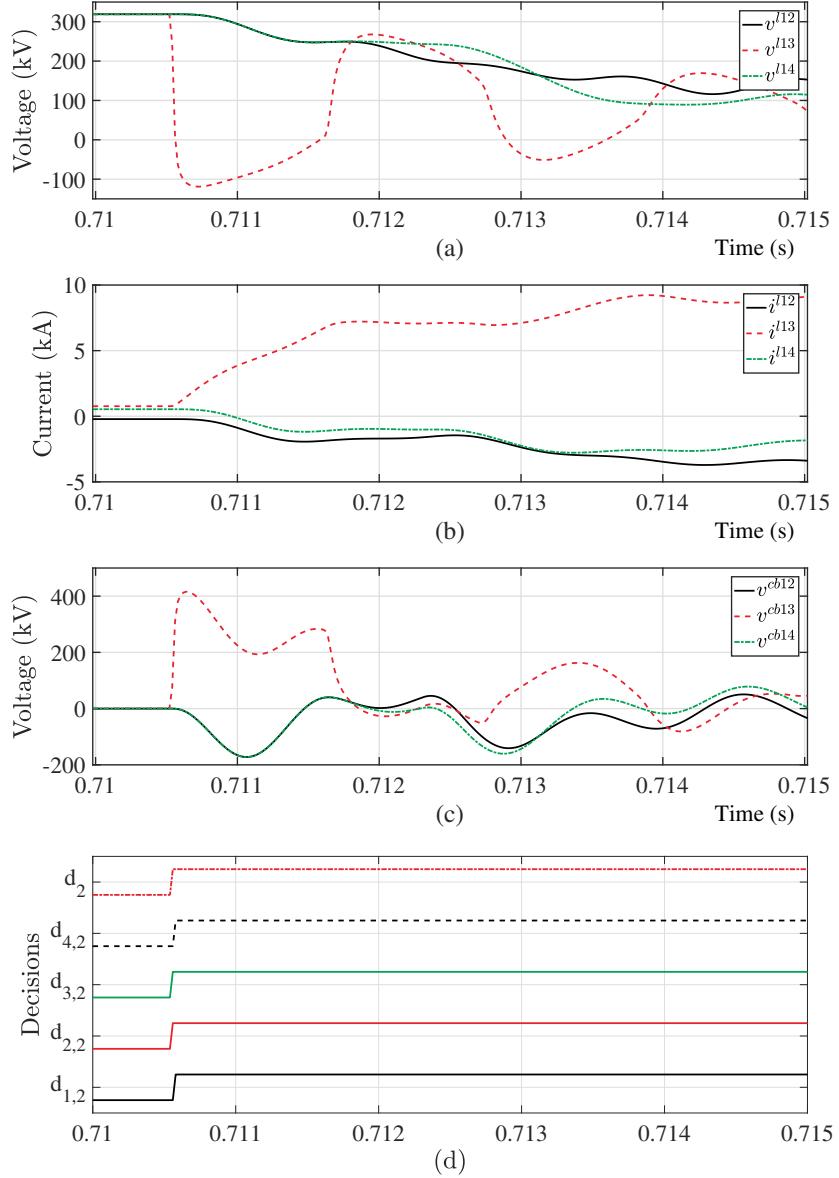


Figure 5.8: Simulation results with a P2P fault in the middle of Line13: (a) line voltages measured at Converter 1, (b) line currents measured at Converter 1, (c) voltages across DC reactors close to Converter 1, and (d) decisions made by the detectors from detector pool and detector learner.

nominal line current in the study.

The current derivative and ROCOV based detectors [53, 59] computes the derivative of line currents and voltages beyond current limiting reactors, respectively. To make these detectors more robust under noisy signals, a moving average filtering is performed on the given inputs. The window size is selected to be three in this work.

The QCD based detector [23] takes the same inputs as the ROCOV based detector. However, the input signals are not pre-processed using the moving average filter.

As shown in Fig. 5.3, there are three cluster labels. The updated weights $w_{n,c}$ for each detector given the cluster labels are presented in Table. 5.3.

Table 5.2: The weights used in detector learner

Detector	Current threshold	Current derivative	ROCOV	QCD
Label 1	0.246	0.262	0.262	0.230
Label 2	0.193	0.281	0.281	0.246
Label 3	0.365	0.044	0.080	0.511

P2P Fault: In this scenario, the system of Fig. 3.8 is subjected to a P2P fault located in the middle of Line13, which is 100 km away from Converter 1. This fault is triggered at $t = 0.71$ s. The propagation of travelling wave takes around 0.5 ms to reach this terminal [67].

The simulation results are demonstrated in Fig. 5.8. The positive-pole line voltages measured beyond the current limiting reactors v^{lij} , positive-pole line currents measured at the end of the transmission lines i^{lij} , and voltage across the DC reactors v^{cbij} are presented in Figs. 5.8(a)-(c), respectively. The measurements from negative poles are also used in the proposed approach but are not shown in the figures. In the detector pool, three types of detectors are implemented based on these measurements. The ROCOV detectors are applied with signals v^{lij} . Signals i^{lij} and v^{cbij} are used in threshold-based detectors.

Fig. 5.8(d) shows the decisions made by the four detectors $d_{n,2}$ and the final decision d_2 . The context is clustered to be label 2. The detector 1 (current threshold) and detector 4 (QCD) are slightly slower than the other two derivative based detector (2&3). According to Table. 5.2, the summation of weights from detector 2 & 3 are higher than 0.5, the final decision is made when these two detectors vote true. This makes the proposed algorithm works as good as the fastest detectors given they are reliable from the past experience. The trip signal of DC circuit breaker CB_{13} , T_{13} is triggered at $t = 0.7111$ s, less than 1 ms after

the arrival of fault wave front. The rest of DC circuit breakers are safely kept untripped.

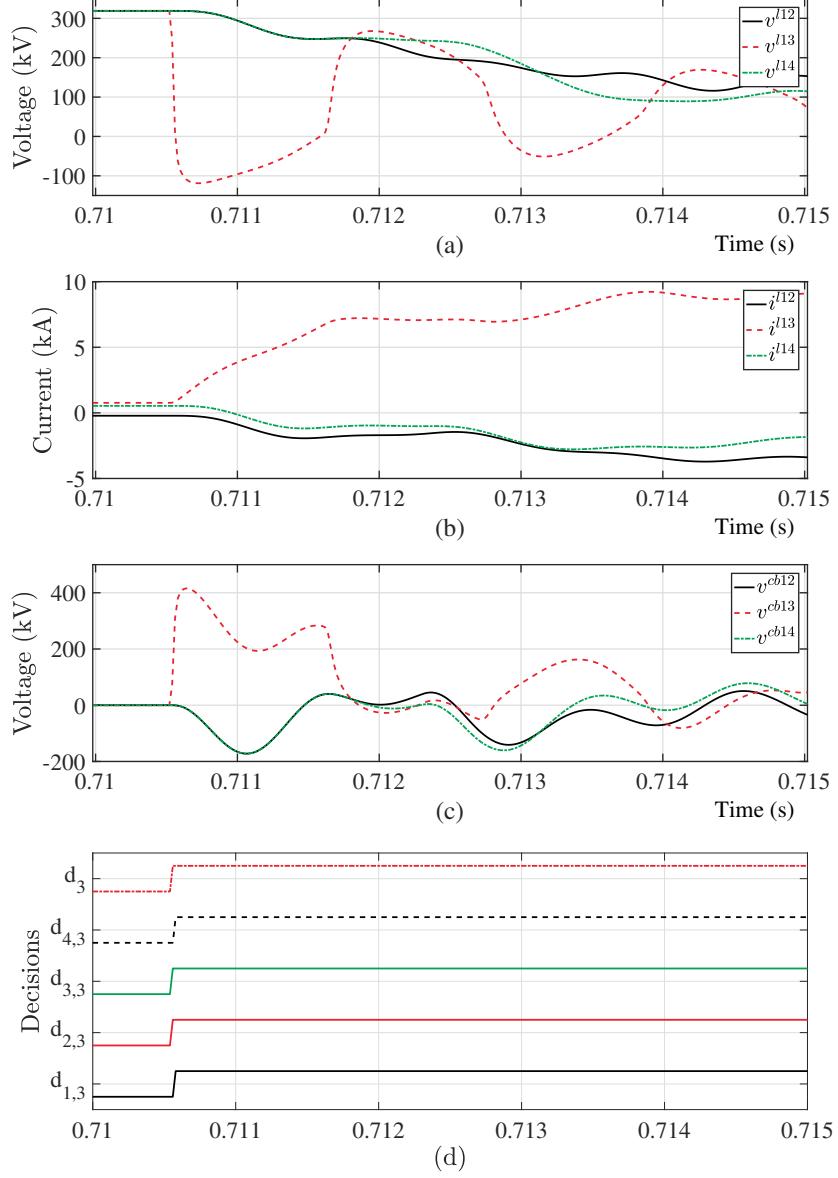


Figure 5.9: Simulation results with a P2G fault in the middle of Line13: (a) line voltages measured at Converter 1, (b) line currents measured at Converter 1, (c) voltages across DC reactors close to Converter 1, and (d) decisions made by the detectors from detector pool and detector learner.

P2G Fault: Another fault type that has been tested is the low-impedance P2G fault. The positive pole of Line13 is grounded in the middle of the line. The measured signals are presented in Fig. 5.9.

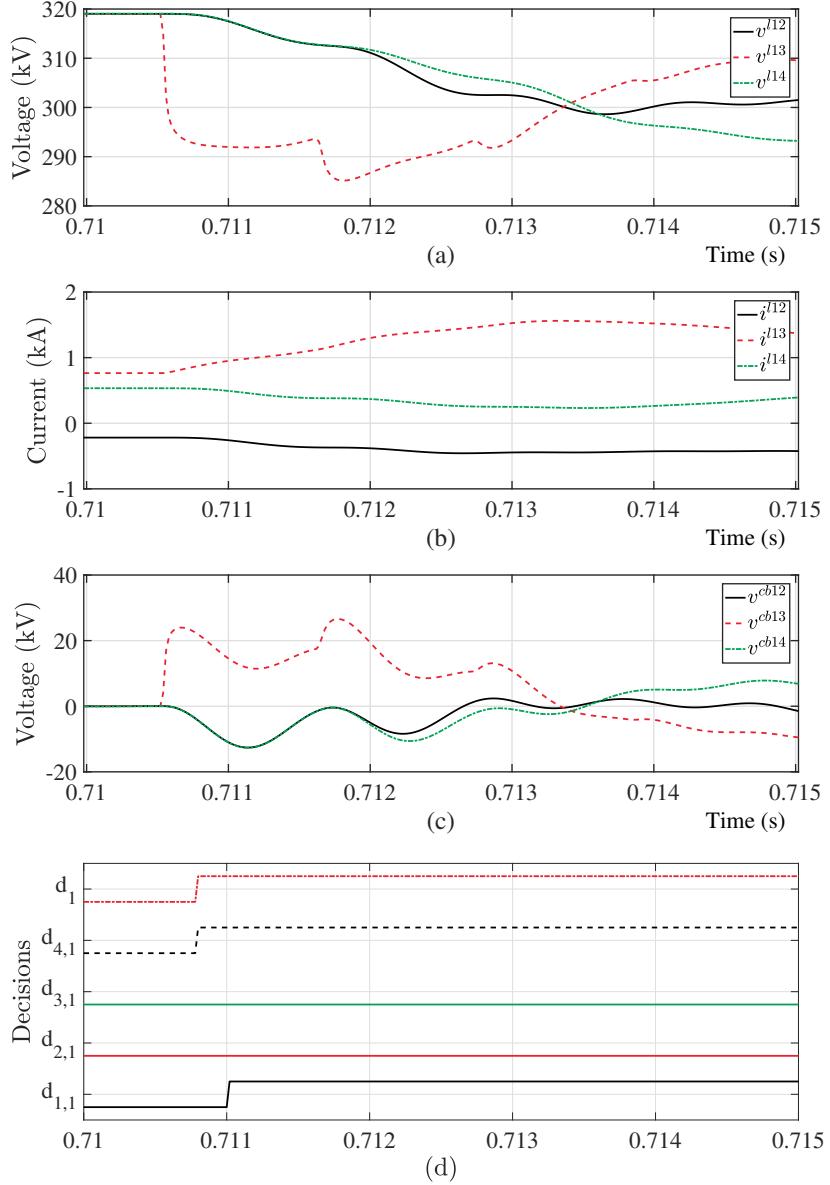


Figure 5.10: Simulation results with a high impedance P2G fault in the middle of Line13:
 (a) line voltages measured at Converter 1, (b) line currents measured at Converter 1, (c)
 voltages across DC reactors close to Converter 1, and (d) decisions made by the detectors
 from detector pool and detector learner.

Since only the measurements from the positive poles are shown in the figures, the waveforms look almost identical to the P2P case. The signals from negative poles, however, do not significantly deviate away from their nominal states. This P2G fault is detected by the proposed primary detector and the trip signal for DC circuit breaker CB_{13} is generated.

High-Impedance P2G Fault: High-impedance P2G faults are hard to be detected given their little deviated signals from nominal values. The context of this case is clustered to be label 1.

In this scenario, a high-impedance P2G fault is imposed on the positive pole of Line13 (100 km from Bus 1). A $300\ \Omega$ fault impedance is inserted between the fault location and the ground. With a higher fault impedance applied, the drop of voltage magnitude is even smaller compared to the low-impedance P2G case. The simulation results are presented in Fig. 5.10.

The parameters of detector 2 & 3 are determined to be not too sensitive to the change of current or voltage derivatives to withstand noisy signals. Therefore, under this case, they are not able to detect the faults. Detector 1 successfully detects the fault. However, it is slow since it has to wait for the fault current to go across the pre-defined threshold. The rate of rise of current is not as high as the P2P or low impedance P2G cases. Therefore, it takes longer for detector 1 to be triggered. Detector 4 performs best in this scenario. It is not as fast as in previous cases due to the smaller deviation of voltage signals, but it is faster than detector 1. According to Table 5.2, detector 4 performs well and is trustworthy when the context is labelled 1 given its high weight. The final decision is made and the trip signal for DC circuit breaker CB_{13} is generated when detector 4 is triggered.

False Alarms and Detection Failure: The proposed primary fault detection algorithm improves its robustness and reliability by performing a majority voting from detectors in the detector pool. As a result, the overall performance metrics like miss-detection and false alarm rates are as good as the performance metrics of the best candidate detector. The QCD detector is robust to signals where noise and spikes are introduced, at the expense of sacrificing the detection speed. The current derivative and ROCOV based detectors can be tuned to be sensitive to high impedance faults, but they will be more likely to raise false alarms. These trade-offs worsen the performance of individual detector and are hard to be

balanced. The proposed hybrid approach, however, combines the best of each detector and avoid their drawbacks. The candidate detectors are thus be tuned to work best on particular scenarios, and are not necessarily well balanced to all cases. The choices and optimized tuning of detector pool will be addressed in future works.

5.5.3 Evaluation of Backup Relaying Algorithm

In this section, a set of simulation results are presented to evaluate performance and effectiveness of the proposed backup protection algorithm under five scenarios: a) a P2P fault under normal operation conditions; b) a low-impedance P2G fault; c) a high-impedance P2G fault d) reversed power flow; and e) presence of noise and spike.

Base Case: This is the reference case where 800 MW and 600 MW are distributed to Converters 3 and 4, respectively, from Converters 1 and 2, which both input 700 MW to the MTDC grid. In this scenario, the test system is subjected to a P2P fault located on the middle of Line13.

The simulation results are demonstrated in Fig. 5.11. As described in Section 5.4, the voltage across the circuit breaker (CB_{13P} in this case) is used for breaker failure detection. v^{cb13p} with both proper breaker operation and breaker failure are depicted in Fig. 5.11(a). Under the breaker failure condition, v^{cb13p} remains close to zero while the signal jumps to a high value in the case where the fault is successfully cleared. In the proposed algorithm, the accumulated sum g and the decision variable d are updated within every step in Algorithm 2. A zoomed-in view of g and d is presented in Fig. 5.11(c). When the breaker works properly, v^{cb13p} starts to increase at $t = 3.66$ ms, which means that the fault current is being commutated from the main breaker branch to the arresters. g keeps accumulating because of the high value of signal v^{cb13p} . At $t = 3.76$ ms, g becomes higher than the threshold h (marked as the horizontal line), resulting in the change of d from 0 to 1. This change indicates that the breaker operates normally. In this case, AND gate 1 is satisfied and

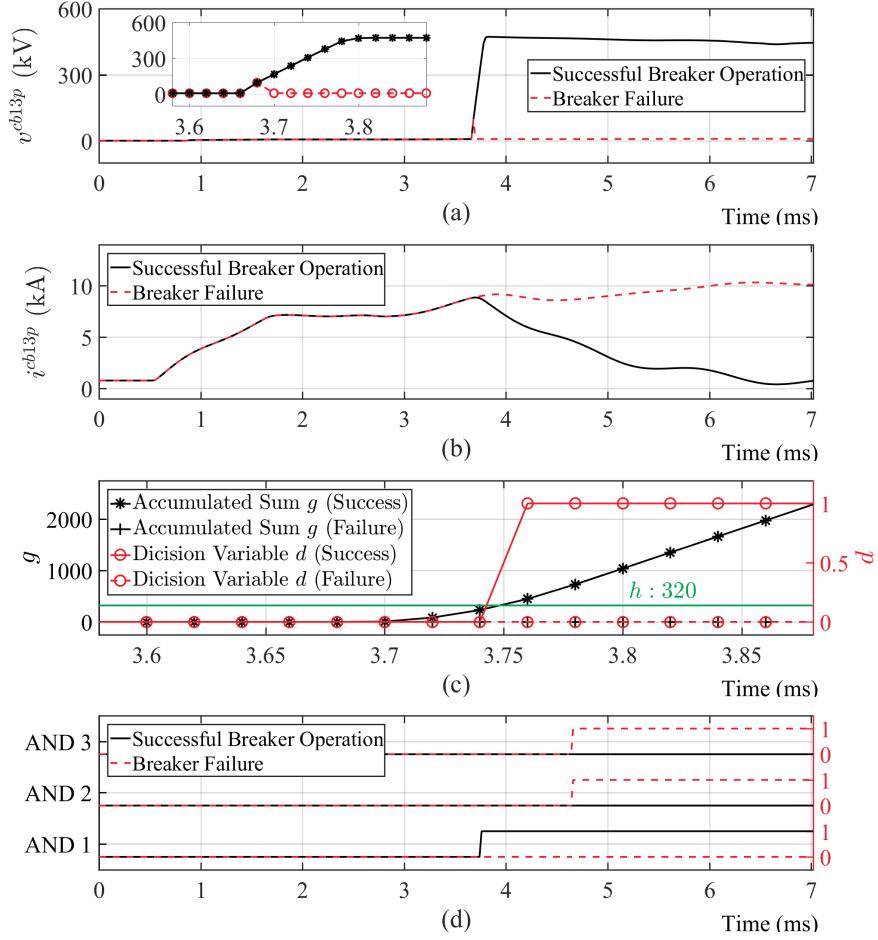


Figure 5.11: Simulation results with a P2P fault in the middle of Line13, under both successful breaker operation and breaker failure: (a) voltage across circuit breaker v_{cb13p} , (b) current flowing through circuit breaker i_{cb13p} , (c) zoomed-in portion of outputs from breaker failure QCD algorithm, and (d) outputs of AND gates 1, 2, and 3 from Fig. 5.5.

outputs 1, as shown in Fig. 5.11(d). The condition 1 from AND gate 1 deactivates AND gate 3, preventing a backup trip. However, if the breaker fails to operate properly, g and d remain zero, which result in a zero output from AND gate 1. Then, the state of AND gate 3 is dominated by the state of AND gate 2, which is determined by two conditions, i.e., the delayed trip signal from the primary relay and the presence of uncleared current flow. After a time delay of Δt_{bf} , the primary relay trip signal is sent to AND gate 2 at $t = 4.68$ ms. As shown in Fig. 5.11(b), the current (i^{cb13p}) flowing through breaker is higher than twice the nominal current. Therefore, the outputs of both AND gate 2 and 3 switch to 1, indicating a breaker failure condition.

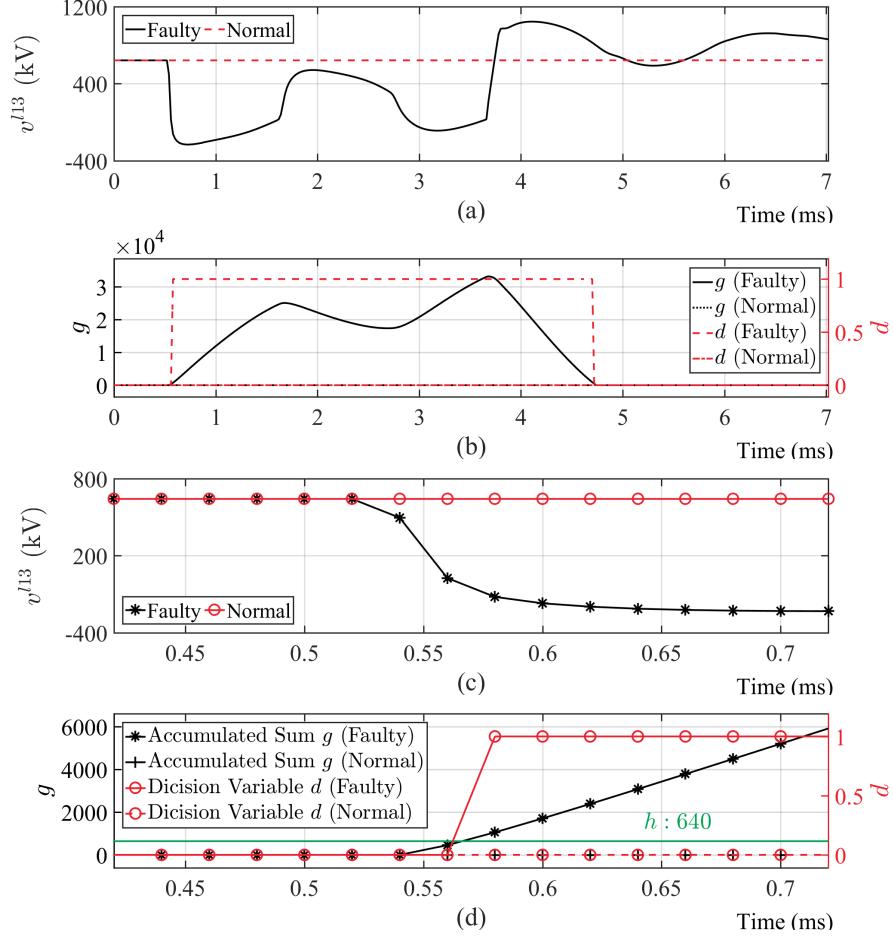


Figure 5.12: Simulation results with a P2P fault in the middle of Line13, under both normal and faulty conditions: (a) v^{L13} , voltage of Line13 at Bus 1, (b) outputs from breaker relay backup algorithm, (c) and (d) zoomed-in portion of (a) and (b), respectively.

It is noteworthy that the threshold h and minimum detectable magnitude ν in Algorithm 2 are simply selected to be 320 kV, which is the nominal voltage of the HVDC system. The pre-fault mean, θ_0 , is zero here. h , ν and θ_0 are kept unchanged for all the following breaker failure protection scenarios.

Similarly, the results of the relay backup protection algorithm is provided in Fig. 5.12. v^{L13} , the P2P voltage of Line13 at Bus 1 is the measurement being monitored (Fig. 5.12(a)). To adopt the same algorithm as the breaker failure detection, $-v^{L13}$ is fed into Algorithm 2. When the wavefront arrives at the terminal of Bus 1 during a fault, v^{L13} drops quickly, which results in an increase in g (Fig. 5.12(b)). At $t = 0.58$ ms, d changes to 1, indicating

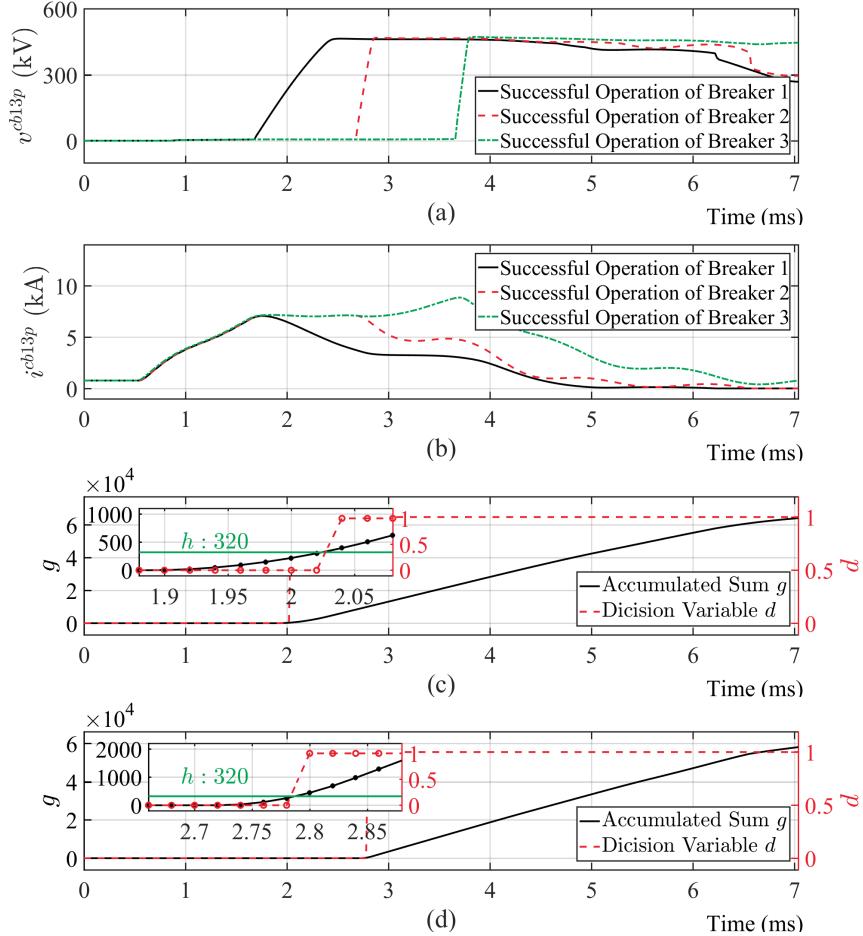


Figure 5.13: Simulation results with different breaker configurations: (a) voltage across the circuit breaker v_{cb13p} , (b) current flowing through the circuit breaker i_{cb13p} , (c) outputs of the breaker failure QCD algorithm under successful breaker operation for breaker 1, (d) outputs of the breaker failure QCD algorithm under successful breaker operation for breaker 2.

a fault detection. On the contrary, both g and d remain zero under normal conditions. As described in Section III, the relay failure protection will trip if the primary relay does not detect the fault prior to $t = 3.58$ ms, which is the summation of 0.58 ms, the detection time and 3 ms, the delay Δt_{rf} . The zoomed-in views of Figs. 5.12(a) and (b) are presented in Figs. 5.12(c) and (d), respectively. h and ν are set to be 640 kV and 320 kV, which are the nominal values of the P2P and P2G voltage of the DC links, respectively. $\theta_0 = -640$ kV is adopted in Algorithm 2. These values of h , ν and θ_0 are used for all the following relaying failure protection scenarios.

Proper selection of the threshold values ensures that the abrupt changes are precisely detected while keeping a low false alarm rate. The values selected in this study, i.e., 320 kV and 640 kV, can be easily obtained from the system parameters. These thresholds keep a balance between the detection speed and false alerts.

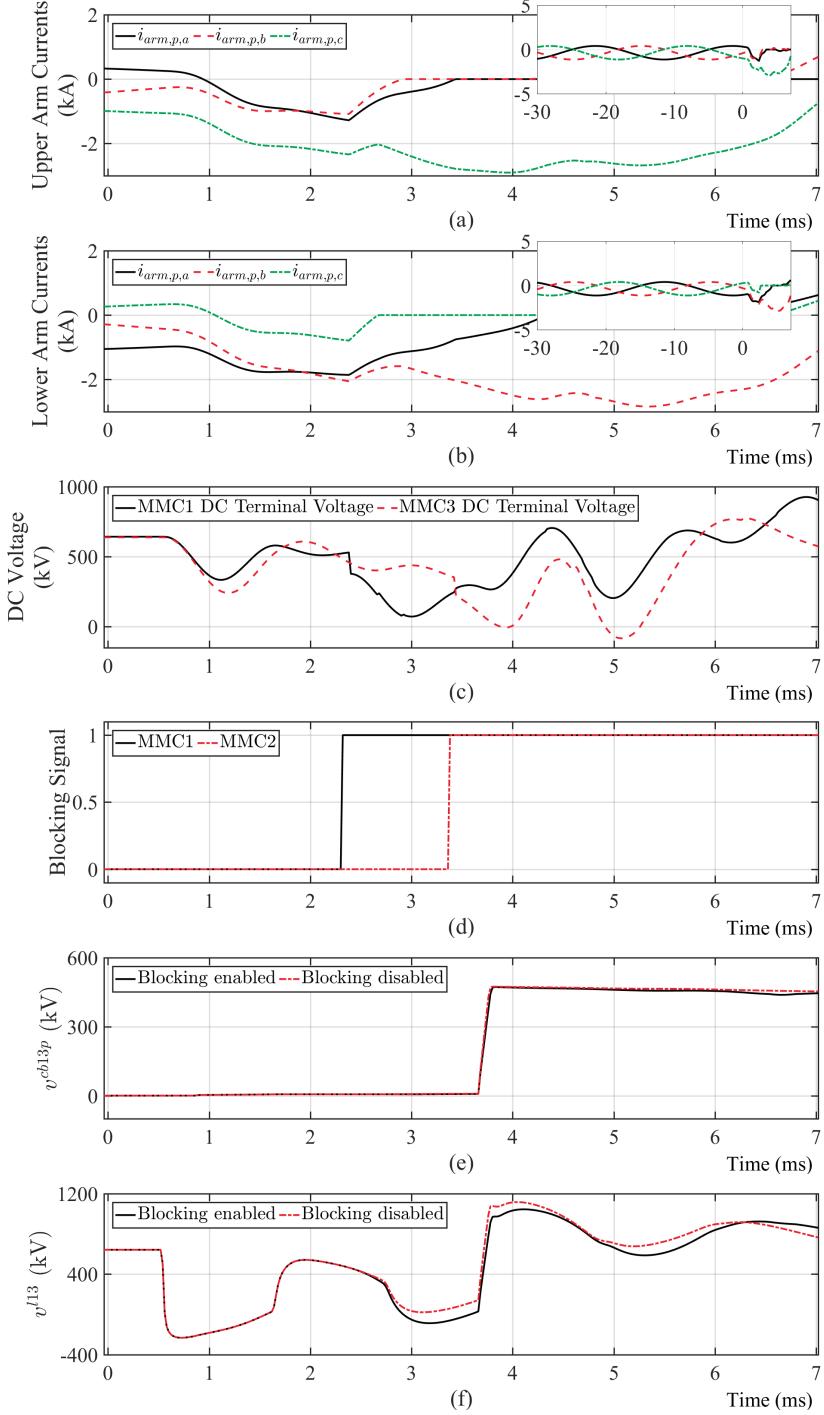


Figure 5.14: Simulation results of converter internal protection quantities with a P2P fault in the middle of Line13: (a) upper arm currents of MMC1, (b) lower arm currents of MMC1, (c) DC voltage on MMC1 terminal side and MMC3 terminal side (for undervoltage internal protection), (d) blocking signals of MMC1 and MMC2., (e) voltage across the circuit breaker v_{cb13p} with and without converter blocking enabled, and (f) v_{l13} , voltage of Line13 at Bus 1 with and without converter blocking enabled.

Compatibility with Different Breaker Configuration: In this section, two more breakers, i.e., breakers 1 and 2, are implemented to test the compatibility of proposed backup algorithm with different breaker configurations. These two new breakers have different delays and fault clearance times, as depicted in Fig. 5.13(a). Breaker 3 is the same breaker used in the base case and is presented here as a reference. The currents flowing through these breakers are shown in Fig. 5.13(b). As shown in Fig. 5.13, with different breakers deployed, the fault is cleared with different speeds. The outputs from the QCD algorithm applied to breakers 1 and 2 are shown in Figs. 5.13(c) and (d), respectively. These results verify that the proposed backup algorithm is equally applicable to different breaker configurations.

Blocking of IGBTs: Subsequent to a fault on any DC link, the MMC arm currents exceed their rating values. Once the arm currents exceed a threshold value, the desaturation detection of IGBTs will act, thereby blocking them to avoid any thermal overload. The converter is also blocked under low DC voltage due to the loss of controllability. The implemented scheme is presented in Fig. 5.7(c). A P2P fault in the middle of Line13 is imposed on the test system at $t = 0.71$ s. The six arm currents of MMC1 are plotted in Figs. 5.14(a) and (b). The current threshold I_{thres} is set to be 2.31 kA based on the rating of MMC1, i.e., 80% of the maximum instantaneous arm current, which is 2.88 kA. Subsequent to the fault occurrence, MMC1 and MMC2 are blocked after 2.3 ms and 3.4 ms, respectively. In this case, as shown in Fig. 5.14(c), the DC voltage on MMC1 terminal drops below 20% of the DC nominal voltage after the blocking of MMC1. The converter will not be re-blocked by the undervoltage protection. The voltage across breaker v^{cb13p} (used for breaker failure backup) and the voltage of Line13 v^{l13} (whose first wave is used for relay failure backup) are presented in Figs. 5.14(e) and (f), respectively. These voltages are measured with and without converter blocking enabled. The waveforms of Figs. 5.14(e) and (f) highlight that the sequence of converter blocking/de-blocking does not interfere with the operation

and performance of the proposed backup protection algorithms, which rely on the voltage across the breaker and the first wave of line side DC voltage. Therefore, the functionalities of the breaker and relay failure backup protection algorithms are not affected.

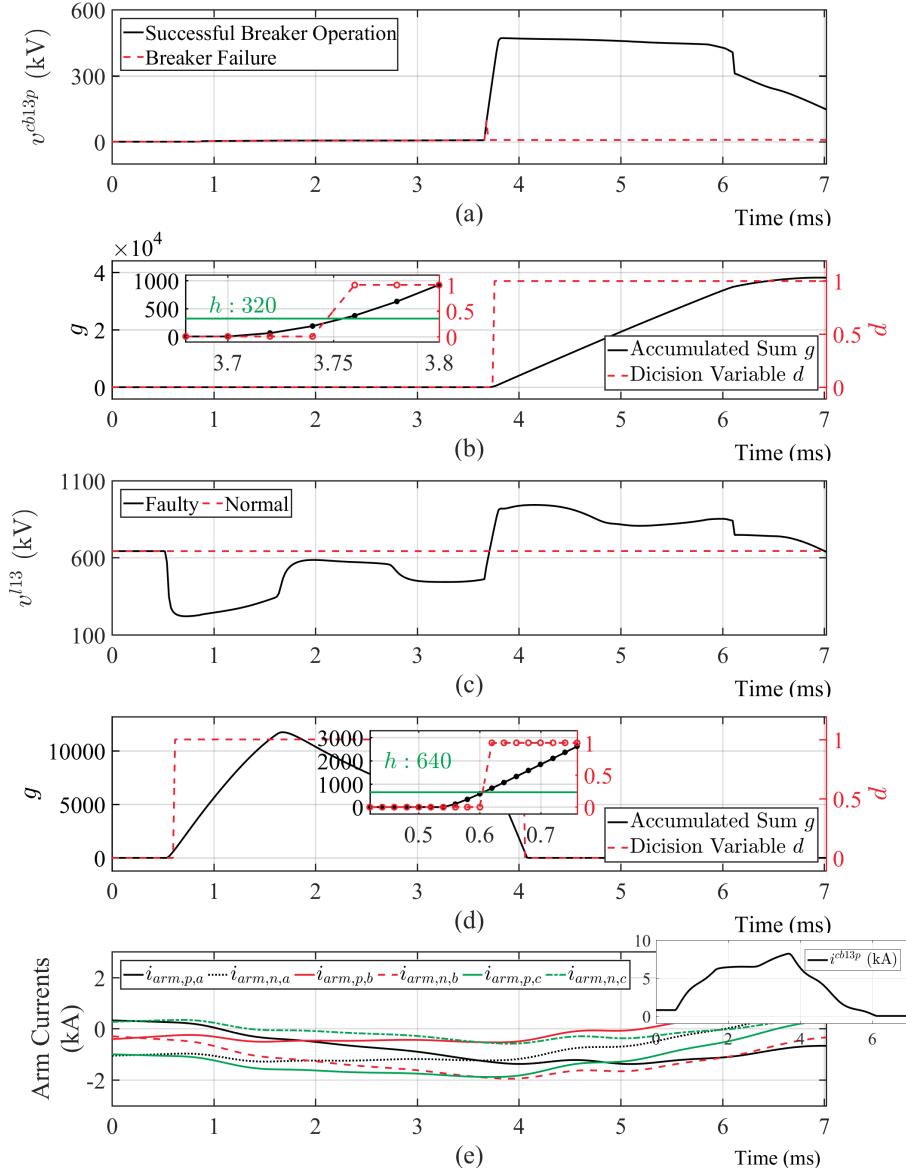


Figure 5.15: Simulation results with a low-impedance fault in the middle of Line13: (a) voltage across the circuit breaker v_{cb13p} , (b) outputs of the breaker failure QCD algorithm under successful breaker operation, (c) v^{l13} , voltage of Line13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i^{l13p} .

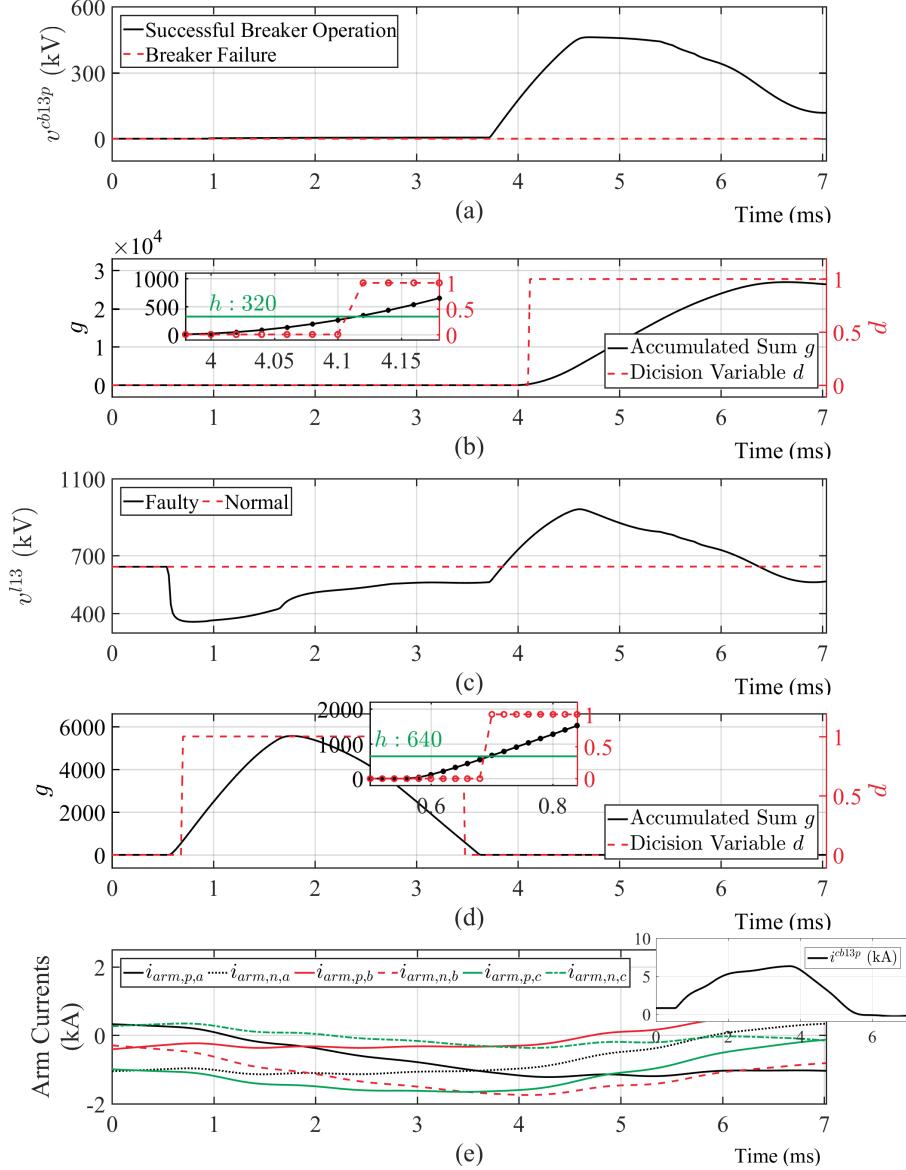


Figure 5.16: Simulation results with a high-impedance fault in the middle of Line13: (a) voltage across the circuit breaker v_{cb13p} , (b) outputs of the breaker failure QCD algorithm under successful breaker operation, (c) v_{l13} , voltage of Line13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i_{l13p} .

Low-Impedance P2G Fault: In this scenario, the system is subjected to a low-impedance P2G fault on the positive pole of Line13 (100 km from Bus 1). The fault impedance is 0.5Ω . The results from the backup protection for both breaker (Figs. 5.15(a) and (b)) and relay failure (Figs. 5.15(c) and (d)) are provided. The QCD algorithm outputs under

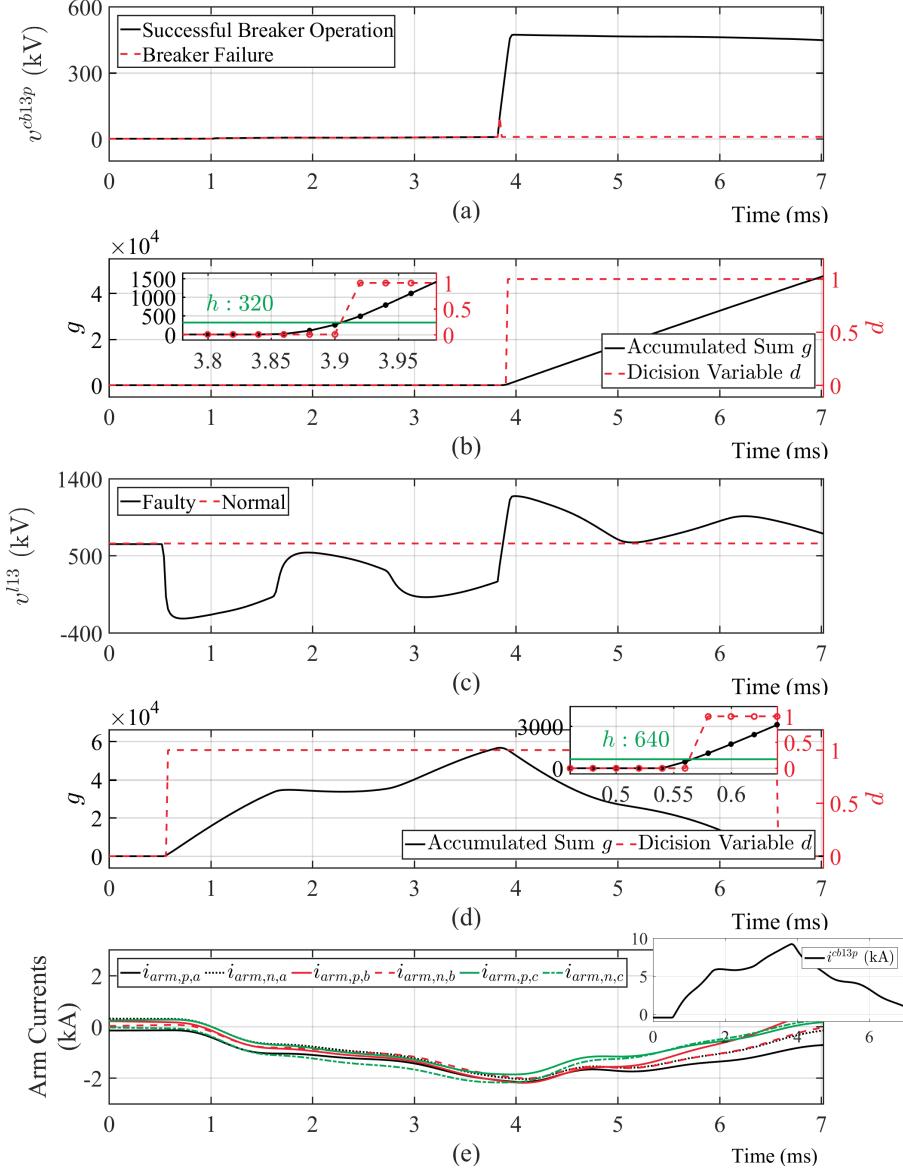


Figure 5.17: Simulation results under reversed power flow: (a) voltage across the circuit breaker v_{cb13p} , (b) outputs of the breaker failure QCD algorithm under successful breaker operation, (c) v_{l13} , voltage of Line13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i^{l13p} .

breaker failure and normal conditions are all zero and not presented. As shown in Fig. 5.15(e), none of the arm currents exceed I_{thres} . As the result, MMC1 is not blocked in the first 7 ms.

In this case, v_{cb13p} presents a similar behavior to the reference scenario. Fig. 5.15(b)

confirms the detection of successful fault clearance at $t = 3.76$ ms, when d changes from zero to one. The voltage drop of v^{l13} (Fig. 5.15(c)) is not as large as the change in the reference case (Fig. 5.12(a)) and, therefore, it results in a slower accumulation of g . However, the relay failure backup algorithm still works well and detects the fault at $t = 0.62$ ms.

High-Impedance P2G Fault: In this scenario, a high-impedance P2G fault is imposed on the positive pole of Line13 (100 km from Bus 1). A 10Ω fault impedance is inserted between the fault location and the ground. With a higher fault impedance applied, the drop of voltage magnitude is even smaller compared to the low-impedance case. However, as shown in Fig. 5.16, both breaker failure backup and relay backup protection algorithms respond well.

Reversed Power Flow: In this scenario, the system is tested under the same fault in the reference case. The difference lies in the direction and distribution of power flow. In this case, Converters 3 and 4 both export 500 MW to the MTDC grid while Converters 1 and 2 transfer 200 MW and 800 MW, respectively, to the AC grid. The results presented in Fig. 5.17 demonstrate satisfactory performance of the proposed algorithm.

Comparison with the Existing Methods: In this section, the results from the proposed backup protection method are compared with the classifier based backup method [69][70]. To this end, both the signals, v^{cb13p} and v^{l13} , are contaminated by adding noise and spikes. These signals are processed by the proposed and existing algorithms. The corresponding results are shown in Figs. 5.18 and 5.19.

To test the impact of noise, an independent and identically distributed sequence drawn from a Gaussian distribution $\mathcal{N}(0, 100)$ is applied and added to the original signals as shown in Figs. 5.18(a) and (b). Unlike the classifier based method, the accumulated sum g , which is shown in Fig. 5.18(c), is not affected by the presence of such noise. Fig.

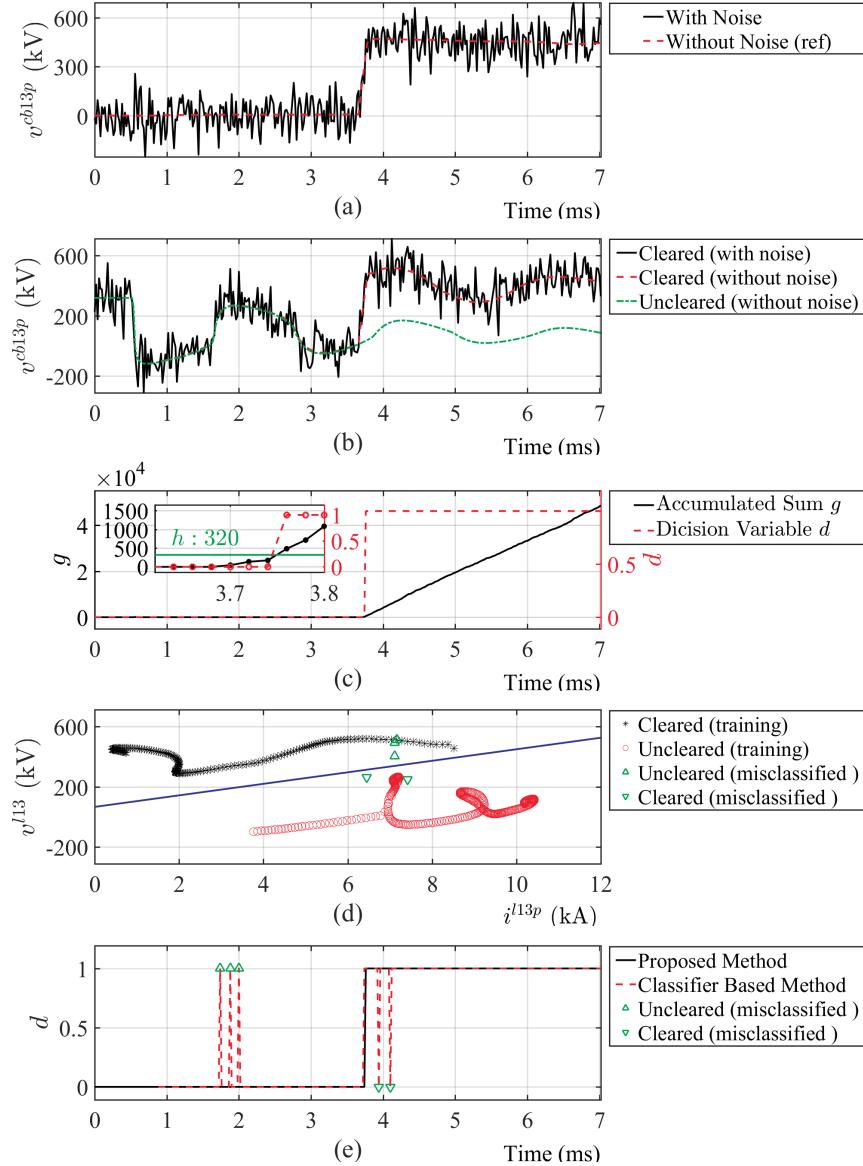


Figure 5.18: Comparison under noise. (a) voltage across the circuit breaker v_{cb13p} , (b) v^{l13} , voltage of Line13 at Bus 1, (c) and (d) results from the proposed and classifier-based methods, and (e) decision variables.

Figure 5.18(d) shows the scatter plot (UI characteristic) of voltage, v^{l13} and current, i^{l13p} used for the classifier based algorithms. The space is separated by a decision boundary (marked in purple line). A fault is said to be cleared if the instantaneous measurement lies in the upper space while it is declared as uncleared when it appears in the lower space. In the presence of noise, some of the samples which should lie in the “uncleared” portion are misclassified into the upper space (marked in upward-pointing triangles). Similarly, some

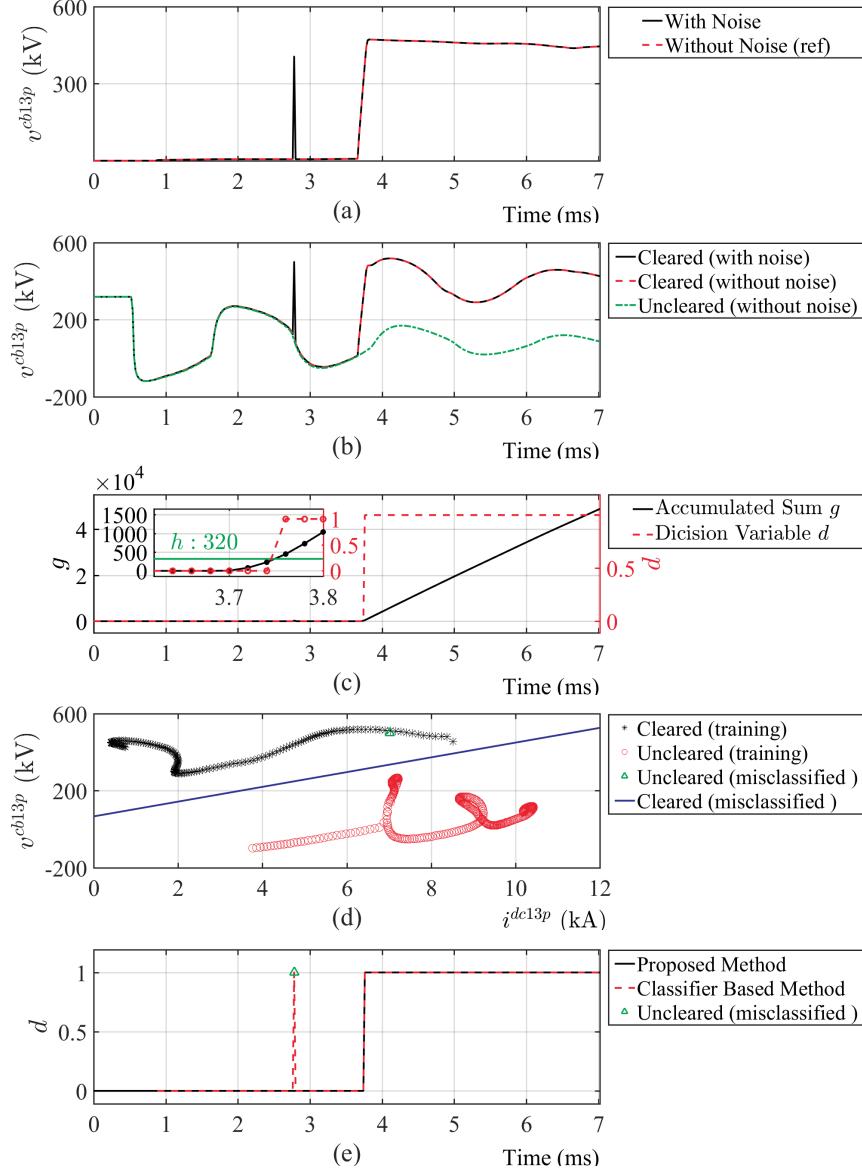


Figure 5.19: Comparison under spike. (a) voltage across the circuit breaker v^{cb13p} , (b) v^{l13} , voltage of Line13 at Bus 1, (c) and (d) results from the proposed and classifier-based method, and (e) decision variables.

“cleared” samples are misclassified into the lower space (marked in downward-pointing triangles). In Fig. 5.18(e), the decision variables from the proposed and classifier-based algorithm are compared. Before the actual starting time of fault clearance at $t = 3.66$ ms, the classifier based algorithm declares detection of successful breaker actions ($d = 1$) at around $t = 2$ ms to $t = 2.5$ ms (upward-pointing triangles). Additionally, after $t = 3.66$ ms, some of the samples (downward-pointing triangles) are classified as “uncleared” again.

These misclassifications result in false trip signals.

Fig. 5.19 shows the performances of the proposed and classifier based algorithms under the effect of a 400 kV spike at $t = 2.8$ ms. The spike introduces an abnormally high voltage prior to fault clearance, resulting in a misclassification of an “uncleared” sample into a “cleared” one by the classifier-based method. As confirmed in Fig. 5.18, performance of the proposed algorithm is not degraded under this case as well.

With respect to the computational burden, there are two additional drawbacks by using the classifier-based method:

- A K nearest neighbor (KNN) classifier, which is used as an example in [70], has to be trained with data from different types of faults under various scenarios. For example, for a P2P fault, the fault characteristic varies with the faulty link, fault location and fault impedance. The classifier has to be trained with data from all possible cases. The proposed method uses the same framework for all scenarios, with a much more simplified procedure.
- To make a correct decision based on the KNN, all historical current and voltage data has to be stored in the relay, thereby demanding a huge amount of data storage. Compared to the classifier-based method, the proposed method only keeps record of the cumulative sum and other three variables, which are fixed sized floating numbers and take a negligible space.

CHAPTER 6

CPU & GPU CO-SIMULATION OF MTDC GRIDS

6.1 Simulation of MTDC Grids

Numerical Simulation plays an important role in evaluation of MTDC grid protection systems. To address the modelling and scalability issues of previous simulation solutions, in this chapter, a cost-effective high-performance faster-than-real-time EMT simulation platform is proposed for large-scale cross-continental MTDC grids. This platform is built on GPU, using hybrid-discretized MMC detailed equivalent model [35, 40], universal line model (ULM) for lines/cables [31, 92], and EMT-type model for synchronous generators and transformers [25, 26, 36]. The GPU-based EMT simulation methods have been developed in previous research for MMC device-level modelling [93], AC grids [94, 95], and MTDC grids [96]. However, faster-than-real-time simulation of a large-scale MTDC grid has not been achieved on GPUs. The proposed CPU & GPU co-simulation platform demonstrates potential of a massive paralleled GPU-based solution with high price-performance ratio.

6.2 United States Cross-continental MTDC Grid

Fig. 6.1 shows the layout of the cross-continental MTDC system originated from one of the Grid Modernization Laboratory Consortium (GMLC) projects [8]. This multi-terminal grid, which is embedded across multiple AC interconnections in the US, enables economic power transfer, mitigation of congestion and loop flow, cross-interconnection frequency support, and loss reduction in the national scale power grid.

Two ± 320 kV DC transmission lines/cables are used to connect the three DC terminals in the radial configuration. The DC terminals, which are based on MMCs, are represented

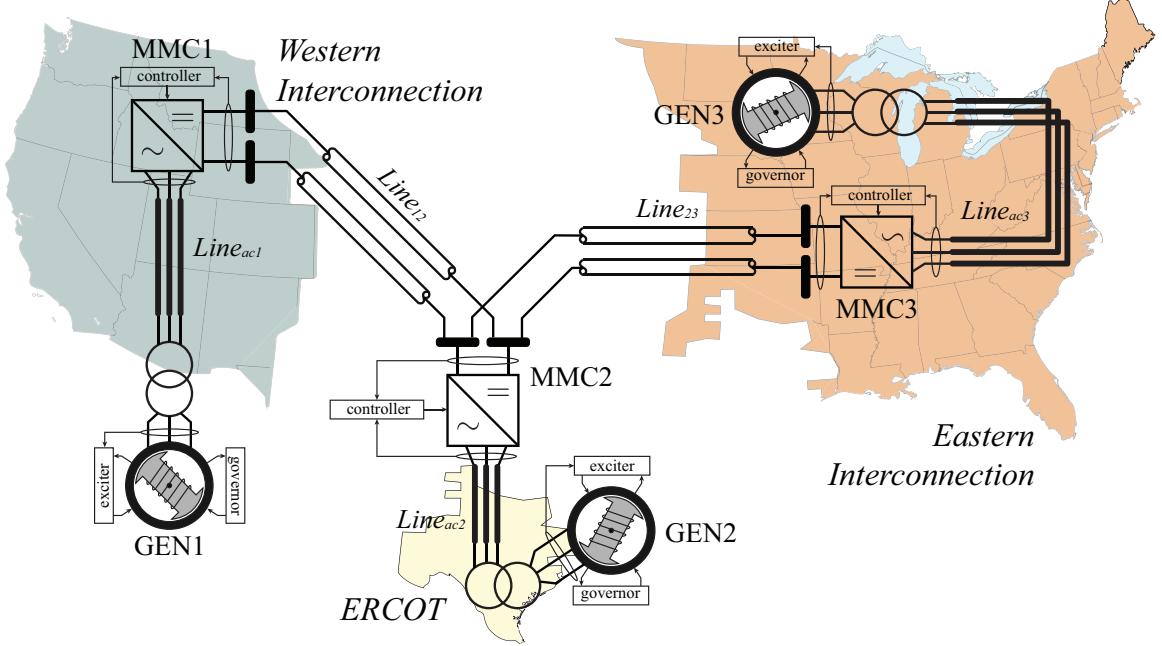


Figure 6.1: Diagrams of the US cross-continental MTDC grid connecting the three major interconnections, i.e., WI, EI, and ERCOT [8].

by their detailed equivalent models using the hybrid discretization method as described in [35]. On the AC sides of the MMC terminals, the AC interconnections are modelled as aggregated generations. They are modeled by the dynamic models of synchronous generators, transformers, and AC transmission lines. The excitors and governors of these synchronous generators are also modelled in details with respect to generic interconnections.

6.3 Modelling of the MTDC-AC Grid

In the demonstrated MTDC-AC grid, there are four major components modelled in details, i.e., the MMCs, transmission lines, generators, and transformers. The modelling assumptions and techniques applied are described in this section.

6.3.1 MMC Modelling

A three-phase MMC consists of six arms, each of which has an inductor and N series-connected half-bridge SMs, as shown in Fig. 6.2. Basics of operation and control of MMC

are summarized in [32] and are not elaborated here.

The dynamics of MMC arm currents are given by

$$\begin{aligned} (L_o + L_s) \frac{di_{p,j}}{dt} - L_s \frac{di_{n,j}}{dt} &= -(R_o + R_s)i_{p,j} + R_s i_{n,j} \\ &+ \frac{V_{dc}}{2} - v_j - v_{cm} - v_{p,j}, \forall j \in \{a, b, c\}, \\ (L_o + L_s) \frac{di_{n,j}}{dt} - L_s \frac{di_{p,j}}{dt} &= -(R_o + R_s)i_{n,j} + R_s i_{p,j} \\ &+ \frac{V_{dc}}{2} - v_j - v_{cm} - v_{n,j}, \forall j \in \{a, b, c\}, \end{aligned} \quad (6.1)$$

where the arm voltages $v_{y,j} = \sum_{l=1}^N v_{sm,y,l,j}$ can be further factorized as functions of switching states and SM capacitor voltages $v_{cy,i,j}$ as provided by

$$\begin{aligned} v_{y,j} &= \sum_{i=1}^N [(1 - S_{yi1,j})(1 - S_{yi2,j})v_{cy,i,j}\text{sgn}(i_{y,j})] \\ &+ S_{yi1,j}v_{cy,i,j}], \forall y \in \{p, n\}, \forall j \in \{a, b, c\}. \end{aligned} \quad (6.2)$$

The dynamics of SM capacitor voltages are represented by

$$\begin{aligned} C_{SM} \frac{v_{cy,i,j}}{dt} &= -\frac{v_{cy,i,j}}{R_p} + S_{yi1,j}i_{y,j} + \text{sgn}(i_{y,j})(1 - S_{yi1,j}) \\ &\times (1 - S_{yi2,j})i_{y,j}, \forall y \in \{p, n\}, \forall j \in \{a, b, c\}. \end{aligned} \quad (6.3)$$

Equations (6.1) and (6.3) are typically discretized with different algorithms, i.e., backward Euler and forward Euler, based on their numerical stiffness. The discretization method applied in this work is the hybrid approach detailed in [35]. The MMC system equations are formed with this approach in the real-time simulation.

6.3.2 Transmission Line Modelling

The AC and DC transmission lines/cables in the MTDC system are modelled using the frequency-dependent models [31]. The frequency-dependency modelling enables the de-

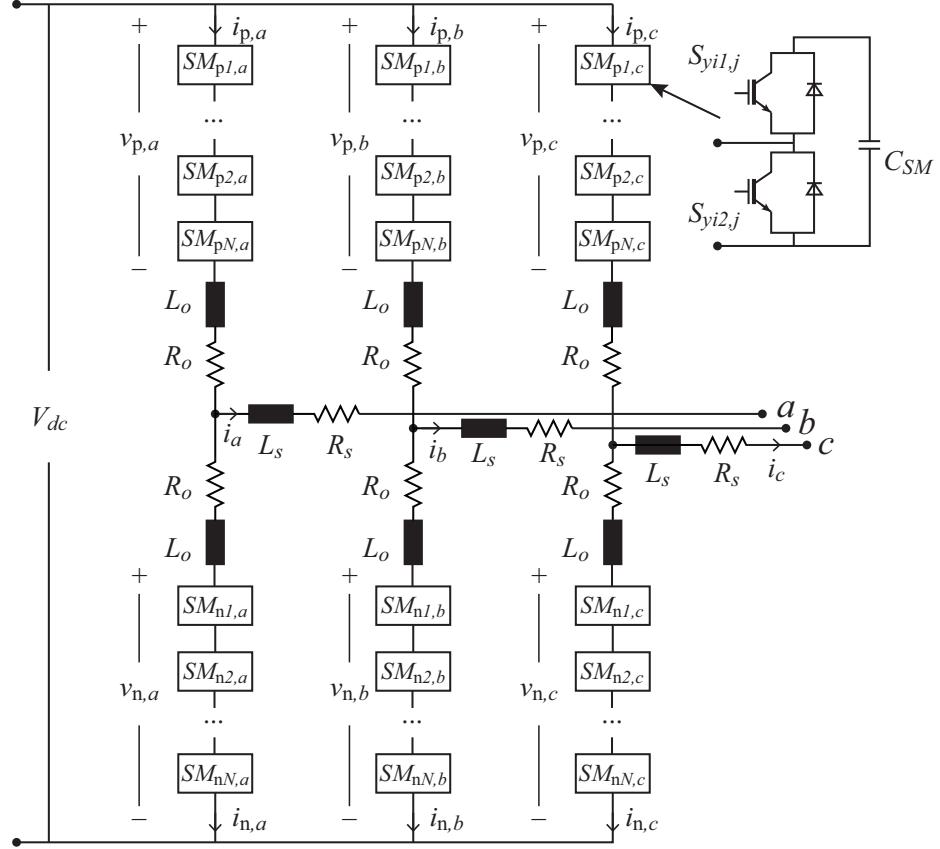


Figure 6.2: Circuit diagram of a three-phase MMC.

tailed characterization of the system dynamics over a wide range of frequency. Such a representation is critical for study of protection and high-bandwidth control methods in the system.

Derived from the well-known transmission line equations,

$$-\frac{d\mathbf{V}}{dx} = \mathbf{ZI}, \quad -\frac{d\mathbf{I}}{dx} = \mathbf{YV}, \quad (6.4)$$

where the voltage \mathbf{V} and current \mathbf{I} at both ends of the transmission line are correlated in the travelling wave form in frequency domain. This correlation is given by

$$\begin{aligned} \mathbf{I}_1 &= \mathbf{Y}_c \mathbf{V}_1 - \mathbf{H}(\mathbf{I}_2 + \mathbf{Y}_C \mathbf{V}_2), \\ \mathbf{I}_2 &= \mathbf{Y}_c \mathbf{V}_2 - \mathbf{H}(\mathbf{I}_1 + \mathbf{Y}_C \mathbf{V}_1), \end{aligned} \quad (6.5)$$

where $\mathbf{Y}_c = \mathbf{Z}^{-1}\sqrt{\mathbf{YZ}}$ is the characteristic admittance matrix, $\mathbf{H} = e^{-\sqrt{\mathbf{YZ}}l}$ is the propagation matrix.

These two frequency-dependent matrices are sampled at a large number of frequency points across a wide range. To transform (6.5) into the time domain, \mathbf{Y}_c and \mathbf{H} are fitted based on these frequency samples and replaced by their time-domain rational function equivalents of lower order (normally less than 20) [97]. These rational functions are discretized and convoluted with their corresponding terminal voltages/currents, and as a result, the time-domain solutions at both ends are obtained, given by

$$\begin{aligned} i_k &= G \cdot v_k - i_{\text{hist},k}, \quad \forall k \in \{1, 2\} \\ i_{\text{hist},k} &= \sum_{i=1}^m \left(\sum_{j=1}^{N_H} h_{j,i,k} \right) - \sum_{i=0}^{N_Y} y_{i,k}, \quad \forall k \in \{1, 2\}, \end{aligned} \quad (6.6)$$

where $i_{\text{hist},k}$ is the history current from the other end, and m is the size of mode groups, as defined in [31]. i_k and v_k are currents and voltages from both ends of line, expressed in time domain. G denotes the admittance. N_H and N_Y represent the fitted order of \mathbf{H} and \mathbf{Y}_C , respectively. $h_{j,i,k}$ and $y_{i,k}$ are the state variables derived from the fitted rational functions. Equation (6.6) can be cast onto an equivalent circuit, as shown in Fig. 6.3. The coupling between two ends of the transmission line is enabled through the history currents, which represent the currents transmitted from the other end after a certain time delay. The circuit interface in Fig. 6.3 is used to represent the transmission lines in the MTDC-AC grid.

6.3.3 Generator and Transformer Modelling

The basic dynamics of a symmetrical, three-phase synchronous generator are derived based upon the physical principles within and between different windings using Kirchhoff's, Faraday's, Newton's laws, and Park transformation. The detailed derivation can be found in [25, 36] and are not repeated here. The set of differential-algebraic equations (DAEs)

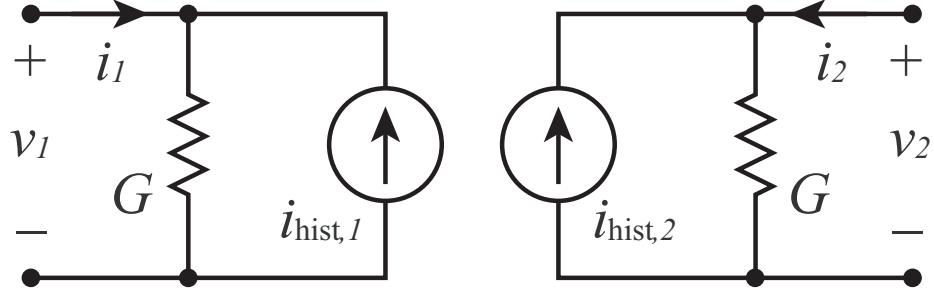


Figure 6.3: Time domain transmission line equivalent circuit.

describing the dynamics is discretized using a combination of forward Euler and backward Euler based on stiffness in the system, given by

$$(\mathbf{M} - \mathbf{A}h) \cdot \mathbf{x}[k] = \mathbf{M} \cdot \mathbf{x}[k-1] + h\mathbf{B}\mathbf{u}[k] \quad (6.7)$$

where

$$\mathbf{x} = \{\psi_d, \psi_q, E'_q, \psi_{1d}, E'_d, \psi_{2q}, I_d, I_q\}'$$

$$\mathbf{u} = \{V_d, V_q, E_{fd}\}'$$

The matrices $\mathbf{A}, \mathbf{M}, \mathbf{B}$ are coefficient matrices derived from the generator dynamic equations.

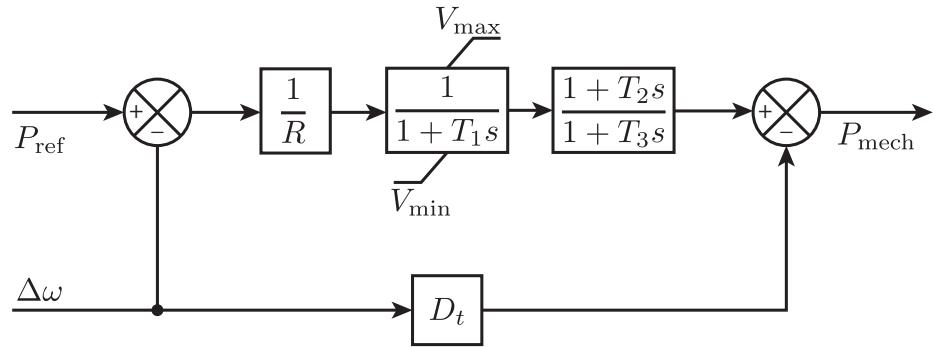


Figure 6.4: Time-domain transmission line equivalent circuit.

The governor model of the generator is shown in Fig. 6.4 using the steam turbine

governor model (TGOV1) [98], representing the turbine-governor droop and motions of steam valve and reheater in multiple stages.

The transformer is modelled using the classical non-ideal equivalent circuit [25] whose detailed derivation is not repeated here. Combined with synchronous generator models and transmission line models, the electromagnetic transient of AC-side system is captured in the proposed real-time platform.

6.4 Implementation of CPU & GPU Co-simulation Platform

The tasks of real-time computation of the cross-continental MTDC-AC grid, as shown in Fig. 6.1, is partitioned into two parts, driven by CPUs and GPUs, respectively.

Compared to CPUs, which are good for serial processing with low latency, the GPUs, composed of thousands of cores running at lower frequency, are capable of handling massive amount of threads simultaneously. As a result, GPUs are good for tasks which can be broken into a large number of mutual independent parts. These parts can be processed at a much higher speed in parallel.

6.4.1 The Platform Architecture

The GPU adopted in this work is Nvidia’s Tesla P100, using Pascal GP100 architecture [43]. Equipped with 3584 CUDA cores and 16 Gigabytes of HBM2 memory, P100 delivers 5.3 TFLOPS FP64 and 10.6 TFLOPS FP32 performance.

The GPU device is connected to the host system via PCI-Express (PCIe) bus, as shown in Fig. 6.5. Data is exchanged between main CPU memory and global GPU memory through this connection. The minimum computation unit on a GPU is a CUDA core, on which a parallel thread is executed. These cores are organized into groups called warps, with a fixed size of 32 cores. The same instruction is executed in parallel by all CUDA cores within the same warp. Above this level of architecture is the streaming multiprocessor. There are 56 streaming multiprocessors in total in a P100. The streaming multiprocessor

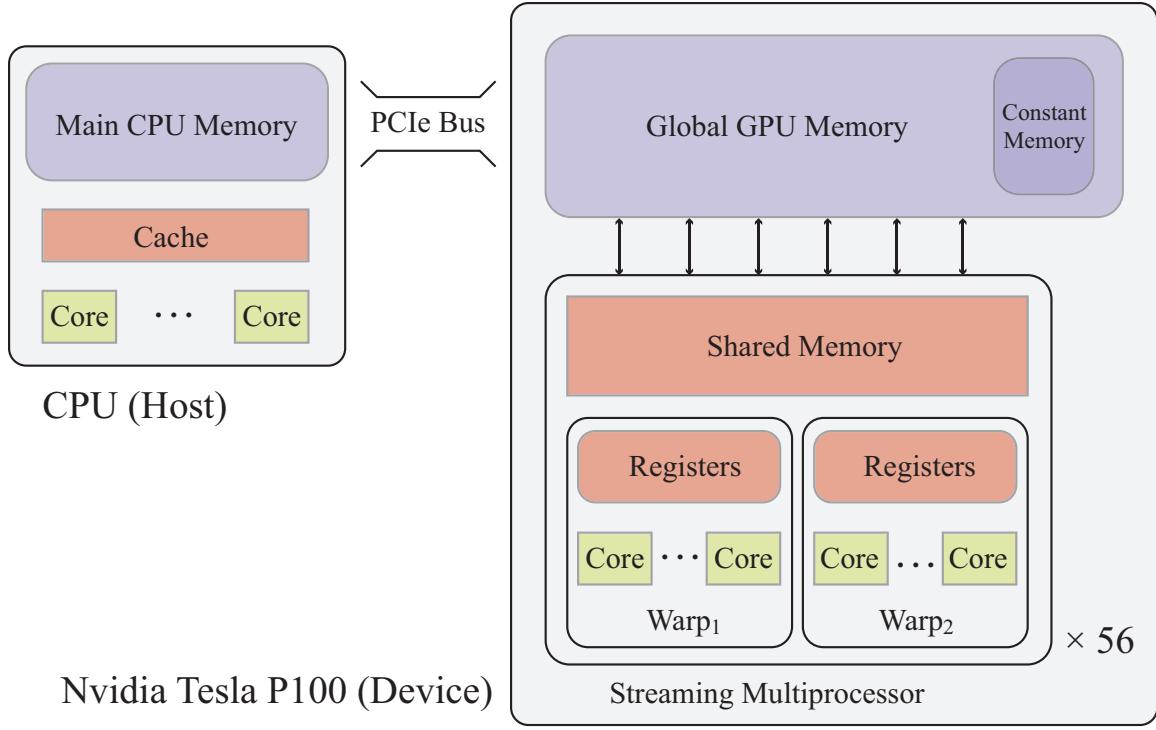


Figure 6.5: Architecture of CPU and GPU simulation platform.

incorporates 2 warps, or 64 CUDA cores equivalently. There are 64 Kilobytes of shared memory allocated to each streaming multiprocessor. The shared memory is accessible from the CUDA cores within the same streaming multiprocessor, at a much higher speed (less than ten clock cycles) compared to global GPU memory access (a few hundreds of clock cycles). The optimum use of this on-chip shared memory is critical in the optimization of MMC and transmission line parallelism.

6.4.2 Implementation of the MMCs on the GPU

The major step of the GPU acceleration design is the partition of simulation algorithm based on its execution logic. It is preferable to move the parallel-friendly part to the GPU, while keeping the heavily-serial part in the CPU. However, since the CPU and GPU programs have to exchange data within each simulation step, the communication latency should also be considered. Therefore, this partition should be well balanced to take advan-

tage of the computational power of both the CPU and GPU and hide the communication latency as much as possible.

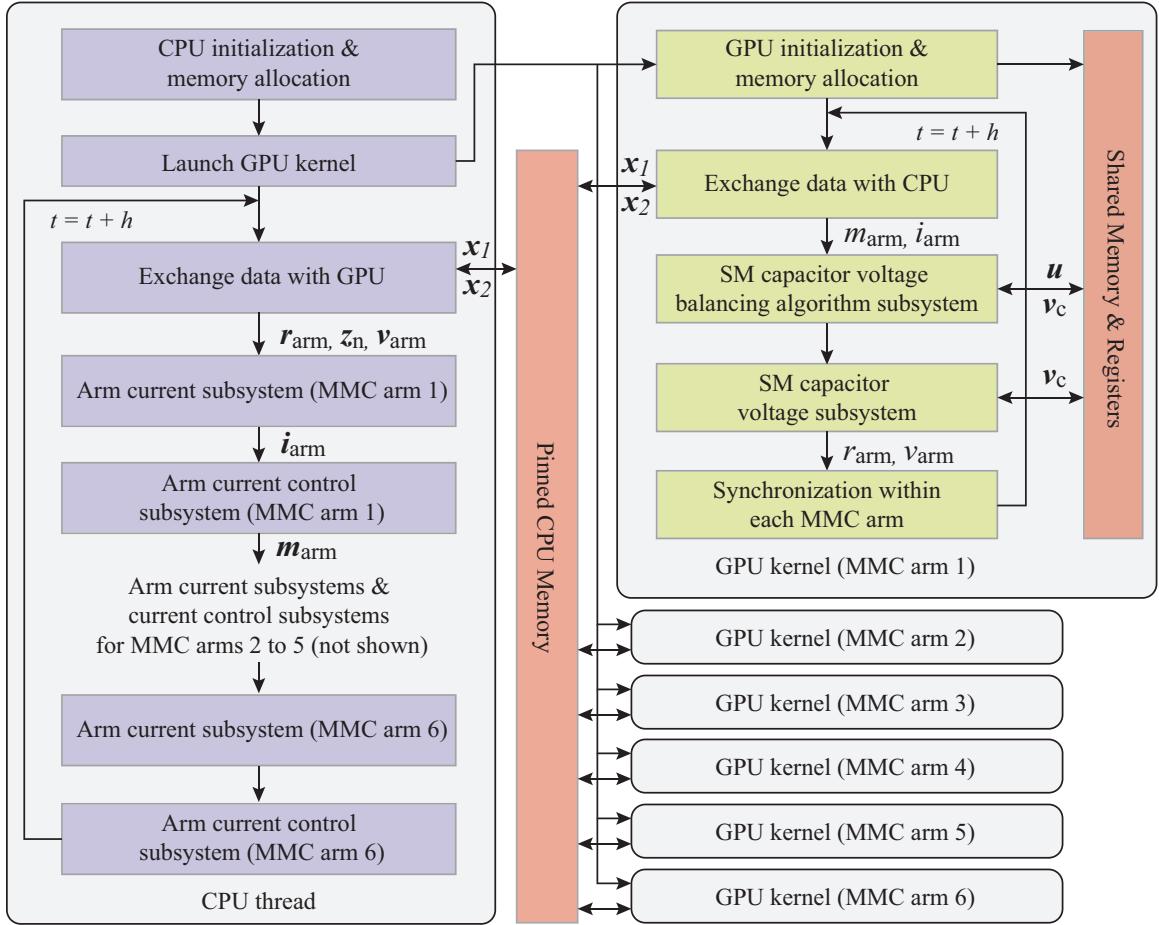


Figure 6.6: Summary of MMC hybrid simulation algorithm.

The CPU implementations of the MMC simulation and control algorithms have been described in [35, 40]. The simulation and control of the MMC within each time step can be divided into four subsystems:

1. Arm current control subsystem, which comprises qd AC-side current control and qd circulating current control of the second- and fourth-order harmonics.
2. SM capacitor voltage balancing algorithm subsystem, which calculates the gating signals for each IGBT in the MMC.

3. SM capacitor voltage subsystem, which solves the dynamics given in (6.3).
4. Arm current subsystem, which computes the currents of each arm based on DAEs provided in (6.1) and (6.2).

Among the four aforementioned subsystems, SM capacitor voltage balancing algorithm and SM capacitor voltage subsystem are suitable to be computed on the GPU. This separation is presented in Fig. 6.6. Assuming the number of SMs in each arm is N (400 in this work), six persistent GPU kernels are launched onto streaming multiprocessors, one for each arm. In each step h , arm current control subsystem and arm current subsystem are computed in series in the CPU while the other two subsystems are calculated in parallel on the GPU. In each GPU kernel, the gating signals \mathbf{u} (400 integer values) and SM capacitor voltages \mathbf{v}_c (400 double precision values) are stored in the shared memory for each arm. Together with other variables that are not as large as \mathbf{u} and \mathbf{v}_c , less than 10 Kilobytes of shared memory is allocated for each kernel, which is well below the limit. The GPU kernels are launched to available streaming multiprocessors and scheduled into warps for execution.

Algorithm 3: Parallel SM capacitor voltage balancing

```

Input:  $m_{\text{arm}}$ ,  $i_{\text{arm}}$ ,  $\mathbf{v}_c$ 
Output:  $\mathbf{u}$ 
Mask out unrelated SMs and convert  $\mathbf{v}_c$  if needed
 $Warp_{\text{modified}} \leftarrow -1$  /* initialize warp index */
Compute  $\Delta N_{\text{on}}$  for current step
while  $\Delta N_{\text{on}} > 0$  do
  if  $Warp_{\text{modified}} = -1$  then /* first run */
    Find top one within each warp
    Copy top one to shared memory
  else /* only re-calculate the modified warp */
    Find top one within warp of index  $Warp_{\text{modified}}$ 
    Update top one in shared memory
  end
  Find top one in shared memory (on thread 0)
   $\Delta N_{\text{on}} \leftarrow \Delta N_{\text{on}} - 1$ 
end

```

For each MMC arm, the SM capacitor voltage balancing algorithm [40, 99] first calculates the minimum number of SMs that should change their states within this step, either turning ON or OFF, given the modulation index of this arm, m_{arm} . One additional SM may change its state if the corresponding SM capacitor voltage exceeds a pre-set value. The number of SMs changing their states is denoted as ΔN_{on} . Then, based on the direction of the arm current i_{arm} , the first ΔN_{on} SMs with either the maximum or minimum capacitor voltages are selected and their states are changed and saved into variable \mathbf{u} in the shared memory. Majority part of the balancing algorithm computation is performed to find the top ΔN_{on} SMs with extreme capacitor voltages. Finding the minimum voltages can be converted to finding the maximum with a sign change. Therefore, this problem can be simplified into finding the top one SM with maximum capacitor voltage, and repeating this process for ΔN_{on} times, as shown in Algorithm 3. To find the top one among all N SMs, these N capacitor voltages are partitioned into groups of 32. Each group is scheduled to a warp, within which the top one of the 32 voltages can be calculated efficiently using CUDA warp-level primitives [100]. These top one candidates ($\lceil 400/32 \rceil = 13$ double precision values) are copied to the shared memory by the first thread in each warp. Then, the global maximum can be picked from these candidates with another run of warp-level maximum selection on one of the warps. Instead of simply rerunning the same program multiple times, on subsequent runs other than the very first one, the same operations can be performed only on the warp where the modified SM on previous run is located. Over 50% speed up has been achieved using this optimization technique in a test with $\Delta N_{\text{on}} = 3$.

Another parallel part on the GPU is the SM capacitor voltage subsystem, which updates v_c and calculates equivalent arm resistance r_{arm} and arm voltage v_{arm} . The most time consuming step in this subsystem is to compute the summation of all SM capacitor voltages within an arm. This can be solved by parallel reduction using the warp-level primitives, based on the same idea implemented on the SM capacitor voltage balancing algorithm.

With the computation of four subsystems distributed onto the CPU and GPU, the data

generated by each partition should be exchanged by the end of each simulation step. This communication between the CPU and the GPU is performed using the mapped pinned memory, as shown in Fig. 6.6, where a pinned allocation of CPU memory is created and two pointers are generated for host and device separately. On launching the GPU kernel, the device pointer is passed to the GPU, which can be used to exchange data with the CPU efficiently. \mathbf{x}_1 and \mathbf{x}_2 are data sent from the GPU and CPU, respectively. \mathbf{x}_1 consists of \mathbf{r}_{arm} and \mathbf{v}_{arm} , \mathbf{x}_2 consists of \mathbf{m}_{arm} , \mathbf{i}_{arm} , and AC-side voltages \mathbf{v}_s . A ping-pong style communication [100] is applied where two additional variables are used to indicate successful completion of read/write on the other side. Once the indicators are verified, data will be exchanged and indicators will be reset. Both CPU and GPU will run in parallel until the next communication is issued.

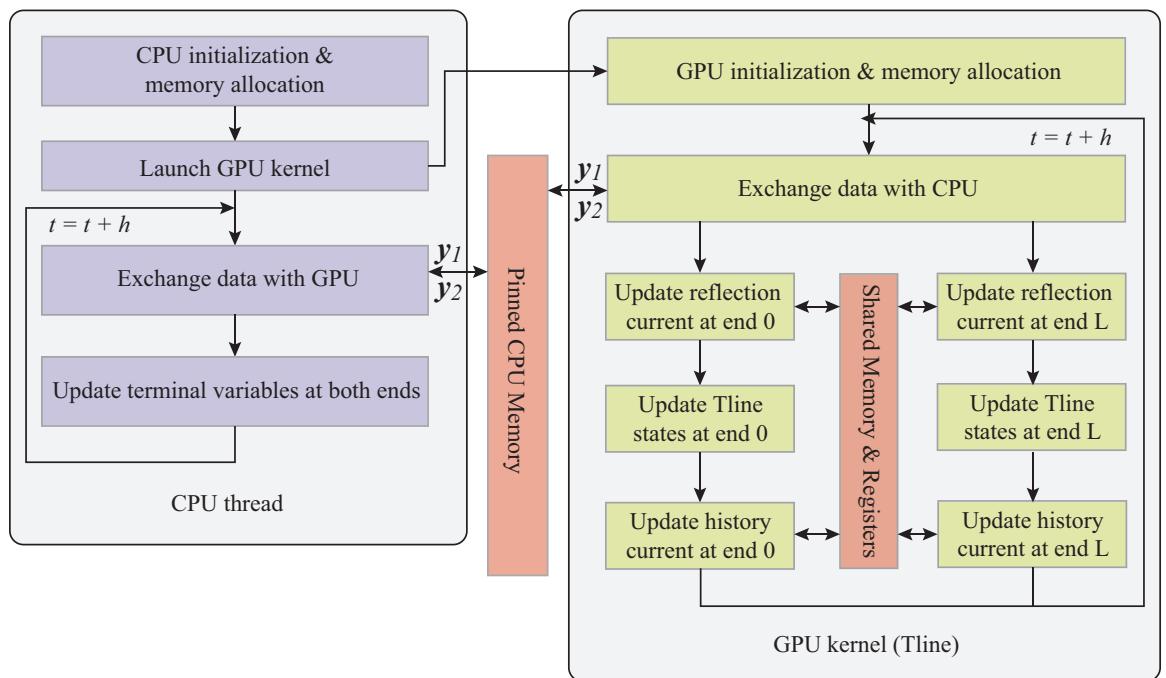


Figure 6.7: Summary of the transmission line simulation algorithm.

6.4.3 Implementation of the Transmission Line on the GPU

The simulation of the transmission line involves extensive operations of matrices. These matrix-related tasks can be better performed on the GPU given its parallelism potential. The simulation algorithm, partitioned on both CPU and GPU, is summarized in Fig. 6.7. Using the same idea as in the MMC simulation, a persistent GPU kernel is launched for each transmission line. The calculation of reflection and history currents is performed on the GPU while the terminal variables are updated on the CPU. The data exchange is implemented using the same strategy as in the MMC simulation.

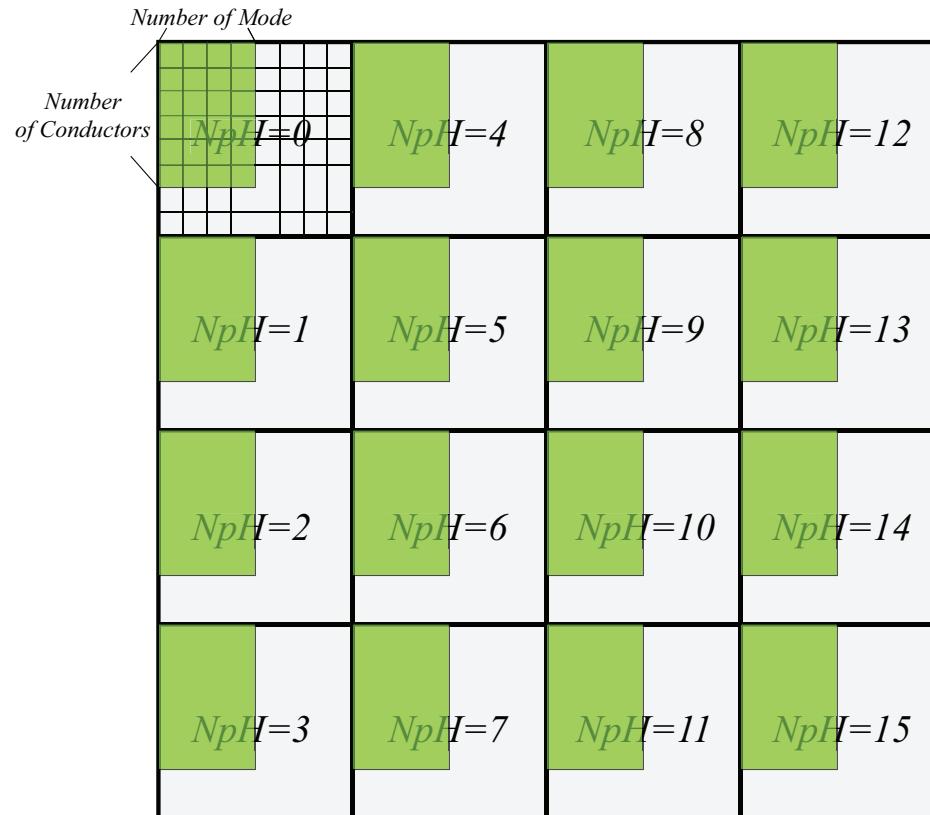


Figure 6.8: Distribution of transmission line variables across a thread block.

The reflection currents on both ends of the line can be calculated based on (6.6). However, these currents will be propagated to the other ends after a certain delay, which is determined by the length of the line. Therefore, a buffer is allocated in the shared memory

to store the reflection currents and a variable index pointer is used to function as the delay. As described in Section 6.3, \mathbf{Y}_c and \mathbf{H} matrices are fitted using time-domain rational functions. Assuming the number of poles for \mathbf{Y}_c and \mathbf{H} are $N_p Y_c$ and $N_p H$, respectively, the poles, residues, and constants for the fittings can be packed into 2- and 3-dimensional matrices [92] and have to be allocated in the shared memory. Another sets of variables allocated in the shared memory are the states variables used in discretization of time-domain expressions of \mathbf{Y}_c and \mathbf{H} [31, 97]. The size of these shared memory variables are largely dependent on the number of conductors in this transmission line. An estimate of 5464, 9264, and 25752 bytes are to be allocated for lines with two, three, and six conductors, respectively. The shared memory space in a streaming multiprocessor is large enough for a typical transmission line.

The matrix-related operations in transmission line simulation include matrix-vector multiplication and one- and 2-dimensional slicing of higher dimensional matrices. To take a better advantage of the parallel capability in the GPU, the computation of these matrices are distributed to the CUDA cores, as shown in Fig. 6.8. Each thread block (consisted of 32×32 threads) is evenly divided into 16 parts, which is beyond the typical number of poles obtained in the fitting. The green area indicates the active CUDA cores. Warp-level primitives are easier to be adopted given the proposed data assignment.

6.4.4 Complete Setup

As shown in Fig. 6.1, there are three MMCs, two DC transmission lines, three generators, transformers, and AC transmission lines in the system. The complete simulation platform is depicted in Fig. 6.9.

On the GPU, 18 kernels are launched for each arm in the three MMCs, while 5 kernels are launched for the 5 transmission lines. The kernel-to-kernel communication is performed using the global GPU memory. Data exchange between the CPU and GPU is implemented using the pinned CPU memory, as introduced in previous sections, using a dedicated CPU

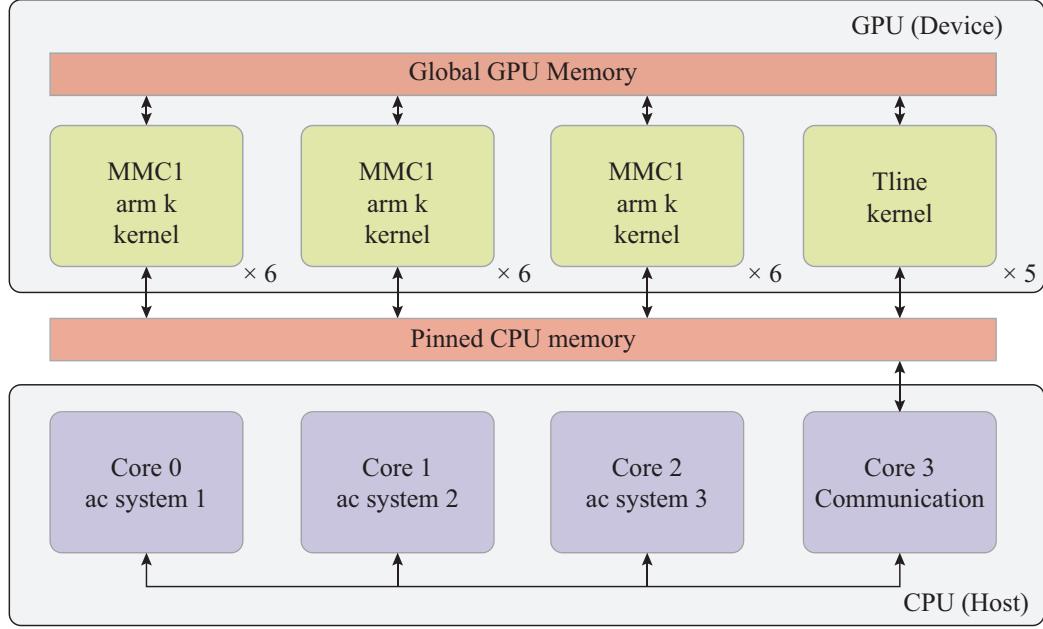


Figure 6.9: Summary of the complete simulation platform.

core. The three other CPU cores are used to compute the AC system dynamics including generators and transformers. These four CPU cores are executed in parallel and communicated through Message Passing Interface (MPI).

6.5 Results and Evaluation

The proposed CPU & GPU co-simulation platform has been tested on the demonstration three-terminal DC network shown in Fig. 6.1. The computed results are compared to the reference system in the PSCAD software under two cases, i.e., normal operation and DC fault propagation, to validate the accuracy and real-time performance of the proposed platform.

6.5.1 Comparison with Reference Results

The simulator is first compared to the PSCAD benchmark system under normal operation where an active power dispatch command of 100 MW is applied to MMC2 and equally distributed to MMC1 and MMC3. The comparison of active power P_{out} and DC terminal

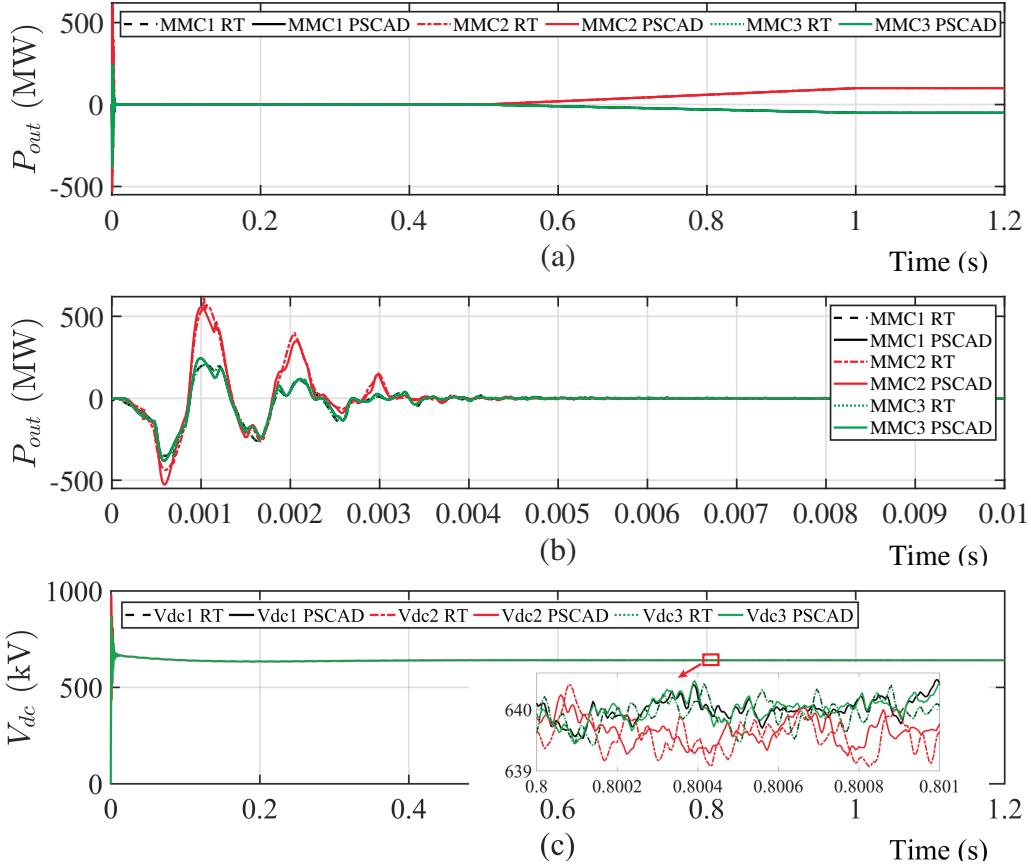


Figure 6.10: Comparison of results simulated by real-time platform and PSCAD benchmark: (a) active power P_{out} , (b) zoomed-in view of active power, and (c) DC terminal voltages V_{dc} .

voltages V_{dc} are presented in Fig. 6.10. The simulation error of the proposed real-time platform is less than 1% as compared to the reference results.

The comparison is also conducted under fault scenario where a P2P DC-side fault is introduced in the middle of DC cable between MMC1 and MMC2. The DC terminal voltage from terminal 1 is shown in Fig. 6.11. It is verified that the transients and propagation of travelling waves on DC cables are fully captured in the proposed real-time platform.

Table 6.1: Performance of 1 s CPU & GPU co-simulation

CPU	GPU	Time Spent
IBM POWER8	NVIDIA Tesla P100	0.94 s
Intel Core i5	NVIDIA GeForce GTX 1080 Ti	0.97 s

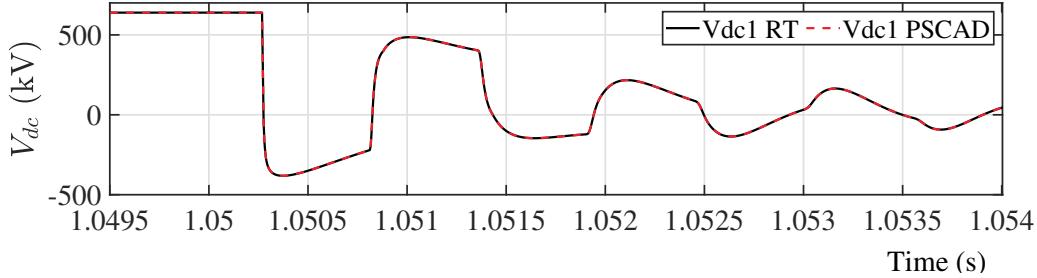


Figure 6.11: Comparison of results simulated by real-time platform and PSCAD benchmark under DC fault.

6.5.2 Evaluation of Real-time Performance

The proposed GPU-accelerated simulation platform has been deployed on two hardware setups, one commercial line setup (Tesla P100) and one consumer line setup (GeForce GTX 1080 Ti), as shown in Table 6.1. Both these hardware platforms achieve faster than real-time simulations at scales of 1 s. The result does not show any apparent difference between the performance of commercial and consumer lines.

The GPU-based platform can simulate up to 1,000 SMs/arm per streaming multiprocessor with a time-step of 5 μ s in real-time, compared to 425 SMs/arm/core using DSP [40] and the best CPU implementation of 230 SMs/arm per CPU core given the same time step [39, 61, 62]. Compared to the CPU setup, which is hard to be scaled vertically due to the limitation on the number of cores, the GPU-based platform can be scaling horizontally by adding more GPUs in parallel. Additionally, considering the per unit cost metric defined as the number of SMs simulated per arm divided by the simulation time-step, the cost of the GPU-based implementation is only 1/2 and 1/10 of the CPU- and FPGA-based platform. These advantages greatly benefit the real-time simulation of large-scale MTDC systems.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

This research focuses on developing an end-to-end approach to address the challenges in MTDC grid protection and to enable the practical applications of such protection approach. The contributions are summarized as follows:

1. Propose a time-domain method to analyse the fault characteristics during DC-side faults in MTDC grids. The proposed method, based on travelling waves, (i) provides a sound representation of fault performance by considering all created travelling waves, (ii) introduces a new approach to estimate the reflection coefficients, and (iii) provides an approximation of the worst-case fault location. This method is applied to calculate the DC fault response and the performance metrics of DC circuit breakers.
2. Develop a design tool to determine the optimal parameters of DC circuit breakers based on the performance metrics, i.e., maximum overcurrent, maximum overvoltage, fault clearance time, and energy absorption in arresters. The optimized parameters are current limiting reactor, arrester rated voltage, and time delay of DC circuit breakers.
3. Propose a new control strategy, named sequential switching strategy, for DC circuit breakers to improve their transient performance during a DC fault interruption in MTDC grids. Compared to the conventional switching strategy, the proposed one, which sequentially trips the breaking modules within a circuit breaker, reduces the peak fault current and overvoltage as well as fault clearance time.

4. Propose a hybrid primary fault detection algorithm for the MTDC grids. The proposed primary detection algorithm provides the following advantages over the existing methods: i) P2P, P2G, and external DC fault are covered; ii) various fault locations and fault impedances are covered; iii) the system is robust to noisy input signals.
5. Propose a cost-effective high-performance real-time EMT simulation platform for large-scale cross-continental MTDC grids based on the CPU & GPU co-simulation architecture. The proposed simulation platform: i) incorporates detailed EMT models of all components of an MTDC-AC grid within a single platform. This setup provides a complete simulation solution to capture fast transient signals required for high-bandwidth controller design [30, 44] and protection studies, without any compromise; ii) implements the first GPU-based simulation architecture and corresponding algorithms for MTDC-AC grids with real-time performance at scales of 1 s; iii) is highly-efficient and balances the high utilization of GPU resources and low latency required for the simulation; and iv) outperforms the existing CPU- and DSP/FPGA-based simulators in terms of its higher scalability on large-scale MTDC-AC grids and superior price-performance ratio on the hardware..

7.2 Future Work

The research presented in this dissertation can be improved from the following aspects in the future:

1. The commercialization of practical DC circuit breakers for MTDC applications need to be pushed forward. This will require complete tests and evaluations of the cost, reliability, robustness, and performance of such breakers.
2. The sequential tripping strategy of DC circuit breakers can be further optimized with respect to its speed and energy balancing performance. It is also important to extend

its application to cover different types of mechanical switches.

3. The protection relaying algorithms need to be further improved to address the cyber security challenges within MTDC grids.
4. The CPU & GPU co-simulation platform needs to be optimized to reach hard real-time criteria. It can also be extended to a Hardware-in-the-loop (HIL) simulation platform to be applied to more use cases.
5. The protection of MTDC grids with different MMC technologies needs to be explored. Some of the MMCs have embedded fault blocking capabilities such as MMCs with full-bridge SMs [101, 102] while the rest MMCs can not block faults but are protected by DC circuit breakers.

Appendices

APPENDIX A

PROOF OF THE EQUIVALENCE OF G_K AND G_K^M

The variables g_k^m and g_k in (5.5) and (5.7) are defined as

$$g_k^m = \max_{1 \leq j \leq k} S_j^k \quad (\text{A.1})$$

$$g_k = \max\{0, g_k^m\} = \max\{0, \max_{1 \leq j \leq k} S_j^k\} \quad (\text{A.2})$$

First, it is to be proved that when an alarm is triggered using g_k^m , an alarm is also triggered using g_k at the same time. Given the alarm time

$$t_a = \min\{k : g_k^m \geq h\} = \min\{k : \max_{1 \leq j \leq k} S_j^k \geq h\} \quad (\text{A.3})$$

where h is a positive threshold.

Equivalently, the following statements hold:

$$\begin{aligned} 0 < h \leq g_{t_a}^m, \\ g_k^m < h, k \in \{0, 1, \dots, t_a - 1\} \end{aligned} \quad (\text{A.4})$$

Therefore, based on the definition of g_k , it is deduced that

$$\begin{aligned} g_k &= \max\{0, g_k^m\} \\ &= \begin{cases} g_{t_a}^m \geq h, \text{if } k = t_a \\ g_k^m < h, \text{if } 0 < g_k^m < h, k \in \{0, 1, \dots, t_a - 1\} \\ 0 < h, \text{if } g_k^m \leq 0, k \in \{0, 1, \dots, t_a - 1\} \end{cases} \end{aligned} \quad (\text{A.5})$$

which means that g_k sets the same alarm time as g_k^m . Next, it is to be proved that whenever g_k triggers an alarm at t_a , g_k^m triggers one as well. This condition can be expressed as

$$\begin{aligned} 0 < h \leq g_{t_a}, \\ 0 \leq g_k < h, k \in \{0, 1, \dots, t_a - 1\} \end{aligned} \tag{A.6}$$

Thus, the value of g_k^m is

$$\begin{aligned} 0 < h \leq g_{t_a} = g_{t_a}^m, \\ g_k^m \leq g_k < h, k \in \{0, 1, \dots, t_a - 1\} \end{aligned} \tag{A.7}$$

which means that g_k^m sets an alarm at t_a as well.

APPENDIX B

DERIVATION OF THE RECURSIVE FORM OF G_K

Considering the non-negative definition of g_k in (5.7), at every time step k , there are two cases, i.e., $g_{k-1} = 0$ and $g_{k-1} > 0$. $g_{k-1} = 0$ implies that the maximum summation of log-likelihood ratio from a certain time step j to the last time step $k - 1$ is either negative or zero. Thus, the newly calculated log-likelihood ratio at current step determines the value of g_k . This condition can be expressed as

$$g_k = \max\{0, \ln \frac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)}\} \quad (\text{B.1})$$

If $g_{k-1} > 0$, the maximum summation at step k can be calculated by summing two parts, i.e., the newly calculated log-likelihood ratio at current step k and the maximum value from last step $k - 1$. This relationship can be written as

$$g_k = \max\{0, g_{k-1} + \ln \frac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)}\} \quad (\text{B.2})$$

Equations (B.1) and (B.2) can be merged into one expression, which is the recursive form of g_k provided in (5.8).

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