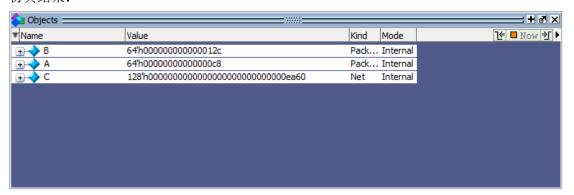
## 64\_bit\_multiplier

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1. 写出 64 位乘法器的结构图或设计思想 设计思想:利用 booth 编码产生部分积,然后累加得到最后的结果。 仿真结果:



结果是 200 x 300=60000 时延报告:

Point	Incr	Path
input external delay	0.00	0.00 f
in1[0] (in)	0.00	0.00 f
U1113/Y (INVX8)	0.03	0.03 r
U1115/Y (NAND2X4)	0.07	0.10 f
U1026/Y (INVX8)	0.08	0.19 r
U1027/Y (NAND2X2)	0.08	0.26 f
U1034/Y (INVX4)	0.09	0.35 r
U1035/Y (AND2X4)	0.19	0.55 r
U1037/Y (XOR2X4)	0.22	0.76 f
U266/Y (BUFX12)	0.16	0.92 f
U275/Y (OAI21X4)	0.12	1.04 r
U1068/S (ADDFHX4)	0.47	1.51 f
U725/CO (ADDFHX2)	0.30	1.81 f
U594/S (ADDFHX2)	0.32	2.13 r
DP_OP_674J1_296_9245/U2446/S (ADDFHX2)	0.42	2.54 r
DP_OP_674J1_296_9245/U2439/S (ADDFHX2)	0.32	2.86 r
U370/CO (ADDFHX4)	0.43	3.29 r
U11232/CO (ADDFHX4)	0.42	3.71 r
U11779/CO (ADDFHX4)	0.45	4.16 r
U11723/S (ADDFHX4)	0.36	4.52 f
U277/Y (NOR2X4)	0.13	4.65 r
U278/Y (OAI21X4)	0.08	4.73 f
U281/Y (A0I21X2)	0.13	4.86 r
U1098/Y (OAI21X2)	0.13	4.99 f
U1099/Y (A0I21X4)	0.14	5.13 r
U1139/Y (OAI21X4)	0.11	5.24 f
U1101/Y (INVX4)	0.09	5.33 r
U1102/Y (INVX4)	0.09	5.42 f
U1109/Y (A0I21X1)	0.16	5.58 r
U1112/Y (XOR2X1)	0.25	5.83 r
out[124] (out)	0.00	5.83 r
data arrival time		5.83
max_delay	1.00	1.00
output external delay	0.00	1.00
data required time		1.00
data required time		1.00
data arrival time		-5.83
slack (VIOLATED)		-4 <b>.</b> 83

## 面积报告:

```
Number of ports: 256
Number of nets: 22491
Number of cells: 20706
Number of references: 154

Combinational area: 515139.610666
Noncombinational area: 0.000000
```

## 功耗报告:

```
Global Operating Voltage = 1.62
Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.0000000pf
Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)
Leakage Power Units = 1pW

Cell Internal Power = 206.7939 mW (70%)
Net Switching Power = 87.2528 mW (30%)

Net Switching Power = 294.0467 mW (100%)

Cell Leakage Power = 59.2239 uW
```