JINGSONG CHEN

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Department of Computer Science & Engineering ⋄ The Chinese University of Hong Kong

RESEARCH INTERESTS

- Logic synthesis & timing optimization
- Physical design of VLSI circuits
- Machine learning-related topics in physical design

EDUCATION

The Chinese University of Hong Kong, NT, Hong Kong SAR Aug. 2017 – July 2021
- Ph.D. student, Department of Computer Science & Engineering.
- Dissertation: "Intelligent Chip Layout Synthesis and Analysis "
- Advisor: Prof. Evangeline F.Y. Young
- (CSRankings: CUHK CSE ranked 1st in the field of Design Automation)

Zhejiang University, Hangzhou, P.R. China Sep. 2013 – July 2017
- B.Eng., Computer Science and Technology. (GPA 88.13/100)
- Dissertation: "Research on StarCraft AI Based on Deep Reinforcement Learning"
- Advisor: Prof. Shijian Li

EXPERIENCE

Principal Engineer | Huawei Technologies Co., Ltd. Oct. 2021 – Present, Shenzhen, China
- Accelerator Technology Dept.
- Logic synthesis, timing optimization, AIG-based Optimization

Software Engineer Intern | Cadence Design Systems, Inc. May 2019 – Oct. 2019, San Jose, CA, USA
- Global Routing Team
- One ICCAD paper on Global Routing Enhancement with Deep Learning
- Advisor: Dr. Dennis Huang

Technical Intern | Synopsys, Inc. June 2018 – Aug. 2018, Shanghai, China
- SEG Proteus Geometry Engine Team
- One SPIE paper on Layout Pattern Detection
- Advisor: Dr. James Shiely

SELECTED AWARDS AND HONORS

Pengcheng Talent Program – Silver Card	Shenzhen Gov.	2024
First Place Award at Contest on Routing with Cell Movement	ICCAD	2020
Young Fellow Award	DAC	2020
First Place Award at Contest on Wafer-Scale Deep Learning Accelerator Placement (Leader)	ISPD	2020
First Place Award at Contest on Initial Detailed Routing	ISPD	2019
First Place Award at Contest on Obstacle-Aware On-Track Bus Routing (Leader)	ICCAD	2018
Second Place Award at Contest on Initial Detailed Routing	ISPD	2018
Full Postgraduate Studentship	CUHK	2017–2021

TECHNICAL SKILLS

Languages	C/C++, Python, Shell, Tcl, LaTeX
Operating Systems	Linux/UNIX
Tools	Synopsys® Design Compiler™, Cadence® Genus™, Cadence® Innovus™, Tensorflow

PUBLICATIONS

Summary
- IEEE TCAD: CCF-A, top journal in EDA, 2
- DAC: CCF-A, top conference in EDA, 2
- ICCAD: CCF-B, top conference in EDA, 5

Journal Papers

[J2] **Jingsong Chen**, Jian Kuang, Guowei Zhao, Dennis Huang, and Evangeline F.Y. Young, "PROS2.0: a Plug-in for Routability Optimization applied in the State-of-the-art Commercial EDA Tool Using Deep Learning" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), 2022.

[J1] Bentian Jiang*, **Jingsong Chen***, Jinwei Liu, Lixin Liu, Fangzhou Wang, Xiaopeng Zhang, and Evangeline F.Y. Young, "CU.POKer: Placing DNNs on Wafer-Scale AI Accelerator with Optimal Kernel Sizing" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), 2021 (* co-first authors).

Conference Proceedings

[C10] Weihua Xiao*, Shanshan Han*, Yue Yang, Shaoze Yang, Cheng Zheng, **Jingsong Chen**, Tingyuan Liang, Lei Li, and Weikang Qian, "MiniTNtk: An exact synthesis-based method for minimizing transistor network", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), San Francisco, CA, USA, Oct. 29–Nov. 2, 2023 (* co-first authors).

[C9] Jinwei Liu, Xiaopeng Zhang, Shiju Lin, Xinshi Zang, **Jingsong Chen**, Bentian Jiang, Martin D.F. Wong, and Evangeline F.Y. Young, "Partition and place finite element model on wafer-scale engine", Annual Design Automation Conference (**DAC**), San Francisco, CA, USA, July 10–14, 2022.

[C8] Tingyuan Liang, **Jingsong Chen**, Lei Li, and Wei Zhang, "AutoCellLibX: Automated Standard Cell Library Extension Based on Pattern Mining", arXiv preprint arXiv:2207.12314, 2022.

[C7] Fangzhou Wang, Lixin Liu, **Jingsong Chen**, Jinwei Liu, Xinshi Zang, and Martin D.F. Wong, "Starfish: An Efficient P&R Co-Optimization Engine with A*-based Partial Rerouting", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Munich, Germany, Nov. 1–4, 2021.

[C6] **Jingsong Chen**, Jian Kuang, Guowei Zhao, Dennis Huang, and Evangeline F.Y. Young, "PROS: a Plug-in for Routability Optimization applied in the State-of-the-art Commercial EDA Tool Using Deep Learning", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Online, Nov. 2–5, 2020.

[C5] Bentian Jiang*, **Jingsong Chen***, Jinwei Liu, Lixin Liu, Fangzhou Wang, Xiaopeng Zhang, and Evangeline F.Y. Young, "CU.POKer: Placing DNNs on Wafer-Scale AI Accelerator with Optimal Kernel Sizing", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Online, Nov. 2–5, 2020 (* co-first authors).

[C4] Haocheng Li, Gengjie Chen, Bentian Jiang, **Jingsong Chen**, and Evangeline F.Y. Young, "Dr. CU 2.0: A Scalable Detailed Routing Framework with Correct-by-Construction Design Rule Satisfaction", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Westminster, CO, USA, Nov. 4–7, 2019.

[C3] **Jingsong Chen**, Jinwei Liu, Gengjie Chen, Dan Zheng, and Evangeline F.Y. Young, "MARCH: Maze Routing Under a Concurrent and Hierarchical Scheme for Buses", Annual Design Automation Conference (**DAC**), Las Vegas, NV, USA, June 2–6, 2019.

[C2] **Jingsong Chen**, James Shiely, and Evangeline F.Y. Young, "Fast Detection of Largest Repeating Layout Pattern", SPIE Advanced Lithography Conference, San Jose, CA, USA, Feb. 24–28, 2019.

[C1] Gengjie Chen, Chak-Wa Pui, Haocheng Li, **Jingsong Chen**, Bentian Jiang, and Evangeline F.Y. Young, "Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search", IEEE/ACM Asia and South Pacific Design Automation Conference (**ASPDAC**), Tokyo, Japan, Jan. 21–24, 2019.

RESEARCH EXPERIENCE

- Routing with Cell Movement
  - Develop a global routing engine which can also do cell movement to improve the routing solution.
- Wafer-Scale Deep Learning Accelerator Placement
  - Place DNNs on wafer-scale AI accelerator with optimal kernel sizing.
- Routing Enhancement with Deep Learning (research internship project in Cadence)
  - Enhance global routing with predicted routing congestion using fully convolutional network.
- Obstacle-Aware On-Track Bus Routing
  - Route buses among small obstacles while maintaining the same routing topology for all bus bits.
- Initial Detailed Routing
  - Initial detailed routing with realistic design rules faced by physical design practitioners in the industry.
- Detection of Largest Repeating Layout Pattern
  - Detect all the largest repeating patterns from a large flat layout in a reasonable runtime and memory.

GRADUATE-LEVEL COURSES

ENGG 5501: Foundations of Optimization
ENGG 5103: Techniques for Data Mining
CSCI 5160: Advanced Algorithms
CENG 5270: EDA for Physical Design of Digital System
ENGG 5781: Matrix Analysis Computations
CSCI 5150: Machine Learning Algorithm & Application
CSCI 5610: Advanced Data Structures