NUM3 sur owncloud

https://cloud-soc.lip6.fr/owncloud/public.php?service=files&t=19a15e3a0fff58e8b260c16fc6e54605

III – Exercice sur l'unité de contrôle

Patrick.Garda@upmc.fr

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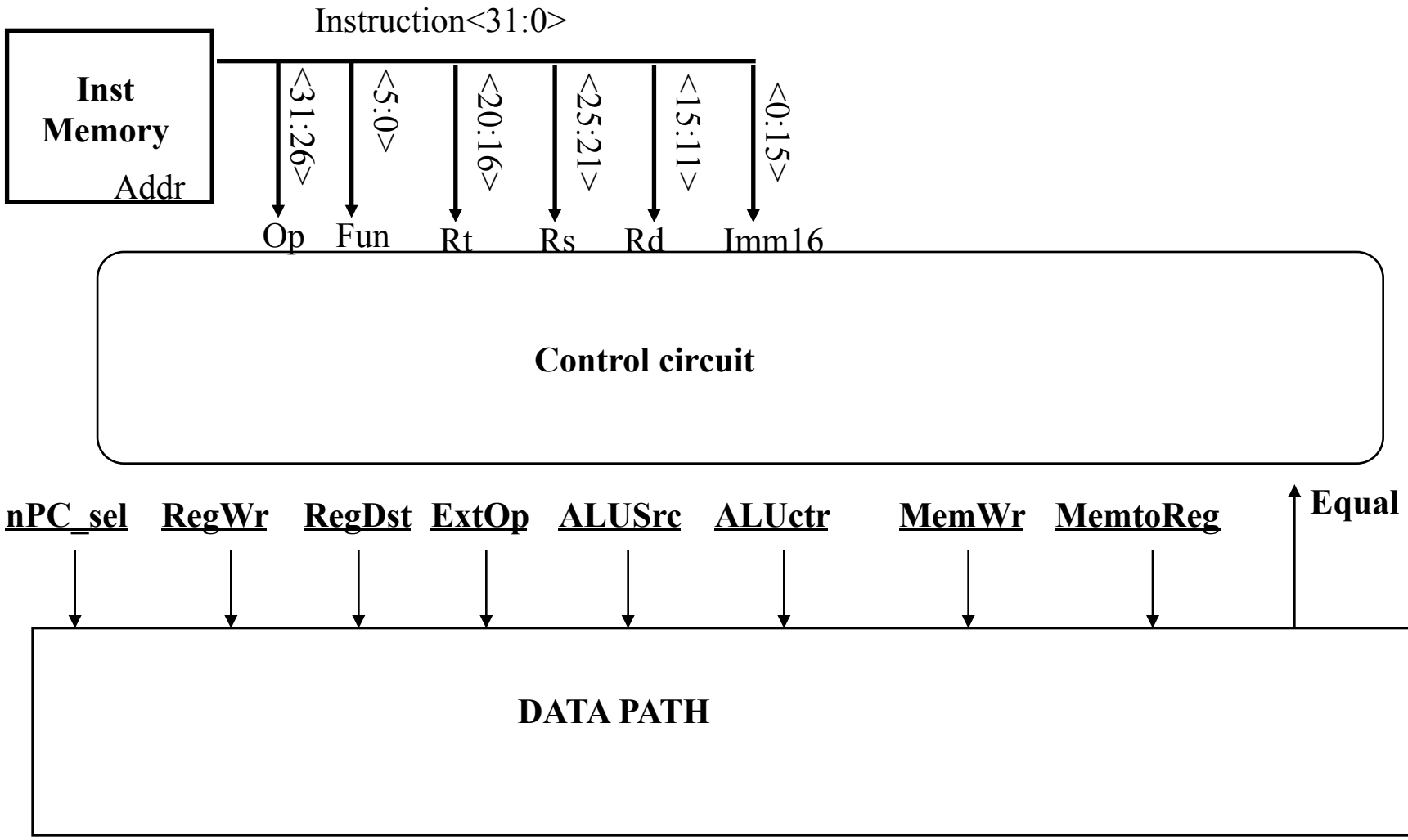
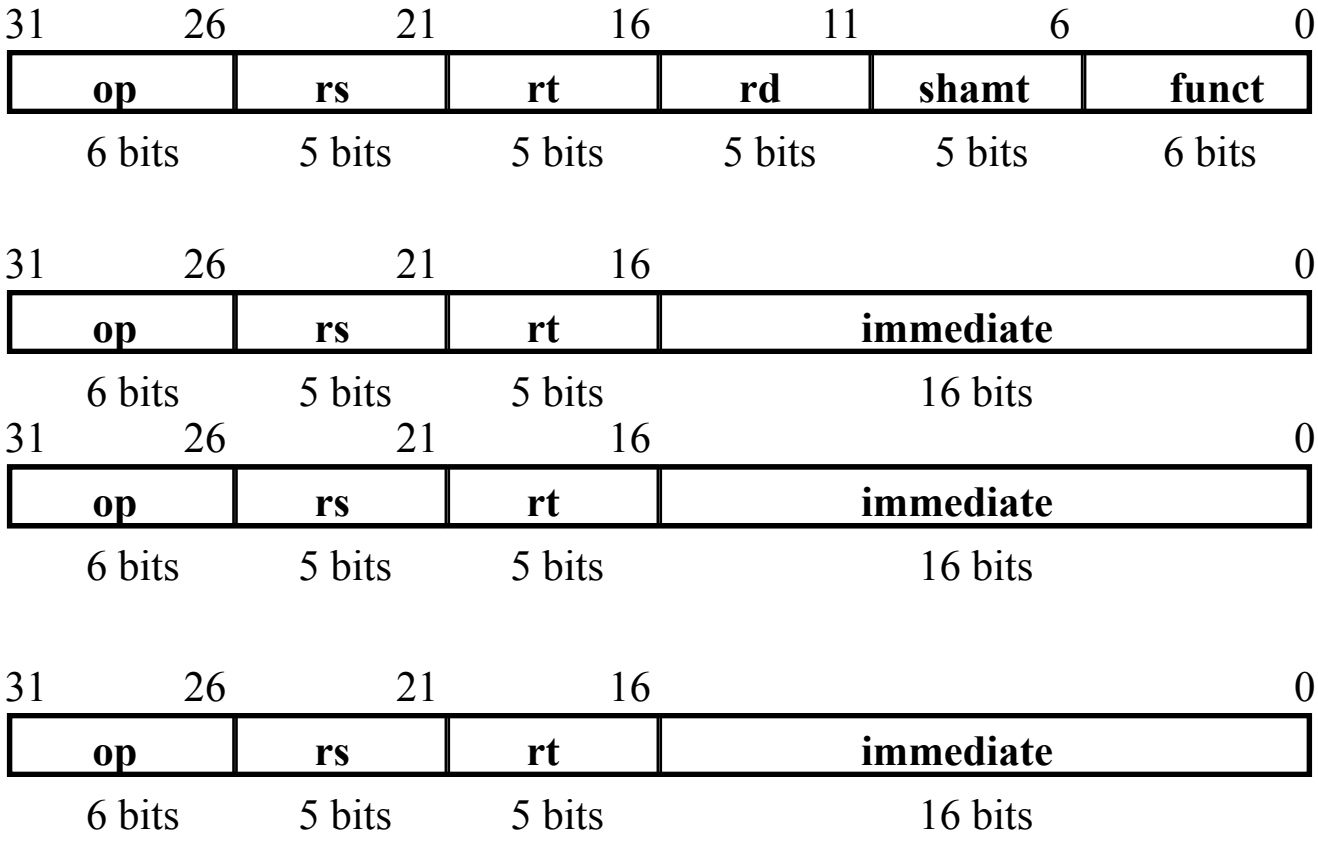
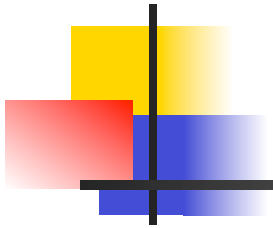
Control Unit



The MIPS-lite Subset

- add, sub, and, or, slt; e.g.
  - add rd, rs, rt
  - sub rd, rs, rt
- immediate; e.g.
  - ori rt, rs, imm16
- memory reference; e.g.
  - lw rt, rs, imm16
  - sw rt, rs, imm16
- branch:
  - beq rs, rt, imm16





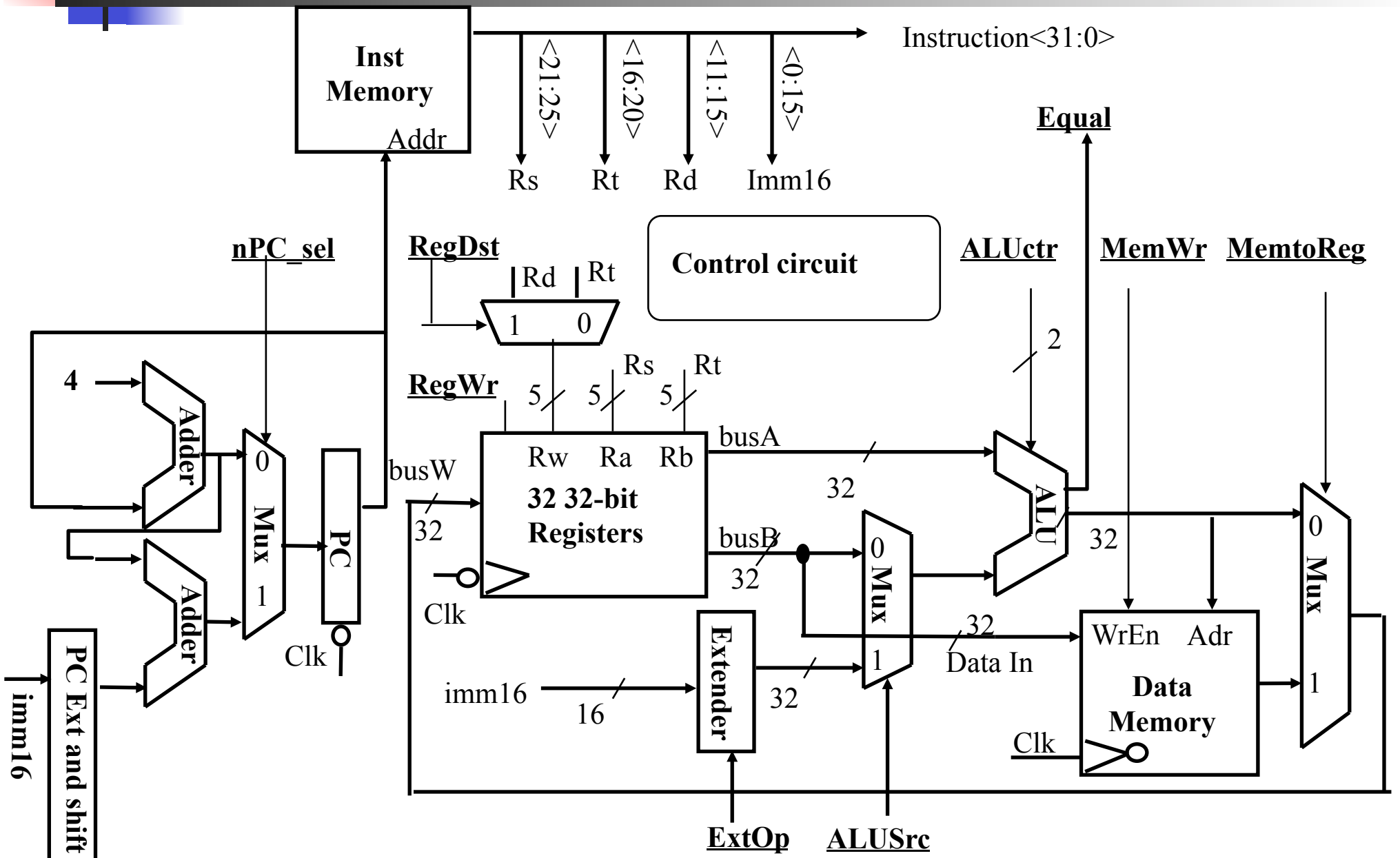
Instruction definition

op | rs | rt | rd | shamt | funct = MEM[PC]

op | rs | rt | Imm16 = MEM[PC]

inst	Register Transfers	
ADD	**R[rd] <– R[rs] + R[rt];**	**PC <– PC + 4**
SUB	**R[rd] <– R[rs] – R[rt];**	**PC <– PC + 4**
ORI	**R[rt] <– R[rs] | zero_ext(Imm16);**	**PC <– PC + 4**
LOAD	**R[rt] <– MEM[R[rs] + sign_ext(Imm16)];**	**PC <– PC + 4**
STORE	**MEM[R[rs] + sign_ext(Imm16)] <– R[rt];**	**PC <– PC + 4**
BEQ		**if (R[rs] == R[rt])** PC <- PC + 4 + (SignExt(imm16) x 4) **else** **PC <– PC + 4**

Single Cycle Datapath



Opcodes and control signal codes

# bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Instruction	OPCODE						rs					rt					?															
ADD	1	1	0	0	0	0	rs					rt					rd					shamt					funct					
SUB	0	1	0	0	0	0	rs					rt					rd					shamt					funct					
ORI	0	0	1	0	0	0	rs					rt					imm16															
LD	0	0	0	1	0	1	rs					rt					imm16															
ST	0	0	0	1	0	0	rs					rt					imm16															
B	0	0	0	0	1	0	rs					rt					imm16															

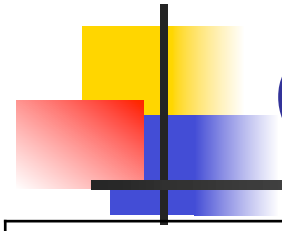
ALUctr Codes

# bit	A1	A0
ZERO	0	0
ADD	0	1
SUB	1	0
OR	1	1

ExtOp Codes

Unsigned extension	0
Signed extension	1

- MUX codes are given in the block diagram



Control signals

Control signals	« 1 » for instructions:	Boolean expression:
nPC_sel		
RegWr		
RegDst		
ExtOp		
ALUSrc		
ALUctr		
MemWr		
MemtoReg		

IV - Bascules : temps de prépositionnement et de maintien

Patrick.Garda@upmc.fr

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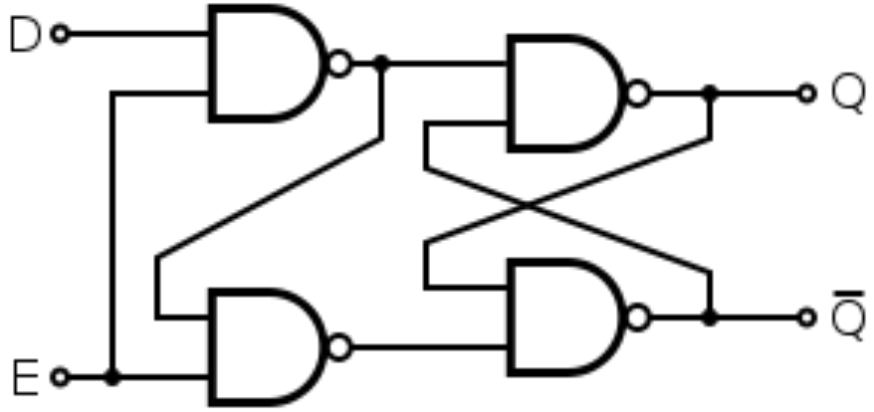
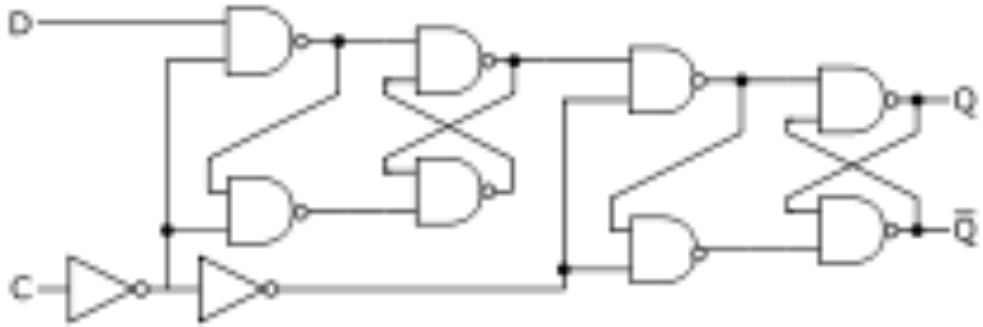
Latch D



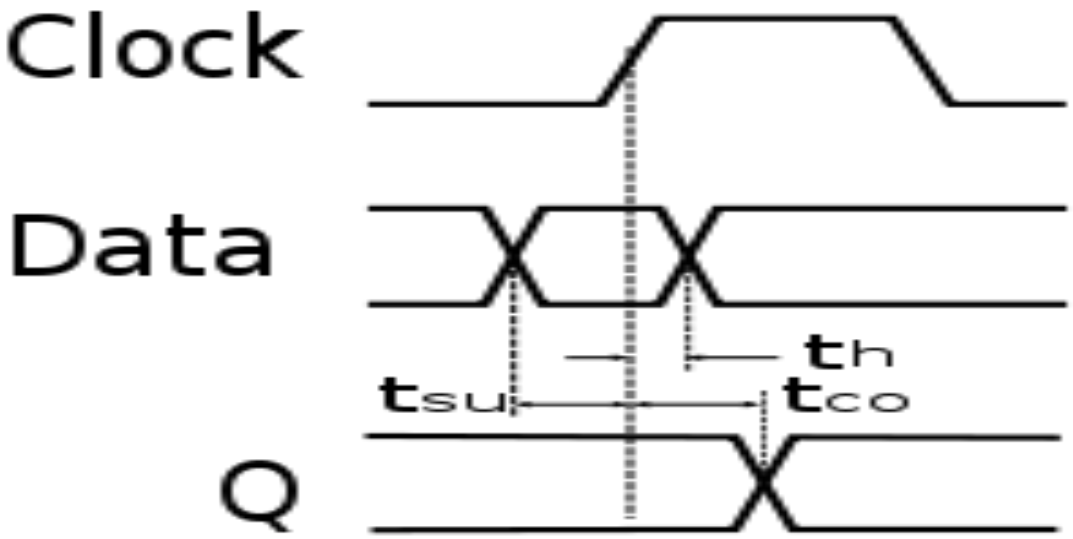
- Si E = 0 Latch verrouillé
- Si E = 1 Latch transparent

Bascule D



- Si C = 0
  - Latch Maître transparent
  - Latch Esclave verrouillé
- Si C = 1
  - Latch Maître verrouillé
  - Latch Esclave transparent

Temps prépositionnement



- Tsu
  - Temps prépositionnement
- Th
  - Temps maintien
- Tco Tc-to-Q Tp
  - Temps propagation

V - Période du processeur monocycle

Patrick.Garda@upmc.fr

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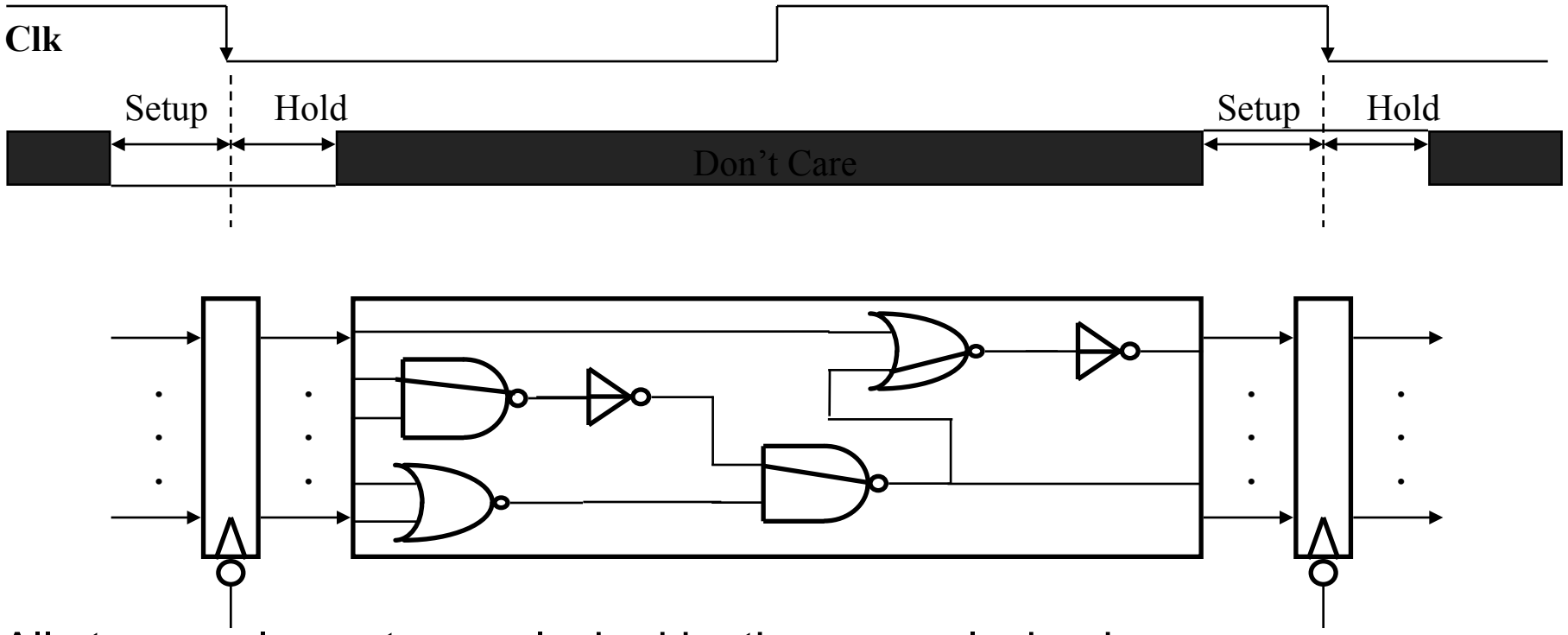
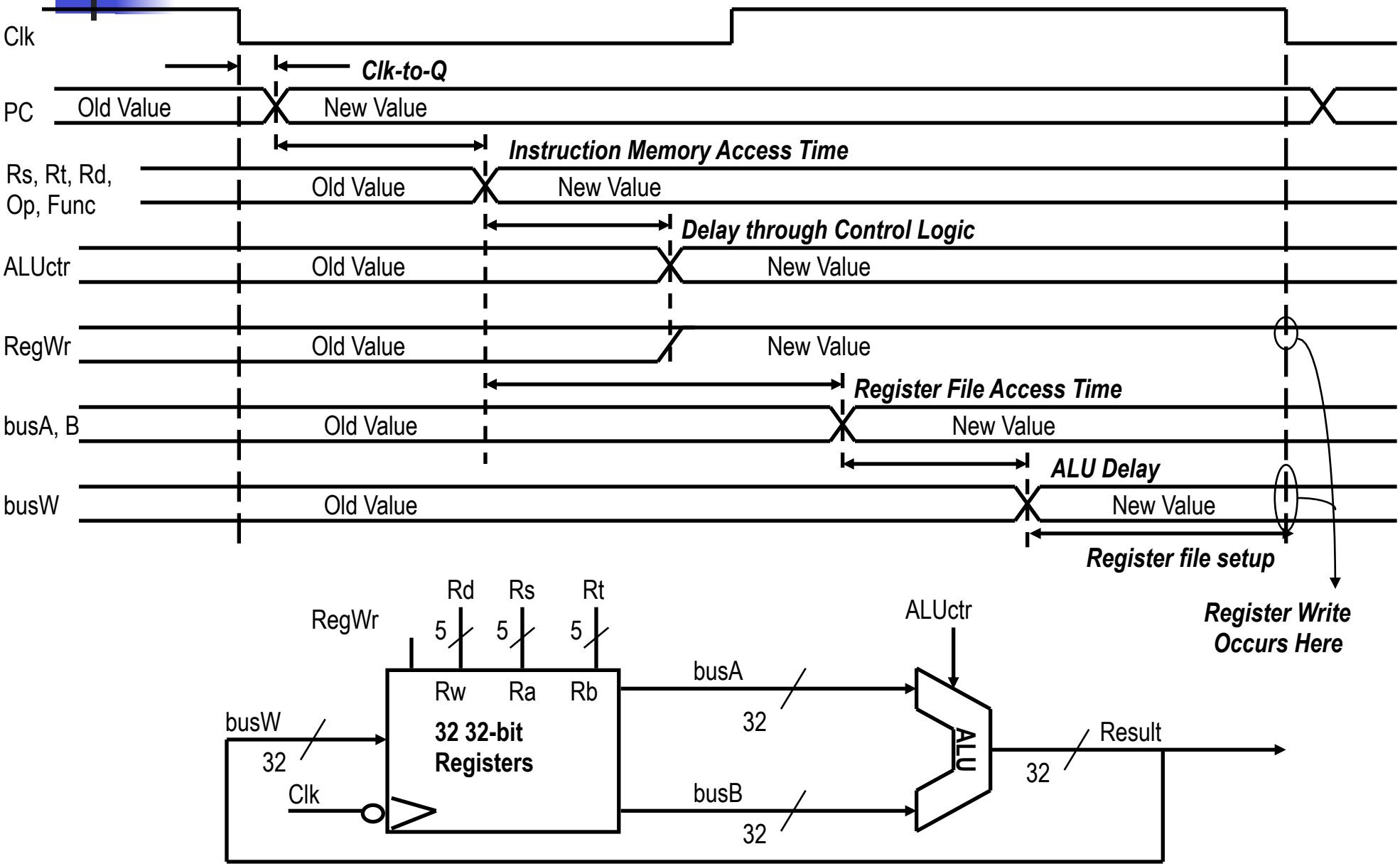
Clocking Methodology

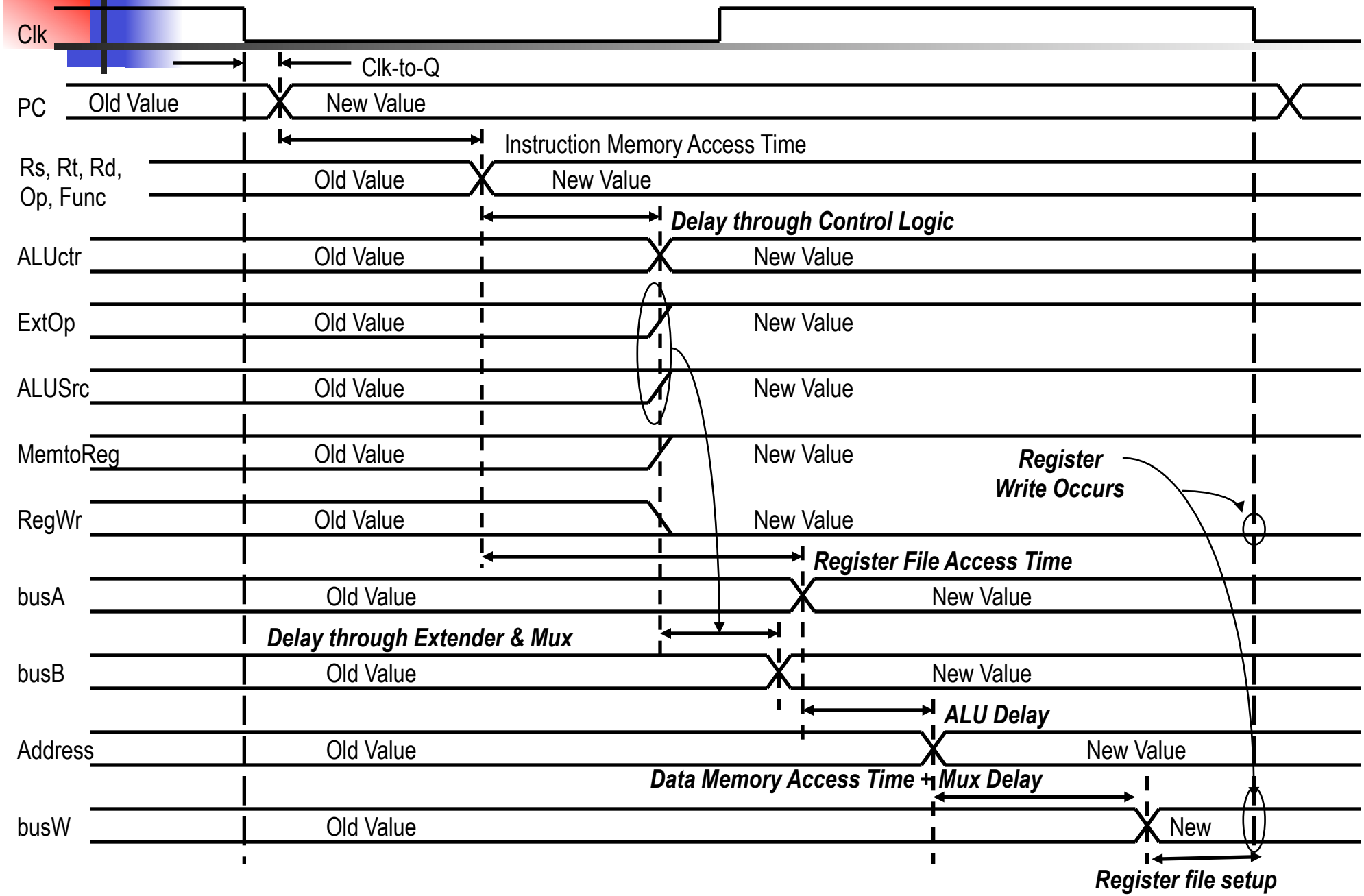


- All storage elements are clocked by the same clock edge
- Cycle Time = CLK-to-Q + Longest Delay Path + Setup + Clock Skew
- (CLK-to-Q + Shortest Delay Path - Clock Skew) > Hold Time

Register-Register Timing



Worst Case Timing (Load instruction)

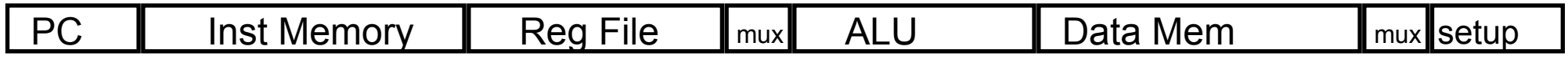


What is the minimum clock period?

ADD and SUB

ORI

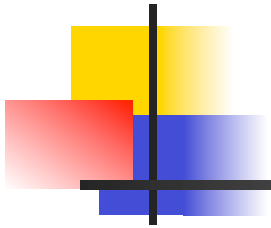
Load



Critical Path

Store

BEQ



Library Timing Data

	ALU/Adder	Extender	MUX	Control circuit	Register file PC	Memory
Propagation time	20 ns	10 ns	10 ns	20 ns	10 ns	20 ns
Setup time					10 ns	10 ns
Hold time					0 ns	0 ns

Exercice

- **Units:**

Instr	Step1	Step2	Step3	Step4	Step5	Step6	Step7	Step8	Step9	Step10	Total
ADD/SUB											
ORI											
LD											
ST											
BEQ											

- **Timing:**

Instr	Step1	Step2	Step3	Step4	Step5	Step6	Step7	Step8	Step9	Step10	Total
ADD/SUB											
ORI											
LD											
ST											
BEQ											