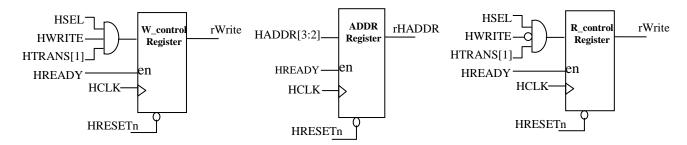
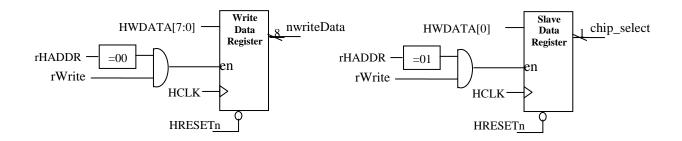
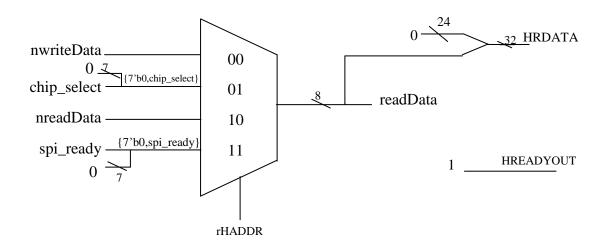
RTL Diagram



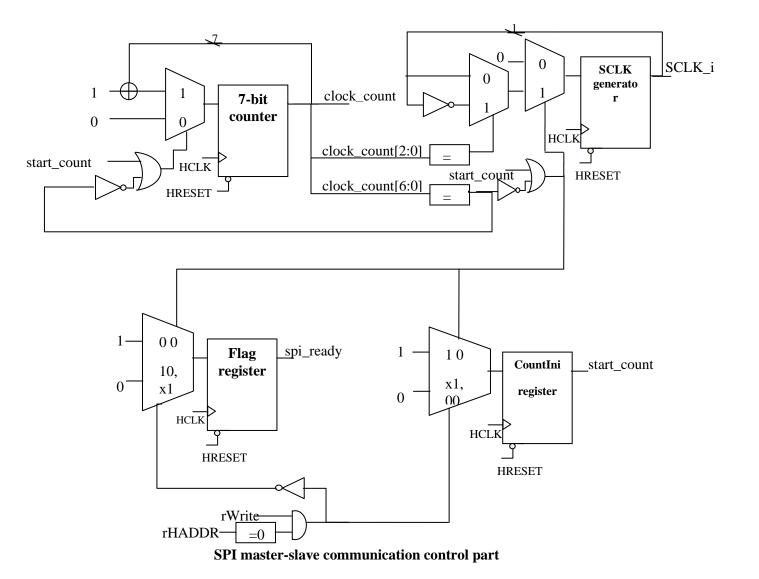
Registers to hold signals from address phase



Data registers for output ports



Read multiplexer



SCLK_i _1 **SCLK** x00x, 01xx, x010 **MOSI** 8 nMOSI nMOSI[7] MOSI nMOSI[7] register x011 nwriteData 11xxchip_select CS HCLK nreadData[6:0] start_count HRESETn **MISO** clock_count[7:0] _ nreadData **MISO** =0register SCLK en clock_count[2:0] -HCLK HRESETn

SPI master-slave data transceive part