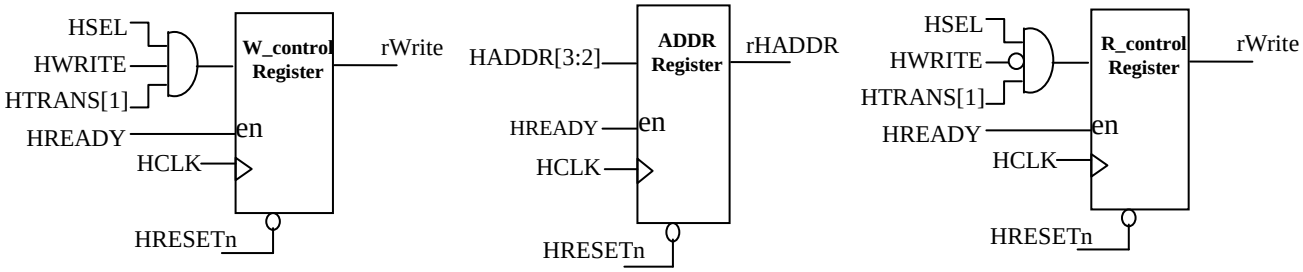
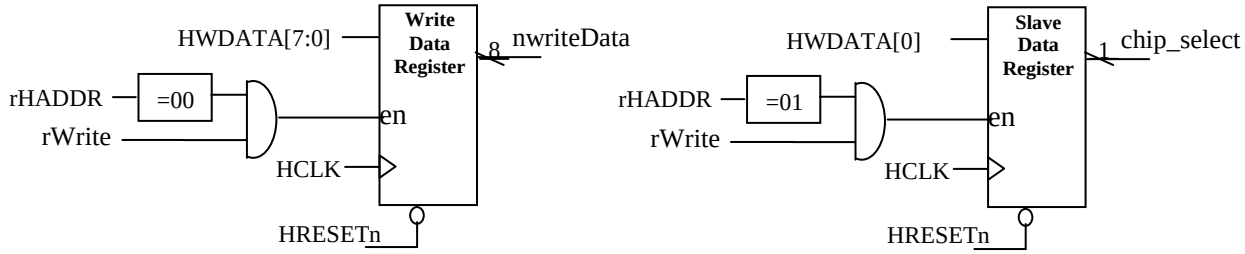
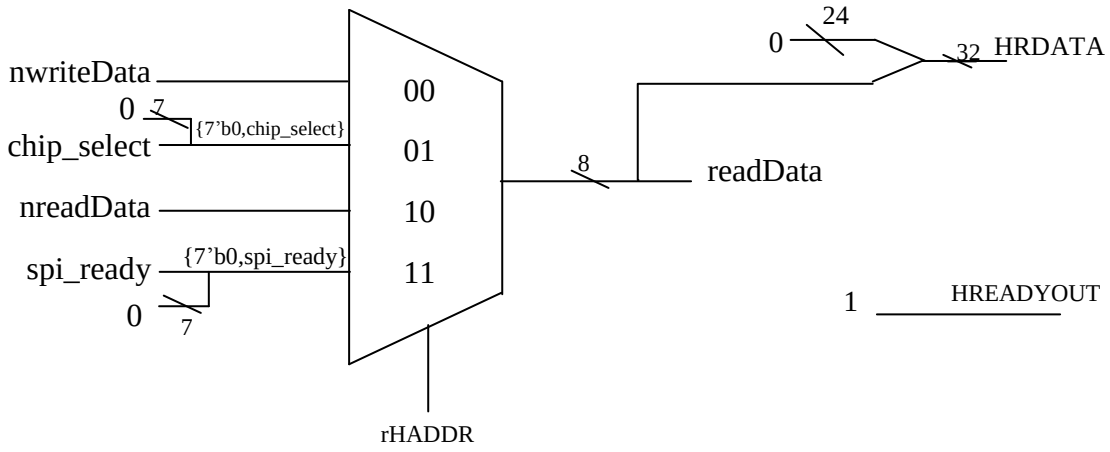
RTL Diagram



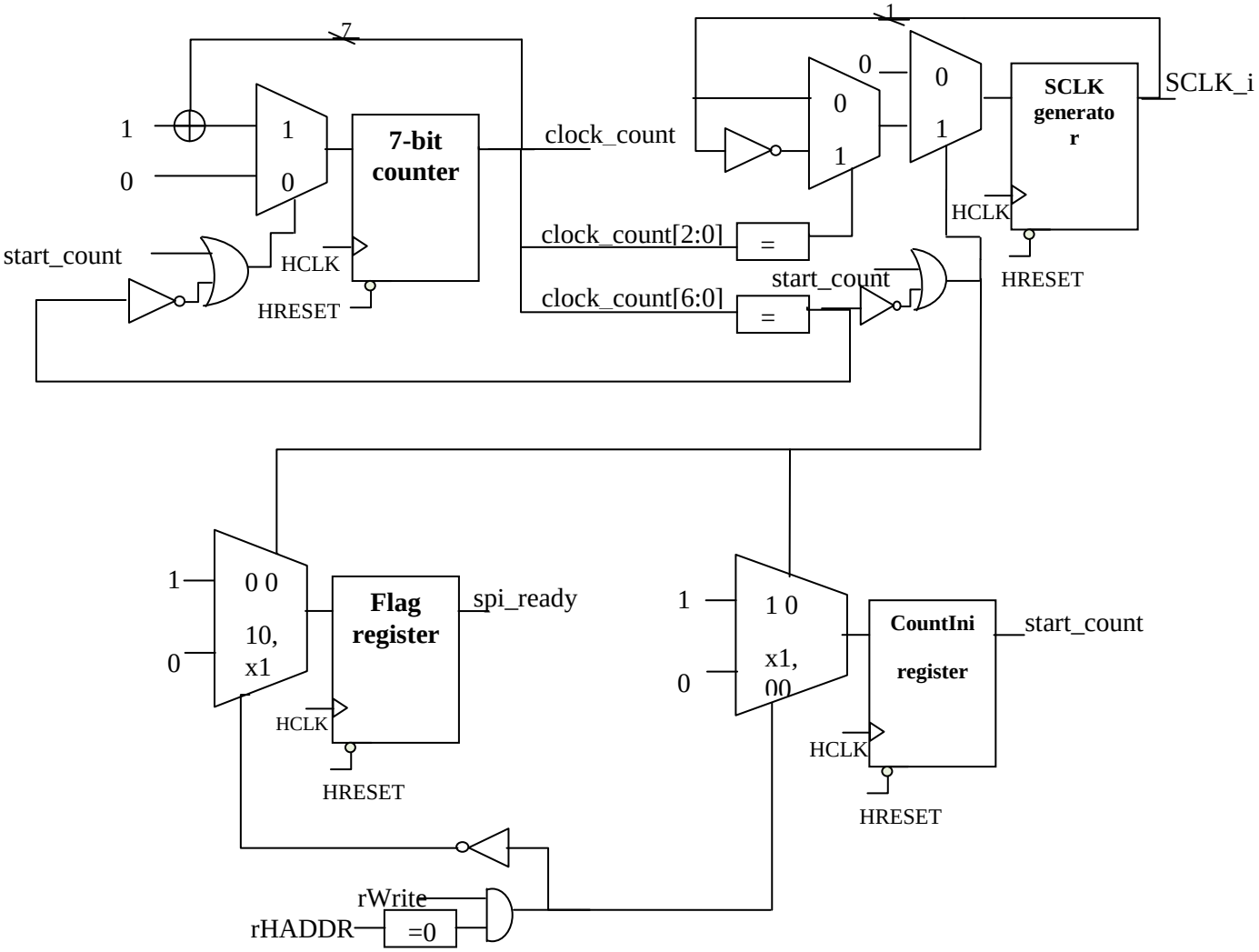
Registers to hold signals from address phase



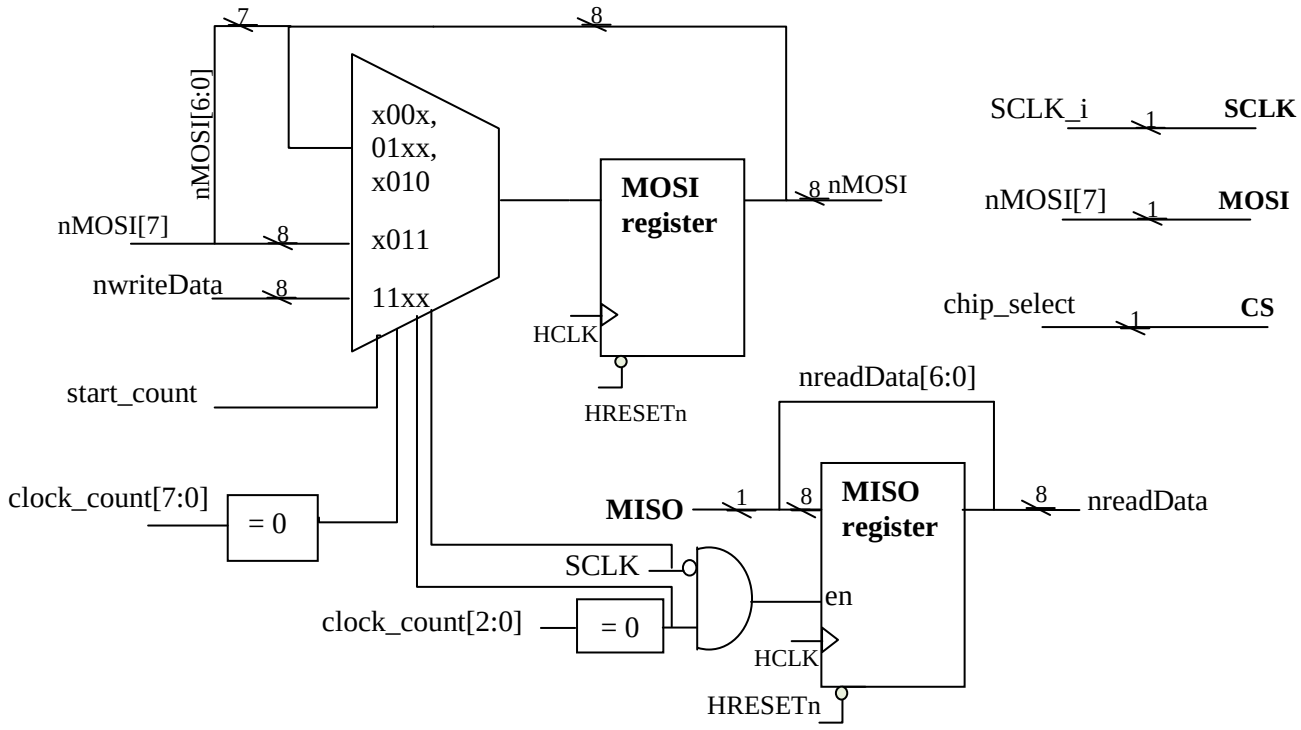
Data registers for output ports



Read multiplexer



SPI master-slave communication control part



SPI master-slave data transceive part