Jingyuan (William) Li

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Education

University of California San Diego **Sep 2024 - Present**

M. S. in Electrical & Computer Engineering (Electronic Circuits & Systems)

- **GPA:** 3.47/4.0
- **Courses:** Analog Integrated Circuits Design, CMOS Analog Integrated Circuits & Systems, Communication Circuit Design, High-Speed Wireline Communications & Systems, VLSI Digital Systems Algorithms & Architectures

University of Electronic Science and Technology of China **Sep 2020 - Jun 2024**

B. Eng in Electronic Information Engineering

- **GPA:** 3.77/4.0 (Top 15%)
- **Courses:** Analog Circuits, Digital Logic, Signals & Systems, Electromagnetic Field & Technology, Digital Signal Processing

University of Glasgow (Dual-Degree) **Sep 2020 - Jun 2024**

B. Eng in Electronic & Electrical Engineering

- **GPA:** 18.26/22 (First Class Honors)
- **Courses:** Circuits Analysis and Design, Electronic Devices, Electronic Systems Design, Power Electronics, VLSI Design

Projects

Design of a 10 Gb/s Tunable Voltage-Mode Transmitter Driver with 3-Tap FFE in 65nm CMOS **Jua 2025 - Mar 2024**

Project Manager, Supervised by Professor Tzu-Chien Hsueh

- Measured the pulse response on a channel model and calculated the tap weights based on zero-forcing method in MATLAB.
- Designed a 5-bit voltage-mode transmitter driver with rigorous sizing for impedance matching under DC simulation.
- Adopted foot transistors and introduced enable signal to realize the function of tunable weights under different data rates.
- Conducted comparisons with current-mode driver and tested the tunability control using pass gate.

Design of a Low Power ECG Amplifier in 180nm CMOS **Sep 2024 - Dec 2024**

Project Manager, Supervised by Professor Patric Mercier

- Designed a low power ECG amplifier with instrumentation amplifier (IA) structure, which consisted of a fully differential input buffer, a differential amplifier and a “drive-right-leg” common mode feedback amplifier with referenced input.
- Constructed a 2-stage amplifier with differential pair-common source structure, which achieves an intrinsic gain of 4000V/V.
- Adopted PMOS differential pair input and sized them to operate in sub-threshold region for noise reduction.
- Achieved a differential mode gain of 40dB, CMRR of 85dB in range of 1-250Hz, a total power consumption of 3.8 millionth watts and a total input-referred noise below 3 millionth Vin.

Design of a Multistage Folded Cascode Amplifier in 180nm CMOS **Sep 2024 - Dec 2024**

Project Manager, Supervised by Professor Drew Hall

- Improved a 2-stage amplifier system consisting of 31 transistors, with folded cascode-common source structure and DC biasing circuits.
- Calculated the optimal expected gain, MOSFET overdrive voltage, sizes and power consumption based on the Gm/Id relation in PDK library.
- Designed the DC biasing circuits with a constant-gm reference and current mirror technology.
- Adopted RC compensation between 2 stages of amplifier for poles splitting, which increased the phase margin.
- Achieved a gain of 77 dB, unity gain bandwidth over 30 MHz, and phase margin over 67 degrees, and power consumption under 2.3 milliwatt.

Research on the Modeling of Computing-in-Memory Architecture with SRAM-based Macro **Apr 2023 - Jun 2024**

Project Manager, Supervised by Professor Liang Chang

- Constructed a behavioral model of PT-8T SRAM in-memory-computation cell by *Verilog* which can perform Boolean AND operation between the data stored in that cell and an extra input.
- Built the SRAM-CIM in 4 banks, each bank had 64 lines of 8-bit SRAM-CIM cells, aiming at storing and processing grayscale/RGB data.
- Constructed the peripheral control circuits, including the CIM value decoder and a 7-level adder tree, enabling the CIM array to perform Multiplication & Accumulation operation in convolutional neural networks.
- Designed an address controller to store a value into several address places each time, which improved the computational parallelism.
- Evaluated the performance by emulating the computation process of convolutional layer computation through the circuit macro, which confirmed that only 34% of clock periods was required when using 3*3 kernel compared with conventional computation methods.

Design of a Multitasking Smart Robot Vehicle **Feb 2023 - Jun 2023**

Main Designed, Supervised by Professor Wasim Ahmad

- Led a team of 10 students to construct a smart robot vehicle capable of performing 6 tasks, including line tracking and pattern recognition.
- Designed a set of inter-board communication method, helping to replace the function of a complex controlled unit with only a camera module.
- Constructed the car’s distance measurement system using *MbedOS* and *HC-SR04* ultrasonic sensors and developed an algorithm in *Micro Python* which could assign a flag for data ignorance to filter out the wrong data generated the distance sensors.
- Produced a pan-silt camera holder and tent-shaped mechanical arm gripper using SolidWorks modeling and 3D printing.

Internship

James Watt School of Engineering, University of Glasgow **Sep 2022 - Jul 2024**

Teaching Assistant

- Monitored 3 courses, including Microelectronics Systems, Circuits Analysis & Design, and Embedded Processors, responsible for question feedback, course tutorial delivery and assignment evaluation, etc., with a cover of over 1500 students.
- Customized comprehensive reviews on lecture materials and mock exam exercise for students as final exam preparation.
- Delivered lab instructions to students, including the utilization of SPICE software and basic applications of programming languages, etc.

Skills

- **Engineering:** Cadence Virtuoso, Vivado, Altium Designer, LTSpice, MbedOS, Keil5, SolidWorks, HFSS
- **Programming:** C/C++, Verilog, MATLAB & Simulink, Python, ASM