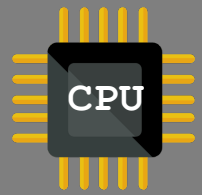


Topic 0

Course Introduction

Xinfei Guo
xinfei.guo@sjtu.edu.cn

May 13th, 2024

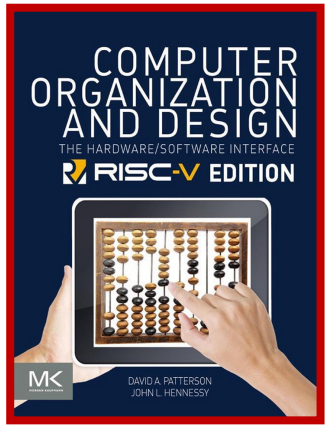
ECE4700J in one sentence…

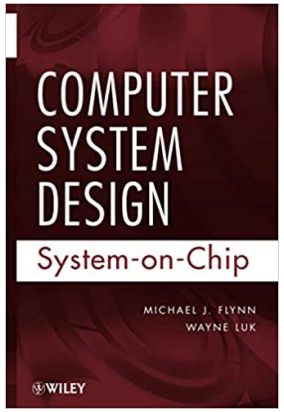
This is a four-level *Major Design Experience* (MDE) or *Upper Level Elective* Computer Engineering course, covering advanced concepts and practical approaches of architecting a computer (mainly **microprocessors**).

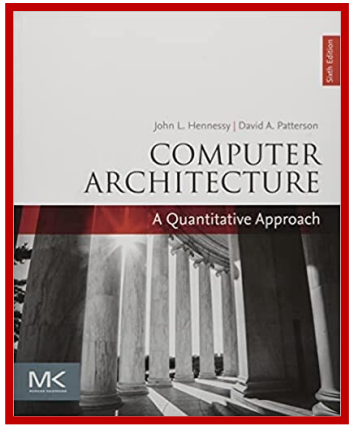
Image: https://nordicdairycongress.com/nyheder/welcome-nordicdairycongresscom#.YnEe5dpBxD8

Who I am?

- Associate Professor @ JI since May 2021
- Computer Engineering Ph.D. (Virginia), M.S (Florida)
- Worked @ NVIDIA & IBM Research in the US
- An enthusiastic computer hardware researcher
  - Circuit/Architecture/System
- Taught VE370 Intro. to Computer Organization (21SU), ECE4810J SoC Design (23, 22 & 21FA) , ECE4700J Computer Architecture (23, 22SU)
- Website: https://sites.ji.sjtu.edu.cn/xinfei-guo/



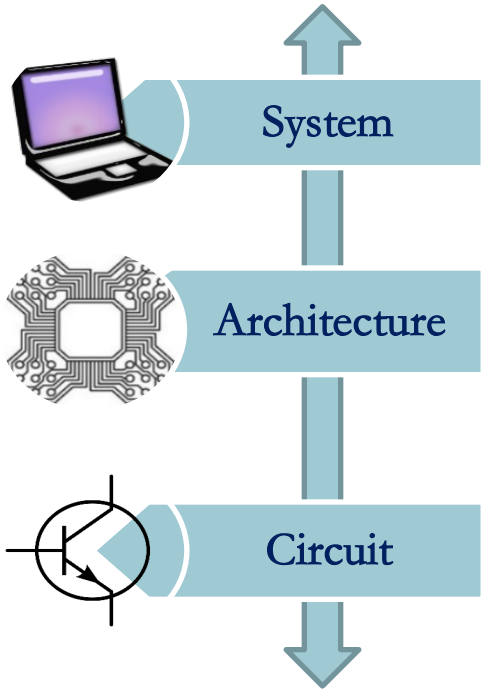




My research @ JI

Intelligent Circuits, Architectures, and Systems (iCAS)

上海交通大学密西根学院 智能电路、架构和系统实验室

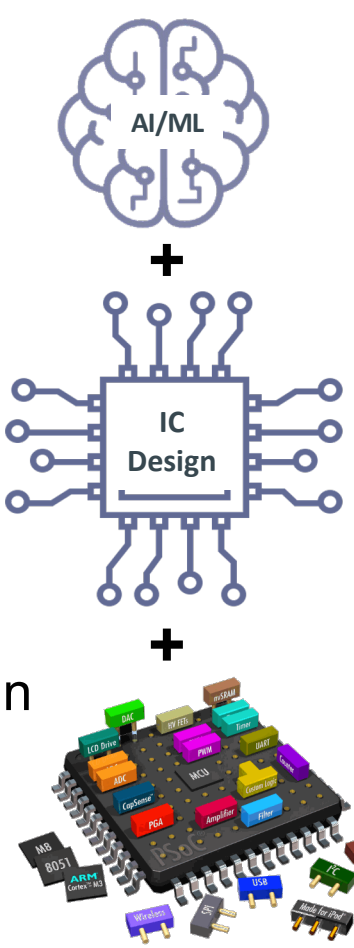


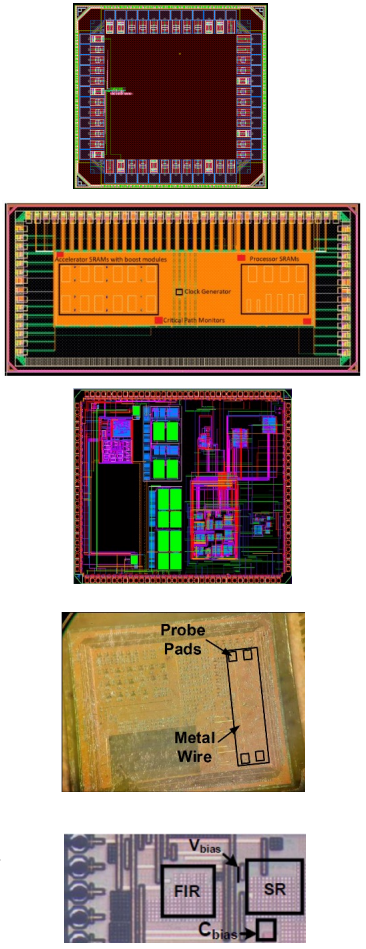
EDA/Design Methodology

- AI/Machine learning-enabled chip design automation

Computer Architectures

- HW/SW Codesign for Edge AI
- Energy Efficient & Reliable Chip Design





https://sites.ji.sjtu.edu.cn/icas

Image: https://www.cleanpng.com/png-introduction-can-stock-photo-clip-art-cliparts-pro-924166/

Logistics

- Course website (Canvas): https://jicanvas.com/courses/750/
- Course schedule: Lectures **MON, WED 10:00-11:40AM** (Beijing Time); Labs **TBD**
- Teaching mode (Lectures): In-person Only - Classroom **DXY303**
- Teaching mode (Labs): In-person Only – Classroom **TBD**
- Office Hours: TBD
- RC: 4hrs (TBD)
- Slides/handouts will be provided before the class most of the time (several might be not, this will be done **on purpose** or will be revised after the lecture)
- Reading materials will be assigned

Who is TA?

- Xinting Jiang (江信廷)
- Junior Student in UM-SJTU JI dual degree program
- Incoming Senior Student at UM in CE
- Took EECS470 at UM
- Research Interests: Computer Architecture and Digital Design
- Email: evans_jiang@sjtu.edu.cn
- TA Office Hours: TBD

Who is TA?

- Mingjian Li(李明鉴)
- Junior Student in UM-SJTU JI dual degree program
- Incoming Senior Student at UM in CE
- Took EECS470 at UM
- Research Interests: Computer Architecture and Digital Design
- Email: lmjhshxhc@sjtu.edu.cn
- TA Office Hours: TBD

Prerequisites

- VE370 & VE280 (Both are **required**)
- Willing to spend time and efforts (The workload won't be light)
- You have strong interests in learning about computer hardware (not just to fulfil your graduation requirement), otherwise you will feel painful when working on labs and final projects, etc.
- Previous Verilog experiences (including how to simulate it) are **required**!
- Basic understandings about ISAs (**any**) and computer organization (basic pipelines, cache) are **required**!
- **If you have taken 470 or equivalent course at UM or other places, please don't take this course again.**

Feishu Group

- For urgent matters, course announcements, logistics, etc. Please join asap! (***Join only you decide to take the course***)

https://applink.feishu.cn/client/chat/chatter/add_by_link?link_token=bc0r893f-1473-4085-841f-251b8853b7ed

Course Outline

- https://jicanvas.com/courses/750

Course Outline: (Note: Tentative and subject to adjustment.)

Week	Lec #	Date	Topics	Readings	Assignments
1	1	5/13	Course introduction, Intro. to Computer Architecture	Syllabus, Slides, Reading Materials on Canvas	Course survey due by 23:00 May 15th.
	2	5/15	Intro. to Computer Architecture, Fundamentals of Quantitative Analysis	Ch. 1.1-1.4, 1.8, 1.9	
2	3	5/20	Fundamentals of Quantitative Analysis	Ch. 1.5 - 1.8, 1.10	
	4	5/22	Fundamentals of Quantitative Analysis Fundamental Processors I - Pipeline	o P&H, Computer Organization and Design RISC-V Edition, Ch. 4.5 – 4.6 o Ch. 3.1	

Piazza group

- For detailed discussions, questions about, projects, labs, clarifications, etc.
- Signup link

https://piazza.com/sjtu.org/summer2024/ece4700j

Course Survey

Please finish by **May 15th, 23:00 Beijing Time,** make sure you answered **ALL** questions.
https://sjtu.feishu.cn/share/base/form/shrcnWEm9DncaboKJtYci90h5ph

Course Objectives (what will be taught)

- To teach students fundamental design tradeoffs of the modern computer architectures;
- To teach advanced computer architecture concepts such as Multiprocessors, Superscalar, GPUs and advanced caches;
- To give students an exposure to state-of-the-art computer architecture simulators through hands-on assignments and/or a project that will help understand the tradeoffs;
- To offer student hands-on experiences of implementing or optimizing major portions of a substantial processor with either Verilog or High-level design approaches;
- To introduce students the most recent computer architecture advances such as Domain specific architectures (DSA) and AI accelerators;
- To provide experiences of executing a project as a team from concept to finish effectively and professionally, and to offer opportunities to present ideas to the public.

Course Outcomes (what students are expected to achieve)

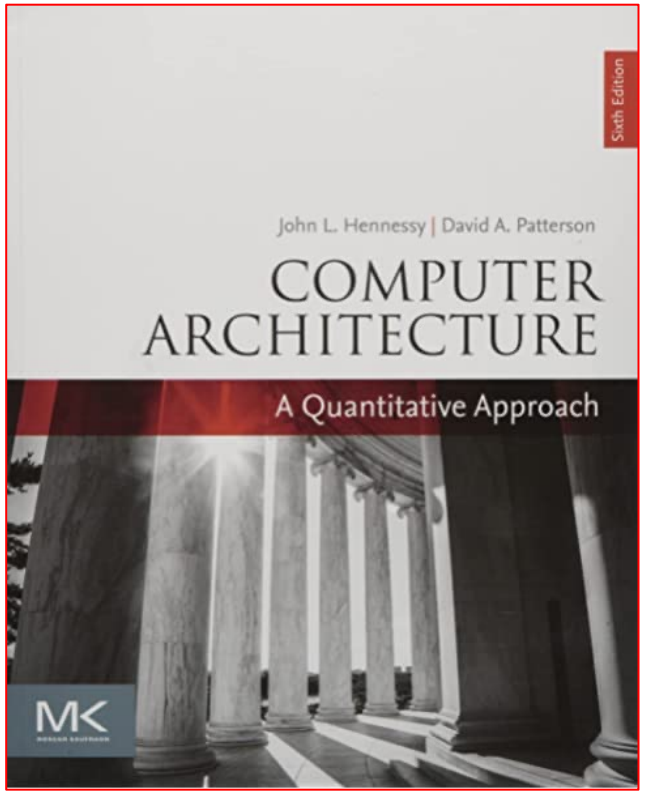
- Understand fundamentals of designing a modern processor and the key metrics;
- Gain fundamental knowledge and understandings of advanced computer architectures such as multiprocessors, superscalars, advanced caches, and prefetching schemes;
- Learn about state-of-the-art computer architecture simulators or frameworks;
- Develop understandings about certain design tradeoffs in implementing the modern computer architectures;
- Learn about the concept of high-level design languages, AI accelerators or domain-specific architectures;
- Work as a team to implement and optimize a given functional description of a major portion of a substantial processor with learned knowledge and tools;
- Be able to present the results and conclusions of an experimental project in a clear, logical, succinct, and informative written format.

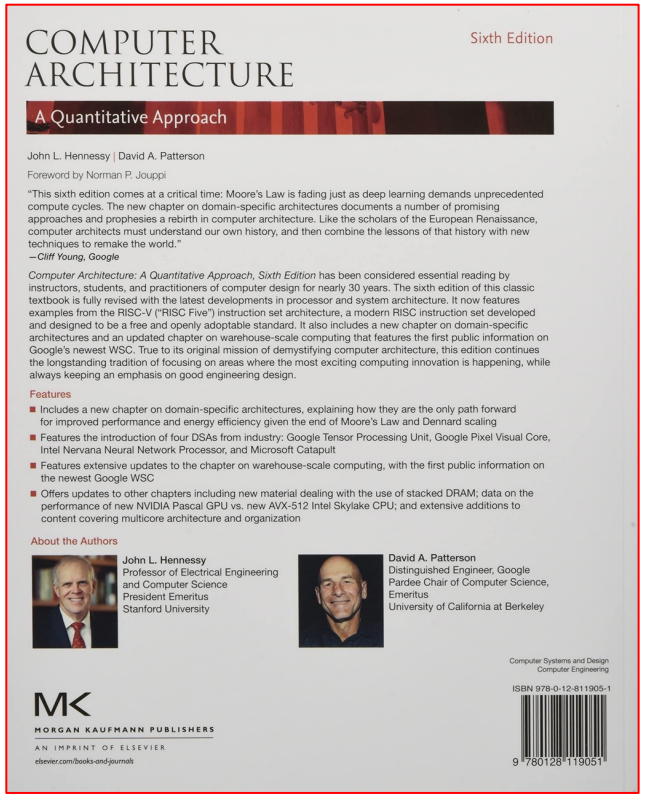
My expectations

- After taking this course (for many, the last course at JI)
  - Be able to understand fundamentals and tradeoffs of designing a modern microprocessor;
  - Be able to develop thinking logics from a hardware perspective;
  - Gain some exposures to real-world design problems;
  - Practice your research ability and critical thinking skills;
  - Be able to present confidently to a broader audience.

Recommended Textbook (the "bible")

- Computer Architecture: A Quantitative Approach, by John L. Hennessy and David A. Patterson, published by Morgan-Kaufmann publishers, November 2017. ISBN: 9780128119051. (**Sixth** Edition)





About the Authors

- 2017 ACM “Turing Award” Winders (Lecture)
- Inventors of the reduced instruction set computer (RISC)
- Distinguished researchers, leaders and long-time educators
- Authors of groundbreaking computer architecture textbooks

About the Authors

John L. Hennessy
Professor of Electrical Engineering and Computer Science
President Emeritus
Stanford University

David A. Patterson
Distinguished Engineer, Google
Pardee Chair of Computer Science, Emeritus
University of California at Berkeley

About the Authors

- “simpler is more efficient”

— John Hennessy

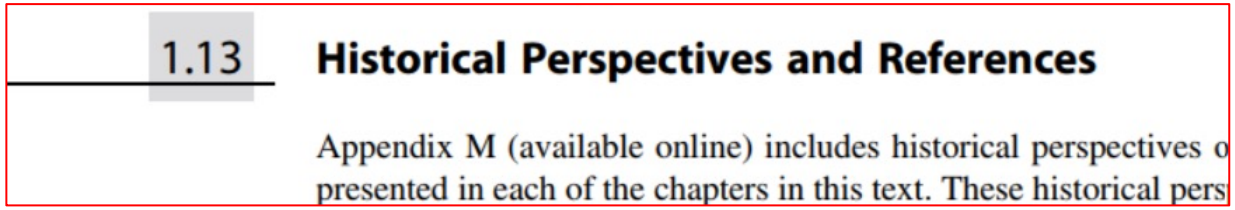
- “Instruction Sets want to be FREE!”

— David Patterson

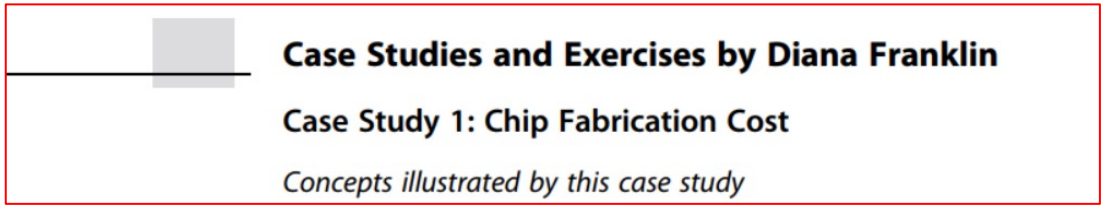
More about this book

Fallacies and Pitfalls

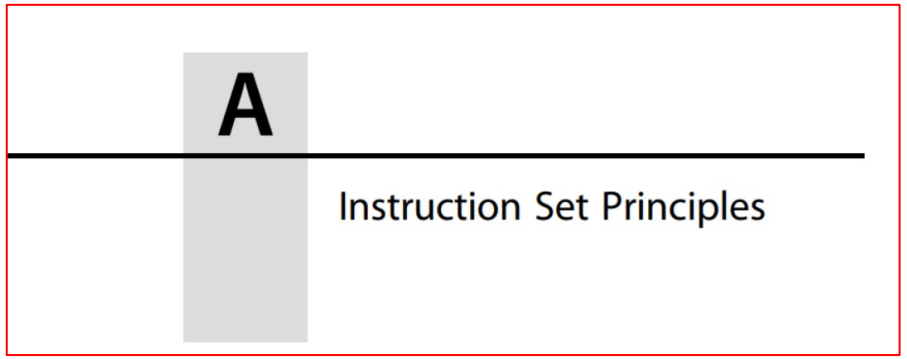
Historical Perspectives



Case Studies



Appendix



Course Topics (Tentative)

- Intro. to Computer Architecture
  - Quantitative Analysis
- The Processing Part
  - Fundamental Processors
  - Advanced Processors
    - Superscalar
    - Out of order
- Memory
  - Advanced Cache
  - Prefetching
  - Virtual Memory
- Multiprocessors
  - GPUs
  - Multicore

Course Topics (as a bonus)

- Domain-Specific Architectures (DSA)
- Processing in Memory (PIM)
- Reconfigurable Computing
- AI Accelerators
- High level synthesis (HLS)
- …

Labs (Tentative plan)

- 36 hours in total
  - Individual based, lectures from TA/Assignment discussion + Finish during the lab or offline
  - 4 labs
  - Verilog/System Verilog focused, C/Python programming focused
  - Logistics will be posted soon

Final Project (Tentative plan)

- Group based (~5 students)
  - Literature review will be part of it
  - Implementing/optimizing an advanced architecture with the knowledge learned in this course.
  - Will be given a pool to select your project (will be released at least 1.5 ~ 2 months before the deadline)
  - You can also initiate or come up with your own ideas (by talking to the instructor/TA)
  - MDE students will be responsible for fulfilling the university and JI requirements (Thesis, design expo, etc.)

Grading Policy

Participation & Etiquette*	10%
Labs	30%
Final Project & Report**	35%
Final Exam	25%
Total	**100%**

- *Participation is highly recommended as there will be NO recordings, it includes lecture (3%) and lab participation (3%). The rest includes piazza questions and answers (2%), lecture/lab/OH involvement (2%), etc.
- **It also includes the literature search and review part.
- Creative ideas in projects will get bonus.
- Final letter grades might be curved, but are not guaranteed.

Course Policies

- **Honor Code:**
  - Honor Code of the Joint Institute
- **Test:**
  - Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an ‘F’ for the test.
- **Attendance:**
  - Strongly encouraged for better understanding of difficult concepts and student engagement during class time
- **Participation:**
  - Active participation is highly expected for all students. This involves:
    - Participation in interactive activities during the lecture time
    - Active involvement in projects & labs
    - Proper assistance to other students in group studying
    - Contributions to the Q&A on Piazza, etc.

Course Policies

- **Labs**
  - This is a “relatively” new course, so bugs/errors are expected.
  - The instructor or TA are not supposed to help with debug the code line by line (as debugging is part of the learning and practice).
  - But high level solutions and resources will be provided if you really get stuck.
  - Asking peers for help is allowed for certain labs, but you need to understand and translate into your own practices.
  - Your work will be measured by reports, demos, and more.

Course Policies

- **Individual Assignments**:
  - Labs
  - OK to discuss course topics and help each other understand the requirements better
  - NOT OK for duplicated submission
  - NOT OK to copy solutions from the Internet
- **Group Assignments**:
  - Final project
- **Submission:**
  - Electronic submission on Canvas before deadline.
  - Extensions need to be approved by the instructor for labs (reasons need to be justified, 10% reduction per day).
  - No extension is allowed for the final project.

Assessment Methods

- Labs (with reports)
- Final project (with presentation & report/thesis)
  - For those who enroll for capstone, corresponding rules need to be followed.
  - Creativity is strongly encouraged and will be credited.
  - Leadership will be credited.
- Final exam
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.

Hours (and hours) of work

Note this is only an *estimation*!!!

- Attend lectures
  - ~4 hrs/week
- Read book & handouts
  - ~2-3 hrs / week
- Labs/Project
  - >8 hrs/week
- Others
  - 1 hr/week

How to survive this class?

- **Have interests on computer hardware**
- Attend/review lectures and participate
  - Involve in discussions
  - Ask questions
- No plagiarism (nor anything like it)
- Write your own code
- Understand what you submit
- Be creative in projects
- Read the materials (!)

Why taking this course is NOT a good idea?

- Time-consuming (Project+Exam+Lab…)
- Might not be relevant to what you are doing after.
- Verilog, Verilog, Verilog! Not C++, not Python!
- Had no interests at all, only because running out of option for MDE.
- Will only start working on the project in the last few weeks…

Some Final Notes

- In-person teaching mode only.
- When you decide to drop the course, please quit the Feishu/Piazza group.
- Feedback and communications are always welcomed.

Q & A

- What if I am not in Shanghai? (Sorry, please take other courses)
- What if I am not taking it as MDE? (Fine)
- What if we need to use hardware? How should we get them? (No need, unless you want to have a cool demo)
- What if I miss the office hour? (Contact me through email and make appointment)
- What if I miss the deadlines? (Follow various late penalty)
- What if I can't find a teammate for my lab/project? (We will assign one for you)
- Lab tutorials/Tool instructions? (We will try our best, but you need to be proactive)
- Similarities between this course and UM EECS 470? (Yes, many!)
- What will be the specific form of labs later? (Lectures + Post-lecture Practices)
- If possible, would like to know the tentative hours required for the final project? (You will need to spend quite some time on it)
- What if I know none of the ISAs? What if I know nothing about Verilog? (Please don't take the course)
- Can I choose my own teammates? (Yes)
- I don't have any other choices for MDE and have to take this course… (are you sure?)
- I just want to graduate, can I take the course? (Please don't)
- Others?

Action Items

- Read syllabus and decide carefully
- Join Feishu group
- Sign up for Piazza
- Finish course survey (by **5/15 23:00** Beijing Time)