Lab #2

Design with High Level Synthesis on Arty Z7 SoC Development Platform

Oct. 14, 2024

From Verilog to SystemVerilog

Verilog	System Verilog
wire	wire / logic
reg	logic
always @(*)	always_comb
always @(posedge clock)	always_ff @(posedge clock)

```
module 1b_register(
    input rst,
    input clk,
    input in,
    output out
);
    always_ff @(posedge clk, posedge rst) begin
        if (rst) begin
            out <= 1'b0;
        end
        else begin
            out <= clk;
        end
    end
endmodule
```

Figure: 1b register in SystemVerilog

```
always_comb begin
    case (var)
        3'b0: begin
            // do sth
        end
        3'b101: begin
            // do sth
        end
        3'b111: begin
            // do sth
        end
        default: begin
            // do sth
        end
    endcase
end
```

Figure: "case" example in SystemVerilog

SystemVerilog

- Use a generate block to build the hardware

```
1  generate
2      genvar i;
3      for (i=0; i<N; i++) begin
4          one_bit_adder (
5              .a(a[i]), .b(b[i]),
6              .cin( carries [i]),
7              .sum(sum[i]),
8              .cout( carries [i+1])
9          );
10     end
11 endgenerate
```

- The tool will "elaborate" the design
- It will evaluate "if" statement and unroll "for" loops

Pipelined Multiplication

- Objective: optimize time-consuming traditional simple to enhance execution efficiency
- General Steps
  - Multiply parts of the multiplicand and multiplier for a partial product (pipelined)
  - Sum up the partial products to obtain the results

Example: 4-stage Pipelined Multiplication

```
   multiplicand: 00001011   << 2
     multiplier: 00000111   >> 2
partial product: 00100001
   multiplicand: 00101100   << 2
     multiplier: 00000001   >> 2
partial product: 00101100
                + 00100001
                = 01001101
```

Lab #2

Goals

- Get familiar with the concept of High-level Synthesis (HLS)
- Learn to use HLS to create an IP block in C/C++
- Learn about differences between programming with HLS vs. Verilog in terms of design quality
- Get started with the Arty Z-7 board as a Python accelerator and be able to run example Jupyter notebooks with the board
- Load PYNQ overlays, use overlays and create overlays

Deliverables

- Details are in the Lab #2 description
- Peer evaluation form (individual grade)

References

- Yichen Cai, 2023 Lab #2