ECE4810J LAB 4 Group 8 Report

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Contents

1 Overview

In this lab, we learned about ASIC design flow, especially, OpenROAD-flow-scripts and the automated ASIC flow based on the Tencent EDA platform.

2 OpenROAD

2.1 Section 2.4: the final exported GDS file

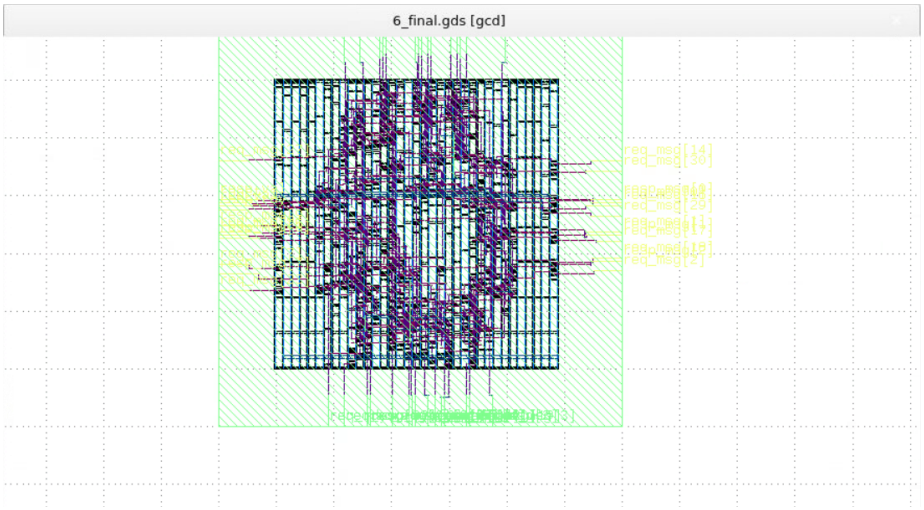

Figure 1: final figure of section 2.4

2.2 Section 2.5: the answers to the questions

2.2.1 What is half perimeter wire length?

Half Perimeter Wire Length (HPWL) is a metric to estimate the wiring required for connecting components in a circuit. It's calculated by taking half the perimeter of the smallest bounding box that encloses all the pins or terminals of a net (a group of points that need to be electrically connected).

2.2.2 What does the Nesterov gradient descent do in global placement?

In global placement, **Nesterov Gradient Descent** is a technique used to optimize the positions of cells efficiently by accelerating convergence towards an optimal placement. This method builds on traditional gradient descent by adding a "momentum" term, which anticipates the next position based on the current gradient and past steps.

2.2.3 During global placement, the half perimeter wire length, worst slack, and the number of weighted nets when the iteration number of the second Nesterov gradient descent is 320, and the final RC value.

half perimeter wire length :5224694um

worst slack :-6.32 e11

number of weighted nets :41

final RC : 0.930995

2.2.4 What do the global placement and the detailed placement do?

Global Placement is to find an approximate, non-overlapping position for all cells in the chip layout while minimizing a cost function, typically focused on wire length, timing, and congestion. It doesn't determine the final, precise locations but rather achieves an initial, optimized layout that places cells in general regions.

Detailed Placement refines the positions of cells to meet specific design rules, ensuring legal and physically feasible locations without overlaps after global placement. It adjusts cells locally, improving aspects like wire length, density, and timing further at a finer granularity.

2.2.5 What are the names of algorithms that the global placement use? What are the names of algorithms that the detailed placement use?

- **Global Placement:**
  - Simulated Annealing
  - Kernighan-Lin (KL) Algorithm
  - Quadratic Placement
- **Detailed Placement:**
  - Window-based Branch-and-Bound Method
  - Greedy Cell Exchange Algorithm
  - Network Flow Algorithms

2.2.6 Select one algorithm you list above and briefly introduce the core part of the algorithm.

Simulated Annealing is an optimization algorithm inspired by the annealing process in metallurgy. It begins with a high "temperature," allowing exploration by making random changes to a solution and probabilistically accepting

worse solutions to escape local minima. As the temperature gradually lowers, the algorithm becomes more selective, favoring improvements until reaching a stable, near-optimal solution.

2.2.7 What are the post-pair critical path delay and slack during the clock-tree synthesis?

Post-pair critical path delay is the maximum delay on timing-critical paths after clock-tree balancing.

Slack measures timing compliance. Positive slack indicates timing is met, while negative slack shows violations.

Clock-tree synthesis aims to minimize critical path delay and maintain positive slack for optimal performance.

2.2.8 What is the name of the algorithm that the global routing use? What is the name of the algorithm that the detailed routing use?

- **Global Routing:**
  - Maze Routing Algorithm
- **Detailed Routing:**
  - A Algorithm* or Negotiated Congestion Routing

2.2.9 What is parasitic extraction?

Parasitic extraction is a process that calculates the unintended resistances, capacitances, and sometimes inductances (collectively known as parasitics) of interconnections (wires and vias) in an integrated circuit layout.

2.2.10 What are the finish critical path delay and slack during the timing signoff?

Finish Critical Path Delay is the final delay measured along the longest (or critical) path in the design after all optimizations, routing, and parasitic effects have been accounted for. It determines the minimum achievable clock period and ultimately the maximum operating frequency of the chip.

Slack is the difference between the required time and the actual arrival time of signals along a path. Positive slack indicates that timing requirements are met, while negative slack shows timing violations. During timing signoff, the goal is to achieve positive slack across all paths, indicating that the design can operate reliably at the target clock frequency.

2.3 Section 2.6: the modified config.mk file

2.4 Section 2.7: the modified config.mk file, calculated 2, 4, 5, and 6

2.4.1 Max Frequency

$Frequency_{max} = \frac{1}{constraint - slack}$

constraint = 0.46ns

Measured: slack = -0.08ns

Manual: slack = -0.09ns

$Frequency_{max} \approx 1.85GHz$

2.4.2 Die Area

$\text{Area}_{\text{Die}} = (70.11 - 0) \times (70 - 0) = 4907.7\,\mu\text{m}^2$

2.4.3 Core Area

$\text{Area}_{\text{Core}} = (60.04 - 10.07) \times (60.2 - 11.2) = 2448.53\,\mu\text{m}^2$

2.4.4 Core Area by Formula

$\text{Area}_{\text{core}} = \frac{593}{0.24} \approx 2470.83\,\mu\text{m}^2$