Lab #1

Getting Started with Arty Z7 SoC development platform

Sept. 30, 2024

Group Assignment

Group 1	Group 2	Group 3	Group 4	Group 5
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Group 6	**Group 7**	**Group 8**	**Group 9**	**Group 10**
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Lab logistics

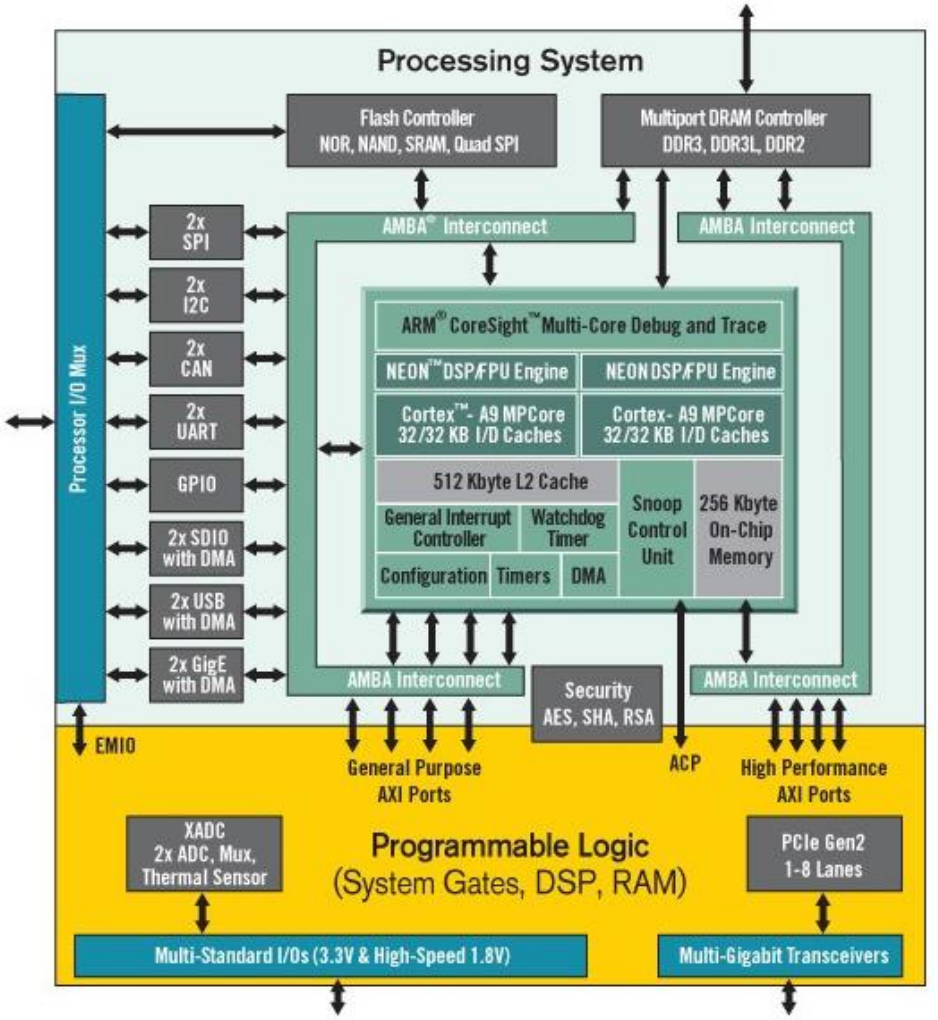
- **Ahead notification**
  - If you can't make it, please justify your reasons and let the instructor/lab management know at least three days ahead!
- **Attendance** is required, and you can leave after an hour if needed
- **Lab deliverables** include reports, codes, demos, and individual contributions (evaluation of your peer's performance).
- Internet search and discussion with others are allowed, especially for bugs, and interesting ideas, but not for direct copy and paste.
- Please read the documents (references) carefully before you ask questions.

Lab logistics

- Please **take good care of the board**, cables, and other accessories. You will not be able to get grades if your lab kit is not returned or pieces are broken/missing.
- Try to understand why you do it before you do it.
- Debugging should be a fun process instead of a painful headache.
- **Teamwork**
  - Share what you learned with each other.
  - Plan the workload division with your teammates early
  - Know each other's work even if you are working on different parts

Arty Z7

- ready-to-use development platform designed around the **Zynq-7000™** All Programmable System-on-Chip (AP SoC) from Xilinx
- Zynq-7000 architecture
  - 650 MHz dual-core ARM Cortex-A9 processor with Xilinx 7-series FPGA logic.
  - Programmable from JTAG, Quad-SPI flash, and microSD card
  - Enables software-defined peripherals and controllers



Source: arty-z7 reference manual

Image: Diligent

Arty Z7-20

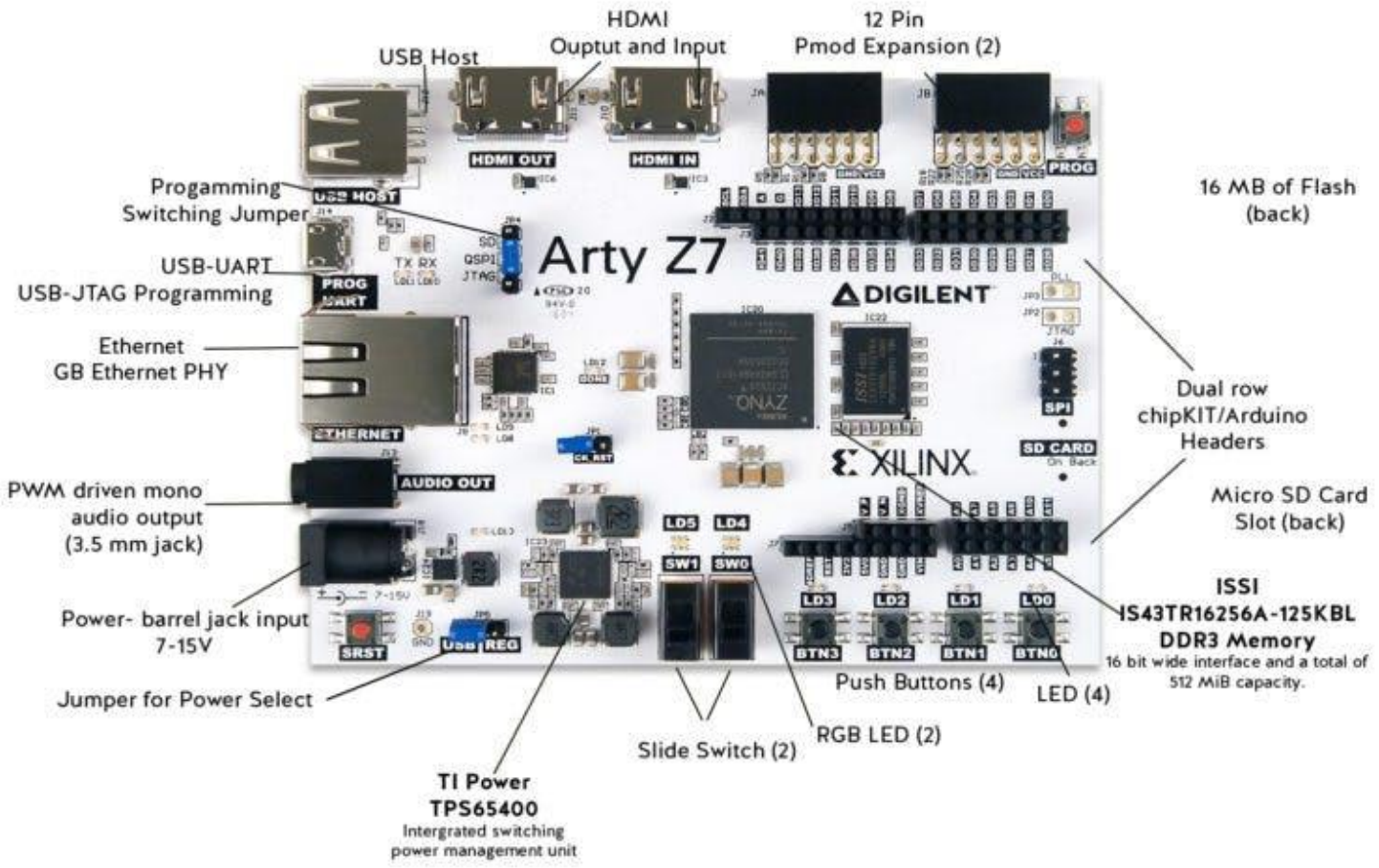


Image: Diligent

Arty Z7-20

- **Memory**
  - 512MB DDR3 with 16-bit bus @ 1050Mbps
  - 16MB Quad-SPI Flash with factory programmed 48-bit globally unique EUI-48/64™ compatible identifier
  - microSD slot
- **USB and Ethernet**
  - Gigabit Ethernet PHY
  - USB-JTAG Programming circuitry
  - USB-UART bridge
  - USB OTG PHY (supports host only)

Source: Diligent

Arty Z7-20

- **Audio and Video**
  - HDMI sink port (input)
  - HDMI source port (output)
  - PWM driven mono audio output with 3.5mm jack
- **Power**
  - Powered from USB or any 7V-15V external power source
- **Switches, Push-buttons, and LEDs**
  - 4 push-buttons
  - 2 slide switches
  - 4 LEDs
  - 2 RGB LEDs

Source: Diligent

Boot Modes

- The Arty Z7 supports three different boot modes: microSD, Quad SPI Flash, and JTAG.

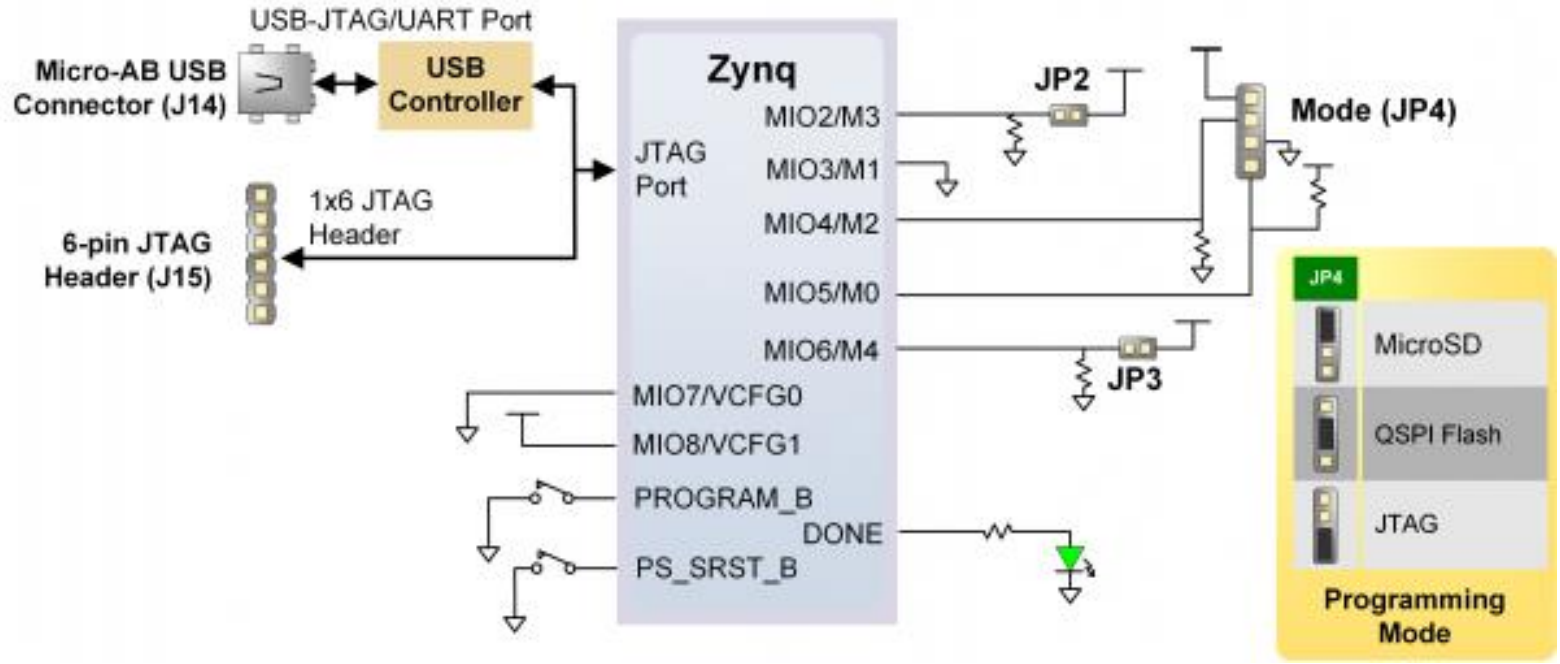
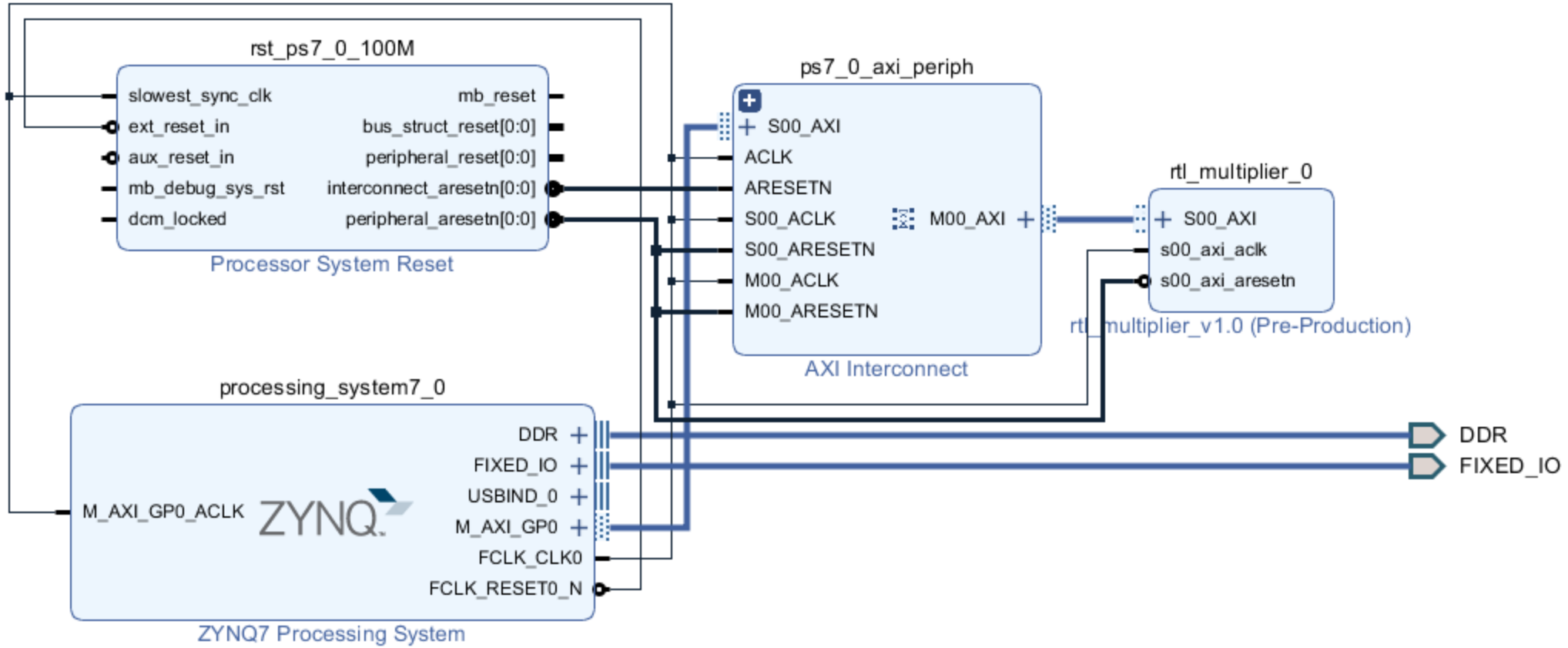


Image: Diligent

AXI Interconnect

- Manages data flow between AXI devices in FPGAs.



Software Support

- Utilize the **FPGA** part of Zynq AP SoC
  - Customize hardware with Verilog
- Utilize the **ARM-R9 processor** (with customized FPGA)
  - Programming with codes written in C
  - Programming with embedded Linux targets
    - e.g. using a PYNQ-Z1 image
    - Involves pre-built overlays, which define the connection between the processor and FPGA
    - Enables application written in Python

Tcl

- Simple, high-level, general-purpose, interpreted, dynamic programming language created in 1988.
- **Widely used in Electronic Design Automation (EDA)** for scripting and automating tasks within EDA tools such as Xilinx Vivado
- You will use Tcl in **Vivado Tcl Console** most of the time.
- See: *Reduced Tcl Tutorial All-in-One.pdf* on Canvas

```
start_gui
create_project lab1_1 F:/Documents/GitHub/ECE4810J_FA2022_TA/Lab1/lab1_1
 ↪  -part xc7z020clg400-1
set_property board_part digilentinc.com:arty-z7-20:part0:1.1
 ↪  [current_project]
```

Lab #1 Overview

- Setup Zynq7 Processing System
  - Add IP named “ZYNQ7 Processing System”
  - Connect with external hardware by “Run Block Automation”
  - Connect clock signal to AXI buses (for peripheral connection)
  - Add peripheral IPs to the Zynq7 platform
    - AXI GPIO through direct IP adding (e.g. buttons, LEDs)
    - Or use customized IP by Verilog definition (e.g. multiplier)
  - Create HDL Wrapper
  - Generate Bitstream
  - Connect everything by “Run Block Automation” again

Lab #1 Overview

- Interfacing with the IP Block in software
  - Export the hardware platform to Vitis (.xsa file)
  - Application setup (.c)
- Board Connection
  - Power supply through USB, configured by jumper JP5
  - Chip configuration through JTAG, configured by jumper JP4

Lab #1 Overview

Goals

- Get familiar with the board
- Set up the environment correctly
- Be able to build a basic Zynq system on the board
- Be able to create a custom IP in Verilog
- Be able to use AXI bus to connect an IP block with the Zynq programing system

Deliverables

- Details are in the Lab #1 description
- Peer evaluation form (individual grade)

References

- https://digilent.com/reference/programmable-logic/arty-z7/reference-manual
- Yichen Cai, 2023 Lab #1