ECEN 664 Nanotech Fabrication

Final Presentation

Enhancement on Ferroelectric Material Fabrication and Its Applications based on Computation In-Memory

Reference Paper

Y. -S. Kuo, S. -Y. Lee, C. -C. Lee, S. -W. Li and T. -S. Chao, "**CMOS-Compatible Fabrication of Low-Power Ferroelectric Tunnel Junction for Neural Network Applications**," in IEEE Transactions on Electron Devices, vol. 68, no. 2, pp. 879-884, Feb. 2021, doi: 10.1109/TED.2020.3045955.

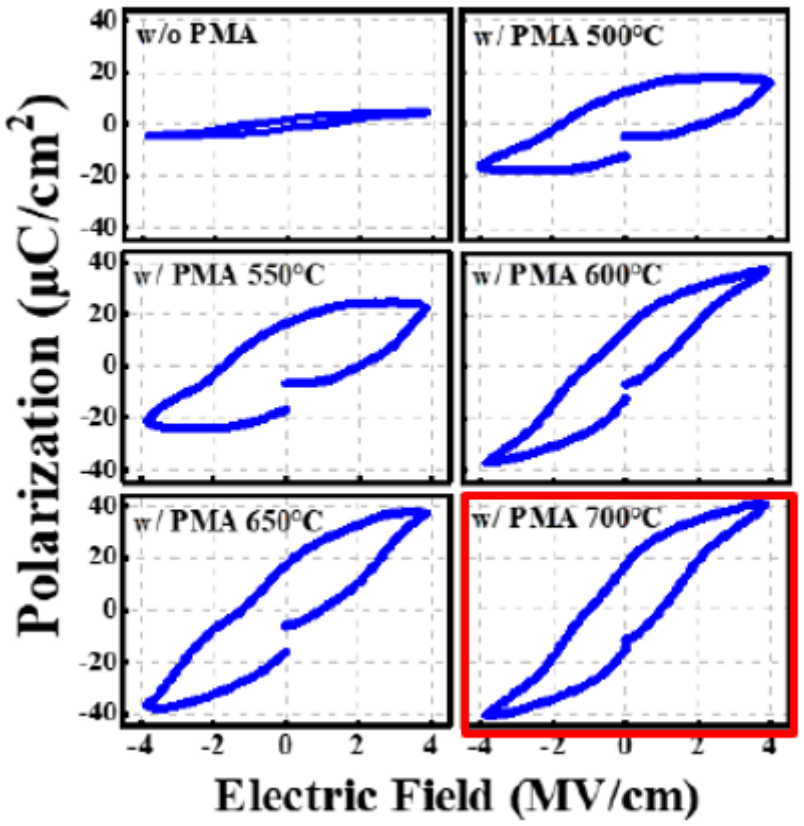
CEEN, Chun-Sheng Wu

Outline

- Ferroelectric Material Introduction – Why Important?
- Ferroelectric Material Based Transistor
  - Ferroelectric Tunnelling Junction (FTJ) Transistor
  - Ferroelectric Field Effect Transistor (FeFET) <= Challenge
- Improvement
  - Transistor Characteristic: Gate-All-Around (GAA) Double Layer FeFET
  - Applications: Novel SRAM, Computation In-Memory (CIM) Unit
- Summary

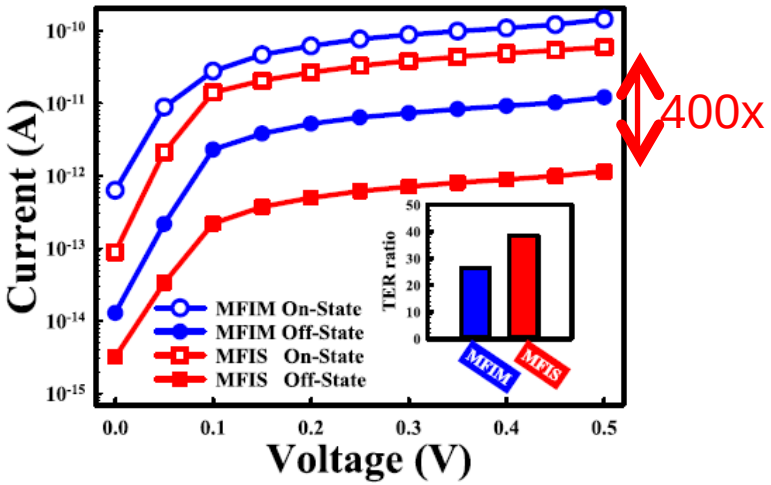
Ferroelectric Material Introduction

- Under different fabrication factors, ferroelectric material behaves various hysteresis curves



Negative Capacitance

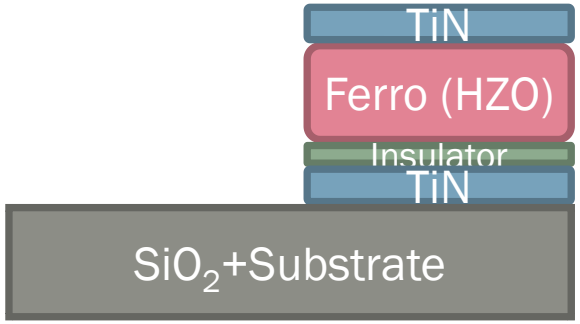
- By imposing positive voltage, the alignment of ferroelectric material becomes uniform. On the contrary, the alignment becomes amorphous with negative voltage
- Uniformity helps increasing the current



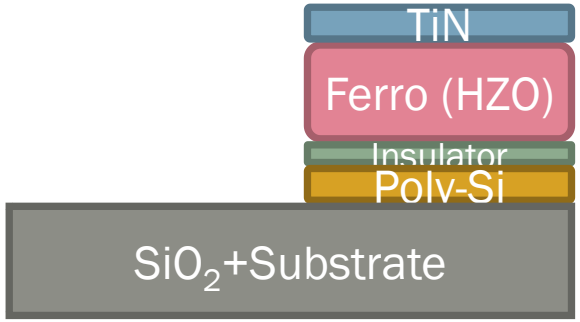
- Determine high/low (1/0) states by distinguishing current level => Phenomenal Non-volatile Memory!!

Ferroelectric Material Based Transistor

- Ferroelectric Tunneling Junction (FTJ) Transistor

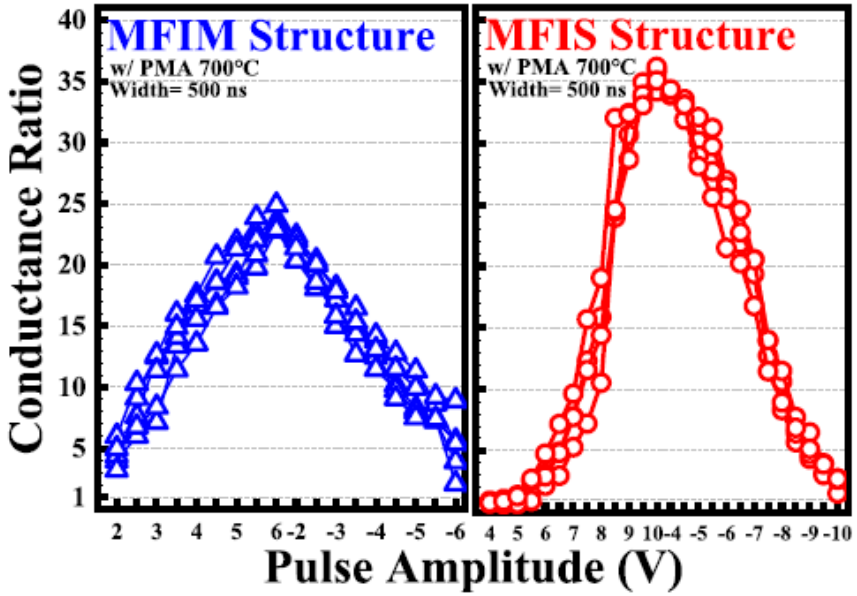


Metal-Ferro-Insulator-Metal
(MFIM)



Metal-Ferro-Insulator-Poly_Si
(MFIS)

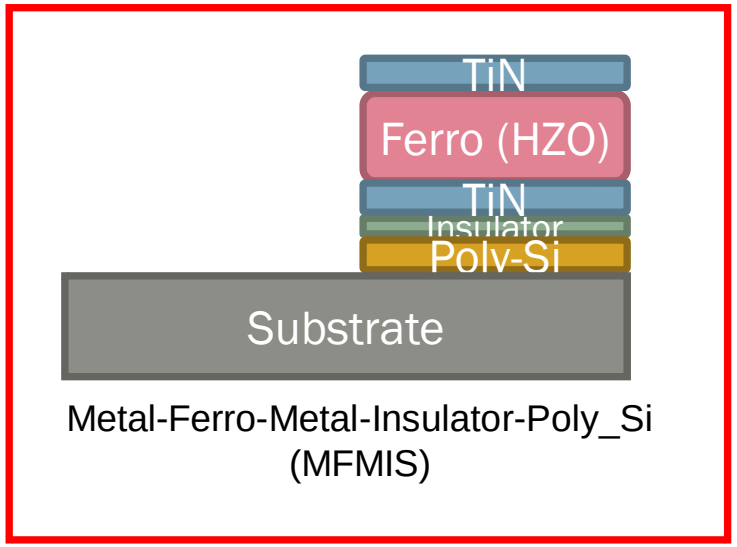
- Two common stacking methods are MFIM and MFIS
- Due to the screening length and series resistance, MFIS has much better conductance than MFIM
- Higher conductance lowers the action voltage, which is beneficial for dynamic energy consumption



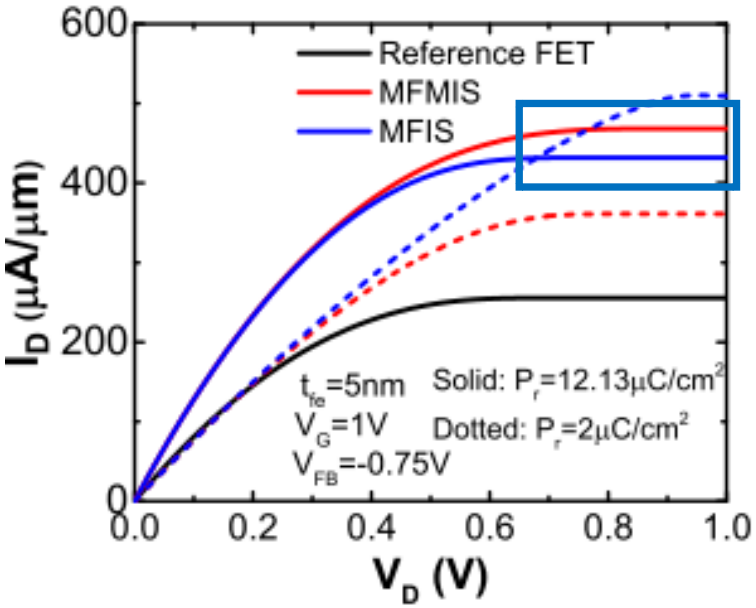
Ferroelectric Material Based Transistor (Cont.)

- Ferroelectric Tunneling Junction (FTJ) Transistor

Best Performance



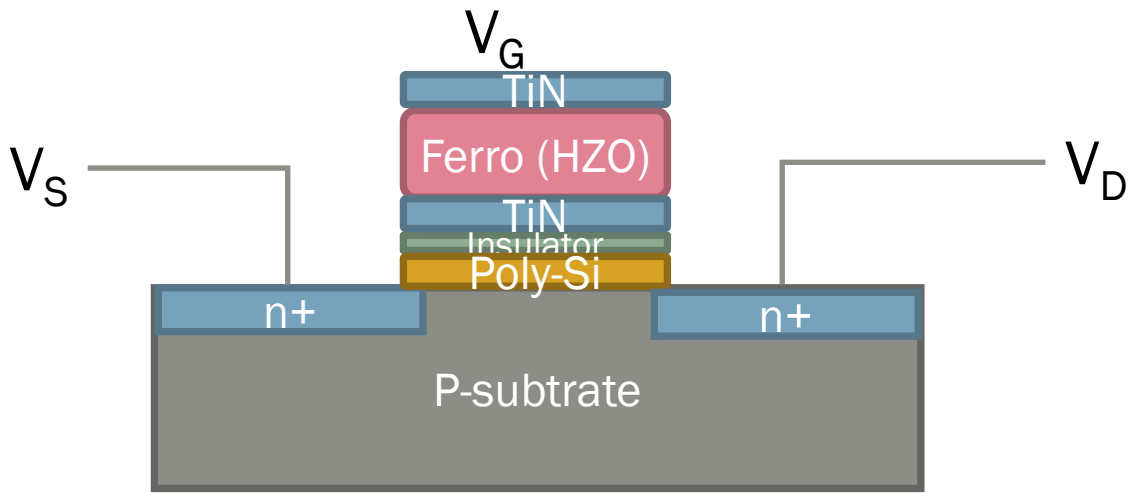
Metal-Ferro-Metal-Insulator-Poly_Si
(MFMIS)



- Additional metal layer to increase the electrons transmission
- Potential to gate fabrication

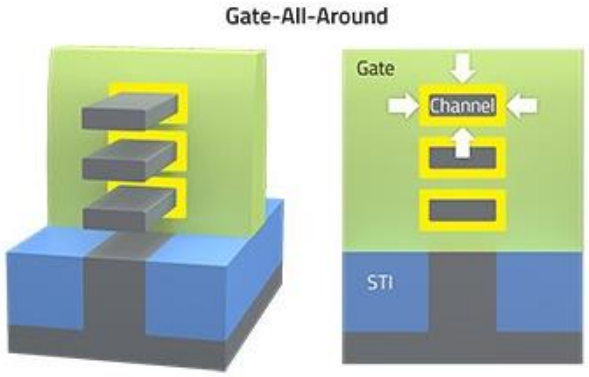
Ferroelectric Material Based Transistor (Cont.)

- Ferroelectric Field Effect Transistor (FeFET)



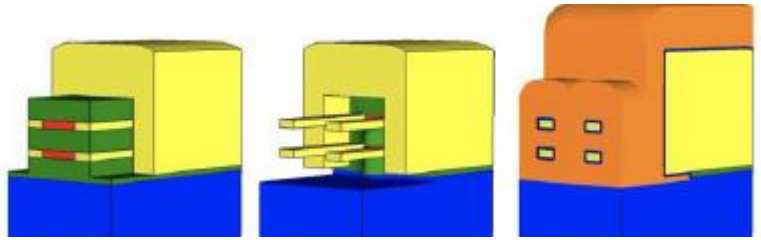
- Imposed V_G makes internal ferro structure changed to uniform (1) or amorphous (0)
- Stored states can be applied to memory without dynamic updating
- BUT, How to increase the current to at least mA?

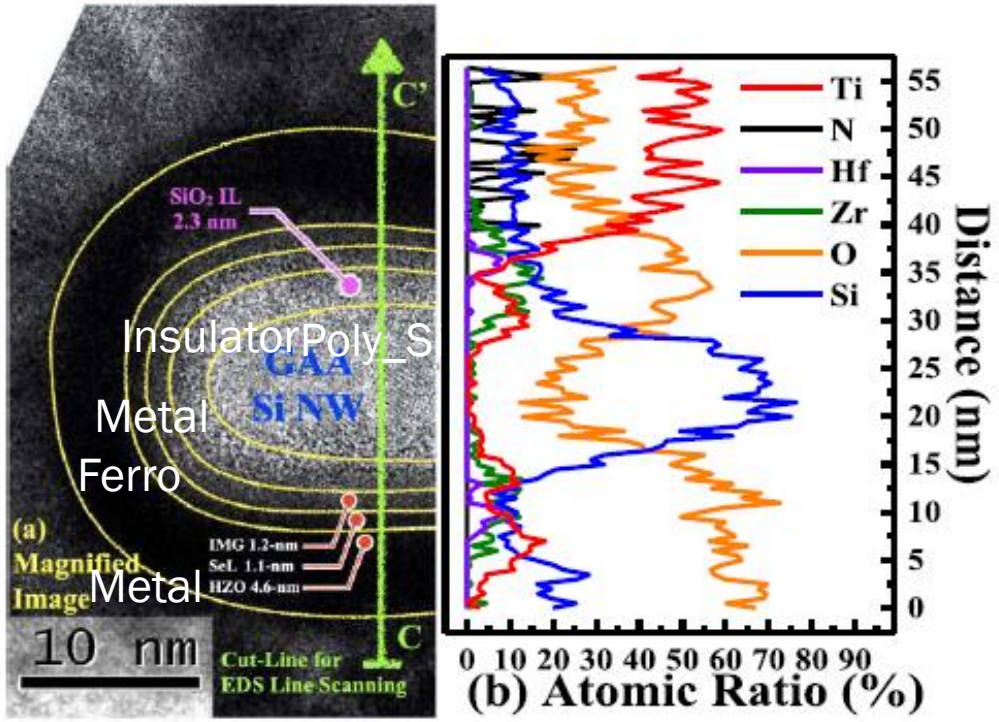
Improvement - Gate-All-Around (GAA) Double Layer FeFET



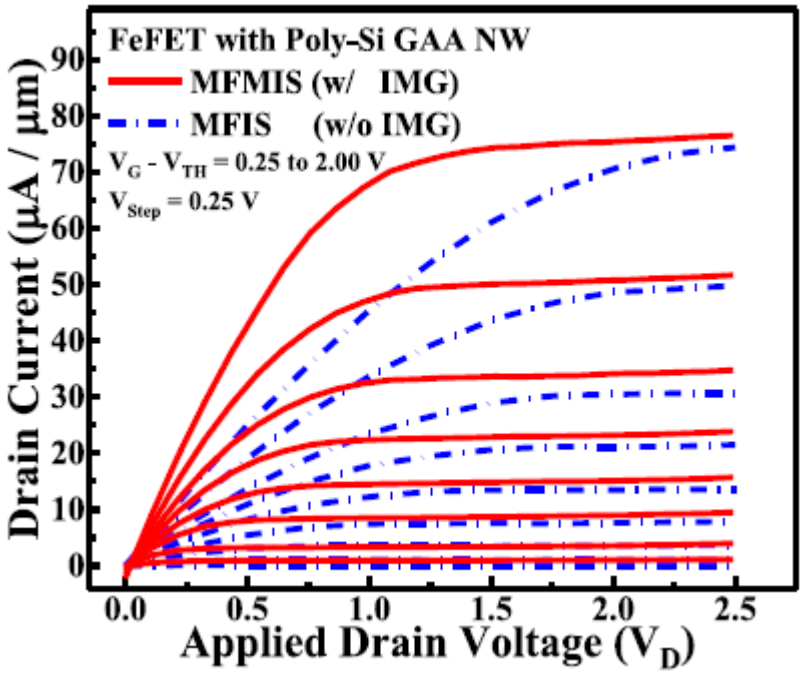
Wet-etching to fabricate nanowires
-> 4-directional ALD to deposit enclosing structures

- Every stick is a single channel connected from gate to active regions, stacking from body (metal) to internal poly-silicon (Poly-Si)
- Double Layer GAA nanowire can further increase current with multiple gate channels

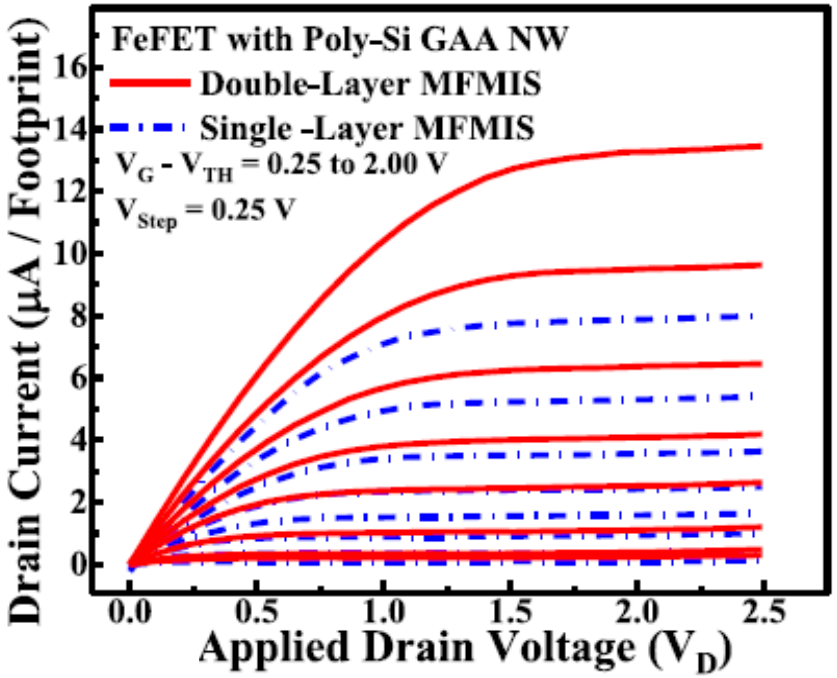




Improvement – GAA Double Layer FeFET (Cont.)



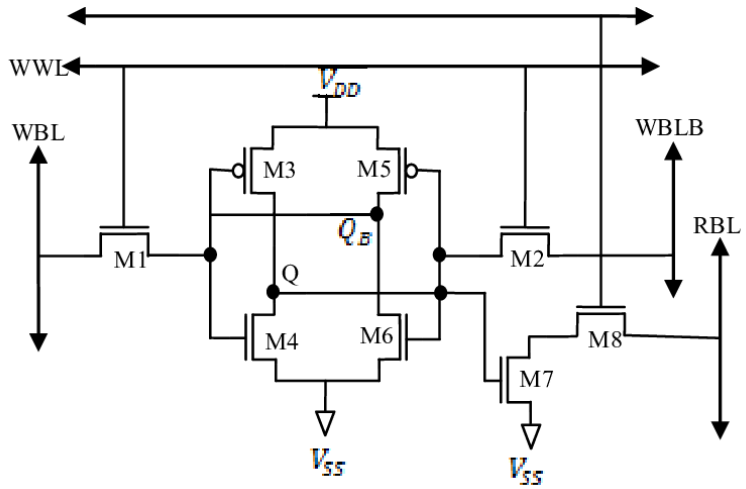
Footprint = 10nm



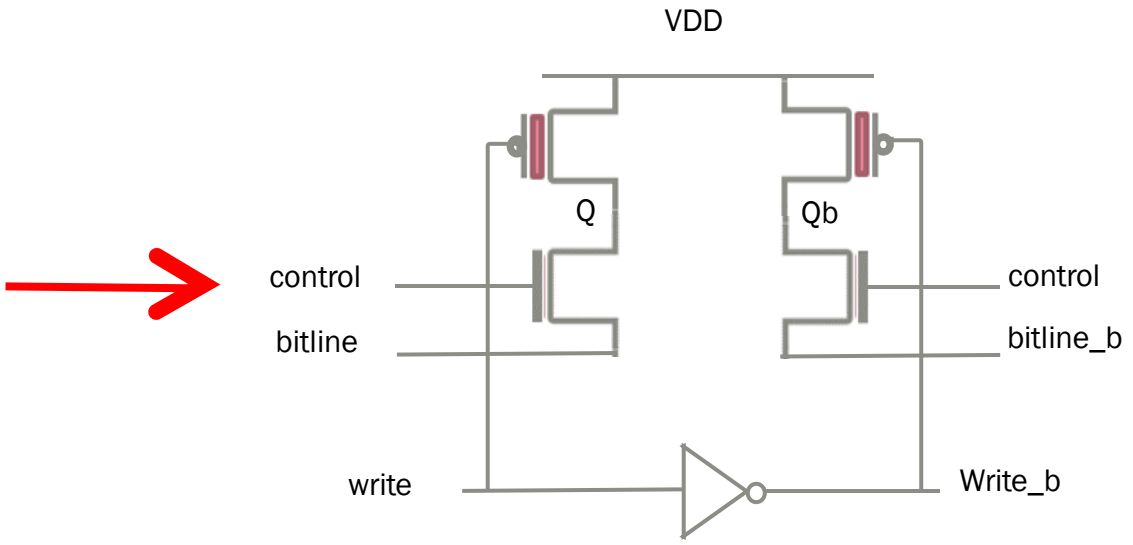
- Significantly reduce the channel length modulation (CLM)
- With GAA double layer structure, current increase from 0.5 mA/um to 1.1mA/um @V_D = 1V, V_G = 1V
- Besides active current increase, GAA structure benefits the gate controllability by more contact areas between channels and gate

Improvement - Replace 8T SRAM with 4T structure

- Replace conventional PMOS to p-FeFET to store the desired states
  - Keep similar read/write accessibility
  - Enable dynamic modulation by synchronize control with time signal
  - Reduce the area by 50%

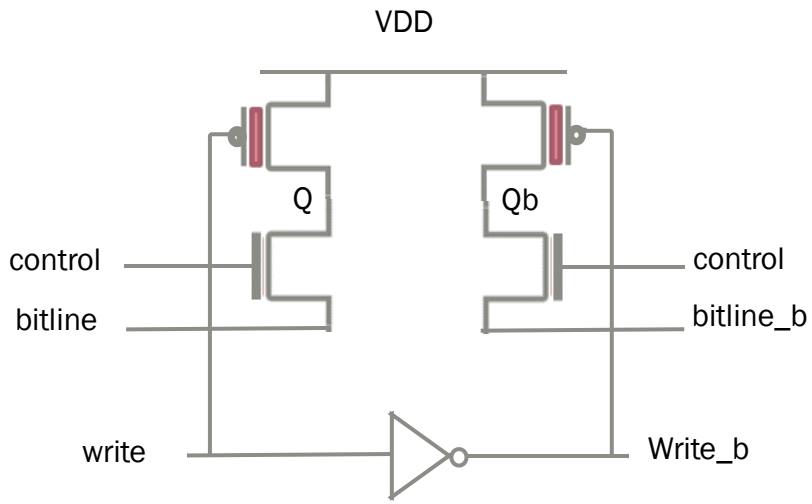


Conventional 8T SRAM



Modified 4T Fe-SRAM

Read / Write in This SRAM



Read

1. bitline & blitline_b & control precharge to be “1”
2. “0” will pass from Q/Qb
3. Turn control & bitline & bitline_b into “0” to regain initial state (gnd depends on the piplining)
4. Float ports

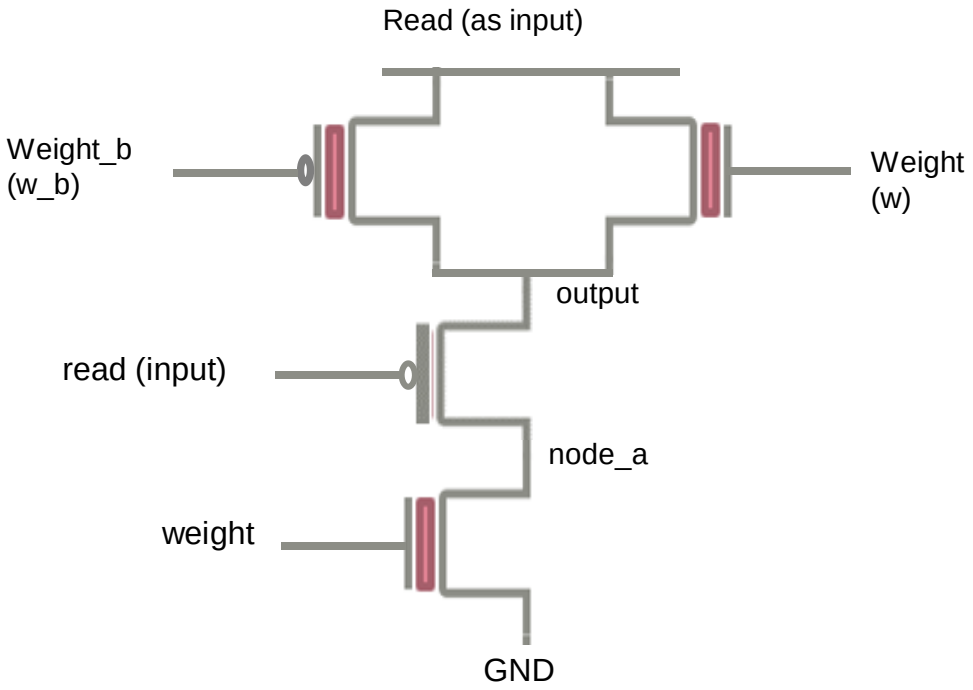
Write

1. Precharge control to “1” and bitline & bitline_b to be “0”
2. Write to the gate of FeFETs to change states
3. Turn off ports

**need big width in nmos to make sure data passing

Improvement - Transform FeFET into a Convolution Unit

- Convolution layer with non-volatile stored weights
  - Eliminate redundant time of computing and communication
  - In universal pipelining machine, it can reduce 65% time with parallelized instructions
  - Better reinforce training efficiency while the neural network grows deeper



Proposed CIM Unit

w_b / w	read (input)	node_a	output
0 / 1	GND	0	0
0 / 1	VDD	0	0
1 / 0	GND	X	0
1 / 0	VDD	X	1

Summary

- GAA Double Layer Technology helps increase active current by 120%
- Modified Fe-SRAM can reduce the effective area by 50%
- Applying FeFET into CIM can eliminate the time of computing and communication between processors, therefore decreasing 65% of time in universal pipelining machine

Thanks for Your Attention :)