專題進度報告

NEURAL NETWORK BASED ON CIM WITH FERRO-MATERIAL

0612020 吳峻陞 0612119 呂宗翰

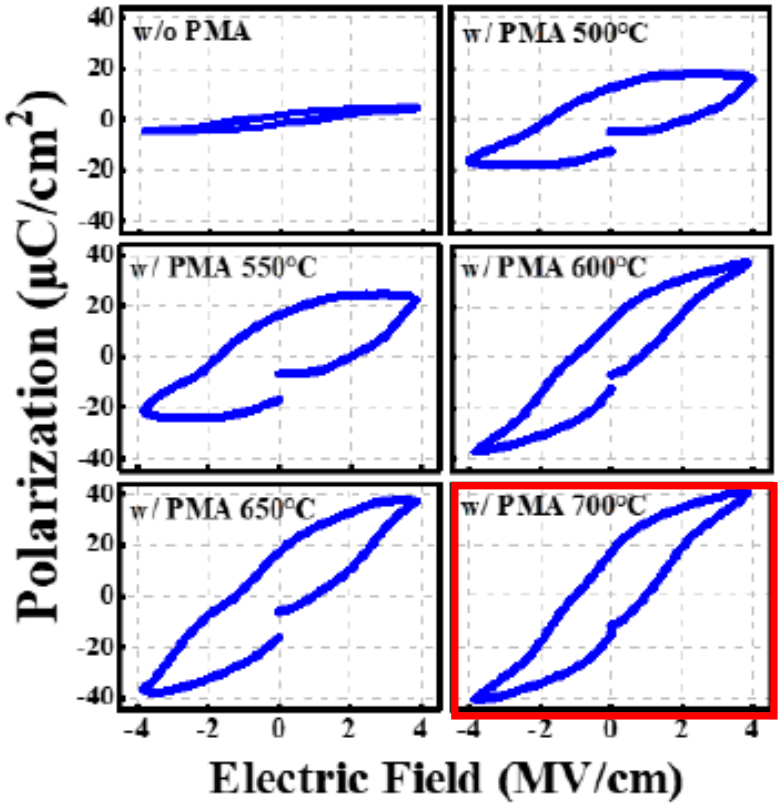
Structure and Implementation

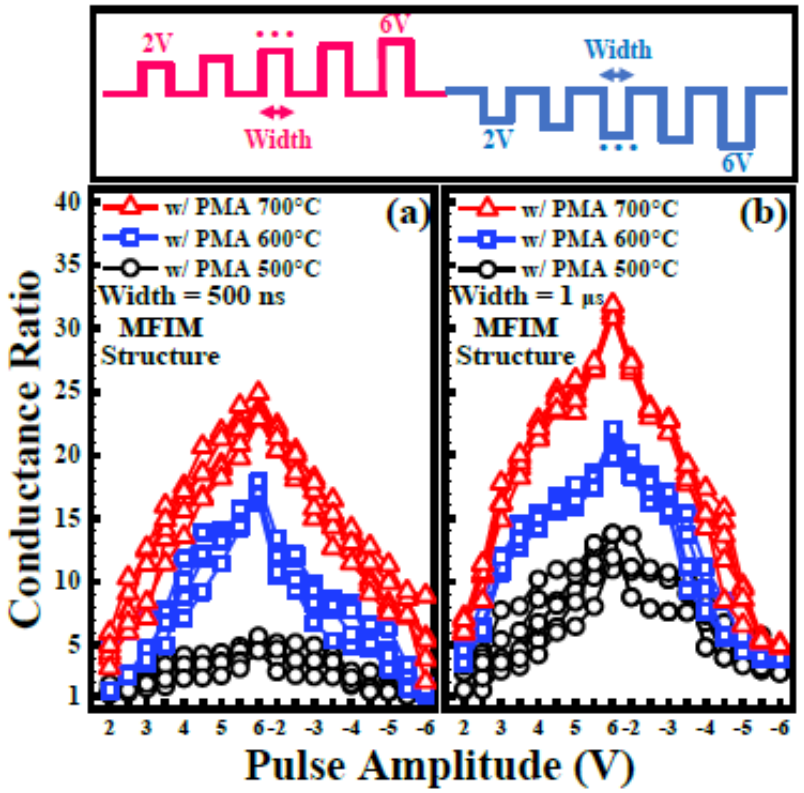
a. Ferroelectric Material Characteristic Applications
   - Ferroelectric Tunnelling Junction
   - Ferroelectric FET

b. Intrinsic Logic Design and Unit Cell (Neuron) Design

- Ferroelectric Tunnelling Junction

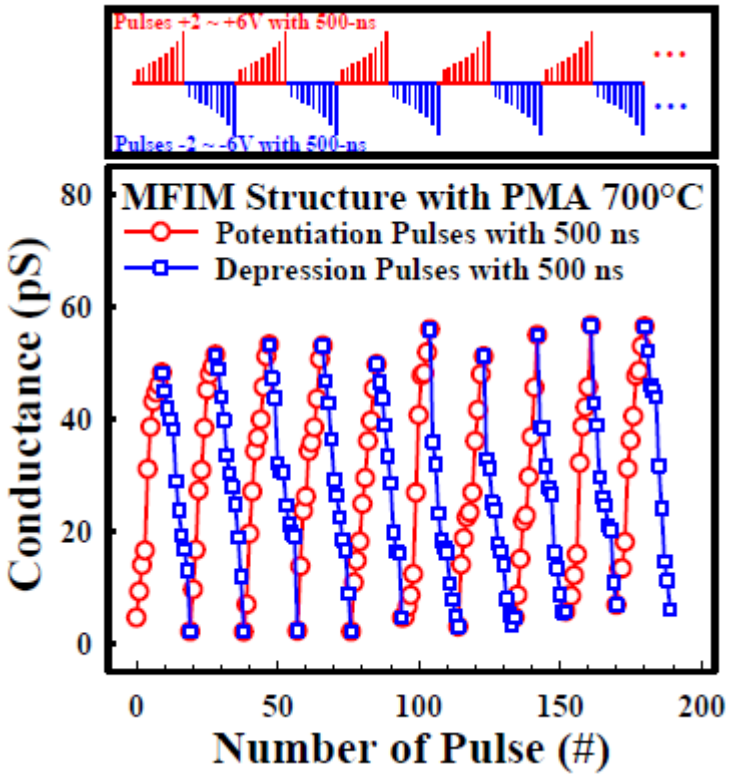
Variation by Temperature

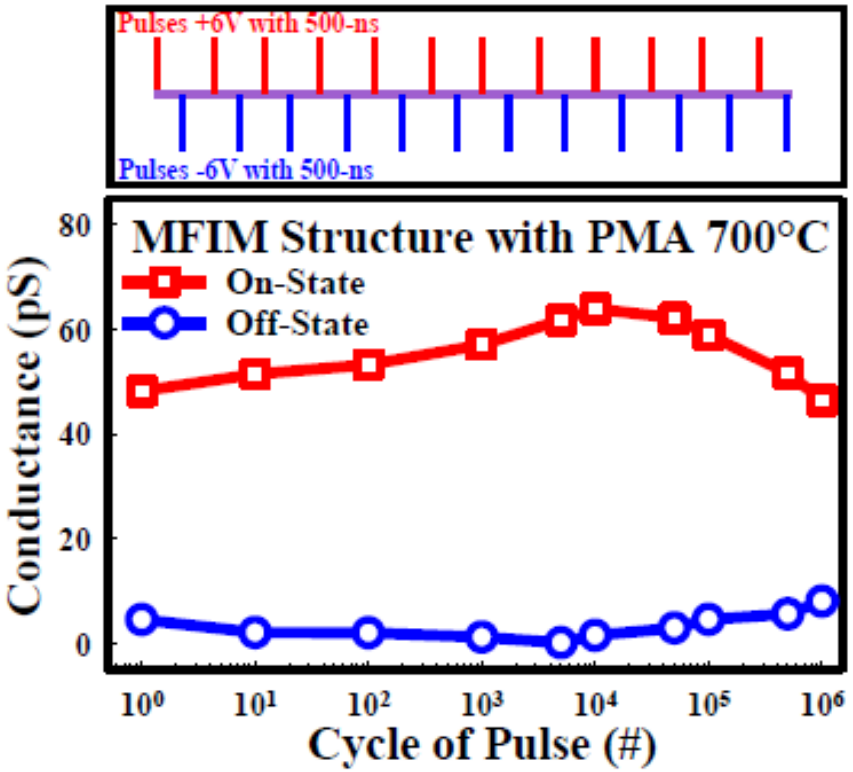




FTJ processed by PMA 700°C has the best window and symmetrical alignment distribution

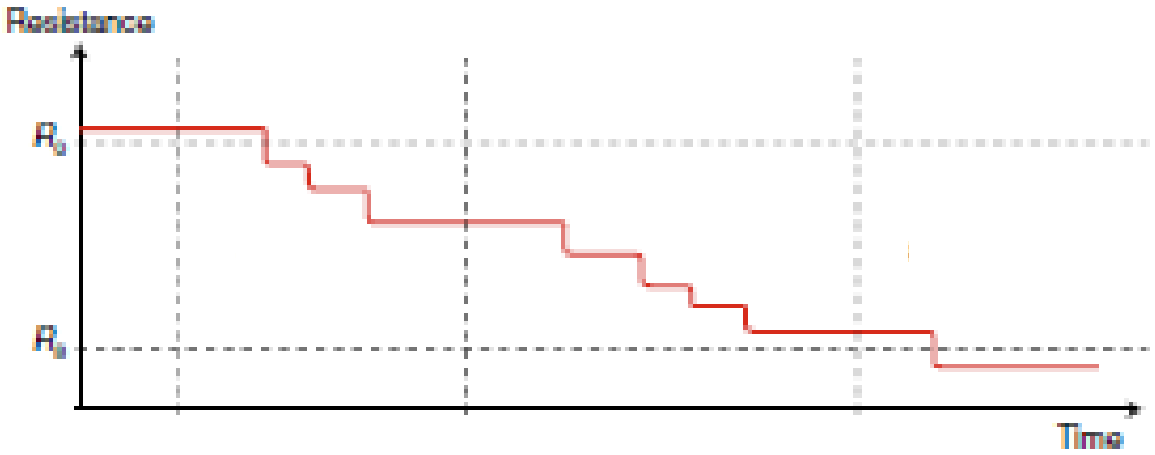
Binary State of Ferroelectric Material





Using Conductance Difference to determine 0-1 state

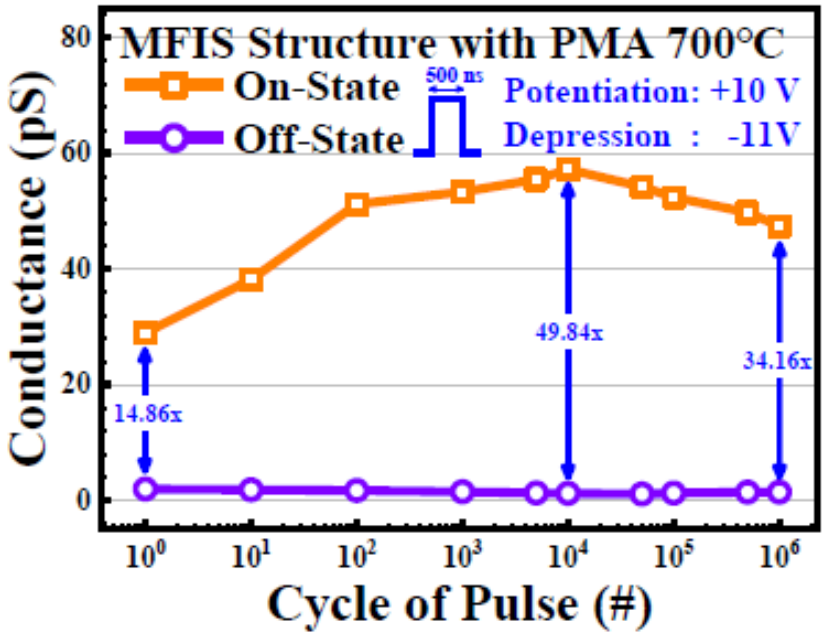
Multi-state Feasibility in long-term pulse exertion

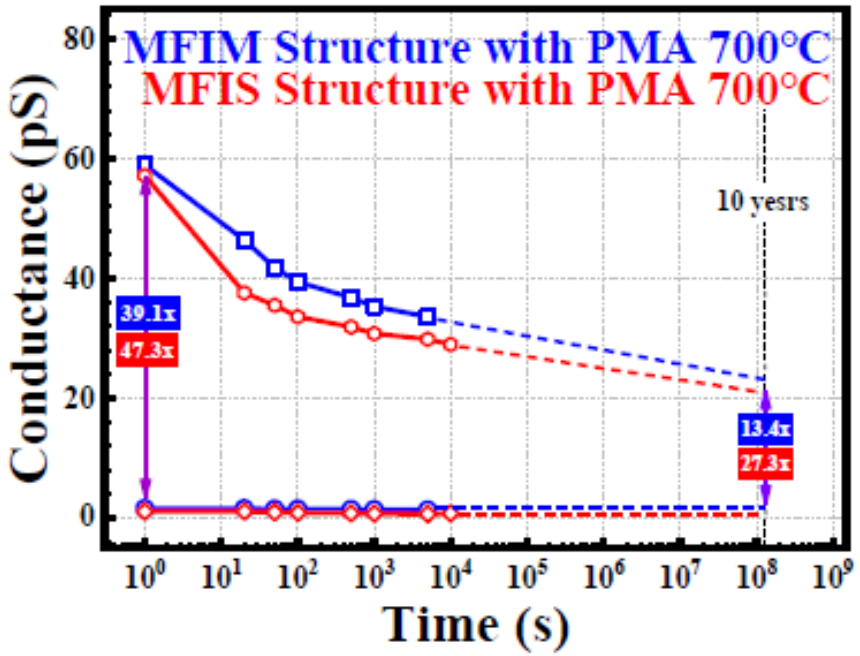


By applying appropriate buffer layer, the step-like resistance change have the possibility to implement multi-state in a single neuron

Endurance and Memory Effect after operations

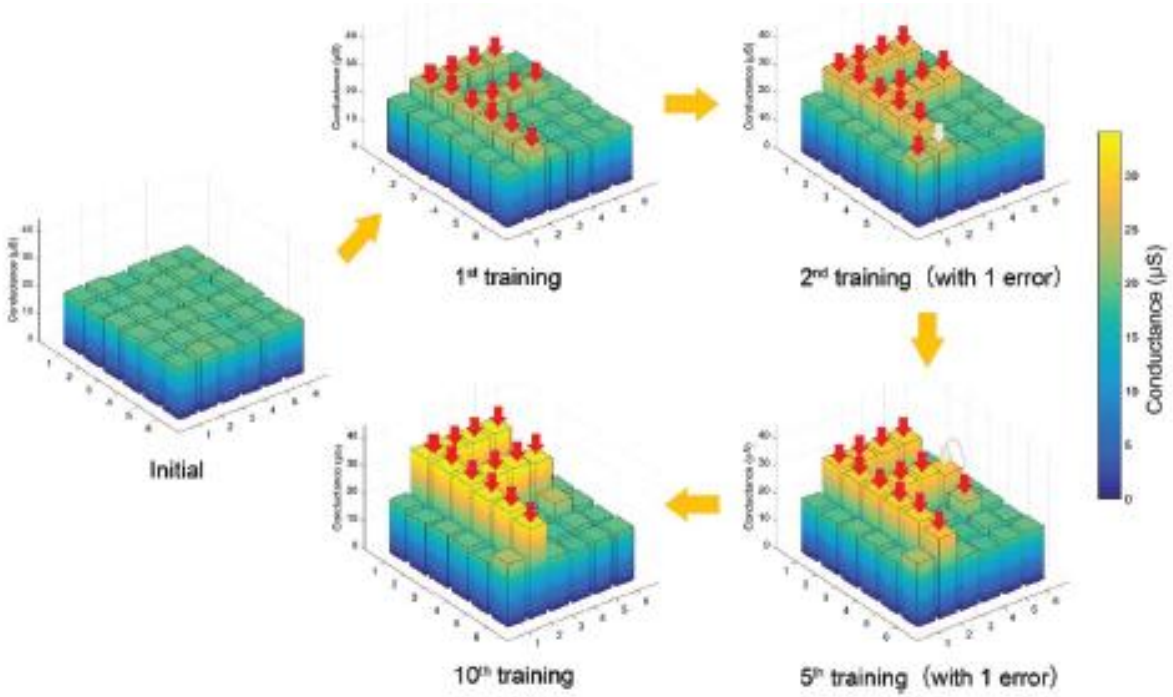
Fatigue!





FTJ provides sufficient gap for sensoring

As training interface



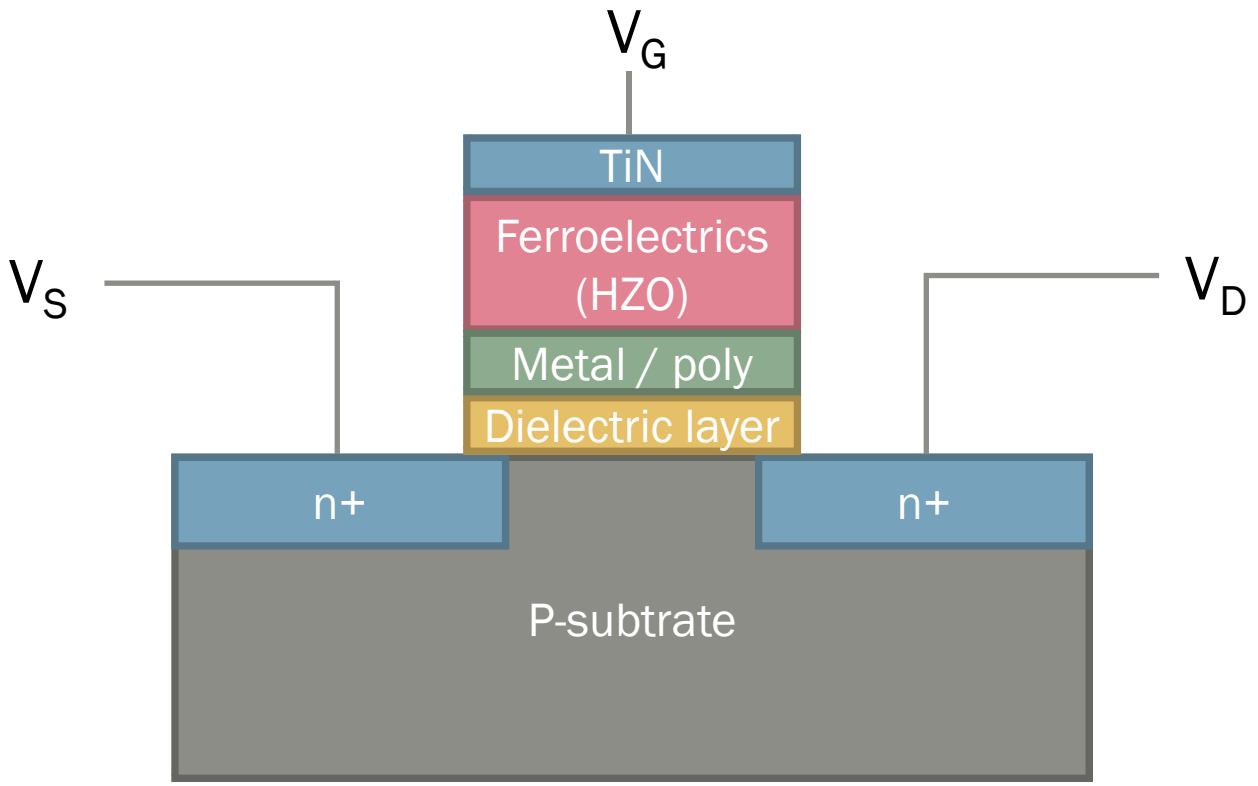
1. With repeatedly inputting same training pattern, the increasing conductance can augment the performance as neurons

2. Flexibility to assign higher on/off standard to eliminate possible errors

一、Structure and Implementation

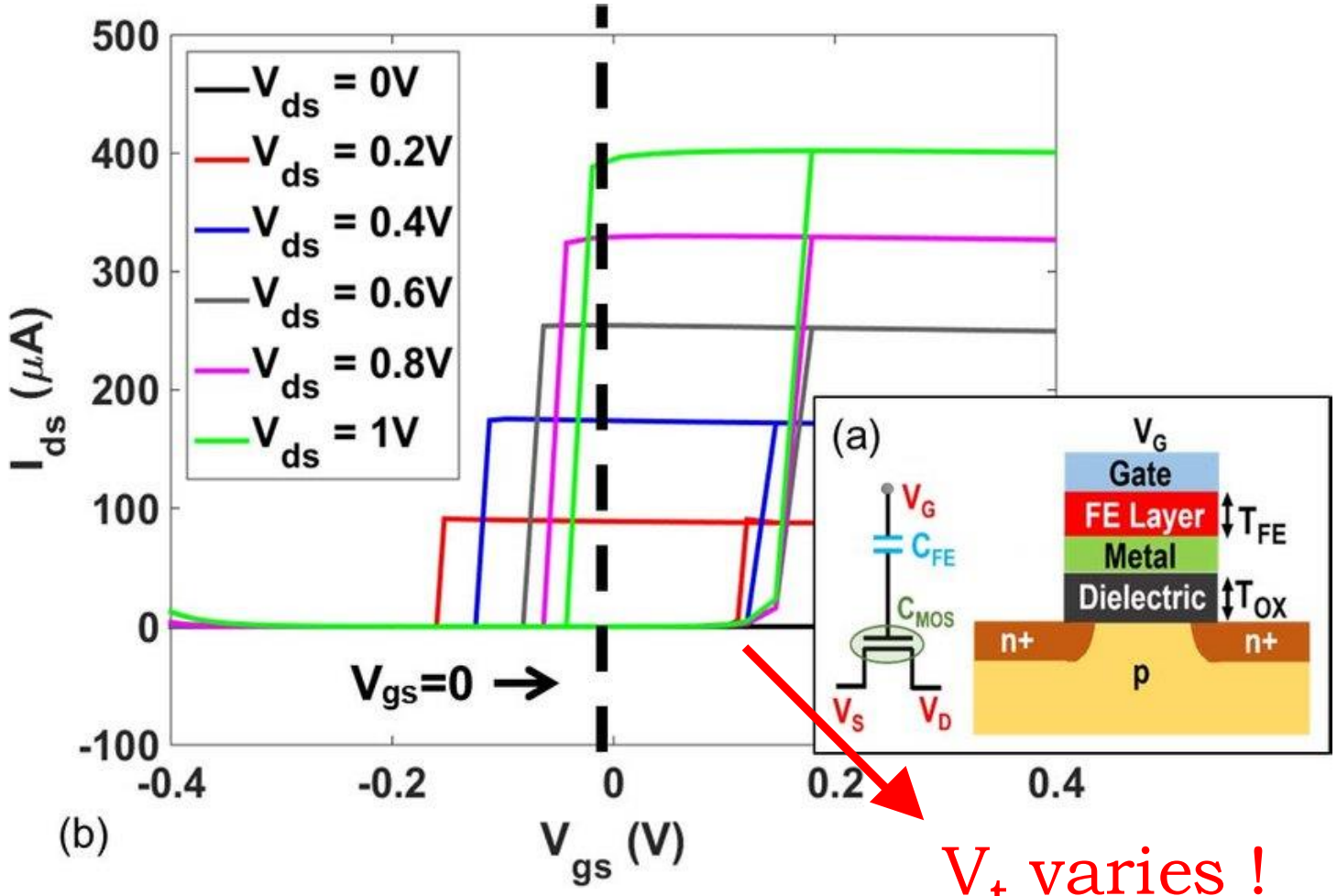
- Ferroelectric FET

FET with Ferro-Material in Gate

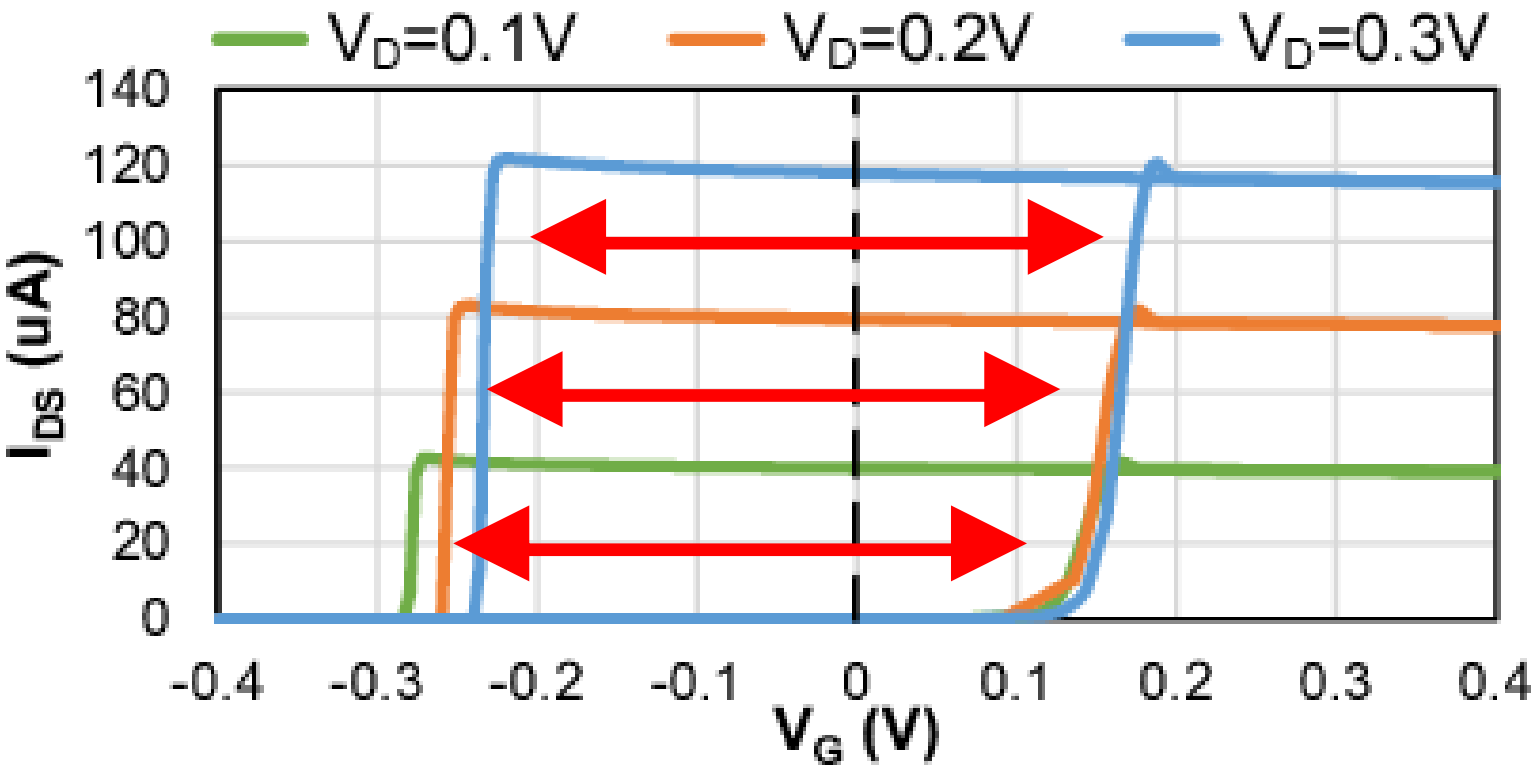


VGS -> Charge and discharge (HRS or LRS)
VDS -> On or Off FeFET

FeFET Characteristics



Method to distinguish states



The states will be distinguished due to different V_t (FET on or off) by employing the same V_{DS}

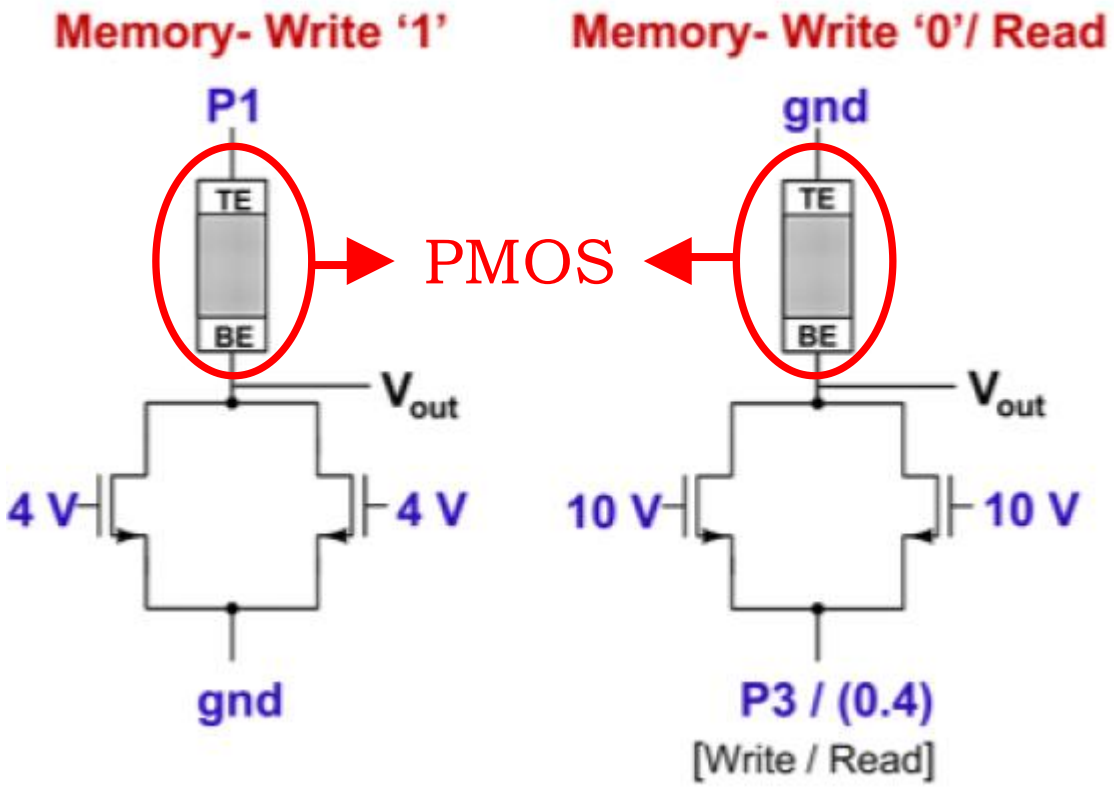
Benefits

- Same memory architecture with common MOS
- Non-Volatile MOS (no leakage current)
- Compatible speed and scalability with MOS nowadays

b. Intrinsic Logic Design and Unit Cell (Neuron) Design

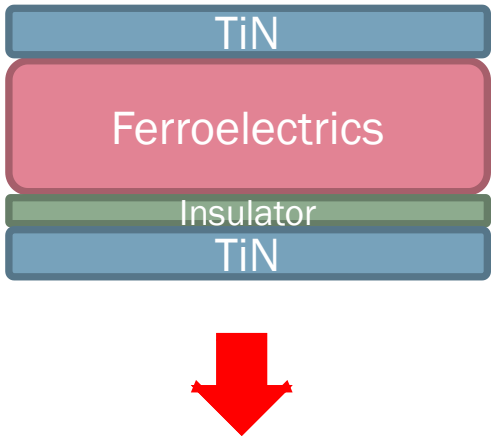
- FTJ

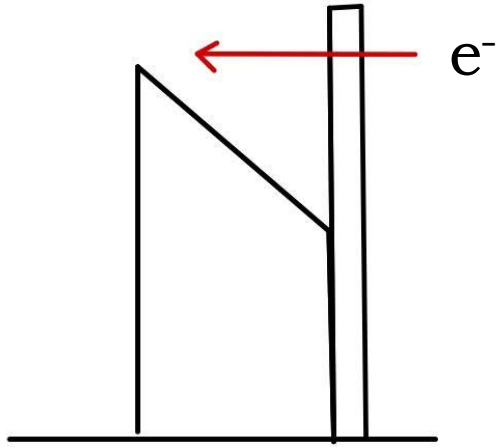
Concept with FTJ

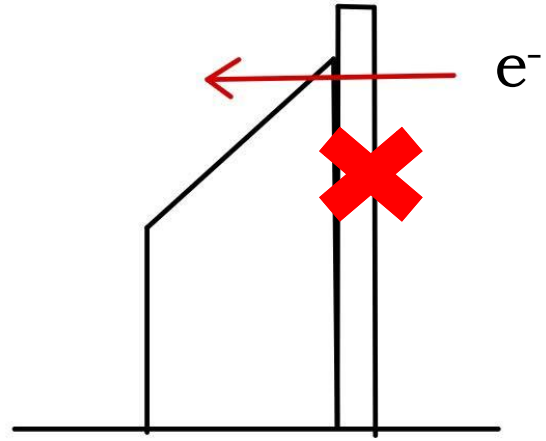


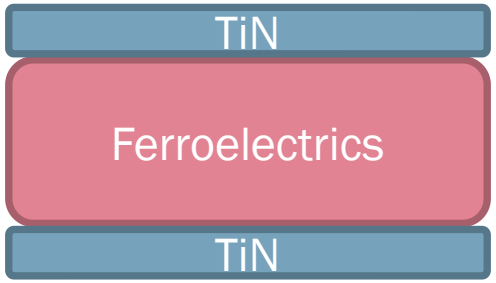
Inspired by this seemingly pseudo circuit, FTJ has potential to be operated like a complementary NMOS

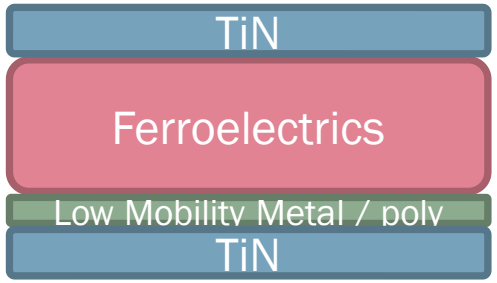
Concept with FTJ





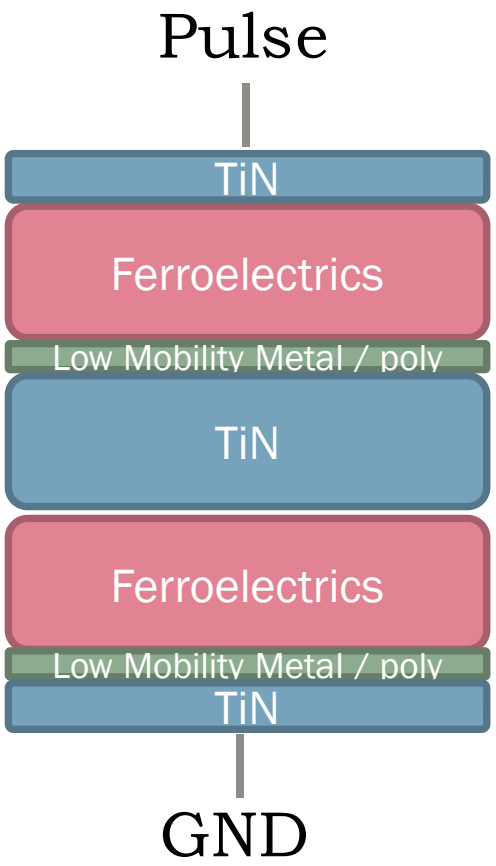




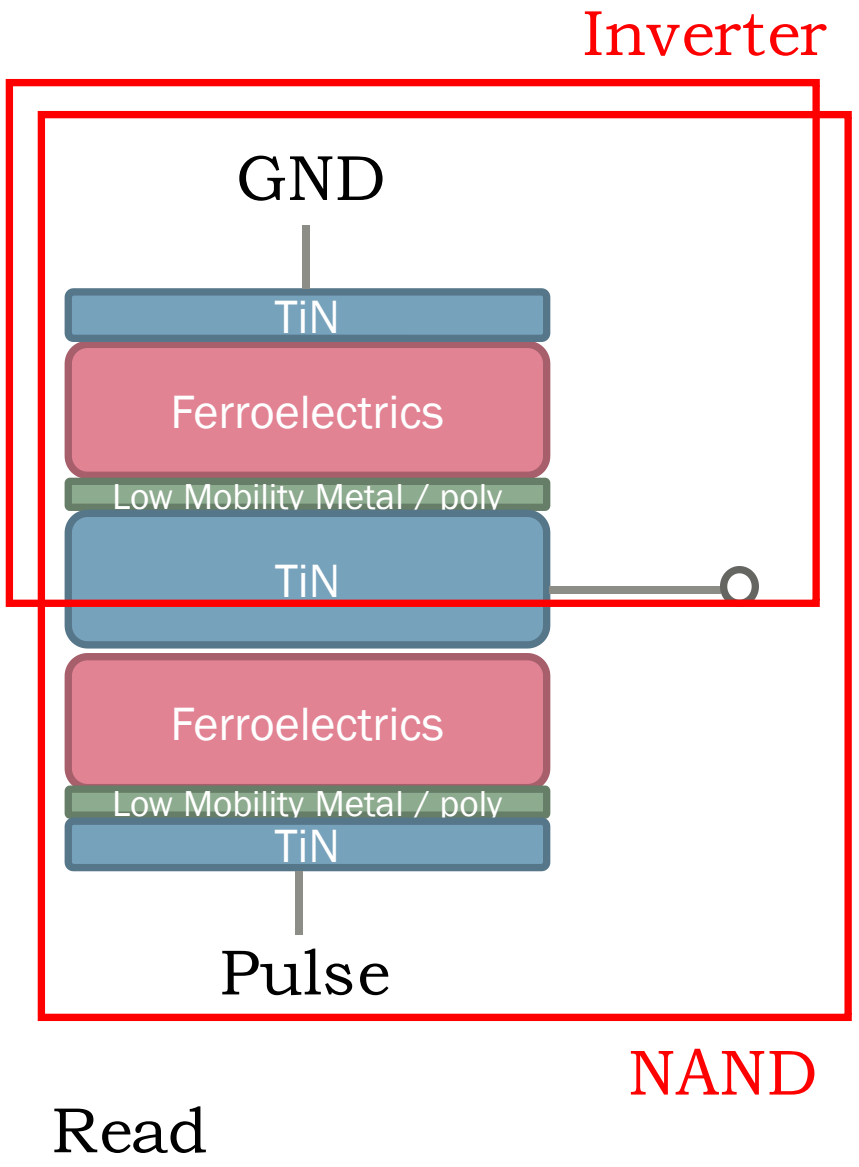


To deal with the barrier problem of inverse direction of read and write, I attempt to use loss mobility metal, which has the same effect to release trapped electrons as insulator, or eliminate insulator to perform logics

Logics of FTJ

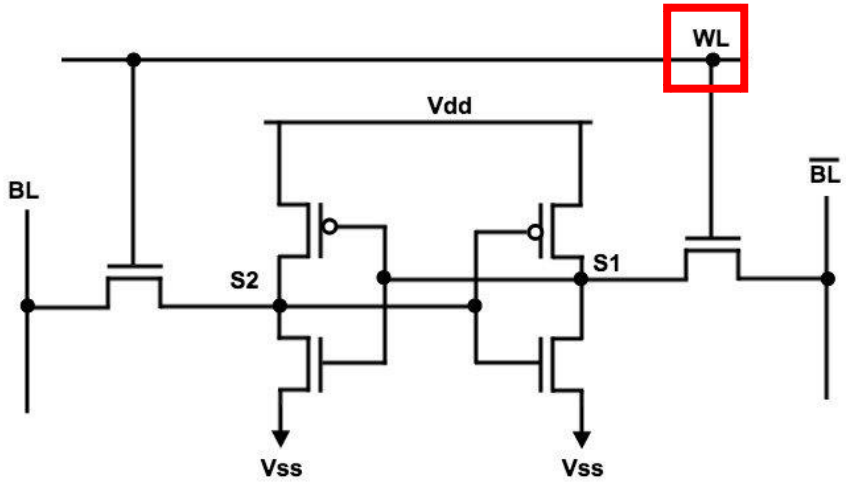


Write

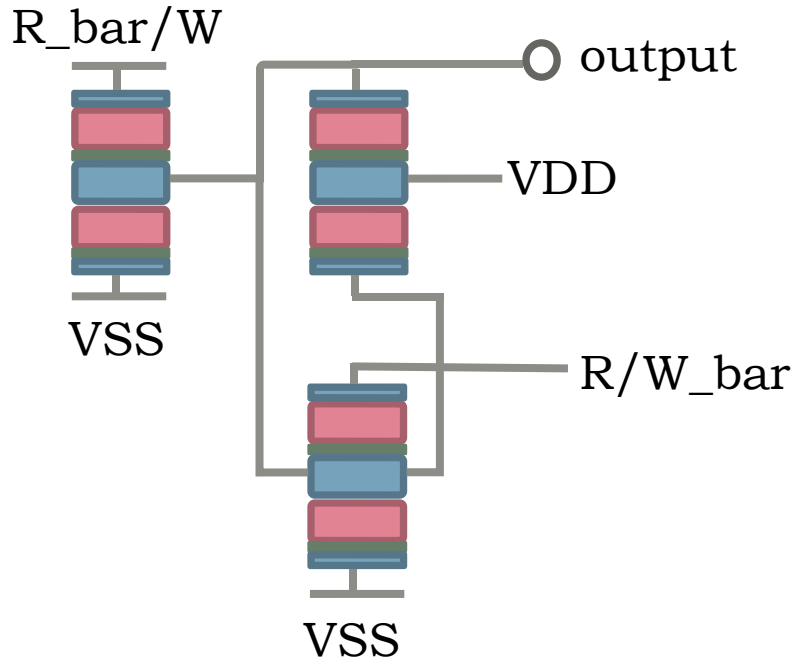


Read

SRAM with FTJ



=

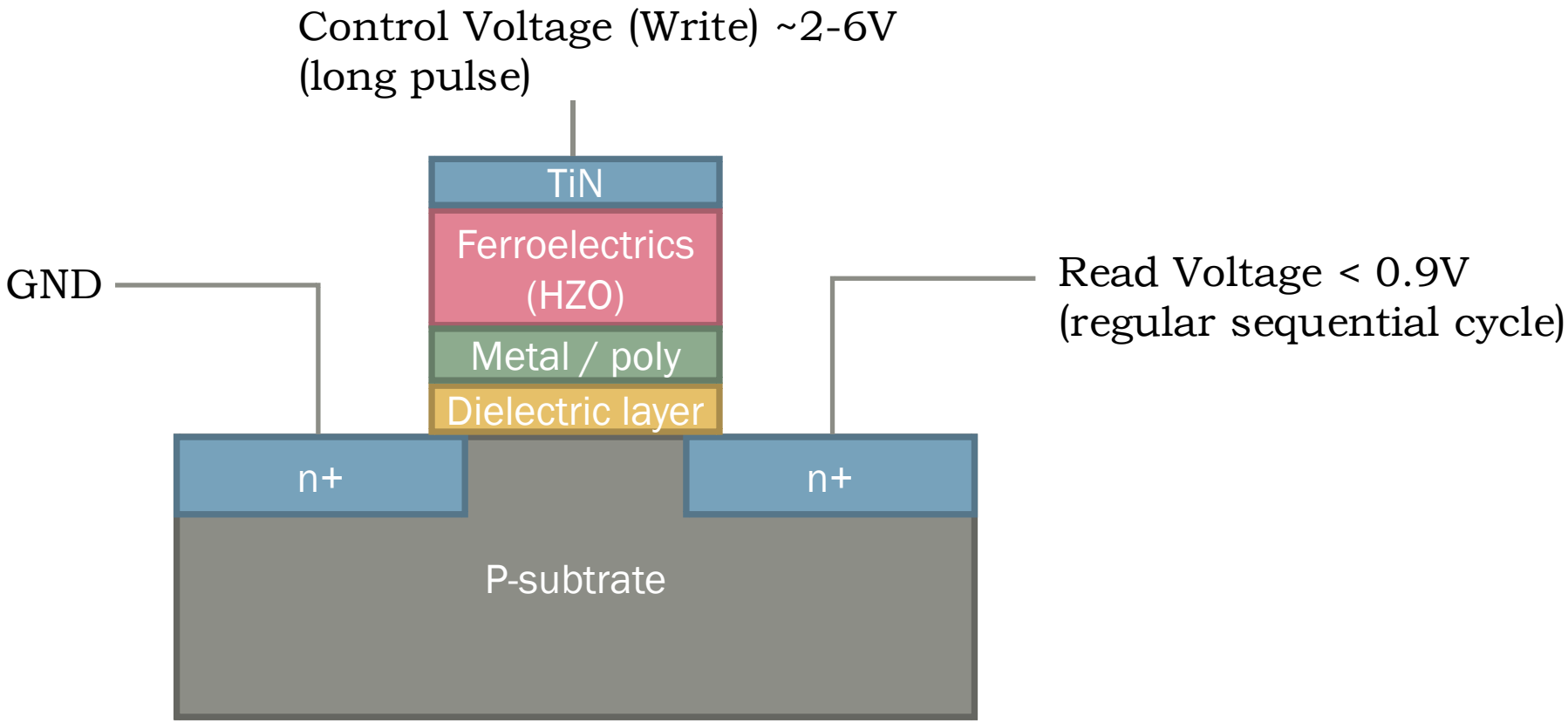


Simulating the structure of SRAM, we can accordingly design FTJ SRAM while inputting write pulse as 6V and read pulse as 0.8V in reverse directions,

b. Intrinsic Logic Design and Unit Cell (Neuron) Design

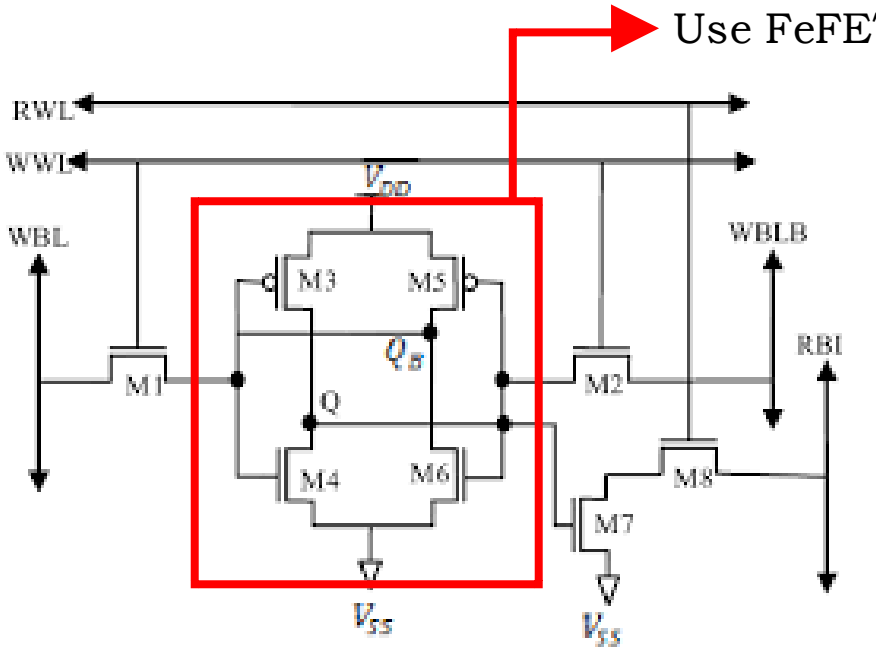
- FeFET

Concept with FeFET

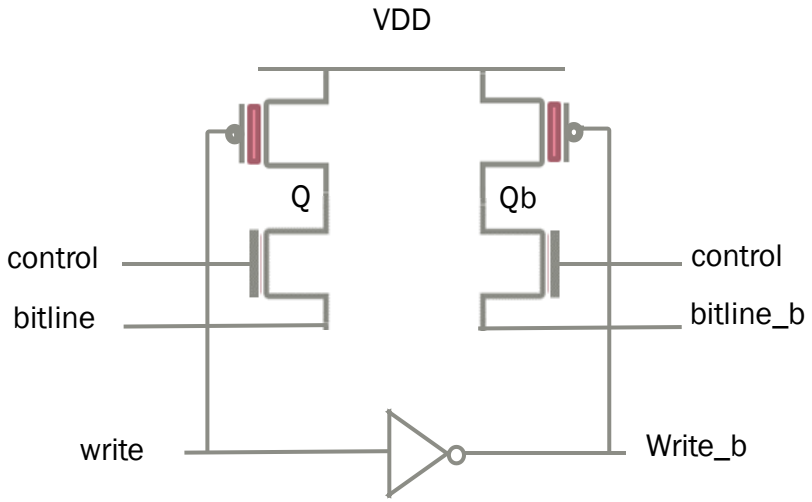


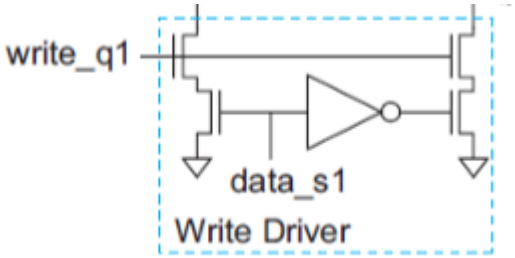
As controlling V_{GS}, we can make FeFET 1/0 by inspecting its I_D and correspondent resistance

FeFET as novel-SRAM



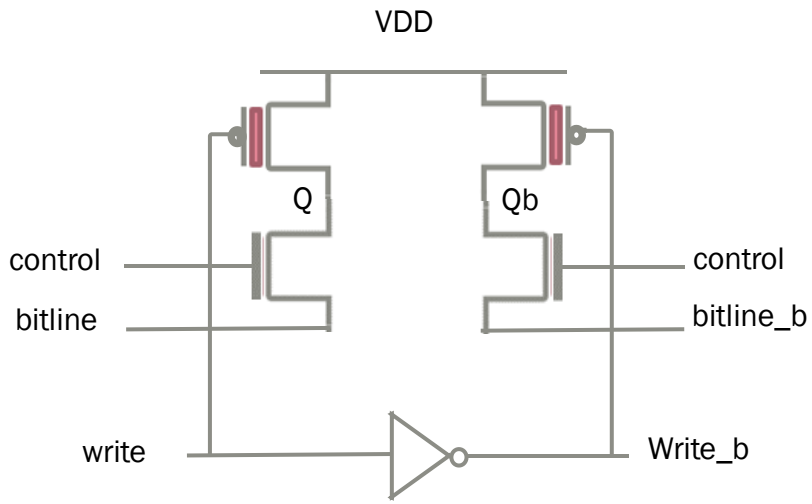
8T SRAM nowadays





Modified into just ports

Read / Write in This SRAM



Read

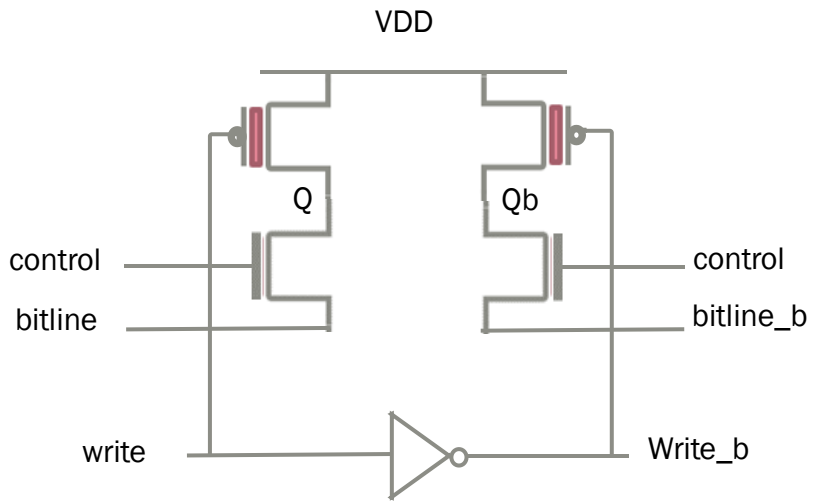
1. bitline & blitline_b & control precharge to be “1”
2. “0” will pass from Q/Qb
3. Turn control & bitline & bitline_b into “0” to regain initial state (gnd depends on the piplining)
4. Float ports

Write

1. Precharge control to “1” and bitline & bitline_b to be “0”
2. Write to the gate of FeFETs to change states
3. Turn off ports

**need big width in nmos to make sure data passing

Pros and Cons in This SRAM



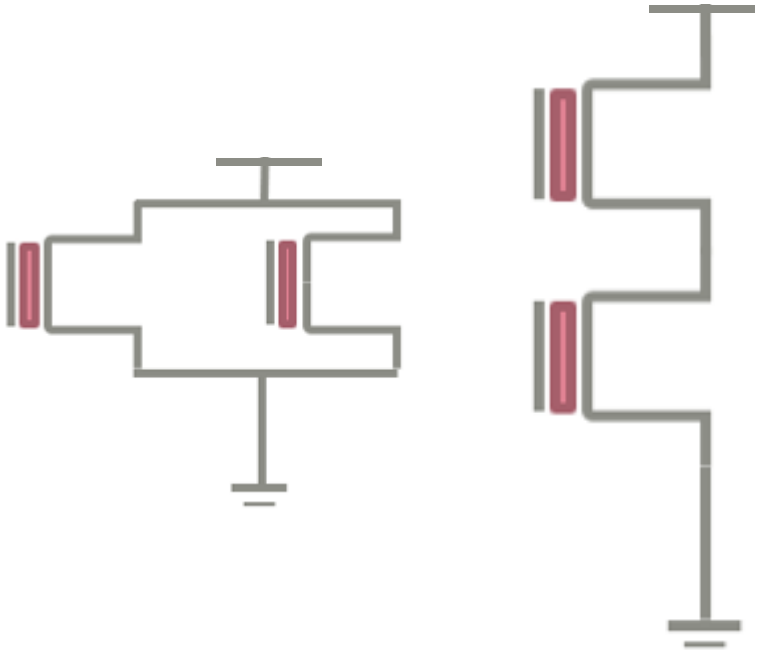
Pros

1. Less area and No. of mos
2. Less data fluctuation due to FeFET
3. Easy Operations
4. High potential to circuit extensions
5. Good Flexibility

Cons

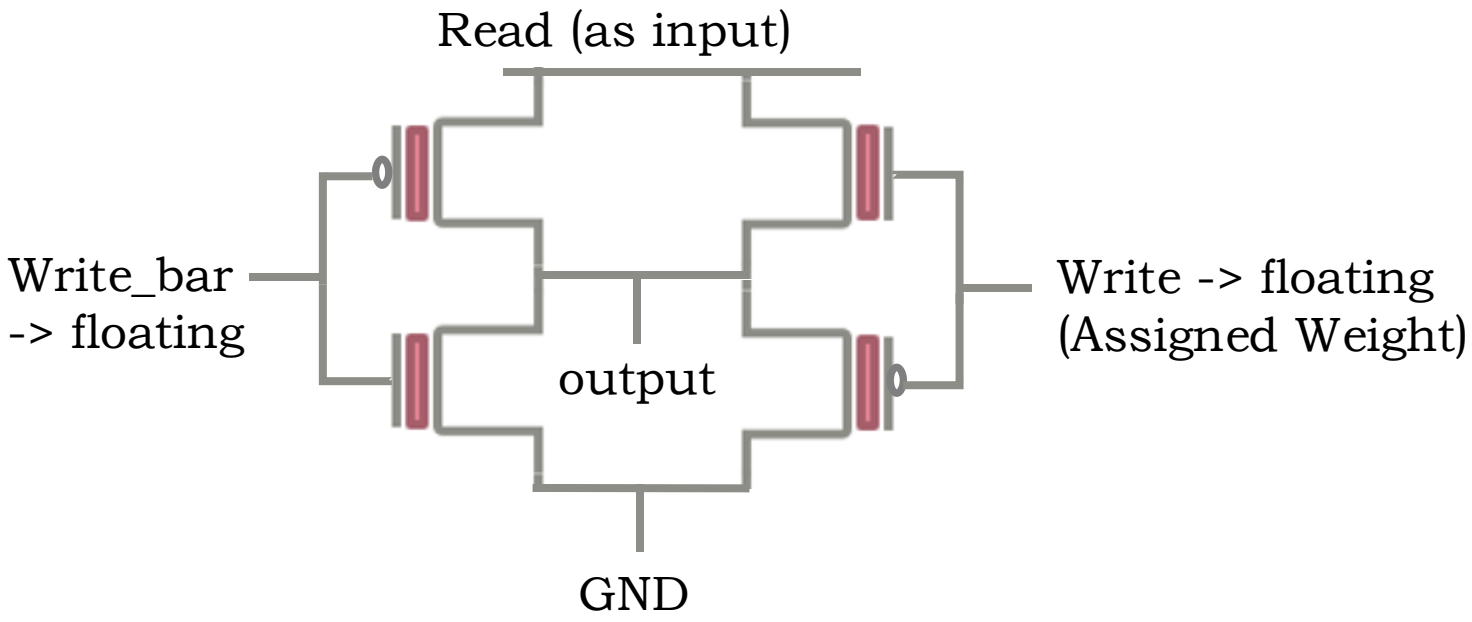
1. More ports to satisfy operations
2. More complicated datapath and routing

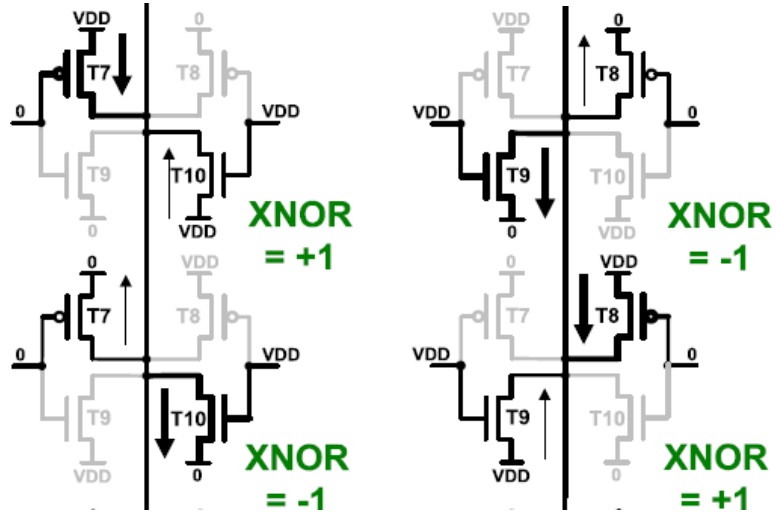
Logics of FeFET



FeFET has the same logic rules as normal MOS, it is beneficial for us to operate following logic circuits of computing

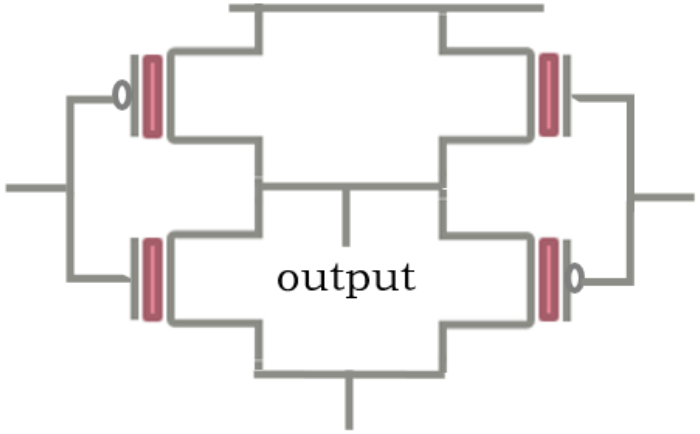
FeFET as XNOR





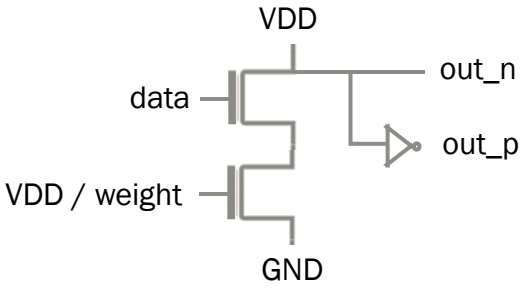
1. Exerting the write pulse as weight parameter (1/0) to FeFET and then floating to remove interference and speed up
2. While training, the read pulse can be assigned as 1 (1V above) or 0 (1V below) and obtain the calculated results

FeFET into Convolution



gate of p / n	source of p	source of n	data out
0 / 0	GND	VDD	0
0 / 1	GND	VDD	0
1 / 0	VDD	GND	X
1 / 1	VDD	GND	1

Have advantages to deep pipelines

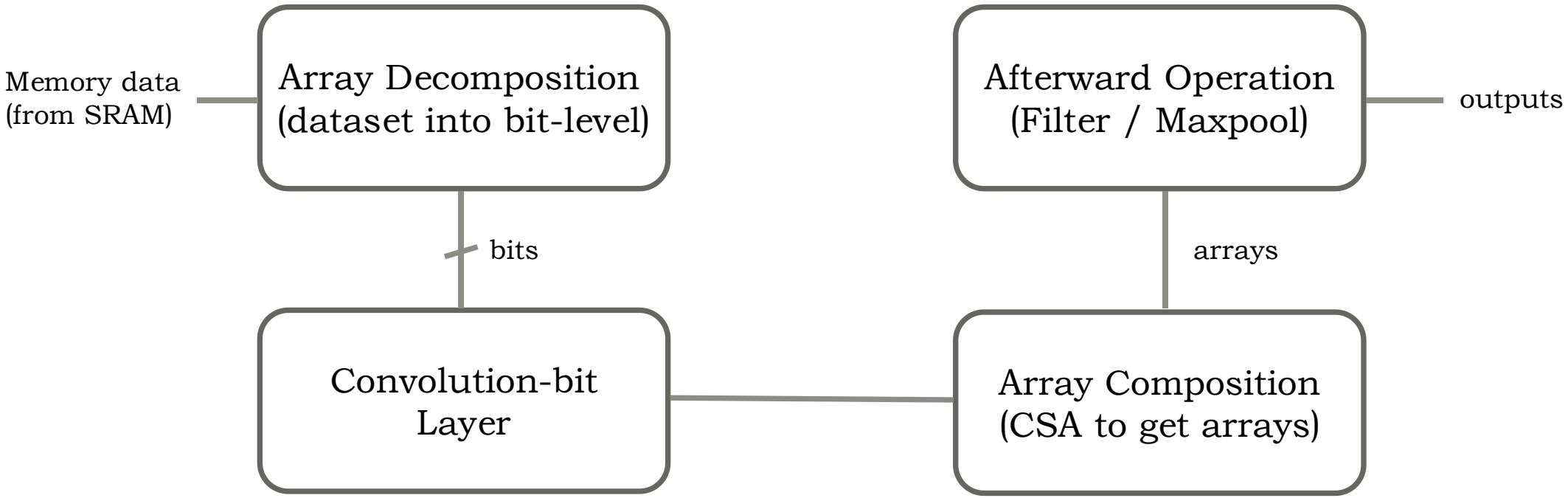


Supply control to FeFET cross pair

Imagine every FeFET to be a single bit. Convolution can be applied into FeFET charging/discharging with additional NAND

** need reset after computing (because of the x of 1/0)

Layer-level Operations of Convolution



Pros and Cons in FeFET Convolution

Pros

1. Successfully implement CIM in hardware level
2. Speed enhancement by eliminating memory access
3. Great tradeoff between area and additional computation
4. Weight can be stored in FeFET and be used repeatedly

Cons

1. Need another nmos to reset after every convolution (like DRAM)
2. Need NAND to have conditional computing
3. Stability

Citations

1. CMOS-Compatible Fabrication of Low-Power Ferroelectric Tunneling Junction for Neural Network Applications by Yi-Shan Kuo, Shen-Yang Lee, Chia-Chin Lee, Shou-Wei Li, and Tien-Sheng Chao

2. SLIM: Simultaneous Logic-in-Memory Computing Exploiting Bilayer Analog OxRAM Devices by Sandeep Kaur Kingra, Vivek Parmar, Che-Chia Chang, Boris Hudec, Tuo-Hung Hou, and Manan Suri

3. FeFET details supports by Yi-Shan Kuo

4. DIC course instructed by S. J. Jou

5. All other reference papers in https://reurl.cc/o99aKl

Thanks for Your Attention :)