2019 DCS Lab 2

除頻器

- Some system have stable Clock Source
  - FPGA
- Need different frequency
  - Use counter

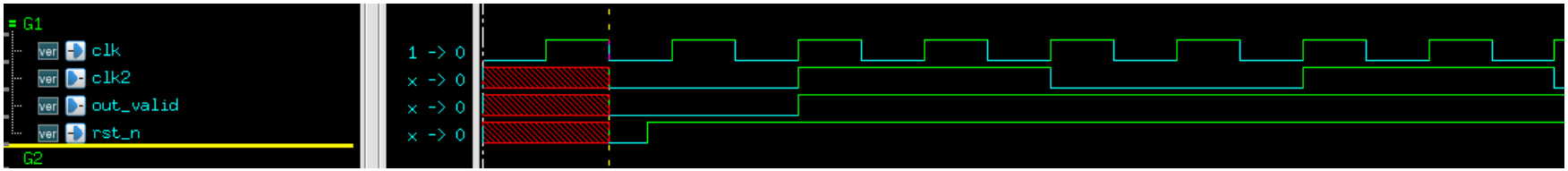
Counter.sv

Input Signal	Bit Width	Definition
clk	1	10 ns Clock
rst_n	1	非同步reset 當reset negedge時，所有output須都為0

Output Signal	Bit Width	Definition
clk2	1	Clk2 = 4 倍的clk
out_valid	1	Outvalid = 1 在clk2 posedge的時候

Output & Waveform

- Waveform



Command

- tar -xvf ~dcsta01/Lab03.tar
- Need 02_SYN(without any latch and error)

E3 rule

- Please upload your design to Lab02_1de
  - Rename Counter_dcsxx.sv