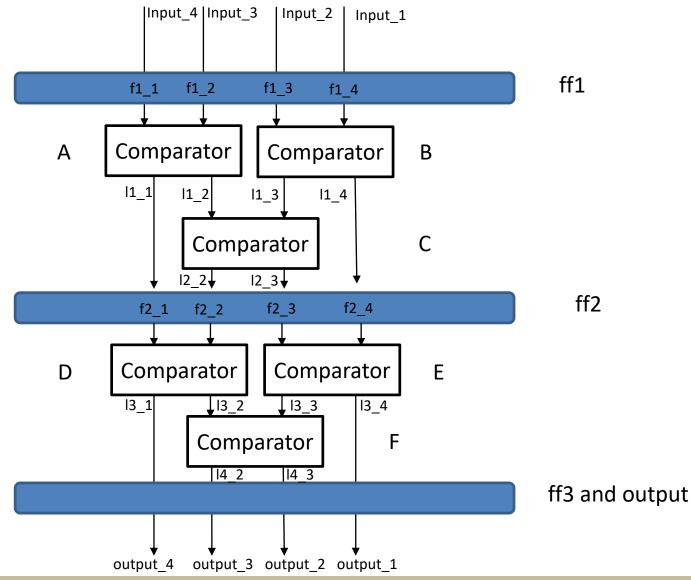


2019 DCS Lab 04

Sorting with pipeline(debug)

- 數字排序 4,5,1,2 → 5,4,2,1
 - Bubble sort , Merge sort
- Bubble sort
 - Easy for software.
 - Use recursive function ,for loop
- Merge sort
 - Easy for hardware
 - Use comparator

Block diagram



Merge Sorting

Input Signal	Bit Width	Definition
in_number1	5	4 random 5-bits numbers
in_number2	5	
in_number3	5	
in_number4	5	
Clk	1	5 ns Clock
rst_n	1	非同步reset 當reset negedge時,所有output須都為0
In_valid	1	當high時,代表in_number開始給值。

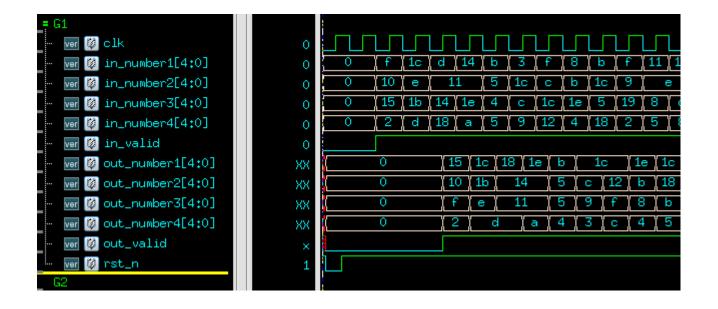
Output Signal	Bit Width	Definition
out_number1	5	Output_1≥Output_2≥Output_3≥Output_4
out_number2	5	
out_number3	5	
out_number4	5	
out_valid	1	隨著out_number有效時,給予high

Spec

- 01 pass
- 02 without error, latch and timing violated
- 這次LAB屬於Debug型,所以Design(錯誤的)已經 附在資料夾內,請修正錯誤的Design。
- 之後作業可參考這次LAB助教提供的程式碼中的 coding style, pipeline寫法,較為容易debug與理 解。

Output & Waveform

Waveform



Command

tar xvf ~dcsta01/Lab04.tar

- Upload
 - cd 09_upload
 - ./01_upload
 - ./02_download demoX