2019 DCS Lab 10

Clock Domain Crossing (CDC)

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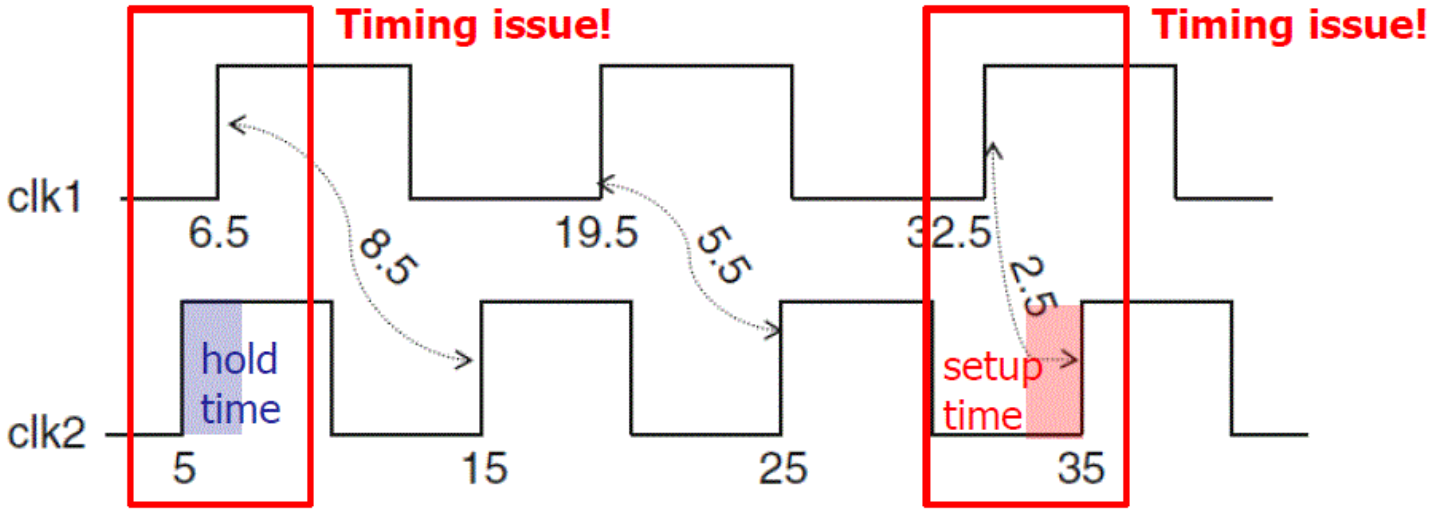
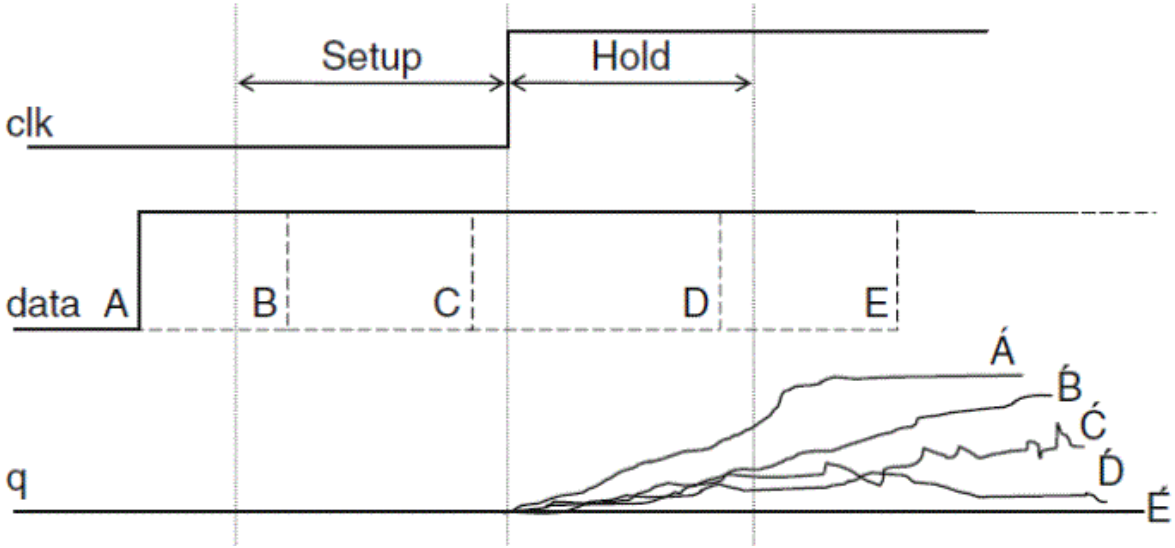
- CDC: When the data launched and captured by different (asynchronous) clock domain, this case is called Clock Domain Crossing.
- Consider two clocks, clk1 and clk2, with periods 13 and 10 respectively.



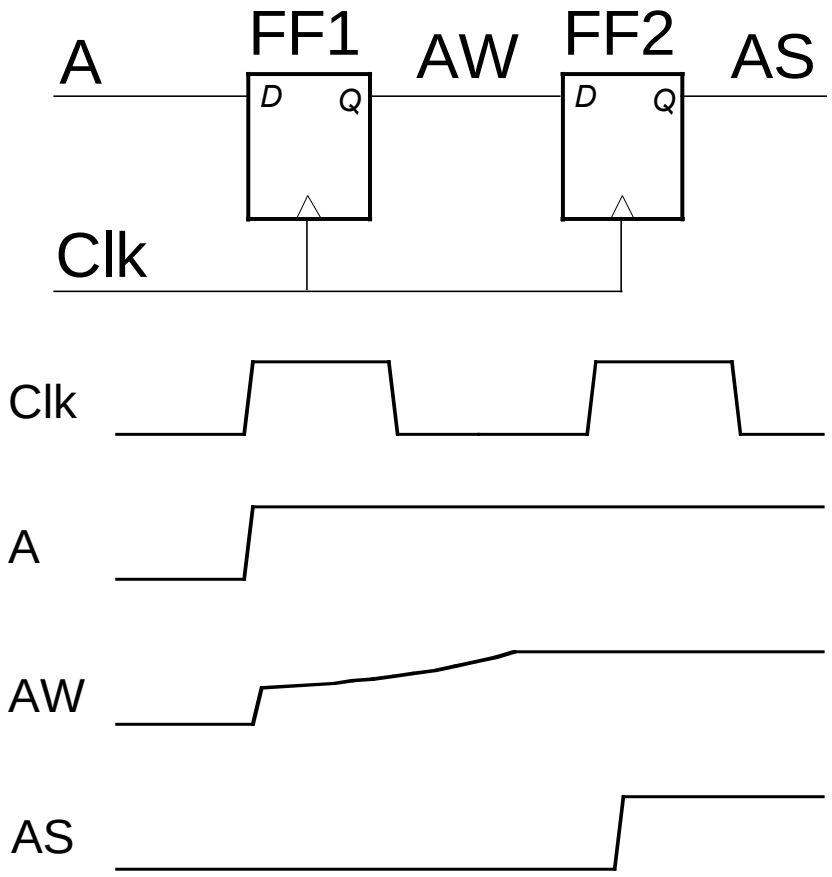
Asynchronous clocks

Metastability

- The unstable status due to non-ideal data transition is called metastability.
- To avoid this phenomenon, we have to ensure data transition during setup/hold timing check.
- However, CDC designs will inevitably face this problem.



Solution: A Brute-Force Synchronizer

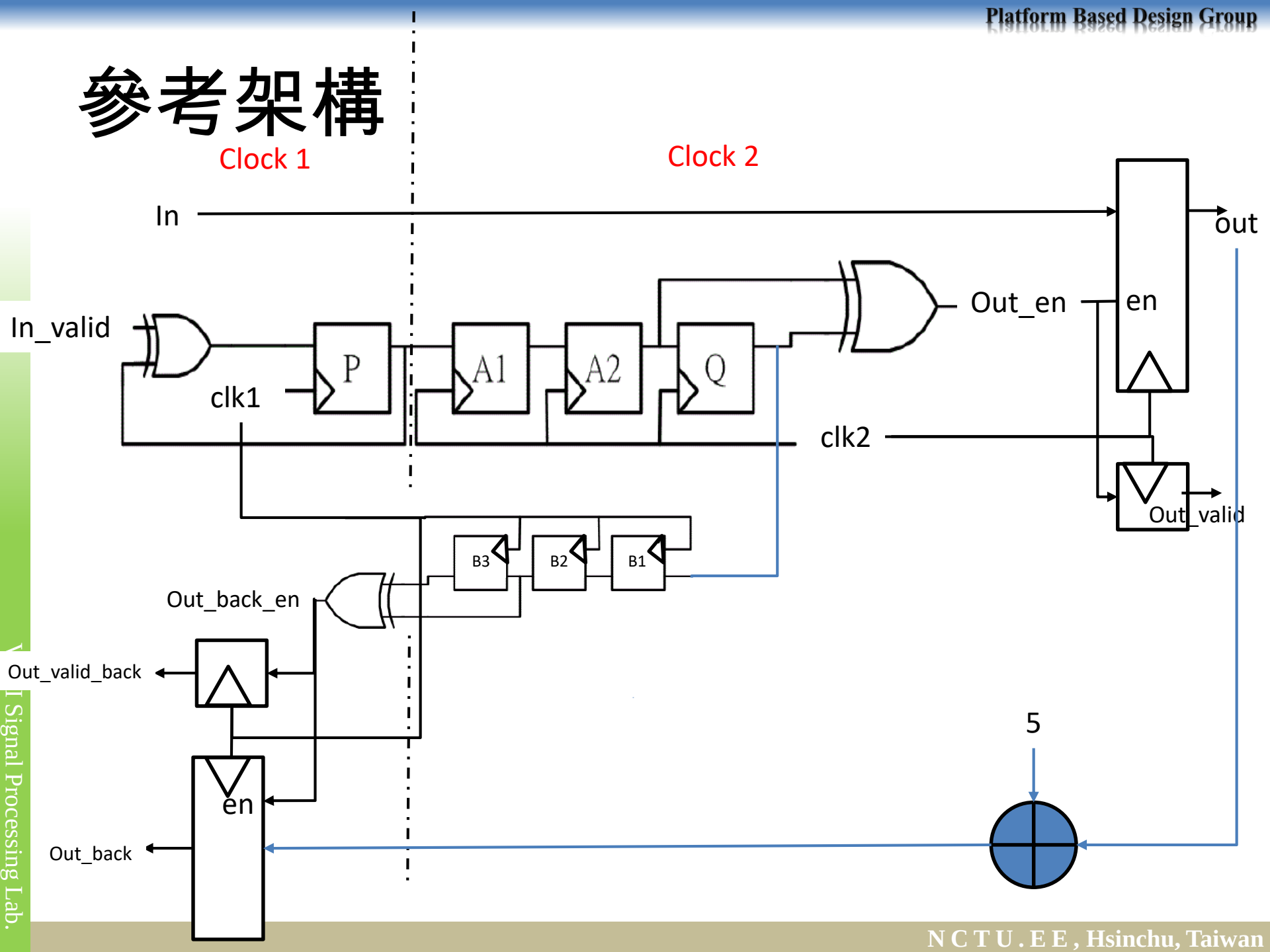


細節請參考: 上課講義 Lecture 12

You need to design

- Clk1 = 1.7 ns , clk2 = 3.1 ns
- Input 在clk1 domain傳送一筆4bit資料
- Out 在clk2 domain接收一筆4bit資料
- 在clk2 domain計算並傳送 out + 5(decimal)
- Out_back在clk1 domain接收out + 5資料

參考架構


Clock 1
Clock 2
In
out
In_valid
P
A1
A2
Q
Out_en
en
clk1
clk2
Out_valid
B3
B2
B1
Out_back_en
Out_valid_back
en
Out_back
5

cdc.sv

Input Signal	Bit Width	Definition
clk1	1	Clock 1 domain 3.1ns
clk2	1	Clock 2 domain 1.7ns
rst_n	1	Asynchronous active-low reset
In	4	在clock 1 domain 且 in_valid = 1時，給予一筆資料
in_valid	1	當此訊號拉起時給in資料

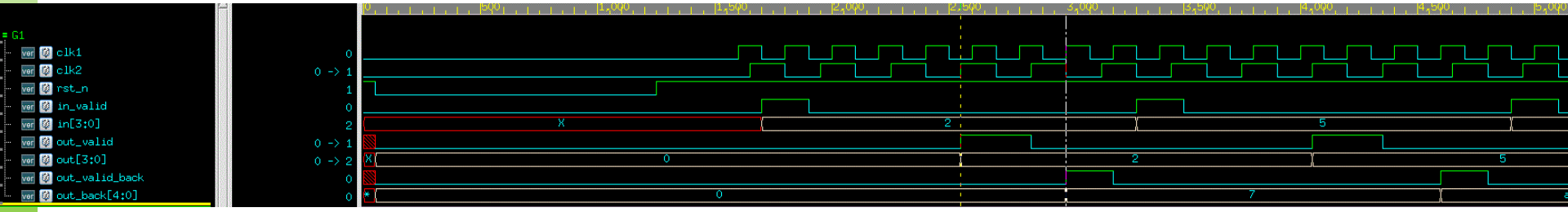
Output Signal	Bit Width	Definition
out_valid	1	在clock 2 domain且out_valid = 1時，檢查out。
Out	4	由clock 1 domain傳送的in資料
Out_valid_back	1	在clock 1 domain且out_valid _back= 1時，檢查out_back。
Out_back	5	由clock 2 domain傳送的out+5資料

Spec

- 請使用Synchronizer完成本次作業
- 所有output必須非同步負準位reset。
- 01_RTL 需要PASS。
- 02_SYN不能有error跟latches。
- 02_SYN，clock 1 period = 3.1ns，clock 2 period = 1.7ns ，timing slack必須為MET。

Output & Waveform

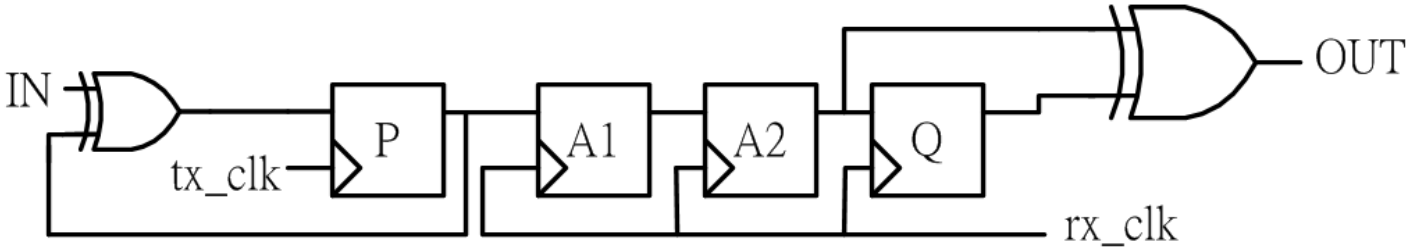
- Waveform

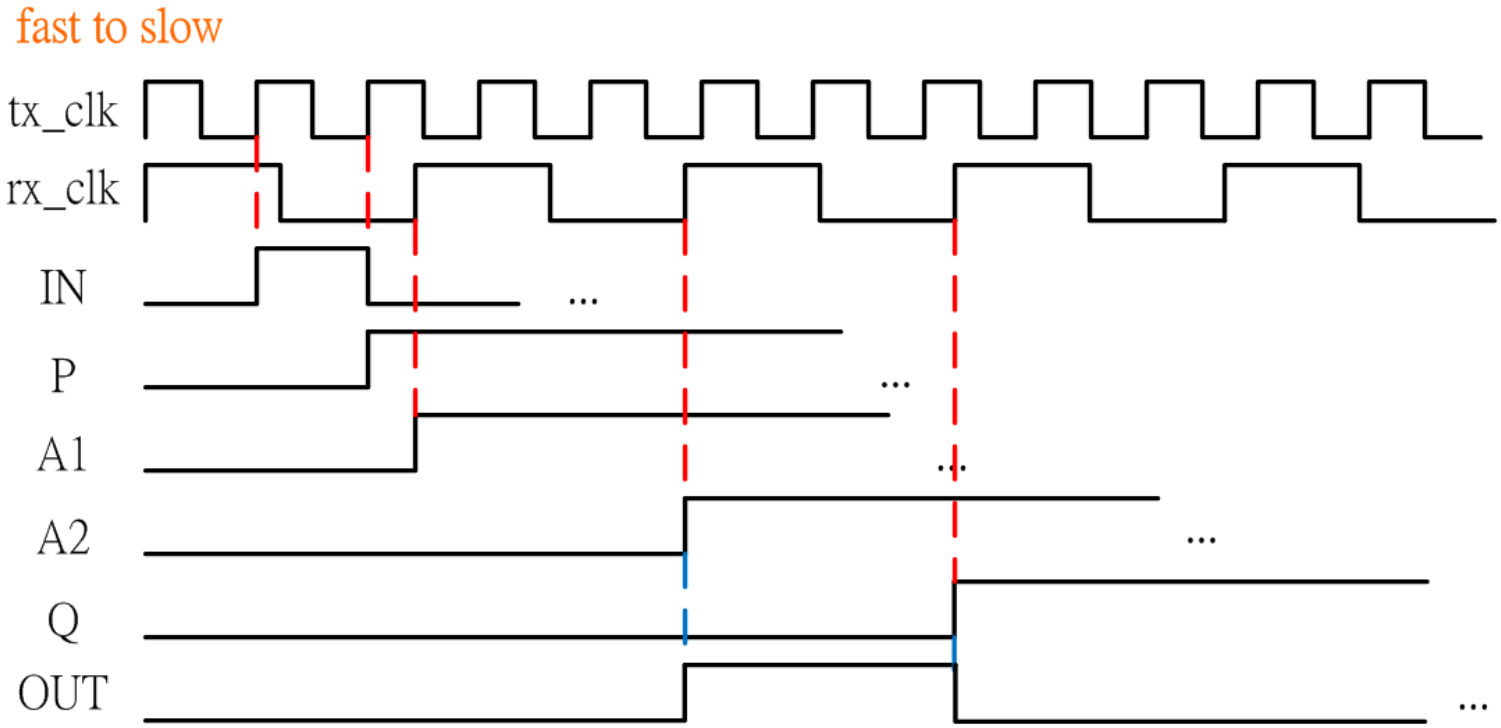


Command

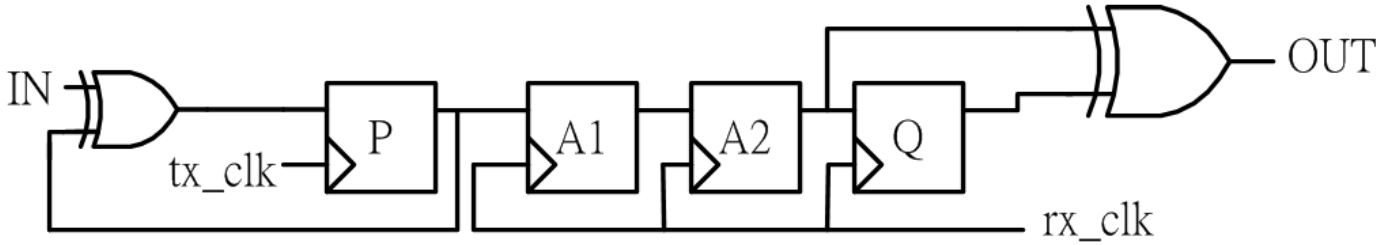
- tar -xvf ~dcsta01/Lab10.tar
- Upload
  - cd 09_upload
  - ./01_upload
  - ./02_download demoX

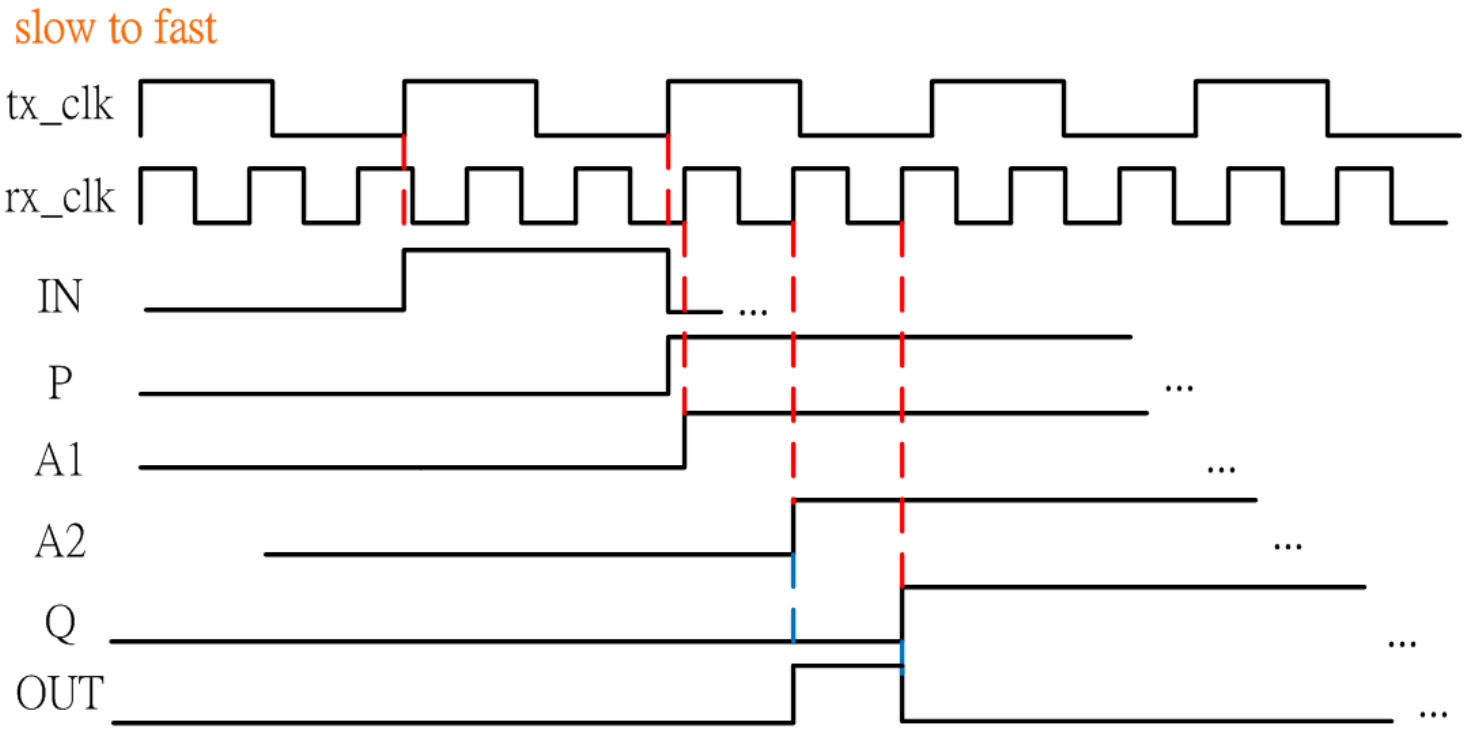
Reference


IN
tx_clk
P
A1
A2
Q
OUT
rx_clk

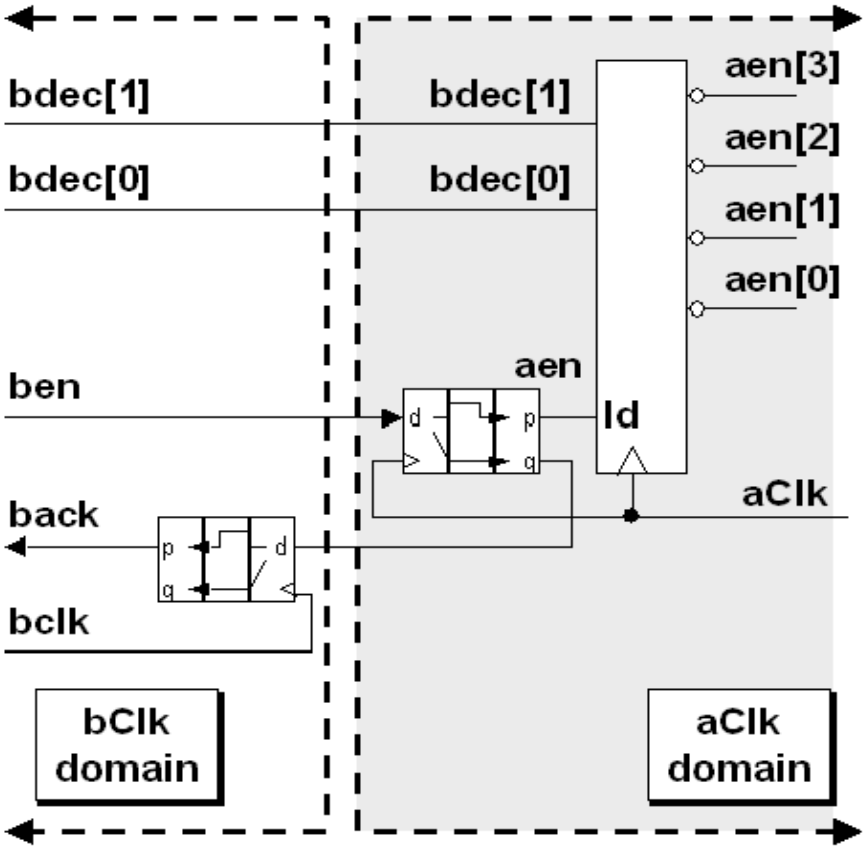

fast to slow
tx_clk
rx_clk
IN
P
A1
A2
Q
OUT

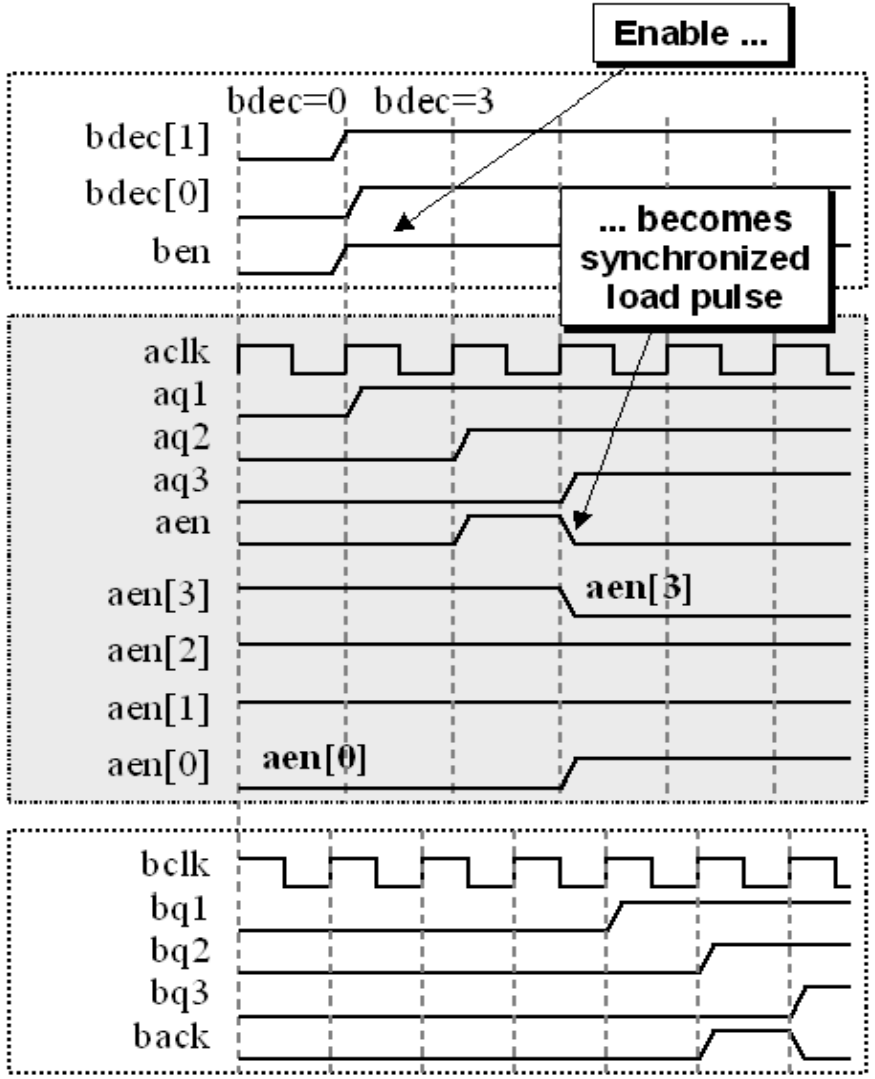
Reference


IN
tx_clk
P
A1
A2
Q
OUT
rx_clk


slow to fast
tx_clk
rx_clk
IN
P
A1
A2
Q
OUT

Reference


bdec[1]
bdec[0]
ben
back
bclk
bdec[1]
bdec[0]
aen
ld
aen[3]
aen[2]
aen[1]
aen[0]
aClk
d
p
q
bClk domain
aClk domain


Enable ...
bdec=0
bdec=3
bdec[1]
bdec[0]
ben
... becomes synchronized load pulse
aclk
aq1
aq2
aq3
aen
aen[3]
aen[2]
aen[1]
aen[0]
aen[3]
aen[0]
bclk
bq1
bq2
bq3
back