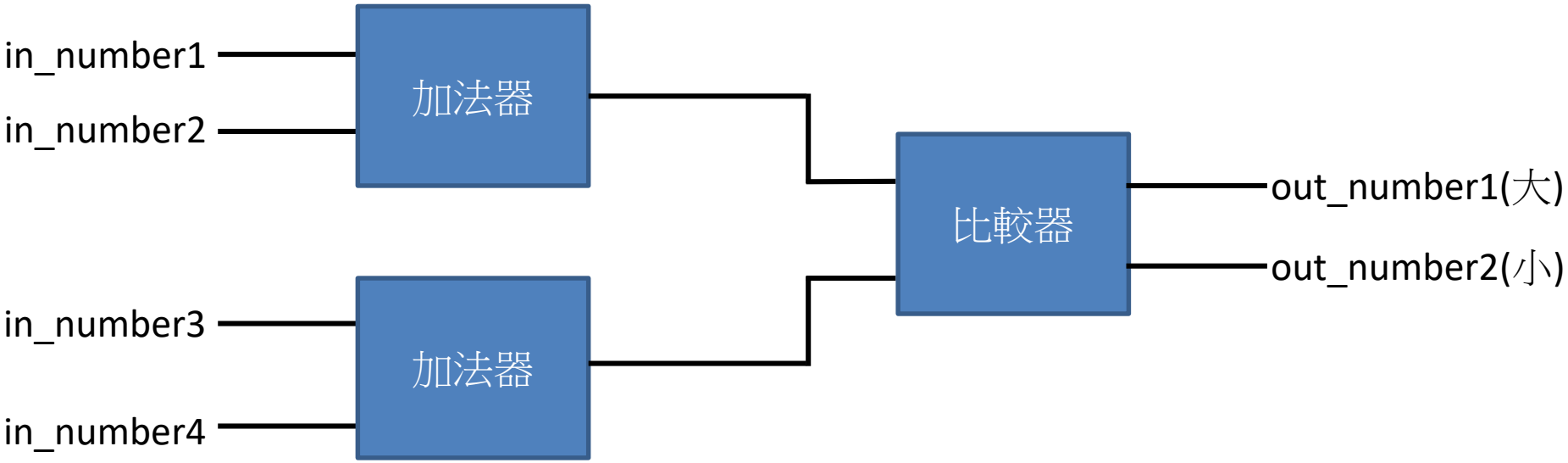
2019 DCS Lab 01

隋建德 張國威

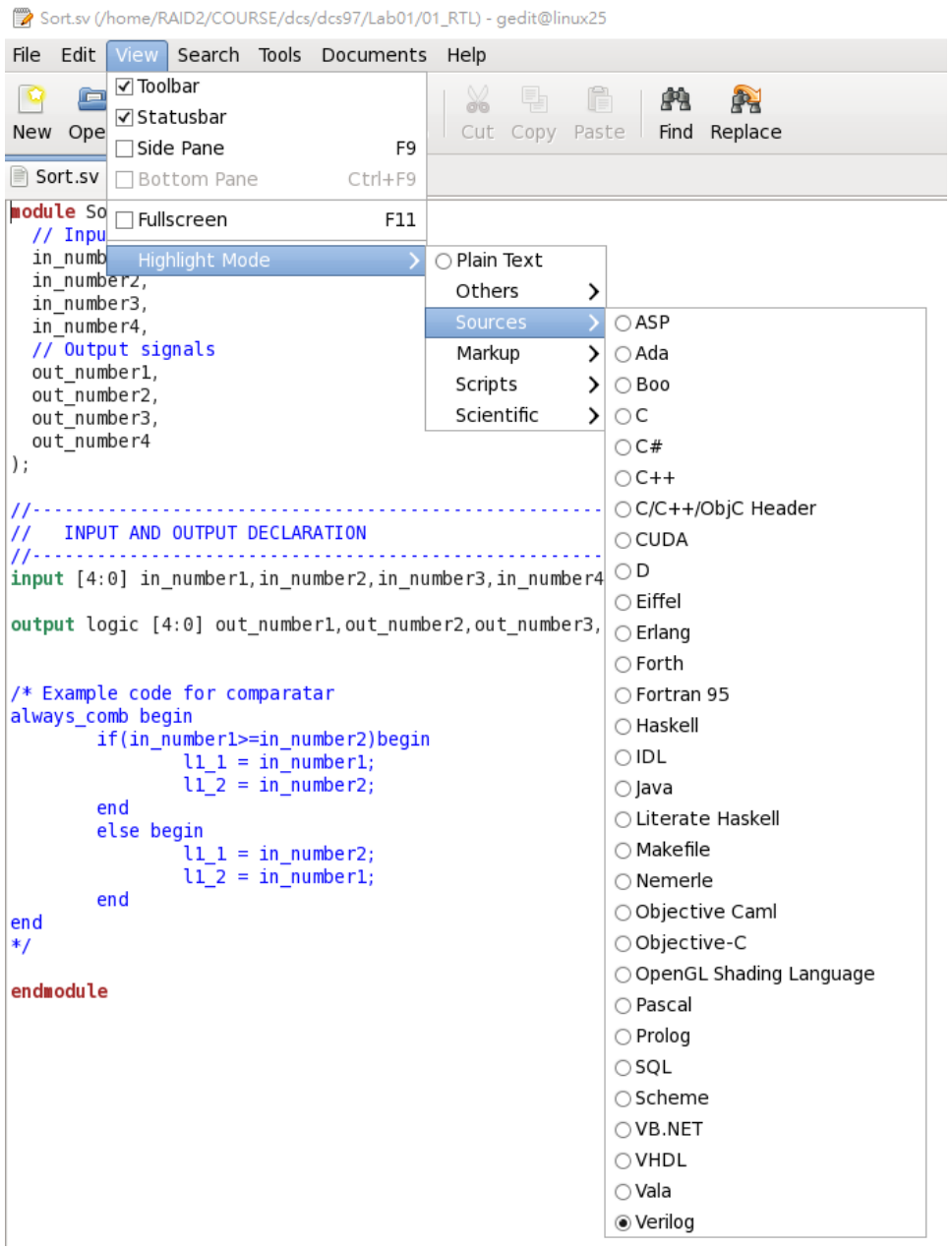
Lab01

- 加法
  - A = B + C;
- 排序(大到小)
  - 4,5 -> 5,4


in_number1
in_number2
加法器
in_number3
in_number4
加法器
比較器
out_number1(大)
out_number2(小)

Command

- tar xvf ~dcsta01/Lab01.tar
- cd Lab01/01_RTL/
- gedit
  - If you use Windows ,you can use Notepad++
  - view →Highlight Mode →Sources→Verilog


Sort.sv (/home/RAID2/COURSE/dcs/dcs97/Lab01/01_RTL) - gedit@linux25
File Edit View Search Tools Documents Help
Toolbar
Statusbar
Side Pane F9
Bottom Pane Ctrl+F9
Fullscreen F11
Highlight Mode
Plain Text
Others
Sources
Markup
Scripts
Scientific
ASP
Ada
Boo
C
C#
C++
C/C++/ObjC Header
CUDA
D
Eiffel
Erlang
Forth
Fortran 95
Haskell
IDL
Java
Literate Haskell
Makefile
Nemerle
Objective Caml
Objective-C
OpenGL Shading Language
Pascal
Prolog
SQL
Scheme
VB.NET
VHDL
Vala
Verilog
New Cut Copy Paste Find Replace
Sort.sv
// Output signals
out_number1,
out_number2,
out_number3,
out_number4
);
// INPUT AND OUTPUT DECLARATION
input [4:0] in_number1,in_number2,in_number3,in_number4
output logic [4:0] out_number1,out_number2,out_number3,
/* Example code for comparatar
always_comb begin
if(in_number1>=in_number2)begin
l1_1 = in_number1;
l1_2 = in_number2;
end
else begin
l1_1 = in_number2;
l1_2 = in_number1;
end
end
*/
endmodule

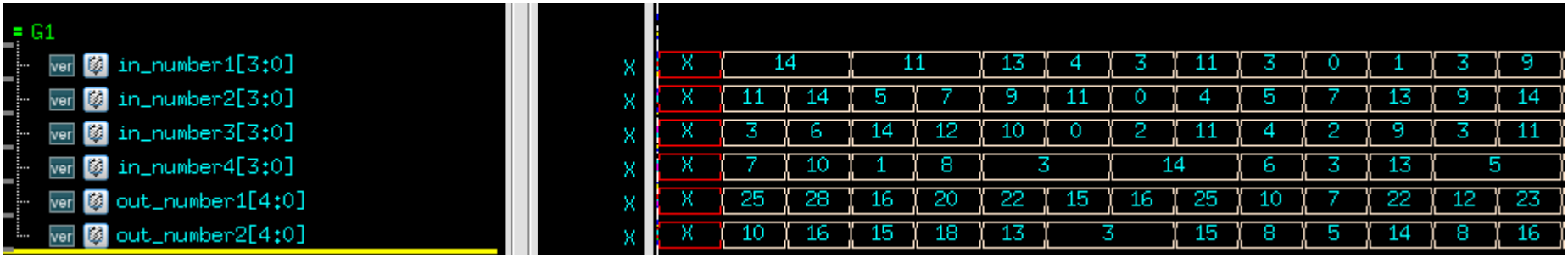
Port

Input Signal	Bit Width	Definition
in_number1	4	4 random 4-bits numbers
in_number2	4	
in_number3	4	
in_number4	4	

Output Signal	Bit Width	Definition
out_number1	5	out_number1 ≥ out_number2
out_number2	5	

Output & Waveform

- Waveform



E3 rule

- 請寫完的同學找助教Demo，Demo完仍然要上傳E3
- Rename Lab01_dcsxx.sv
- 補交請在晚上12點前補交