\*\*\* Running vivado

with args -log Lab10\_Adder.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab10\_Adder.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab10\_Adder.tcl -notrace

Command: synth\_design -top Lab10\_Adder -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 91124

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Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1380.352 ; gain = 0.000 ; free physical = 931 ; free virtual = 1892

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INFO: [Synth 8-6157] synthesizing module 'Lab10\_Adder' [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/sources\_1/new/Lab10\_Adder.sv:22]

INFO: [Synth 8-6155] done synthesizing module 'Lab10\_Adder' (1#1) [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/sources\_1/new/Lab10\_Adder.sv:22]

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1387.277 ; gain = 6.926 ; free physical = 940 ; free virtual = 1903

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1387.277 ; gain = 6.926 ; free physical = 940 ; free virtual = 1903

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1387.277 ; gain = 6.926 ; free physical = 940 ; free virtual = 1903

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc]

WARNING: [Vivado 12-584] No ports matched 'rst\_n'. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:25]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:25]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'rst\_n'. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:89]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:89]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'dp'. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:94]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:94]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'dp'. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:95]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc:95]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

Finished Parsing XDC File [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.srcs/constrs\_1/new/Lab10\_Adder.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Lab10\_Adder\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Lab10\_Adder\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.152 ; gain = 0.000 ; free physical = 665 ; free virtual = 1647

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.152 ; gain = 0.000 ; free physical = 665 ; free virtual = 1647

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.152 ; gain = 0.000 ; free physical = 665 ; free virtual = 1647

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.152 ; gain = 0.000 ; free physical = 665 ; free virtual = 1647

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Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 734 ; free virtual = 1716

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 734 ; free virtual = 1716

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 736 ; free virtual = 1718

---------------------------------------------------------------------------------

INFO: [Synth 8-5545] ROM "abcd" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5545] ROM "an" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5545] ROM "display" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5545] ROM "abcd" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5545] ROM "an" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5545] ROM "display" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5544] ROM "i" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "i" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "display" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 727 ; free virtual = 1709

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 5 Bit Adders := 1

+---Registers :

14 Bit Registers := 1

8 Bit Registers := 2

4 Bit Registers := 3

1 Bit Registers := 1

+---Muxes :

3 Input 14 Bit Muxes := 1

5 Input 8 Bit Muxes := 1

10 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 7

2 Input 4 Bit Muxes := 9

4 Input 4 Bit Muxes := 1

8 Input 4 Bit Muxes := 1

10 Input 4 Bit Muxes := 1

2 Input 1 Bit Muxes := 11

7 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module Lab10\_Adder

Detailed RTL Component Info :

+---Adders :

2 Input 5 Bit Adders := 1

+---Registers :

14 Bit Registers := 1

8 Bit Registers := 2

4 Bit Registers := 3

1 Bit Registers := 1

+---Muxes :

3 Input 14 Bit Muxes := 1

5 Input 8 Bit Muxes := 1

10 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 7

2 Input 4 Bit Muxes := 9

4 Input 4 Bit Muxes := 1

8 Input 4 Bit Muxes := 1

10 Input 4 Bit Muxes := 1

2 Input 1 Bit Muxes := 11

7 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-3886] merging instance 'i\_reg[4]' (FDRE) to 'i\_reg[5]'

INFO: [Synth 8-3886] merging instance 'i\_reg[5]' (FDRE) to 'i\_reg[6]'

INFO: [Synth 8-3886] merging instance 'i\_reg[6]' (FDRE) to 'i\_reg[1]'

INFO: [Synth 8-3886] merging instance 'i\_reg[1]' (FDRE) to 'i\_reg[2]'

INFO: [Synth 8-3886] merging instance 'i\_reg[2]' (FDRE) to 'i\_reg[3]'

INFO: [Synth 8-3886] merging instance 'i\_reg[3]' (FDRE) to 'i\_reg[11]'

INFO: [Synth 8-3886] merging instance 'i\_reg[11]' (FDRE) to 'i\_reg[13]'

INFO: [Synth 8-3886] merging instance 'i\_reg[13]' (FDRE) to 'i\_reg[12]'

INFO: [Synth 8-3886] merging instance 'i\_reg[12]' (FDRE) to 'i\_reg[7]'

INFO: [Synth 8-3886] merging instance 'i\_reg[7]' (FDRE) to 'i\_reg[8]'

INFO: [Synth 8-3886] merging instance 'i\_reg[8]' (FDRE) to 'i\_reg[9]'

INFO: [Synth 8-3886] merging instance 'i\_reg[9]' (FDRE) to 'i\_reg[10]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\i\_reg[10] )

INFO: [Synth 8-3333] propagating constant 1 across sequential element (\display\_reg[7] )

INFO: [Synth 8-3886] merging instance 'an\_reg[2]' (FDSE) to 'an\_reg[7]'

INFO: [Synth 8-3886] merging instance 'an\_reg[3]' (FDSE) to 'an\_reg[7]'

INFO: [Synth 8-3886] merging instance 'an\_reg[4]' (FDSE) to 'an\_reg[7]'

INFO: [Synth 8-3886] merging instance 'an\_reg[5]' (FDSE) to 'an\_reg[7]'

INFO: [Synth 8-3886] merging instance 'an\_reg[6]' (FDSE) to 'an\_reg[7]'

INFO: [Synth 8-3333] propagating constant 1 across sequential element (\an\_reg[7] )

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:08 ; elapsed = 00:00:10 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 708 ; free virtual = 1694

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 583 ; free virtual = 1572

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 583 ; free virtual = 1571

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 5|

|3 |LUT1 | 2|

|4 |LUT2 | 8|

|5 |LUT3 | 6|

|6 |LUT4 | 12|

|7 |LUT5 | 13|

|8 |LUT6 | 27|

|9 |FDRE | 38|

|10 |FDSE | 1|

|11 |IBUF | 6|

|12 |OBUF | 20|

+------+-------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 139|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.152 ; gain = 339.801 ; free physical = 582 ; free virtual = 1571

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:10 ; elapsed = 00:00:12 . Memory (MB): peak = 1720.152 ; gain = 6.926 ; free physical = 637 ; free virtual = 1625

Synthesis Optimization Complete : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.160 ; gain = 339.801 ; free physical = 647 ; free virtual = 1635

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 5 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.160 ; gain = 0.000 ; free physical = 577 ; free virtual = 1567

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

43 Infos, 4 Warnings, 4 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:15 ; elapsed = 00:00:17 . Memory (MB): peak = 1720.160 ; gain = 339.883 ; free physical = 635 ; free virtual = 1624

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.160 ; gain = 0.000 ; free physical = 635 ; free virtual = 1624

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab10\_Adder/Lab10\_Adder.runs/synth\_1/Lab10\_Adder.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab10\_Adder\_utilization\_synth.rpt -pb Lab10\_Adder\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Thu May 23 18:07:02 2019...