\*\*\* Running vivado

with args -log Lab05\_Display.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab05\_Display.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

\*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab05\_Display.tcl -notrace

Command: synth\_design -top Lab05\_Display -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 21156

WARNING: [Synth 8-1935] empty port in module declaration [/home/jinson/vivado/Lab05\_Display/Lab05\_Display.srcs/sources\_1/new/Lab05\_Display.v:54]

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1350.762 ; gain = 6.676 ; free physical = 885 ; free virtual = 2120

---------------------------------------------------------------------------------

INFO: [Synth 8-6157] synthesizing module 'Lab05\_Display' [/home/jinson/vivado/Lab05\_Display/Lab05\_Display.srcs/sources\_1/new/Lab05\_Display.v:23]

WARNING: [Synth 8-308] ignoring empty port [/home/jinson/vivado/Lab05\_Display/Lab05\_Display.srcs/sources\_1/new/Lab05\_Display.v:55]

INFO: [Synth 8-6155] done synthesizing module 'Lab05\_Display' (1#1) [/home/jinson/vivado/Lab05\_Display/Lab05\_Display.srcs/sources\_1/new/Lab05\_Display.v:23]

---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1379.887 ; gain = 35.801 ; free physical = 903 ; free virtual = 2140

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Start Handling Custom Attributes

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1379.887 ; gain = 35.801 ; free physical = 902 ; free virtual = 2139

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1379.887 ; gain = 35.801 ; free physical = 902 ; free virtual = 2139

---------------------------------------------------------------------------------

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab05\_Display/Lab05\_Display.srcs/constrs\_1/new/Lab05\_Display.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab05\_Display/Lab05\_Display.srcs/constrs\_1/new/Lab05\_Display.xdc]

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1713.730 ; gain = 0.000 ; free physical = 618 ; free virtual = 1884

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1713.730 ; gain = 0.000 ; free physical = 618 ; free virtual = 1884

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

Constraint Validation Runtime : Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1713.730 ; gain = 0.000 ; free physical = 617 ; free virtual = 1884

---------------------------------------------------------------------------------

Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 685 ; free virtual = 1952

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Loading Part and Timing Information

---------------------------------------------------------------------------------

Loading part: xc7a100tcsg324-1

---------------------------------------------------------------------------------

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 685 ; free virtual = 1951

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Applying 'set\_property' XDC Constraints

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 687 ; free virtual = 1954

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 686 ; free virtual = 1953

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start RTL Component Statistics

---------------------------------------------------------------------------------

Detailed RTL Component Info :

---------------------------------------------------------------------------------

Finished RTL Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

Hierarchical RTL Component report

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

---------------------------------------------------------------------------------

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

---------------------------------------------------------------------------------

Finished Part Resource Summary

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Cross Boundary and Area Optimization

---------------------------------------------------------------------------------

Warning: Parallel synthesis criteria is not met

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 674 ; free virtual = 1944

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Applying XDC Timing Constraints

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 544 ; free virtual = 1820

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Timing Optimization

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Timing Optimization : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 544 ; free virtual = 1820

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Technology Mapping

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Technology Mapping : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Flattening Before IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Start Renaming Generated Instances

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Instances : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Rebuilding User Hierarchy

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Renaming Generated Ports

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Ports : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Handling Custom Attributes

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Handling Custom Attributes : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Renaming Generated Nets

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Nets : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Writing Synthesis Report

---------------------------------------------------------------------------------

Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |LUT1 | 9|

|2 |LUT3 | 1|

|3 |LUT4 | 6|

|4 |IBUF | 13|

|5 |OBUF | 16|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 45|

+------+---------+-------+------+

---------------------------------------------------------------------------------

Finished Writing Synthesis Report : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.730 ; gain = 369.645 ; free physical = 543 ; free virtual = 1819

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:11 . Memory (MB): peak = 1713.730 ; gain = 35.801 ; free physical = 597 ; free virtual = 1874

Synthesis Optimization Complete : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1713.738 ; gain = 369.645 ; free physical = 602 ; free virtual = 1878

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1713.738 ; gain = 0.000 ; free physical = 537 ; free virtual = 1814

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

11 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1713.738 ; gain = 369.727 ; free physical = 586 ; free virtual = 1863

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1713.738 ; gain = 0.000 ; free physical = 586 ; free virtual = 1863

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab05\_Display/Lab05\_Display.runs/synth\_1/Lab05\_Display.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab05\_Display\_utilization\_synth.rpt -pb Lab05\_Display\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Thu Apr 11 15:50:57 2019...