\*\*\* Running vivado

with args -log Lab05\_FullSubtractor.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab05\_FullSubtractor.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab05\_FullSubtractor.tcl -notrace

Command: link\_design -top Lab05\_FullSubtractor -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/constrs\_1/new/Lab05\_FullSubtractor.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/constrs\_1/new/Lab05\_FullSubtractor.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1535.348 ; gain = 0.000 ; free physical = 152 ; free virtual = 3658

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

5 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

link\_design: Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1539.348 ; gain = 175.332 ; free physical = 151 ; free virtual = 3657

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.20 . Memory (MB): peak = 1572.363 ; gain = 33.016 ; free physical = 150 ; free virtual = 3656

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 1d0467d90

Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 1999.863 ; gain = 427.500 ; free physical = 224 ; free virtual = 3281

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 1d0467d90

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 155 ; free virtual = 3212

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 1d0467d90

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 155 ; free virtual = 3212

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 1d0467d90

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 155 ; free virtual = 3212

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 1d0467d90

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 155 ; free virtual = 3212

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 1d0467d90

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3212

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 1d0467d90

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3212

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt\_design Change Summary

=========================

-------------------------------------------------------------------------------------------------------------------------

| Phase | #Cells created | #Cells Removed | #Constrained objects preventing optimizations |

-------------------------------------------------------------------------------------------------------------------------

| Retarget | 0 | 0 | 0 |

| Constant propagation | 0 | 0 | 0 |

| Sweep | 0 | 0 | 0 |

| BUFG optimization | 0 | 0 | 0 |

| Shift Register Optimization | 0 | 0 | 0 |

| Post Processing Netlist | 0 | 0 | 0 |

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Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3212

Ending Logic Optimization Task | Checksum: 1d0467d90

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3212

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 1d0467d90

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3211

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 1d0467d90

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3211

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3211

Ending Netlist Obfuscation Task | Checksum: 1d0467d90

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3211

INFO: [Common 17-83] Releasing license: Implementation

21 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 2078.863 ; gain = 539.516 ; free physical = 154 ; free virtual = 3211

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2078.863 ; gain = 0.000 ; free physical = 154 ; free virtual = 3211

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2110.879 ; gain = 0.000 ; free physical = 150 ; free virtual = 3209

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2110.879 ; gain = 0.000 ; free physical = 150 ; free virtual = 3209

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.runs/impl\_1/Lab05\_FullSubtractor\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab05\_FullSubtractor\_drc\_opted.rpt -pb Lab05\_FullSubtractor\_drc\_opted.pb -rpx Lab05\_FullSubtractor\_drc\_opted.rpx

Command: report\_drc -file Lab05\_FullSubtractor\_drc\_opted.rpt -pb Lab05\_FullSubtractor\_drc\_opted.pb -rpx Lab05\_FullSubtractor\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.runs/impl\_1/Lab05\_FullSubtractor\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 4 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2118.883 ; gain = 0.000 ; free physical = 118 ; free virtual = 3171

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 178618ab2

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2118.883 ; gain = 0.000 ; free physical = 118 ; free virtual = 3171

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2118.883 ; gain = 0.000 ; free physical = 118 ; free virtual = 3171

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 178618ab2

Time (s): cpu = 00:00:00.42 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2122.879 ; gain = 3.996 ; free physical = 107 ; free virtual = 3161

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 26f4996f2

Time (s): cpu = 00:00:00.44 ; elapsed = 00:00:00.46 . Memory (MB): peak = 2122.879 ; gain = 3.996 ; free physical = 106 ; free virtual = 3161

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 26f4996f2

Time (s): cpu = 00:00:00.45 ; elapsed = 00:00:00.46 . Memory (MB): peak = 2122.879 ; gain = 3.996 ; free physical = 106 ; free virtual = 3161

Phase 1 Placer Initialization | Checksum: 26f4996f2

Time (s): cpu = 00:00:00.45 ; elapsed = 00:00:00.46 . Memory (MB): peak = 2122.879 ; gain = 3.996 ; free physical = 106 ; free virtual = 3161

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 26f4996f2

Time (s): cpu = 00:00:00.46 ; elapsed = 00:00:00.47 . Memory (MB): peak = 2122.879 ; gain = 3.996 ; free physical = 104 ; free virtual = 3159

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 1def70f1f

Time (s): cpu = 00:00:00.85 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2123.875 ; gain = 4.992 ; free physical = 121 ; free virtual = 3151

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 1def70f1f

Time (s): cpu = 00:00:00.86 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2123.875 ; gain = 4.992 ; free physical = 122 ; free virtual = 3151

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 195215cc3

Time (s): cpu = 00:00:00.87 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2123.875 ; gain = 4.992 ; free physical = 121 ; free virtual = 3151

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 252cc2646

Time (s): cpu = 00:00:00.88 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2123.875 ; gain = 4.992 ; free physical = 121 ; free virtual = 3151

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 252cc2646

Time (s): cpu = 00:00:00.89 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2123.875 ; gain = 4.992 ; free physical = 121 ; free virtual = 3151

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 121 ; free virtual = 3151

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 121 ; free virtual = 3151

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 121 ; free virtual = 3151

Phase 3 Detail Placement | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 121 ; free virtual = 3151

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 121 ; free virtual = 3151

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 123 ; free virtual = 3153

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 123 ; free virtual = 3153

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2138.258 ; gain = 0.000 ; free physical = 123 ; free virtual = 3153

Phase 4.4 Final Placement Cleanup | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 123 ; free virtual = 3153

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 263cd27bc

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 123 ; free virtual = 3153

Ending Placer Task | Checksum: 1cd320921

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 2138.258 ; gain = 19.375 ; free physical = 132 ; free virtual = 3163

INFO: [Common 17-83] Releasing license: Implementation

39 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2138.258 ; gain = 0.000 ; free physical = 132 ; free virtual = 3163

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00 . Memory (MB): peak = 2138.258 ; gain = 0.000 ; free physical = 133 ; free virtual = 3165

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2138.258 ; gain = 0.000 ; free physical = 132 ; free virtual = 3164

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.runs/impl\_1/Lab05\_FullSubtractor\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file Lab05\_FullSubtractor\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2138.258 ; gain = 0.000 ; free physical = 126 ; free virtual = 3156

INFO: [runtcl-4] Executing : report\_utilization -file Lab05\_FullSubtractor\_utilization\_placed.rpt -pb Lab05\_FullSubtractor\_utilization\_placed.pb

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file Lab05\_FullSubtractor\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2138.258 ; gain = 0.000 ; free physical = 132 ; free virtual = 3163

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 4 CPUs

Checksum: PlaceDB: dcb2e08b ConstDB: 0 ShapeSum: f07f2896 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 1380a56ff

Time (s): cpu = 00:00:22 ; elapsed = 00:00:19 . Memory (MB): peak = 2280.934 ; gain = 142.676 ; free physical = 129 ; free virtual = 3011

Post Restoration Checksum: NetGraph: 988948eb NumContArr: 9f810e14 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 1380a56ff

Time (s): cpu = 00:00:22 ; elapsed = 00:00:19 . Memory (MB): peak = 2287.930 ; gain = 149.672 ; free physical = 113 ; free virtual = 2995

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 1380a56ff

Time (s): cpu = 00:00:22 ; elapsed = 00:00:19 . Memory (MB): peak = 2287.930 ; gain = 149.672 ; free physical = 113 ; free virtual = 2995

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: a14de092

Time (s): cpu = 00:00:22 ; elapsed = 00:00:19 . Memory (MB): peak = 2295.195 ; gain = 156.938 ; free physical = 110 ; free virtual = 2992

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 15d5ab0e7

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 108 ; free virtual = 2990

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: fba30447

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 109 ; free virtual = 2991

Phase 4 Rip-up And Reroute | Checksum: fba30447

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 109 ; free virtual = 2991

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: fba30447

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 109 ; free virtual = 2991

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: fba30447

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 109 ; free virtual = 2991

Phase 6 Post Hold Fix | Checksum: fba30447

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 109 ; free virtual = 2991

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.000261131 %

Global Horizontal Routing Utilization = 0.000710429 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 1.8018%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 0.900901%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: fba30447

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 109 ; free virtual = 2991

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: fba30447

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 108 ; free virtual = 2991

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 12af55a4f

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 108 ; free virtual = 2991

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 125 ; free virtual = 3007

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

52 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2299.629 ; gain = 161.371 ; free physical = 125 ; free virtual = 3007

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2299.629 ; gain = 0.000 ; free physical = 126 ; free virtual = 3008

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2299.629 ; gain = 0.000 ; free physical = 126 ; free virtual = 3009

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2299.629 ; gain = 0.000 ; free physical = 124 ; free virtual = 3008

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.runs/impl\_1/Lab05\_FullSubtractor\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab05\_FullSubtractor\_drc\_routed.rpt -pb Lab05\_FullSubtractor\_drc\_routed.pb -rpx Lab05\_FullSubtractor\_drc\_routed.rpx

Command: report\_drc -file Lab05\_FullSubtractor\_drc\_routed.rpt -pb Lab05\_FullSubtractor\_drc\_routed.pb -rpx Lab05\_FullSubtractor\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.runs/impl\_1/Lab05\_FullSubtractor\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file Lab05\_FullSubtractor\_methodology\_drc\_routed.rpt -pb Lab05\_FullSubtractor\_methodology\_drc\_routed.pb -rpx Lab05\_FullSubtractor\_methodology\_drc\_routed.rpx

Command: report\_methodology -file Lab05\_FullSubtractor\_methodology\_drc\_routed.rpt -pb Lab05\_FullSubtractor\_methodology\_drc\_routed.pb -rpx Lab05\_FullSubtractor\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 4 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.runs/impl\_1/Lab05\_FullSubtractor\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file Lab05\_FullSubtractor\_power\_routed.rpt -pb Lab05\_FullSubtractor\_power\_summary\_routed.pb -rpx Lab05\_FullSubtractor\_power\_routed.rpx

Command: report\_power -file Lab05\_FullSubtractor\_power\_routed.rpt -pb Lab05\_FullSubtractor\_power\_summary\_routed.pb -rpx Lab05\_FullSubtractor\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

64 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file Lab05\_FullSubtractor\_route\_status.rpt -pb Lab05\_FullSubtractor\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file Lab05\_FullSubtractor\_timing\_summary\_routed.rpt -pb Lab05\_FullSubtractor\_timing\_summary\_routed.pb -rpx Lab05\_FullSubtractor\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file Lab05\_FullSubtractor\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file Lab05\_FullSubtractor\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file Lab05\_FullSubtractor\_bus\_skew\_routed.rpt -pb Lab05\_FullSubtractor\_bus\_skew\_routed.pb -rpx Lab05\_FullSubtractor\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

INFO: [Common 17-206] Exiting Vivado at Thu Apr 11 13:04:49 2019...

\*\*\* Running vivado

with args -log Lab05\_FullSubtractor.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab05\_FullSubtractor.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab05\_FullSubtractor.tcl -notrace

Command: open\_checkpoint Lab05\_FullSubtractor\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1378.266 ; gain = 0.000 ; free physical = 1019 ; free virtual = 3922

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1980.262 ; gain = 0.000 ; free physical = 319 ; free virtual = 3236

Restored from archive | CPU: 0.130000 secs | Memory: 0.997307 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1980.262 ; gain = 0.000 ; free physical = 319 ; free virtual = 3236

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1980.262 ; gain = 0.000 ; free physical = 320 ; free virtual = 3236

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 1980.262 ; gain = 601.996 ; free physical = 319 ; free virtual = 3236

Command: write\_bitstream -force Lab05\_FullSubtractor.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 4 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Bitstream compression saved 27847520 bits.

Writing bitstream ./Lab05\_FullSubtractor.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

INFO: [Common 17-83] Releasing license: Implementation

20 Infos, 1 Warnings, 2 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:07 ; elapsed = 00:00:11 . Memory (MB): peak = 2421.098 ; gain = 440.836 ; free physical = 450 ; free virtual = 3176

INFO: [Common 17-206] Exiting Vivado at Thu Apr 11 13:05:30 2019...