\*\*\* Running vivado

with args -log Lab05\_FullSubtractor.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab05\_FullSubtractor.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab05\_FullSubtractor.tcl -notrace

Command: synth\_design -top Lab05\_FullSubtractor -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 92360

WARNING: [Synth 8-1935] empty port in module declaration [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/sources\_1/new/Lab05\_FullSubtractor.v:30]

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1366.668 ; gain = 36.426 ; free physical = 75 ; free virtual = 729

---------------------------------------------------------------------------------

INFO: [Synth 8-6157] synthesizing module 'Lab05\_FullSubtractor' [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/sources\_1/new/Lab05\_FullSubtractor.v:23]

WARNING: [Synth 8-308] ignoring empty port [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/sources\_1/new/Lab05\_FullSubtractor.v:31]

INFO: [Synth 8-6155] done synthesizing module 'Lab05\_FullSubtractor' (1#1) [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/sources\_1/new/Lab05\_FullSubtractor.v:23]

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1395.918 ; gain = 65.676 ; free physical = 124 ; free virtual = 748

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Start Handling Custom Attributes

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1395.918 ; gain = 65.676 ; free physical = 122 ; free virtual = 749

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1395.918 ; gain = 65.676 ; free physical = 122 ; free virtual = 749

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/constrs\_1/new/Lab05\_FullSubtractor.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/constrs\_1/new/Lab05\_FullSubtractor.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.srcs/constrs\_1/new/Lab05\_FullSubtractor.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Lab05\_FullSubtractor\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Lab05\_FullSubtractor\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1649.789 ; gain = 0.000 ; free physical = 65 ; free virtual = 495

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1649.789 ; gain = 0.000 ; free physical = 74 ; free virtual = 494

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1649.789 ; gain = 0.000 ; free physical = 76 ; free virtual = 495

Constraint Validation Runtime : Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1649.789 ; gain = 0.000 ; free physical = 75 ; free virtual = 495

---------------------------------------------------------------------------------

Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:12 . Memory (MB): peak = 1649.789 ; gain = 319.547 ; free physical = 96 ; free virtual = 558

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:12 . Memory (MB): peak = 1649.789 ; gain = 319.547 ; free physical = 95 ; free virtual = 559

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:13 . Memory (MB): peak = 1649.789 ; gain = 319.547 ; free physical = 96 ; free virtual = 560

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:13 . Memory (MB): peak = 1649.789 ; gain = 319.547 ; free physical = 88 ; free virtual = 559

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---XORs :

2 Input 1 Bit XORs := 2

---------------------------------------------------------------------------------

Finished RTL Component Statistics

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---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

Hierarchical RTL Component report

Module Lab05\_FullSubtractor

Detailed RTL Component Info :

+---XORs :

2 Input 1 Bit XORs := 2

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

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---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:07 ; elapsed = 00:00:13 . Memory (MB): peak = 1649.789 ; gain = 319.547 ; free physical = 71 ; free virtual = 549

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:18 . Memory (MB): peak = 1673.789 ; gain = 343.547 ; free physical = 62 ; free virtual = 429

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:12 ; elapsed = 00:00:18 . Memory (MB): peak = 1673.789 ; gain = 343.547 ; free physical = 68 ; free virtual = 428

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:12 ; elapsed = 00:00:18 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 76 ; free virtual = 428

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:12 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 64 ; free virtual = 429

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:12 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 64 ; free virtual = 429

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:12 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 63 ; free virtual = 429

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:12 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 63 ; free virtual = 429

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:12 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 63 ; free virtual = 429

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:12 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 63 ; free virtual = 429

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |LUT3 | 2|

|2 |IBUF | 3|

|3 |OBUF | 2|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 7|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:12 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.805 ; gain = 352.562 ; free physical = 63 ; free virtual = 429

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:13 . Memory (MB): peak = 1682.805 ; gain = 98.691 ; free physical = 116 ; free virtual = 483

Synthesis Optimization Complete : Time (s): cpu = 00:00:13 ; elapsed = 00:00:19 . Memory (MB): peak = 1682.812 ; gain = 352.562 ; free physical = 111 ; free virtual = 483

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1690.805 ; gain = 0.000 ; free physical = 77 ; free virtual = 424

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

12 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:14 ; elapsed = 00:00:20 . Memory (MB): peak = 1690.805 ; gain = 360.637 ; free physical = 121 ; free virtual = 473

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1690.805 ; gain = 0.000 ; free physical = 118 ; free virtual = 473

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab05\_FullSubtractor/Lab05\_FullSubtractor.runs/synth\_1/Lab05\_FullSubtractor.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab05\_FullSubtractor\_utilization\_synth.rpt -pb Lab05\_FullSubtractor\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Thu Apr 11 12:55:50 2019...