\*\*\* Running vivado

with args -log Mux\_2.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Mux\_2.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Mux\_2.tcl -notrace

Command: open\_checkpoint /home/jinson/vivado/Mux\_2/Mux\_2.runs/impl\_1/Mux\_2.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1378.270 ; gain = 0.000 ; free physical = 873 ; free virtual = 2089

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1911.289 ; gain = 0.000 ; free physical = 214 ; free virtual = 1431

Restored from archive | CPU: 0.110000 secs | Memory: 0.995911 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1911.289 ; gain = 0.000 ; free physical = 214 ; free virtual = 1431

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1911.289 ; gain = 0.000 ; free physical = 215 ; free virtual = 1431

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 1911.289 ; gain = 533.020 ; free physical = 214 ; free virtual = 1430

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.08 . Memory (MB): peak = 1943.305 ; gain = 32.016 ; free physical = 213 ; free virtual = 1429

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 1978.305 ; gain = 35.000 ; free physical = 213 ; free virtual = 1429

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.18 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.18 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.18 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.11 ; elapsed = 00:00:00.18 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.19 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.19 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt\_design Change Summary

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| Phase | #Cells created | #Cells Removed | #Constrained objects preventing optimizations |

-------------------------------------------------------------------------------------------------------------------------

| Retarget | 0 | 0 | 0 |

| Constant propagation | 0 | 0 | 0 |

| Sweep | 0 | 0 | 0 |

| BUFG optimization | 0 | 0 | 0 |

| Shift Register Optimization | 0 | 0 | 0 |

| Post Processing Netlist | 0 | 0 | 0 |

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Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

Ending Logic Optimization Task | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.20 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

Ending Netlist Obfuscation Task | Checksum: 21d00e1fe

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Common 17-83] Releasing license: Implementation

25 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2054.305 ; gain = 0.000 ; free physical = 144 ; free virtual = 1360

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2086.320 ; gain = 0.000 ; free physical = 142 ; free virtual = 1359

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2086.320 ; gain = 0.000 ; free physical = 142 ; free virtual = 1359

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Mux\_2/Mux\_2.runs/impl\_1/Mux\_2\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Mux\_2\_drc\_opted.rpt -pb Mux\_2\_drc\_opted.pb -rpx Mux\_2\_drc\_opted.rpx

Command: report\_drc -file Mux\_2\_drc\_opted.rpt -pb Mux\_2\_drc\_opted.pb -rpx Mux\_2\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Mux\_2/Mux\_2.runs/impl\_1/Mux\_2\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 4 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 114 ; free virtual = 1330

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 1251e1f02

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 114 ; free virtual = 1330

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 114 ; free virtual = 1330

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 1251e1f02

Time (s): cpu = 00:00:00.38 ; elapsed = 00:00:00.37 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 103 ; free virtual = 1320

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 1646dc83c

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 103 ; free virtual = 1320

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 1646dc83c

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 103 ; free virtual = 1320

Phase 1 Placer Initialization | Checksum: 1646dc83c

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 103 ; free virtual = 1320

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 1646dc83c

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2126.340 ; gain = 0.000 ; free physical = 102 ; free virtual = 1318

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 197a9090d

Time (s): cpu = 00:00:00.80 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2132.332 ; gain = 5.992 ; free physical = 118 ; free virtual = 1310

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 197a9090d

Time (s): cpu = 00:00:00.81 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2132.332 ; gain = 5.992 ; free physical = 118 ; free virtual = 1310

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 2183b58cb

Time (s): cpu = 00:00:00.81 ; elapsed = 00:00:00.57 . Memory (MB): peak = 2133.332 ; gain = 6.992 ; free physical = 118 ; free virtual = 1309

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 2106e042a

Time (s): cpu = 00:00:00.82 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2133.332 ; gain = 6.992 ; free physical = 118 ; free virtual = 1309

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 2106e042a

Time (s): cpu = 00:00:00.82 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2133.332 ; gain = 6.992 ; free physical = 118 ; free virtual = 1309

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1501d4d04

Time (s): cpu = 00:00:00.98 ; elapsed = 00:00:00.73 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 115 ; free virtual = 1306

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1501d4d04

Time (s): cpu = 00:00:00.98 ; elapsed = 00:00:00.73 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 115 ; free virtual = 1306

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1501d4d04

Time (s): cpu = 00:00:00.98 ; elapsed = 00:00:00.73 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 115 ; free virtual = 1306

Phase 3 Detail Placement | Checksum: 1501d4d04

Time (s): cpu = 00:00:00.98 ; elapsed = 00:00:00.73 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 115 ; free virtual = 1306

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1501d4d04

Time (s): cpu = 00:00:00.99 ; elapsed = 00:00:00.73 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 115 ; free virtual = 1306

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1501d4d04

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.73 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 117 ; free virtual = 1308

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1501d4d04

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 117 ; free virtual = 1308

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2143.336 ; gain = 0.000 ; free physical = 117 ; free virtual = 1308

Phase 4.4 Final Placement Cleanup | Checksum: 1501d4d04

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 117 ; free virtual = 1308

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1501d4d04

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 117 ; free virtual = 1308

Ending Placer Task | Checksum: f92fd09c

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2143.336 ; gain = 16.996 ; free physical = 127 ; free virtual = 1318

INFO: [Common 17-83] Releasing license: Implementation

43 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2143.336 ; gain = 0.000 ; free physical = 127 ; free virtual = 1318

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00 . Memory (MB): peak = 2143.336 ; gain = 0.000 ; free physical = 128 ; free virtual = 1320

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2143.336 ; gain = 0.000 ; free physical = 127 ; free virtual = 1319

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Mux\_2/Mux\_2.runs/impl\_1/Mux\_2\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file Mux\_2\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2143.336 ; gain = 0.000 ; free physical = 120 ; free virtual = 1311

INFO: [runtcl-4] Executing : report\_utilization -file Mux\_2\_utilization\_placed.rpt -pb Mux\_2\_utilization\_placed.pb

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file Mux\_2\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.08 . Memory (MB): peak = 2143.336 ; gain = 0.000 ; free physical = 127 ; free virtual = 1318

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 4 CPUs

Checksum: PlaceDB: c0dd19a2 ConstDB: 0 ShapeSum: 3852b6fa RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 1c082e0dd

Time (s): cpu = 00:00:21 ; elapsed = 00:00:18 . Memory (MB): peak = 2281.387 ; gain = 138.051 ; free physical = 128 ; free virtual = 1170

Post Restoration Checksum: NetGraph: e4a9695a NumContArr: dbd97783 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 1c082e0dd

Time (s): cpu = 00:00:21 ; elapsed = 00:00:18 . Memory (MB): peak = 2288.383 ; gain = 145.047 ; free physical = 112 ; free virtual = 1154

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 1c082e0dd

Time (s): cpu = 00:00:21 ; elapsed = 00:00:18 . Memory (MB): peak = 2288.383 ; gain = 145.047 ; free physical = 112 ; free virtual = 1154

Phase 2 Router Initialization | Checksum: 1c082e0dd

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2294.648 ; gain = 151.312 ; free physical = 109 ; free virtual = 1151

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: d052fad5

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2299.082 ; gain = 155.746 ; free physical = 106 ; free virtual = 1148

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 2

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2299.082 ; gain = 155.746 ; free physical = 107 ; free virtual = 1149

Phase 4 Rip-up And Reroute | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2299.082 ; gain = 155.746 ; free physical = 107 ; free virtual = 1149

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2299.082 ; gain = 155.746 ; free physical = 107 ; free virtual = 1149

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2299.082 ; gain = 155.746 ; free physical = 107 ; free virtual = 1149

Phase 6 Post Hold Fix | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2299.082 ; gain = 155.746 ; free physical = 107 ; free virtual = 1149

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.0043957 %

Global Horizontal Routing Utilization = 0.00127877 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 4.41176%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2299.082 ; gain = 155.746 ; free physical = 107 ; free virtual = 1149

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2301.082 ; gain = 157.746 ; free physical = 106 ; free virtual = 1148

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 1705440d8

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2301.082 ; gain = 157.746 ; free physical = 106 ; free virtual = 1148

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2301.082 ; gain = 157.746 ; free physical = 123 ; free virtual = 1165

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

56 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2301.082 ; gain = 157.746 ; free physical = 124 ; free virtual = 1166

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2301.082 ; gain = 0.000 ; free physical = 124 ; free virtual = 1166

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2301.082 ; gain = 0.000 ; free physical = 124 ; free virtual = 1167

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2301.082 ; gain = 0.000 ; free physical = 123 ; free virtual = 1166

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Mux\_2/Mux\_2.runs/impl\_1/Mux\_2\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Mux\_2\_drc\_routed.rpt -pb Mux\_2\_drc\_routed.pb -rpx Mux\_2\_drc\_routed.rpx

Command: report\_drc -file Mux\_2\_drc\_routed.rpt -pb Mux\_2\_drc\_routed.pb -rpx Mux\_2\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Mux\_2/Mux\_2.runs/impl\_1/Mux\_2\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file Mux\_2\_methodology\_drc\_routed.rpt -pb Mux\_2\_methodology\_drc\_routed.pb -rpx Mux\_2\_methodology\_drc\_routed.rpx

Command: report\_methodology -file Mux\_2\_methodology\_drc\_routed.rpt -pb Mux\_2\_methodology\_drc\_routed.pb -rpx Mux\_2\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 4 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /home/jinson/vivado/Mux\_2/Mux\_2.runs/impl\_1/Mux\_2\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file Mux\_2\_power\_routed.rpt -pb Mux\_2\_power\_summary\_routed.pb -rpx Mux\_2\_power\_routed.rpx

Command: report\_power -file Mux\_2\_power\_routed.rpt -pb Mux\_2\_power\_summary\_routed.pb -rpx Mux\_2\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

68 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file Mux\_2\_route\_status.rpt -pb Mux\_2\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file Mux\_2\_timing\_summary\_routed.rpt -pb Mux\_2\_timing\_summary\_routed.pb -rpx Mux\_2\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file Mux\_2\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file Mux\_2\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file Mux\_2\_bus\_skew\_routed.rpt -pb Mux\_2\_bus\_skew\_routed.pb -rpx Mux\_2\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

INFO: [Common 17-206] Exiting Vivado at Thu Apr 11 19:49:22 2019...

\*\*\* Running vivado

with args -log Mux\_2.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Mux\_2.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

\*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Mux\_2.tcl -notrace

Command: open\_checkpoint Mux\_2\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory (MB): peak = 1387.266 ; gain = 0.000 ; free physical = 1054 ; free virtual = 2089

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1980.191 ; gain = 0.000 ; free physical = 366 ; free virtual = 1401

Restored from archive | CPU: 0.120000 secs | Memory: 1.001831 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1980.191 ; gain = 0.000 ; free physical = 366 ; free virtual = 1401

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1980.191 ; gain = 0.000 ; free physical = 367 ; free virtual = 1401

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 1980.191 ; gain = 592.926 ; free physical = 366 ; free virtual = 1401

Command: write\_bitstream -force Mux\_2.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 4 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./Mux\_2.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

INFO: [Common 17-83] Releasing license: Implementation

20 Infos, 1 Warnings, 2 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:09 . Memory (MB): peak = 2421.027 ; gain = 440.836 ; free physical = 443 ; free virtual = 1349

INFO: [Common 17-206] Exiting Vivado at Thu Apr 11 19:50:15 2019...

\*\*\* Running vivado

with args -log Mux\_2.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Mux\_2.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

\*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Mux\_2.tcl -notrace

Command: open\_checkpoint Mux\_2\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1355.004 ; gain = 0.000 ; free physical = 961 ; free virtual = 1965

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1980.000 ; gain = 0.000 ; free physical = 270 ; free virtual = 1274

Restored from archive | CPU: 0.140000 secs | Memory: 1.001831 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1980.000 ; gain = 0.000 ; free physical = 270 ; free virtual = 1274

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1980.000 ; gain = 0.000 ; free physical = 270 ; free virtual = 1274

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 1980.000 ; gain = 624.996 ; free physical = 270 ; free virtual = 1274

Command: write\_bitstream -force Mux\_2.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 4 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./Mux\_2.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

INFO: [Common 17-83] Releasing license: Implementation

20 Infos, 1 Warnings, 2 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 2420.836 ; gain = 440.836 ; free physical = 453 ; free virtual = 1214

INFO: [Common 17-206] Exiting Vivado at Thu Apr 11 19:53:37 2019...