\*\*\* Running vivado

with args -log Lab09\_PWM.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab09\_PWM.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab09\_PWM.tcl -notrace

Command: link\_design -top Lab09\_PWM -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 5 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/constrs\_1/new/Lab09\_PWM.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/constrs\_1/new/Lab09\_PWM.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1535.539 ; gain = 0.000 ; free physical = 669 ; free virtual = 2643

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:00.96 ; elapsed = 00:00:01 . Memory (MB): peak = 1578.555 ; gain = 39.016 ; free physical = 662 ; free virtual = 2637

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: b2d4c73f

Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 2038.055 ; gain = 459.500 ; free physical = 265 ; free virtual = 2256

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: b2d4c73f

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2187

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: b2d4c73f

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2187

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 899224d4

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2188

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 899224d4

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2188

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: c5b924ec

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2187

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: c5b924ec

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2187

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt\_design Change Summary

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-------------------------------------------------------------------------------------------------------------------------

| Phase | #Cells created | #Cells Removed | #Constrained objects preventing optimizations |

-------------------------------------------------------------------------------------------------------------------------

| Retarget | 0 | 0 | 0 |

| Constant propagation | 0 | 0 | 0 |

| Sweep | 0 | 0 | 0 |

| BUFG optimization | 0 | 0 | 0 |

| Shift Register Optimization | 0 | 0 | 0 |

| Post Processing Netlist | 0 | 0 | 0 |

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Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2187

Ending Logic Optimization Task | Checksum: c5b924ec

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 196 ; free virtual = 2187

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: c5b924ec

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 195 ; free virtual = 2186

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: c5b924ec

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 195 ; free virtual = 2186

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 195 ; free virtual = 2186

Ending Netlist Obfuscation Task | Checksum: c5b924ec

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 195 ; free virtual = 2186

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 2117.055 ; gain = 577.516 ; free physical = 195 ; free virtual = 2186

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2117.055 ; gain = 0.000 ; free physical = 195 ; free virtual = 2186

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2149.070 ; gain = 0.000 ; free physical = 192 ; free virtual = 2185

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2149.070 ; gain = 0.000 ; free physical = 191 ; free virtual = 2184

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/impl\_1/Lab09\_PWM\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab09\_PWM\_drc\_opted.rpt -pb Lab09\_PWM\_drc\_opted.pb -rpx Lab09\_PWM\_drc\_opted.rpx

Command: report\_drc -file Lab09\_PWM\_drc\_opted.rpt -pb Lab09\_PWM\_drc\_opted.pb -rpx Lab09\_PWM\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/impl\_1/Lab09\_PWM\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 4 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 154 ; free virtual = 2155

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 480047ac

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 154 ; free virtual = 2155

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 154 ; free virtual = 2155

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 17d0e8609

Time (s): cpu = 00:00:00.75 ; elapsed = 00:00:00.64 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 133 ; free virtual = 2138

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 1c3e7ee9f

Time (s): cpu = 00:00:00.78 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 132 ; free virtual = 2138

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 1c3e7ee9f

Time (s): cpu = 00:00:00.78 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 132 ; free virtual = 2138

Phase 1 Placer Initialization | Checksum: 1c3e7ee9f

Time (s): cpu = 00:00:00.78 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 132 ; free virtual = 2138

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 1c3e7ee9f

Time (s): cpu = 00:00:00.79 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 130 ; free virtual = 2137

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 259efac96

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 106 ; free virtual = 2113

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 259efac96

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 106 ; free virtual = 2113

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1fd4df039

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 106 ; free virtual = 2113

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 23c812018

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 106 ; free virtual = 2113

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 23c812018

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 106 ; free virtual = 2113

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1db36f6ac

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 124 ; free virtual = 2109

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1db36f6ac

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 124 ; free virtual = 2109

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1db36f6ac

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 124 ; free virtual = 2109

Phase 3 Detail Placement | Checksum: 1db36f6ac

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 124 ; free virtual = 2109

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1db36f6ac

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 124 ; free virtual = 2109

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1db36f6ac

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 125 ; free virtual = 2110

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1db36f6ac

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 125 ; free virtual = 2110

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 125 ; free virtual = 2110

Phase 4.4 Final Placement Cleanup | Checksum: 208645d21

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 125 ; free virtual = 2110

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 208645d21

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 125 ; free virtual = 2110

Ending Placer Task | Checksum: 114c9f2e5

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 136 ; free virtual = 2122

INFO: [Common 17-83] Releasing license: Implementation

41 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 136 ; free virtual = 2122

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 135 ; free virtual = 2122

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 135 ; free virtual = 2121

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/impl\_1/Lab09\_PWM\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file Lab09\_PWM\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 129 ; free virtual = 2115

INFO: [runtcl-4] Executing : report\_utilization -file Lab09\_PWM\_utilization\_placed.rpt -pb Lab09\_PWM\_utilization\_placed.pb

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file Lab09\_PWM\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2197.094 ; gain = 0.000 ; free physical = 136 ; free virtual = 2122

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 4 CPUs

Checksum: PlaceDB: 472e0325 ConstDB: 0 ShapeSum: cd9befc0 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 16a8c0623

Time (s): cpu = 00:00:22 ; elapsed = 00:00:19 . Memory (MB): peak = 2306.125 ; gain = 109.031 ; free physical = 117 ; free virtual = 1988

Post Restoration Checksum: NetGraph: 7e22a54e NumContArr: ec6960d5 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 16a8c0623

Time (s): cpu = 00:00:22 ; elapsed = 00:00:19 . Memory (MB): peak = 2313.121 ; gain = 116.027 ; free physical = 104 ; free virtual = 1971

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 16a8c0623

Time (s): cpu = 00:00:22 ; elapsed = 00:00:19 . Memory (MB): peak = 2313.121 ; gain = 116.027 ; free physical = 107 ; free virtual = 1970

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 148d81d21

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2322.387 ; gain = 125.293 ; free physical = 124 ; free virtual = 1957

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 4d54f8dc

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 125 ; free virtual = 1958

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 8

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 1685b2243

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 127 ; free virtual = 1960

Phase 4 Rip-up And Reroute | Checksum: 1685b2243

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 127 ; free virtual = 1960

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 1685b2243

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 126 ; free virtual = 1959

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 1685b2243

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 126 ; free virtual = 1959

Phase 6 Post Hold Fix | Checksum: 1685b2243

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 126 ; free virtual = 1959

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.0100535 %

Global Horizontal Routing Utilization = 0.00760159 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 10.8108%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 9.90991%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 13.2353%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 10.2941%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 1685b2243

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 126 ; free virtual = 1959

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 1685b2243

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 125 ; free virtual = 1958

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: b2bf5941

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 125 ; free virtual = 1958

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 143 ; free virtual = 1976

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2328.242 ; gain = 131.148 ; free physical = 143 ; free virtual = 1976

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2328.242 ; gain = 0.000 ; free physical = 143 ; free virtual = 1976

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2328.242 ; gain = 0.000 ; free physical = 141 ; free virtual = 1975

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2328.242 ; gain = 0.000 ; free physical = 142 ; free virtual = 1976

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/impl\_1/Lab09\_PWM\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab09\_PWM\_drc\_routed.rpt -pb Lab09\_PWM\_drc\_routed.pb -rpx Lab09\_PWM\_drc\_routed.rpx

Command: report\_drc -file Lab09\_PWM\_drc\_routed.rpt -pb Lab09\_PWM\_drc\_routed.pb -rpx Lab09\_PWM\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/impl\_1/Lab09\_PWM\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file Lab09\_PWM\_methodology\_drc\_routed.rpt -pb Lab09\_PWM\_methodology\_drc\_routed.pb -rpx Lab09\_PWM\_methodology\_drc\_routed.rpx

Command: report\_methodology -file Lab09\_PWM\_methodology\_drc\_routed.rpt -pb Lab09\_PWM\_methodology\_drc\_routed.pb -rpx Lab09\_PWM\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 4 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/impl\_1/Lab09\_PWM\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file Lab09\_PWM\_power\_routed.rpt -pb Lab09\_PWM\_power\_summary\_routed.pb -rpx Lab09\_PWM\_power\_routed.rpx

Command: report\_power -file Lab09\_PWM\_power\_routed.rpt -pb Lab09\_PWM\_power\_summary\_routed.pb -rpx Lab09\_PWM\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file Lab09\_PWM\_route\_status.rpt -pb Lab09\_PWM\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file Lab09\_PWM\_timing\_summary\_routed.rpt -pb Lab09\_PWM\_timing\_summary\_routed.pb -rpx Lab09\_PWM\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file Lab09\_PWM\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file Lab09\_PWM\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file Lab09\_PWM\_bus\_skew\_routed.rpt -pb Lab09\_PWM\_bus\_skew\_routed.pb -rpx Lab09\_PWM\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

INFO: [Common 17-206] Exiting Vivado at Thu May 16 18:54:08 2019...

\*\*\* Running vivado

with args -log Lab09\_PWM.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab09\_PWM.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab09\_PWM.tcl -notrace

Command: open\_checkpoint Lab09\_PWM\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1387.270 ; gain = 0.000 ; free physical = 1085 ; free virtual = 2914

INFO: [Netlist 29-17] Analyzing 5 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2016.195 ; gain = 0.000 ; free physical = 334 ; free virtual = 2198

Restored from archive | CPU: 0.150000 secs | Memory: 1.097092 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2016.195 ; gain = 0.000 ; free physical = 334 ; free virtual = 2198

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2016.195 ; gain = 0.000 ; free physical = 334 ; free virtual = 2198

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:09 ; elapsed = 00:00:11 . Memory (MB): peak = 2016.195 ; gain = 628.926 ; free physical = 333 ; free virtual = 2197

Command: write\_bitstream -force Lab09\_PWM.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 4 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Bitstream compression saved 27452832 bits.

Writing bitstream ./Lab09\_PWM.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

INFO: [Common 17-186] '/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/impl\_1/usage\_statistics\_webtalk.xml' has been successfully sent to Xilinx on Thu May 16 18:54:48 2019. For additional details about this file, please refer to the WebTalk help file at /tools/Xilinx/Vivado/2018.3/doc/webtalk\_introduction.html.

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 1 Warnings, 2 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:15 . Memory (MB): peak = 2458.031 ; gain = 441.836 ; free physical = 436 ; free virtual = 2134

INFO: [Common 17-206] Exiting Vivado at Thu May 16 18:54:48 2019...