\*\*\* Running vivado

with args -log Lab09\_PWM.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab09\_PWM.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab09\_PWM.tcl -notrace

Command: synth\_design -top Lab09\_PWM -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 14416

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Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1389.352 ; gain = 0.000 ; free physical = 826 ; free virtual = 2800

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INFO: [Synth 8-6157] synthesizing module 'Lab09\_PWM' [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/sources\_1/new/Lab09\_PWM.sv:23]

WARNING: [Synth 8-6014] Unused sequential element j\_reg was removed. [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/sources\_1/new/Lab09\_PWM.sv:65]

INFO: [Synth 8-6155] done synthesizing module 'Lab09\_PWM' (1#1) [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/sources\_1/new/Lab09\_PWM.sv:23]

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1389.352 ; gain = 0.000 ; free physical = 838 ; free virtual = 2812

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1389.352 ; gain = 0.000 ; free physical = 837 ; free virtual = 2812

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1389.352 ; gain = 0.000 ; free physical = 837 ; free virtual = 2812

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/constrs\_1/new/Lab09\_PWM.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/constrs\_1/new/Lab09\_PWM.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/constrs\_1/new/Lab09\_PWM.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Lab09\_PWM\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Lab09\_PWM\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1707.137 ; gain = 0.000 ; free physical = 581 ; free virtual = 2556

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1707.137 ; gain = 0.000 ; free physical = 582 ; free virtual = 2556

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1707.137 ; gain = 0.000 ; free physical = 582 ; free virtual = 2556

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1707.137 ; gain = 0.000 ; free physical = 582 ; free virtual = 2556

---------------------------------------------------------------------------------

Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 651 ; free virtual = 2626

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 651 ; free virtual = 2626

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 653 ; free virtual = 2627

---------------------------------------------------------------------------------

INFO: [Synth 8-5546] ROM "cycle\_demo" won't be mapped to RAM because it is too sparse

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 643 ; free virtual = 2618

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 21 Bit Adders := 1

2 Input 8 Bit Adders := 1

+---Registers :

21 Bit Registers := 1

8 Bit Registers := 1

1 Bit Registers := 2

+---Muxes :

2 Input 21 Bit Muxes := 1

2 Input 8 Bit Muxes := 1

8 Input 8 Bit Muxes := 1

2 Input 1 Bit Muxes := 8

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Finished RTL Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module Lab09\_PWM

Detailed RTL Component Info :

+---Adders :

2 Input 21 Bit Adders := 1

2 Input 8 Bit Adders := 1

+---Registers :

21 Bit Registers := 1

8 Bit Registers := 1

1 Bit Registers := 2

+---Muxes :

2 Input 21 Bit Muxes := 1

2 Input 8 Bit Muxes := 1

8 Input 8 Bit Muxes := 1

2 Input 1 Bit Muxes := 8

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

---------------------------------------------------------------------------------

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-5546] ROM "cycle\_demo" won't be mapped to RAM because it is too sparse

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:08 ; elapsed = 00:00:10 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 632 ; free virtual = 2608

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 507 ; free virtual = 2483

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 507 ; free virtual = 2483

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 5|

|3 |LUT1 | 1|

|4 |LUT2 | 2|

|5 |LUT3 | 2|

|6 |LUT4 | 13|

|7 |LUT5 | 9|

|8 |LUT6 | 28|

|9 |FDCE | 31|

|10 |IBUF | 9|

|11 |OBUF | 1|

+------+-------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 102|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.137 ; gain = 317.785 ; free physical = 506 ; free virtual = 2482

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:10 ; elapsed = 00:00:11 . Memory (MB): peak = 1707.137 ; gain = 0.000 ; free physical = 560 ; free virtual = 2536

Synthesis Optimization Complete : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1707.145 ; gain = 317.785 ; free physical = 560 ; free virtual = 2536

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 5 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1710.137 ; gain = 0.000 ; free physical = 501 ; free virtual = 2477

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

16 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1710.137 ; gain = 320.859 ; free physical = 557 ; free virtual = 2534

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1710.137 ; gain = 0.000 ; free physical = 557 ; free virtual = 2534

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.runs/synth\_1/Lab09\_PWM.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab09\_PWM\_utilization\_synth.rpt -pb Lab09\_PWM\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Thu May 16 18:52:55 2019...