Vivado Simulator 2018.3

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Running: /tools/Xilinx/Vivado/2018.3/bin/unwrapped/lnx64.o/xelab -wto f6ffe72b2cd44eaf972c42ac4d3a52fd --incr --debug typical --relax --mt 8 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot test\_behav xil\_defaultlib.test xil\_defaultlib.glbl -log elaborate.log

Using 8 slave threads.

Starting static elaboration

ERROR: [VRFC 10-2864] module 'test' having interface port(s) (buttom) cannot be elaborated by itself [/home/jinson/vivado/Lab09\_PWM/Lab09\_PWM.srcs/sim\_1/new/test.sv:23]

ERROR: [XSIM 43-3322] Static elaboration of top level Verilog design unit(s) in library work failed.